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Series-Parallel Switched-Capacitor Balancing Circuit for Hybrid Source Package

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ABSTRACT Energy storage package usually consists of multiple cells. The associated cell equalization is important for cell package design. An innovative and efficient switched-capacitor balancing circuit is proposed in this paper to achieve cell voltage balancing for a package of hybrid energy sources. The key feature is that the balancing is not just restricted to equal cell voltage but is extended to different cell combinations that will be beneficial for non-sorted cell packages, for different types of Li-ion cells, and for other applications, such as second-life retired batteries. The topology and operation process of each switching state for this voltage equalizer are analyzed in detail. The mathematical derivation, software simulation, and laboratory experiment are conducted to verify the feasibility of this model. This proposed voltage equalizer is especially useful with the increasing establishment of hybrid systems, which take advantages of different types of energy sources or energy storage devices.

INDEX TERMS Voltage balancing, hybrid energy sources, supercapacitors.

I. INTRODUCTION

Eco-friendly products become a major player of the global power and renewable energy industry. Batteries and supercapacitors (SC) are widely used in electric vehicles, distributed generation systems, energy storage systems and so on [1]–[3]. As the power of a single cell of battery or SC cannot provide sufficient driving force to loads, a series string of battery or SC units are required to fulfill the voltage and power requirements for high power applications [4]. However, different batteries and SCs in the same series have different characteristics such as capacitance, equivalent series resistance (ESR), equivalent series inductance (ESL) and self-discharging rate, which may lead to voltage imbalance between each cell in a system [4], [5]. In practice, although sorting is used before packaging in order to ease this phenomenon, the imbalance effect becomes more serious when the energy storage devices get aged. This imbalance phenomenon is now a well-known problem in series-parallel connection [1], [4], [6]. Due to unavoidable mismatch of each cell, the capability of the energy storage system cannot be fully used. In a charging cycle, the charging current stops when most or a portion of cells are fully charged while in the discharging cycle, the energy devices stop when most or a portion of cells are discharged to a lower limit [7], [8].

Voltage of cells shall be made equal to the required value to solve these unbalancing problems. The balancing is important especially when a group of electric vehicles (EV) batteries are in series connection to make up the high voltage for driving motor. Balancing for energy storage to the power distribution and renewable energy storage are in high demand and suitable technology of balancing is urgently needed for a number of applications.

A variety of cell voltage equalizers have been presented which can be classified into three main types, including cell selection, passive methods and active methods [9]. Integrating cells with similar performance in one package is the simplest way, but the accuracy and efficiency during sorting are proved to be low. Passive method is the most widely used technology. Resistors in parallel with the cells are switched on when they have higher state-of-charge (SoC) than others or when the cells approach the peak withstanding voltage. As the energy dissipates into the resistor, additional heating loss is generated. For energy-saving purpose, the charging and discharging currents of each cell can be actively controlled to keep the same SoC among all cell units such that the higher energy can be transferred into the cells with lower energy using power converter circuit, instead of wasting as the heat loss. This active method is proved to be more efficient

so that many advanced equalizers have been designed based on it using switched-capacitors, inductors, transformers or converters [1]–[4], [10]–[21].

Voltage balancing based on the switched-capacitor has simple structure and easy control [14]–[16]. References [17] and [18] are used switched-capacitors; the series-parallel switched-capacitor voltage equalizer are presented in [19]; converters applied in [20] to form the equalizer; induction motor in [21] could get the balancing function, but these papers mostly emphasize the balancing of single cells and series-parallel connections are applied for converters and inverters [23], [24]. Future EVs or distributed generation systems with hybrid energy systems are promising which take advantage of both battery and SC. As battery has high energy density while SC has high power density, they are combined to provide better performance of acceleration, emergency response [25] and energy storage [26]. Besides, integrating retired batteries from aged EVs into grid energy storage will greatly promote environmental protection and the re-use concept. However the compatibility issue between different cell brands imposes restraints on the development of energy storage system because cells have different background in age, brand and chemicals.

The technique proposed in this paper is intended to achieve the voltage balancing of a package of energy sources with a newly developed switched-capacitor circuit, regardless of the source types. Balancing techniques for different voltage ratios should be developed to improve the existing balancing methods and prepare for future vast applications of various balancing requirements. The circuit proposed could balance the voltage ratio not only 1:1 but also any preset ratio. Due to the increasing popularity of hybrid energy systems, the balancing system proposed in this paper is practical and useful for further development.

The rest of this paper is organized as follows. Section II describes the operation principle and the state analysis of the circuit. The modeling of the circuit will be obtained in Section III. The simulation and experimental results will be presented in the fourth and fifth sections, respectively.

II. SWITCHED-CAPACITOR VOLTAGE BALANCING CIRCUIT

A. CIRCUITRY DESCRIPTION AND OPERATION PRINCIPLE

As indicated in Fig.1, the circuitry of the series-parallel switched-capacitor balancing circuit system consists of a package of hybrid energy sources and SC. Parameter n is defined in (1) where V_P is the voltage of the source package and V_{SC} is the voltage of SC. Three transistors and two capacitors form a balancing unit. The operation process of the proposed balancing system is divided into clock phase φ_a and clock phase φ_b with different switch positions as shown in Fig.2. The detailed operation principles of clock phase φ_a are shown in Section II.B while the illustration of clock

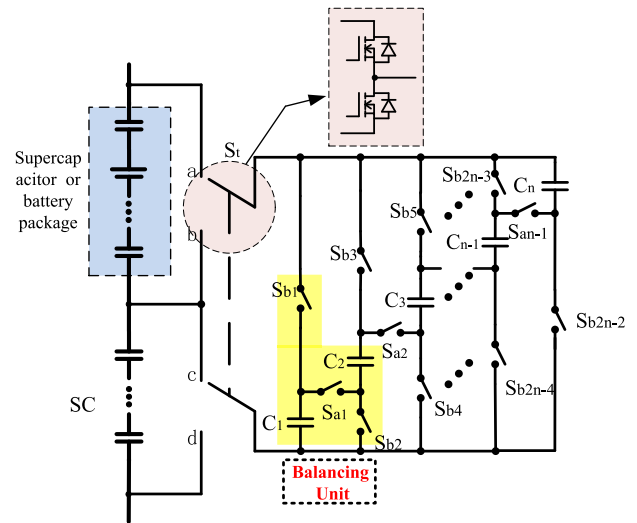


FIGURE 1. Voltage balancing circuit of package series-parallel switched-capacitor.

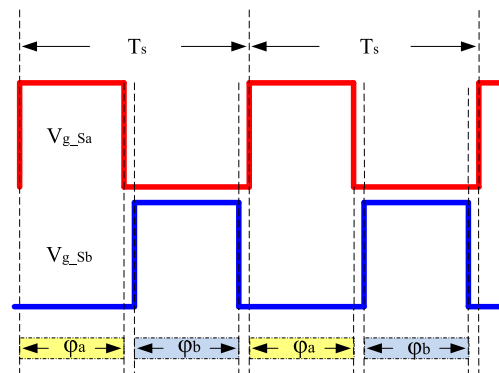


FIGURE 2. Control signal of the switches.

phase φ_b is shown in Section II.C.

$$n = \frac{V_P}{V_{SC}} \quad (1)$$

Fig.3 (a) illustrates the circuit in φ_a . When each pole of the main switch S_t is turned to connect a-c position, the source package is in series connection to the switched-capacitors. When S_t is turned to connect b-d position in φ_b , the SC is in parallel connection to the switched-capacitors as shown in the Fig.3 (b).

B. STATE ANALYSIS IN CLOCK PHASE φ_a

All the switches S_t , S_a and S_b in Fig. 1 can be implemented by N-channel MOSFET and controlled by the signals shown in Fig. 2. Fig. 3(a) shows the connection of the switch S_t . During the clock phase φ_a , S_t is in a-c position and capacitors C_1, C_2 to C_n are in series connection to the source package. If the voltage of source package is higher than that of switched-capacitors C_1, C_2 to C_n , the switched-capacitors will be charged from the package. Fig.4 (a) shows the charging flow between the package and SC.

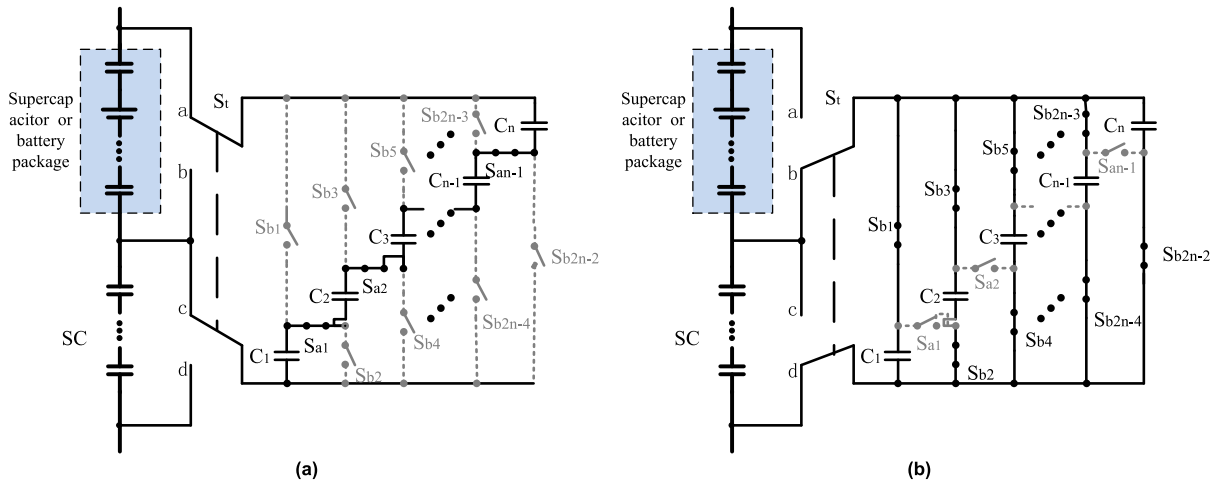


FIGURE 3. Working principle of the proposed balancing system. (a) Series to the source package; (b) Parallel to the SC.

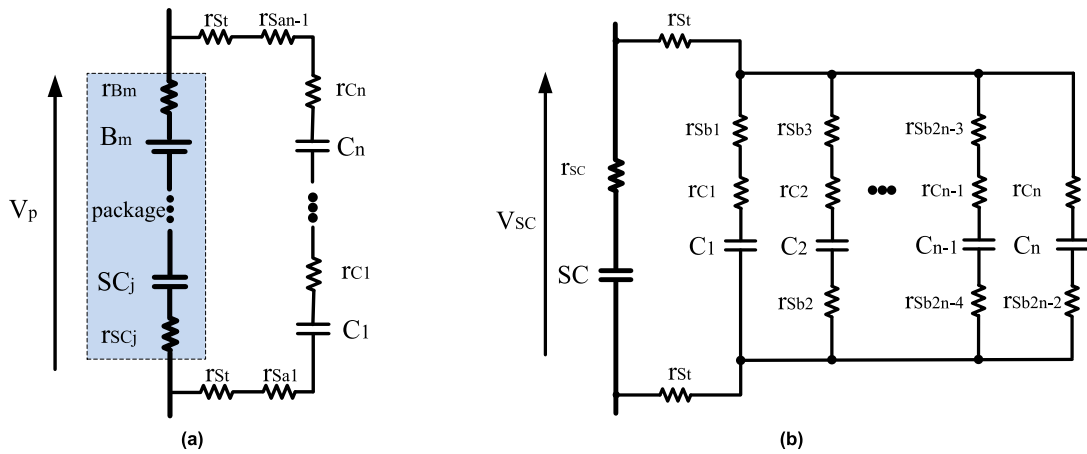


FIGURE 4. Circuit of each state. (a) state of φ_a ; (b) state of φ_b .

The voltage relationship in the package is shown in (2). The voltage of the switched-capacitor v_C and current of the switched-capacitor i_C vary during this state and are given in (3) and (4), respectively.

$$V_p = V_{B_m} + V_{SC_j} - i_p (r_{B_m} + r_{SC_j}) \quad (2)$$

$$v_C(t) = \frac{V_p - (V_p - nV_{C_{s_min}}) e^{-\frac{t}{\tau_a}}}{n} \quad (3)$$

$$i_C(t) = \frac{V_p - nV_{C_{s_min}}}{R_a} e^{-\frac{t}{\tau_a}} \quad (4)$$

where V_p is the voltage of the package; V_{B_m} is the voltage of the batteries and V_{SC_j} is the voltages of the SCs in the package; i_p is the current of the package, given that $i_p = i_C$; r_{B_m} and r_{SC_j} are the ESR of the batteries and SCs in the package respectively; $V_{C_{s_min}}$ is the minimum initial voltage of the switched-capacitor C_s which is one of all the switched-capacitors when $\frac{V_p}{n} > V_{SC}$.

R_a is the total resistance including all the ESR of the switched-capacitors. nr_C and all the ON-resistance

$(n - 1)r_{S_a} + 2r_{S_t}$ of the S_{a1} to $S_{a_{n-1}}$ and S_t in the φ_a , and the time constant τ_a in the φ_a are shown as

$$R_a = nr_C + (n - 1)r_{S_a} + 2r_{S_t} \quad (5)$$

$$\tau_a = R_a C_a = C \left(r_C + \frac{n - 1}{n} r_{S_a} + \frac{2r_{S_t}}{n} \right) \quad (6)$$

where C_a is the capacitance of the series switched-capacitor string, $C_a = \frac{C}{n}$.

Similarly, during the clock phase φ_b , if the voltage of source package is lower than that of the switched-capacitors C_1, C_2 to C_n , the switched-capacitors will be discharged. The variations of the voltage and current during φ_b are given below

$$v_C(t) = \frac{V_p + (nV_{C_{p_max}} - V_p) e^{-\frac{t}{\tau_b}}}{n} \quad (7)$$

$$i_C(t) = \frac{nV_{C_{p_max}} - V_p}{R_a} e^{-\frac{t}{\tau_b}} \quad (8)$$

where V_{Cp_max} is the maximum initial voltage of the switched-capacitor C_p , which is one of all the switched-capacitors when $\frac{V_p}{n} < V_{SC}$.

C. STATE ANALYSIS IN CLOCK PHASE φ_b

In the duration of φ_b , S_t is changed to b-d position and all the switched-capacitors are in parallel as shown in Fig.4 (b). When the voltage of the SC is higher than the voltage of the switched-capacitors connected in parallel, charge will transfer from the SC to switched-capacitors. Otherwise, SC will be charged by the switched-capacitors. $v_{Ci}(t)$ and $i_{Ci}(t)$ are the instantaneous voltage and current of the switched-capacitors.

Regarding the structure in the circuit,

When $i = 1$ or n ,

$$r_{b,i} = r_C + r_{Sb}$$

When $1 < i < n$,

$$r_{b,i} = r_C + 2r_{Sb}$$

where i is the range from 1 to n ; $r_{b,i}$ is the ESR in the i^{th} branch; r_{Sb} is the on-resistance of S_{b1} to S_{b2n-2} .

In the topology analysis, the average resistance of $r_{b,i}$ is assumed to be equal in all branches in φ_b which is

$$r_{b,i} = r_C + \frac{2n - 2}{n} r_{Sb} \tag{9}$$

The time constant τ_b in φ_b is dominated by R_b , their relationship is shown below

$$R_b = \frac{r_C}{n} + \frac{2n - 2}{n^2} r_{Sb} + 2r_{St} \tag{10}$$

$$\tau_b = R_b C_b = C \left(r_C + \frac{2n - 2}{n} r_{Sb} + 2nr_{St} \right) \tag{11}$$

where R_b is the sum of all the ESR of the switched-capacitors and all the ON-resistance of S_{b1} to S_{b2n-2} and S_t ; C_b is the sum of the capacitance of all the switched-capacitors, i.e. $C_b = nC$.

During the clock phase φ_b , if the switched-capacitor voltage, V_{Cp} , is lower than the voltage of SC, the switched-capacitors C_1, C_2 to C_n will be charged. The variation of the voltage and the current is shown below

$$V_{SC} = V'_{SC} - i_{SC} r_{SC} \tag{12}$$

$$v_C(t) = V_{SC} - (V_{SC} - V_{Cp_min}) e^{-\frac{t}{\tau_b}} \tag{13}$$

$$i_C(t) = \frac{V_{SC} - V_{Cp_min}}{R_b} e^{-\frac{t}{\tau_b}} \tag{14}$$

where V'_{SC} is the internal voltage of the SC; i_{SC} is the current of the SC, given that $i_{SC} = ni_C$; r_{SC} is the ESR the SC; V_{Cp_min} is the minimum initial voltage of the switched-capacitor when $\frac{V_p}{n} < V_{SC}$.

If V_{Cp} , is higher than the voltage of SC, the switched-capacitors C_1, C_2 and C_n will be discharged. The variation of the voltage and current is shown below

$$v_C(t) = V_{SC} + (V_{Cs_max} - V_{SC}) e^{-\frac{t}{\tau_b}} \tag{15}$$

$$i_C(t) = \frac{V_{Cs_max} - V_{SC}}{R_b} e^{-\frac{t}{\tau_b}} \tag{16}$$

where V_{Cs_max} is the maximum initial voltage of the switched-capacitor when $\frac{V_p}{n} > V_{SC}$.

III. MODELING FOR SWITCHED-CAPACITOR VOLTAGE EQUALIZER

A. EQUIVALENT RESISTANCE ANALYSIS

During the progress of charge and discharge in one cycle, based on (3) and (15), V_{Cs} reaches maximum at the end of φ_a and reduces to minimum at the end of φ_b . Similarly, based on (7) and (13), V_{Cp} reaches maximum at the end of φ_b and reduces to a minimum at the end of φ_a . Variation principles of V_C are expressed in Table 1.

TABLE 1. Variation principles of V_C .

$\frac{V_p}{n} > V_{SC}$	$\frac{V_p}{n} < V_{SC}$
$V_{Cs_max} = \frac{V_p - (V_p - nV_{Cs_min}) e^{-\frac{T_s}{2\tau_a}}}{n} \tag{17}$	$V_{Cp_min} = \frac{V_p + (nV_{Cp_max} - V_p) e^{-\frac{T_s}{2\tau_b}}}{n} \tag{19}$
$V_{Cs_min} = V_{SC} + (V_{Cs_max} - V_{SC}) e^{-\frac{T_s}{2\tau_b}} \tag{18}$	$V_{Cp_max} = V_{SC} - (V_{SC} - V_{Cp_min}) e^{-\frac{T_s}{2\tau_a}} \tag{20}$

where $T_s = \frac{1}{f}$, f is the switching frequency of the switch.

The difference between V_{Cs_max} and V_{Cs_min} , by subtracting (17) by (18), when $\frac{V_p}{n} > V_{SC}$, is then

$$V_p - nV_{SC} = n(V_{Cs_max} - V_{Cs_min}) \times \frac{1 - e^{-\frac{1}{2\tau_a f}} e^{-\frac{1}{2\tau_b f}}}{1 - e^{-\frac{1}{2\tau_a f}} - e^{-\frac{1}{2\tau_b f}} + e^{-\frac{1}{2\tau_a f}} e^{-\frac{1}{2\tau_b f}}} \tag{21}$$

$$R_{eq} = \frac{V_p - nV_{SC}}{I} \tag{22}$$

When (21) is substituted into (22), given that $I = qf$ and the quantity of electric charge in this cycle is $q = C(V_{Cs_max} - V_{Cs_min})$, the equivalent resistance R_{eq} could be further expressed as

$$R_{eq} = \frac{n}{Cf} \frac{1 - e^{-\frac{1}{2\tau_a f}} e^{-\frac{1}{2\tau_b f}}}{1 - e^{-\frac{1}{2\tau_a f}} - e^{-\frac{1}{2\tau_b f}} + e^{-\frac{1}{2\tau_a f}} e^{-\frac{1}{2\tau_b f}}} \tag{23}$$

Similarly, when $\frac{V_p}{n} < V_{SC}$, by subtracting (20) from (19), R_{eq} can be obtained to be the same as (23).

B. ENERGY CONVERSION LOSS ANALYSIS

After the balancing progress, all the quantity of electric charge Q transfers between source package and SC, from the higher voltage source to lower voltage source. In the end of the progress, total source package voltage is equal to n times voltage of SC which V_{avg} represents the equilibrium voltage value during the transition process between φ_a and φ_b .

V_{avg} can be expressed as

$$V_{avg} = V_P - \frac{Q}{C_P} = n \left(V_{SC} + \frac{nQ}{C_{SC}} \right) = \frac{n(nV_P C_P + V_{SC} C_{SC})}{n^2 C_P + C_{SC}} \quad (24)$$

Energy stored in the SC and source package before balancing is:

$$E(0) = \frac{1}{2} C_{SC} V_{SC}^2 + \frac{1}{2} C_P V_P^2 \quad (25)$$

Energy stored in the SC and source package after the process is:

$$E(\infty) = \frac{1}{2} V_{avg}^2 \left(\frac{C_{SC}}{n^2} + C_P \right) = \frac{1}{2} \frac{(nV_P C_P + V_{SC} C_{SC})^2}{n^2 C_P + C_{SC}} \quad (26)$$

The energy conversion loss is:

$$E_{loss} = E(0) - E(\infty) = \frac{1}{2} \frac{C_{SC} C_P (nV_{SC} - V_P)^2}{n^2 C_P + C_{SC}} \quad (27)$$

As it is shown in (27), the initial voltage and voltage ratio are the parameters that will affect energy conversion loss, instead of the capacitance and the ESR of the switched-capacitors or the switching frequency.

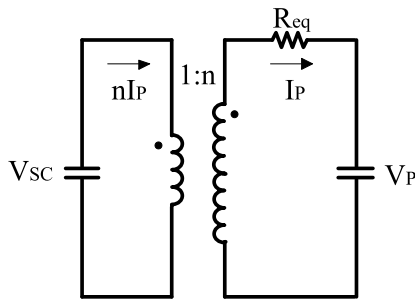


FIGURE 5. Model of the Balance circuit.

C. BALANCING DURATION ANALYSIS

As it is shown in Fig. 5, the source package and SC can be formulated to be charged or discharged between each other with a current conversion ratio, n . The voltage of the SC, V_{SC} , and source package V_P and the current of the source package I_P could be illustrated as:

$$V_{SC}(t) = V_{SC}(0) - \frac{n}{C_{SC}} \int I_P dt \quad (28)$$

$$V_P(t) = V_P(0) + \frac{1}{C_P} \int I_P dt \quad (29)$$

$$I_P = \frac{nV_{SC} - V_P}{R_{eq}} \quad (30)$$

By substituting (30) and solving (28-29) with Laplace Transform, the voltage difference $\Delta V = nV_{SC} - V_P$ during the



FIGURE 6. The experimental application for hybrid source electric vehicle.

balancing process can be expressed as

$$\frac{\Delta V(t)}{\Delta V(0)} = e^{-\left(\frac{n^2}{C_{SC}} + \frac{1}{C_P}\right) \left(\frac{1}{R_{eq}}\right) t} \quad (31)$$

Therefore, by setting a termination voltage difference $\Delta V(end)$, the duration of the balancing process can be derived from (31) and given as

$$t = -\frac{1}{\left(\frac{n^2}{C_{SC}} + \frac{1}{C_P}\right) \left(\frac{1}{R_{eq}}\right)} \ln \frac{\Delta V(end)}{\Delta V(0)} \quad (32)$$

The balancing duration is mainly decided by the capacity of the source package, SC and also the equivalent resistance of the equalizer. If t is large enough, both nV_{SC} and V_P would be very close to V_{avg} when ΔV approaches zero.

IV. SIMULATION RESULTS OF THE SWITCHED-CAPACITOR VOLTAGE EQUALIZER

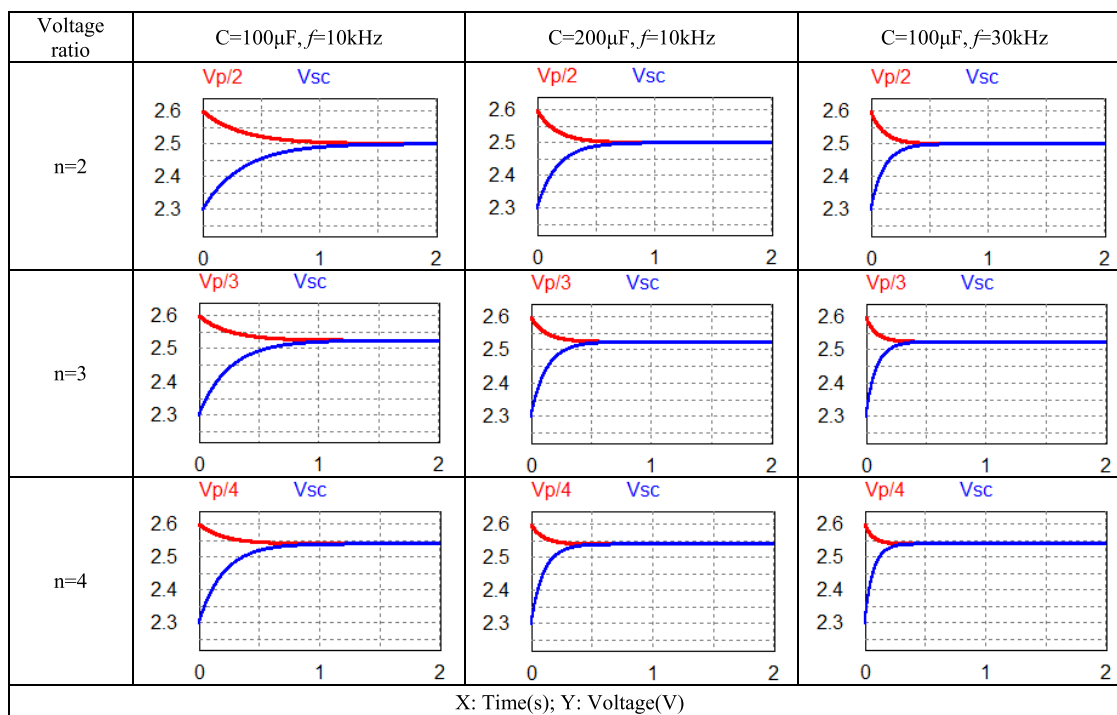
The proposed circuit is simulated by PSIM software which all the components are made ideal. The circuit topologies of voltage ratio $n = 2, 3, 4$ are built in the simulation interface. Assume the source package is composed of the SCs with the same capacitance 1F. For the switched-capacitors two parameters $C = 100\mu F$ and $220\mu F$ are used in simulation while $f = 10$ kHz and 30 kHz of the control signal are used to operate the circuit. The above configuration is only used for case study. In practical application, the composition of source energy storage package can be scaled to one's requirement and the parameters of C and f can be optimized accordingly.

In the simulation analysis, all the components are assumed to be ideal, given that $\tau_a = \tau_b = 0$, the equivalent resistance R_{eq} in (23) could be further expressed as

$$R_{eq} = \frac{n}{C_f} \quad (33)$$

Table 2 illustrates the comparison of the waveforms in the simulation varied with capacitance C , switching frequency f and n . It is observed that both V_{SC} and $\frac{V_P}{n}$ finally converge to the same voltage level in all circumstances. When C is larger, the balancing duration is comparatively shorter because the charging/discharging capacity during one switch cycle is higher. When f is larger, the switching speed is faster that accelerates the equalization process. The balancing phenomenon conforms the principles in (32).

TABLE 2. Simulation results of the switched-capacitor voltage equalizer.



X: Time(s); Y: Voltage(V)

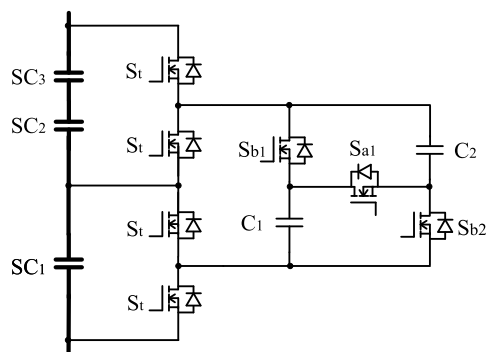


FIGURE 7. Double voltage ratio equalizer built in laboratory.

V. EXPERIMENTAL RESULTS OF THE SWITCHED-CAPACITOR VOLTAGE EQUALIZER

The proposed circuit has the capability of performing balancing for different voltage ratios and it is highly suitable for energy storage cell package where different cell voltage units are integrated into an energy storage package. To verify the validity of mathematical derivation and software simulation, a double voltage ratio balancing circuit is built in the laboratory which is shown in Fig.6, it is the energy storage package for a hybrid electric vehicle with different voltage levels. Two SCs are combined to simulate the performance of the energy source package. Topology of the equalizer is shown in Fig. 7 and the list of components is recorded in Table 3.

The voltage balancing process of the experiment is shown in Fig.8. The initial voltages of the source package and

TABLE 3. Parameters in the experiment.

Units	Quantity
Supercapacitor (DRL357S0TQ60SC)	3
Capacitance of SCs	350F
ESR of SCs	20mΩ
MOSFET (IRFR3607PBF)	7
ON-resistance of MOSFETs	7.34 mΩ
Switched-capacitor (EEHZA1H101P)	2
Capacitance of Switched-capacitors	100µF, 200µF
ESR of Switched-capacitors	28 mΩ
Switch frequency	10kHz, 30kHz

SC are 5.2V and 2.3V, respectively. After the voltage balancing is conducted, both $\frac{V_p}{2}$ and V_{SC} are balanced to the same voltage magnitude, which coincides with the results of theoretical analysis. The voltage after balance operation is 4.96V and 2.49V. The initial energy stored in the package source and SC is 3291.8J, and energy stored after balance is 3237.7J. The energy conversion loss during the experiment is 54.1J which is close to the results calculated by (27) and the efficiency is 98.4%. Fig. 9 depicts the voltage and current variations of switched-capacitors during different frequencies ($C=100\mu F, f=10\text{ kHz}$; $C=100\mu F, f=30\text{ kHz}$) and phases defined in Fig. 2. In the field test, voltage variation follows

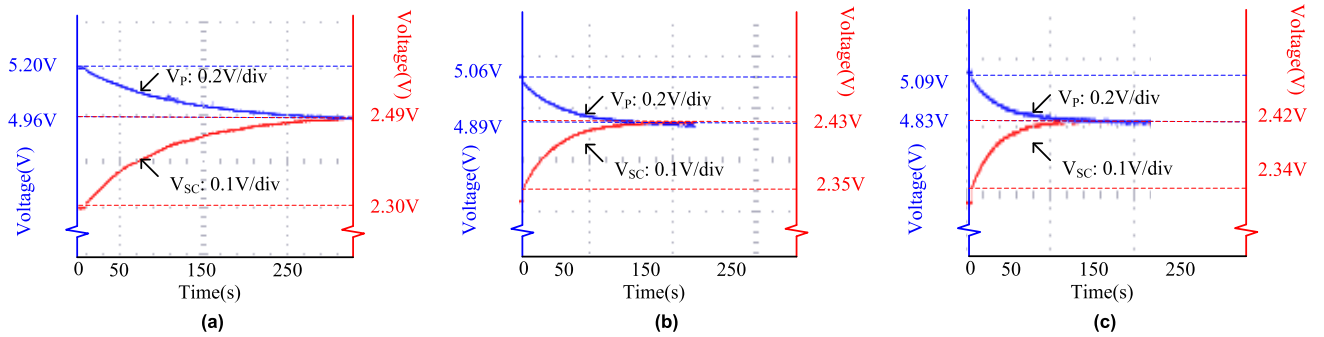


FIGURE 8. The balancing waveform from the experiment in the laboratory (a) $C=100\mu\text{F}$, $f=10\text{ kHz}$; (b) $C=200\mu\text{F}$, $f=10\text{ kHz}$; (c) $C=100\mu\text{F}$, $f=30\text{ kHz}$.

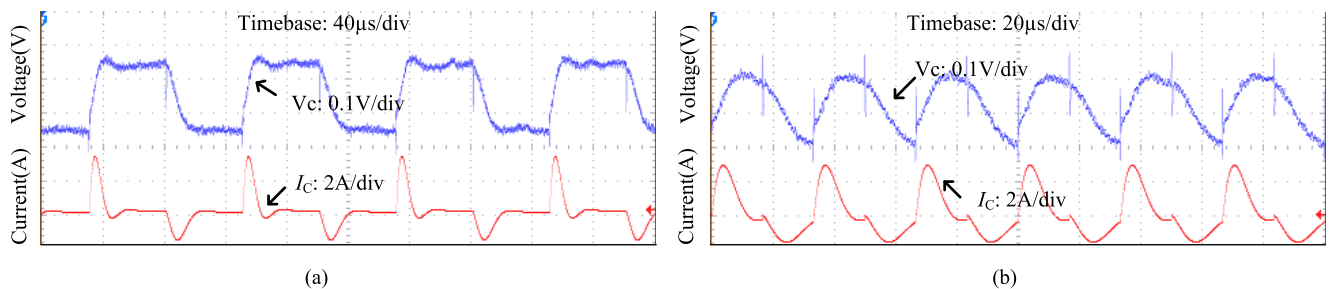


FIGURE 9. The voltage V_C and current I_C waveform of switched-capacitor C_1 during the balancing progress (a) $C=100\mu\text{F}$, $f=10\text{ kHz}$; (b) $C=100\mu\text{F}$, $f=30\text{ kHz}$.

the functions (3) and (15) while current variation conforms to (4) and (16). The experiment results demonstrate that the variation of both voltage and current is conformed to the charging/discharging principles in each phase.

VI. CONCLUSION

In this paper, series-parallel circuit configuration and operation principles of the innovative switched-capacitor voltage equalizer are demonstrated to effectively promote the use of hybrid source package composed of different cells. The equivalent circuit of the balancing model is described to show the process of voltage balancing. The key of the model is the use of an equivalent resistor which corresponds to the switching frequency and capacitance. The switching frequency and capacitance can be further adjusted to obtain the desired operation performance. An equalizer prototype for a package of energy sources with double voltage ratio is built in practical experiment to substantiate the validity of theoretical analysis. This innovative voltage equalizer is proved to be efficient and practical for industrial application. With the coming high demand in energy storage for mobility and renewable energy, the proposed technology provides a future development tool for non-equal cell integration. The components used in balancing is low-cost and of high efficiency.

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