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Modeling and Performance Analysis of Shielded Differential Annular Through-Silicon Via (SD-ATSV) for 3-D ICs

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ABSTRACT A shielded-differential annular through-silicon via (SD-ATSV) is proposed and investigated. The equivalent circuit model is developed with the influence of the electrically floating silicon substrate taken into account. By virtue of the circuit model, the frequency- and time-domain electrical characterizations of the SD-ATSV are conducted. Furthermore, the thermo-mechanical stress of the SD-ATSV is captured and compared with that of the shielded-differential cylindrical through-silicon via. It is demonstrated that by utilizing the SD-ATSV, the keep-out zone can be reduced without performance degradation.

INDEX TERMS Shielded differential annular through-silicon via (SD-ATSV), MOS capacitance, floating silicon substrate, thermal stress, keep-out zone (KOZ).

I. INTRODUCTION

Through-silicon via (TSV), a key interconnect technique for enabling the implementation of three-dimensional integrated circuits (3-D ICs), has gained intense interests in recent years. In comparison with the conventional planar ICs, the TSV-based 3-D ICs have various advantages, including higher integration density, shorter interconnect length, better noise immunity, lower power consumption, and faster data communication [1]. More importantly, the heterogeneous integration of multi-chip modules (e.g., sensors, memory, logic, and radio frequency circuits) becomes possible through the TSV techniques [2].

However, there are several challenges in the real-world applications of TSVs, such as noise coupling among TSVs and electromagnetic interference (EMI) problems, which may result in a wrong logic function switch [3], [4]. Moreover, as the operating frequency increases to improve the bandwidth per channel, these signal integrity problems become more severe. To cope with these problems, several techniques such as coaxial TSV have been proposed and extensively investigated [5]–[10]. It is evident that the concept of coaxial TSV was inspired from the coaxial cable with the self-shielding function. Differential signaling scheme is also an effective solution due to its immunity to the common-mode noise and its EMI reduction [11], [12]. By combining advantages of the coaxial TSV and differential signaling, the shielded-differential through-silicon via (SD-TSV) was proposed and studied [13]–[15]. As ground-signal-signal-ground (GSSG)-type TSVs are inevitably affected by the neighboring TSVs [16], it can be expected that the SD-TSV can provide better noise immunity than the GSSG-type TSVs at the expense of area occupation. The SD-TSV can be very useful when high-quality signal is required.

On the other hand, it is well known that thermal mismatch stresses are inevitable as various materials with different mechanical properties are used in the fabrication of TSVs [17]. These thermal stresses may affect the carrier mobility in the active silicon substrate [18]. Therefore, the keep-out zone (KOZ), i.e., logic forbidden area, is induced around each TSV [19]. In comparison with the conventional cylindrical TSV, annular TSV (ATSV) is demonstrated to induce lower KOZ [20]. Therefore, a coaxial-annular TSV was proposed in [21], with its wideband electromagnetic model developed in [22]. To reduce the KOZ of the conventional SD-TSV, a scheme of shielded differential ATSV (SD-ATSV), which is composed of a pair of inner

ATSVs as the signal transmission paths and an outer shielding shell as the current return path, is herein proposed.

Similar to other kinds of TSVs, the inner ATSVs and outer shielding shell of the SD-ATSV are surrounded by thin oxide layers to prevent leakage current, and the metal-oxide-semiconductor (MOS) structures are thereby formed. According to MOS theory, the parasitic capacitance of the TSV decreases with increasing bias voltage, which has been neglected in early studies [14], [15]. Moreover, for the SD-ATSV with no substrate contacts on the inner silicon, the electric field is from inner ATSVs to the outer shielding shell, i.e., the inner silicon substrate is electrically floating [23]–[25]. Under such circumstances, the minority carriers in the silicon substrate (e.g., electrons in the *p*-type silicon) flow alternatively between the signal and ground vias with varying bias voltage, which makes the TSV capacitance more complicated. It is evident that the influence of the floating silicon substrate on the electrical characteristics of the SD-ATSV should be taken into account.

The aim of this work is to accurately model the SD-ATSV in a wideband frequency range. The rest of this paper is organized as follows. In Section II, the equivalent circuit model of the SD-ATSV is presented, with the nonlinear MOS capacitance treated appropriately by using the symbolically-defined device (SDD) block. Based on the circuit model, the frequency- and time-domain analyses of the SD-ATSV are carried out in Section III. Furthermore, the thermo-mechanical characteristics of the SD-ATSV are captured and compared with that of the conventional SD-TSV in Section IV. Finally, some conclusions are drawn in Section V.

II. CIRCUIT MODEL OF SD-ATSV

The top cross-sectional view of the SD-ATSV and the insight view of an inner ATSV are depicted in Fig. 1, with the related geometrical parameters explained in Table 1. A SD-ATSV is comprised of a pair of inner ATSVs and an outer shielding shell. Herein, the inner ATSVs act as the differential transmission lines and the outer shielding shell serves as the current return path. Each metal via is surrounded by two oxide layers (usually SiO_2) for DC isolation. A metal-oxide-semiconductor (MOS) structure is formed, i.e., a depletion region appears when the bias voltage exceeds the flat-band voltage [26], [27]. The width of the depletion region is determined by the bias voltage, substrate doping concentration, and environment temperature.

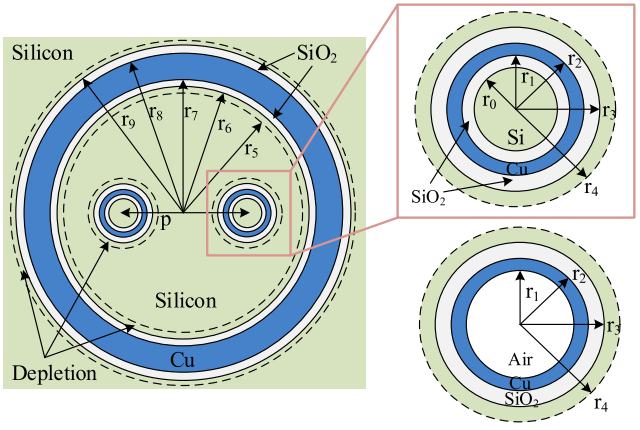

FIGURE 1. Top cross-sectional view of the SD-ATSV and the insight view of an inner ATSV.

TABLE 1. Structural Parameters with their Symbols for the SD-ATSV.

Symbol	Definition
h_{TSV}	TSV height
p	Pitch between two inner signal ATSVs
t_{ox}	Oxide thickness
w_{dep1}	Depletion width of the ATSV
w_{dep2}	Depletion width of the shielding shell
r_0	Inner oxide radius of the ATSV ($= r_1 - t_{ox}$)
r_1	Inner metal radius of the ATSV
r_2	Outer metal radius of the ATSV
r_3	Outer oxide radius of the ATSV ($= r_2 + t_{ox}$)
r_4	Depletion radius of the ATSV ($= r_3 + w_{dep1}$)
r_5	Inner depletion radius of the shielding shell ($= r_6 - w_{dep1}$)
r_6	Inner oxide radius of the shielding shell ($= r_7 - t_{ox}$)
r_7	Inner metal radius of the shielding shell
r_8	Outer metal radius of the shielding shell
r_9	Outer oxide radius of the shielding shell ($= r_8 + t_{ox}$)

From the fabrication perspective, the deep etching process of silicon is one of the fundamental steps for manufacturing SD-ATSV. Although there is no experimental demonstration of the SD-ATSV, the annular trench has been successfully realized, and the TSV aspect ratio continuously increases [28]–[31]. By etching the inner and outer annular trenches simultaneously, the SD-ATSV can be fabricated using the conventional TSV process technology [32]. However, it is very difficult to etch the annular trenches for the inner signal vias due to their large ratio of trench depth to width. This issue can be resolved by etching vias and partially filling Cu inside. By adopting appropriate filling conditions, the inner ATSVs can be built by electroplating Cu on the sidewalls of the vias [33], [34]. In this scenario, the silicon/silicon oxide substrate inside the ATSVs is replaced with air, as shown in Fig. 1. As demonstrated in [35], the material inside the ATSVs has negligible influence on the electrical characteristics, so the modeling procedure of such SD-ATSV is the same as that of the original SD-ATSV.

A. IMPEDANCE EXTRACTION

Fig. 2 shows the equivalent circuit model of the SD-ATSV. It is worth noting that the depletion layers inside the inner ATSVs and outside the shielding shell can be ignored as they have little impact on the overall admittance [35]. The impedance of an inner signal ATSV is given as [36]

$$Z_{\mathrm{ATSV}} = \frac{e^{j\pi/4}}{\pi}\sqrt{\frac{\omega\mu_0}{\sigma_m r_2^2}}\cdot\frac{I_0^1(Tr_2)\,I_1^2(Tr_1)+I_1^1(Tr_1)\,I_0^2(Tr_2)}{I_1^1(Tr_2)\,I_1^2(Tr_1)-I_1^1(Tr_1)\,I_1^2(Tr_2)} \tag{1}$$

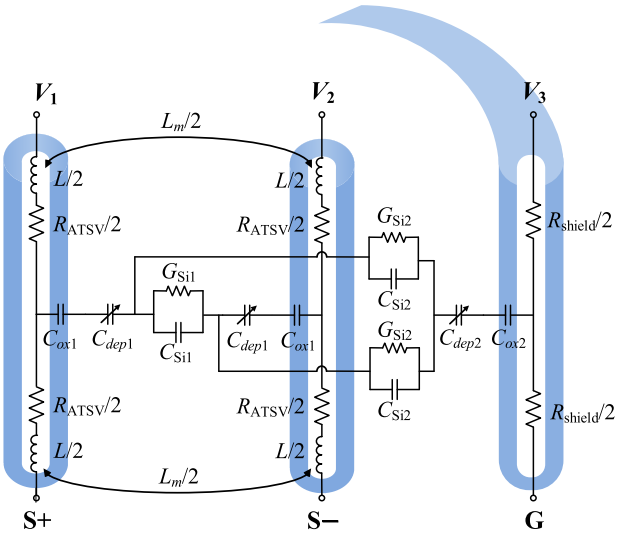

FIGURE 2. Equivalent circuit model of the SD-ATSV.

where $T = \sqrt{\omega\mu_0\sigma_m}e^{j\pi/4}$, ω is the angular frequency, μ_0 is the permeability in vacuum, σ_m is the conductivity of the filling conductive material (usually Cu), and $I_i^j(\cdot)$ $(i, j = 1,$ and 2) is the modified Bessel function of the kind j of order i.

The resistance R_{TSV} and the internal inductance L_{in} of an inner ATSV could be calculated by

$$Z_{\mathrm{ATSV}} = R_{\mathrm{ATSV}} + j\omega L_{in,\mathrm{ATSV}} \tag{2}$$

Similarly, the impedance Z_{shield} of the shielding shell can be calculated by replacing r_1 and r_2 with r_7 and r_8 in (1). The external inductance induced by the ATSV and the shielding shell can be calculated as [37], [38]

$$L_{ex} = \frac{\mu_0}{2\pi}\ln\left(\frac{r_7^2 - (p/2)^2}{r_7 r_2}\right) \tag{3}$$

The loop inductance L between the ATSV and the shielding shell can be given as [39]

$$L = L_{in,\mathrm{ATSV}} + L_{in,\mathrm{shield}} + L_{ex} \tag{4}$$

The mutual inductance between two ATSVs can be obtained as [40]

$$L_m = L_{m,ex} + k\left(L_{in,\mathrm{ATSV}} + L_{in,\mathrm{shield}}\right) \tag{5}$$

Herein, the mutual external inductance $L_{m,ex}$ and the coupling coefficient k can be calculated as [14]

$$L_{m,ex} = \frac{\mu_0}{2\pi}\ln\left(\frac{r_4^2 + (p/2)^2}{r_4 p}\right) \tag{6}$$

$$k = \frac{L_{m,ex}}{L_{ex}} \tag{7}$$

B. ADMITTANCE EXTRACTION

As aforementioned, the depletion layers appear when the bias voltage exceeds the flat-band voltage. Considering the influence of floating silicon substrate, the extraction of the parasitic capacitance is described in the following.

The relationship between the initial surface potential φ_{s0} and the initial oxide potential drop V_{ox0} can be expressed as

$$\varphi_{ms} = -\left(V_{ox0} + \varphi_{s0}\right) \tag{8}$$

where φ_{ms} refers to as the work function difference between the TSV filling conductive material and the silicon substrate. φ_{ms} can be calculated by [41]

$$\varphi_{ms} = \varphi_m - \chi - \frac{E_g}{2q} - \frac{kT}{q}\ln\left(\frac{N_a}{n_i}\right) \tag{9}$$

where φ_m is the work function of TSV filling conductive material, q is the elementary positive charge, k is Boltzmann's constant, T is the temperature, χ and E_g are the electro affinity and energy gap of the silicon substrate, respectively, N_a is the doping concentration of the silicon substrate (which is assumed as 1.25×10^{15} cm^{-3} therein), and n_i is the intrinsic carrier concentration which can be obtained as [8]

$$n_i = 9.38\times10^{19}\left(\frac{T}{300}\right)^2 e^{-\frac{6884}{T}}. \tag{10}$$

As shown in Fig. 2, V_i $(i = 1,$ 2, and 3) denotes the bias voltage applied on each ATSV and the shielding shell. Here, the zero-field potential in the silicon substrate is defined as V_{sub}, and after the bias voltage is applied, the following relationships can be obtained as

$$V_1 - V_{sub} = V_{ox1} + \varphi_{s1} + \varphi_{ms} \tag{11}$$

$$V_2 - V_{sub} = V_{ox2} + \varphi_{s2} + \varphi_{ms} \tag{12}$$

$$V_3 - V_{sub} = V_{ox3} + \varphi_{s3} + \varphi_{ms} \tag{13}$$

where $\varphi_{s,i}$ and $V_{ox,i}$ $(i = 1,$ 2, and 3) represent the surface potential and the oxide voltage drop, respectively. The bias voltages could be calculated by mathematically eliminating V_{sub} and figuring out other unknown variables.

Since the TSV height is much larger than its diameters, the electrostatics of the TSV surrounded by electrically floating silicon substrate can be obtained by solving the following Poisson equations [40], [42]

$$\frac{1}{\rho}\frac{\partial}{\partial\rho}\left(\rho\frac{\partial\varphi(\rho)}{\partial\rho}\right) = \frac{q}{\varepsilon_{\mathrm{Si}}}\left[p_0 - \frac{n_i^2}{p_0} + n(\rho) - p(\rho)\right] \tag{14}$$

with the boundary conditions:

$$\varphi(r_4) = 0 \tag{15}$$

$$\varphi(r_5) = 0 \tag{16}$$

$$\varphi(r_3) = \varphi_{s1} = \varphi_{s2} \tag{17}$$

$$\varphi(r_6) = \varphi_{s3} \tag{18}$$

where $\varphi(\rho)$ denotes the potential of radius ρ, $\varepsilon_{\mathrm{Si}}$ is the permittivity of silicon, and $p(\rho)$ and $n(\rho)$ are functions of $\varphi(\rho)$ as follows:

$$p(\rho) = N_a e^{\frac{-q\varphi(\rho)}{kT}} \tag{19}$$

$$n(\rho) = \frac{n_i^2}{N_a}e^{\frac{q\varphi(\rho)}{kT}} \tag{20}$$

The surface electric field ξ_s and the total surface charge Q_s can be defined as functions of the temperature T and the surface potential φ_s [42]

$$\xi_s(\varphi_s, T) = \frac{\varphi_s}{\rho_s} + \sqrt{\left(\frac{\varphi_s}{\rho_s}\right)^2 2F(\varphi_s, T)} \tag{21}$$

$$Q_s(\varphi_s, T) = -2\pi\rho_s h_{\mathrm{TSV}}\varepsilon_{\mathrm{Si}} \cdot \xi_s(\varphi_s) \tag{22}$$

where $F(\varphi_s, T)$ is derived by integrating equation (14) from zero to silicon surface, and ρ_s denotes the radius of oxide/depletion interface.

Considering an enclosed Gaussian box that consists of the metal, oxide and silicon substrate interfaces, the net charge enclosed inside the box must be zero (since the electric field outside the box is zero) [23]:

$$Q_m(T) + Q_{ox} = -Q_s(\varphi_s, T) \tag{23}$$

The total charge Q_{ox} of the oxide layer is herein set as zero, so the accumulated charges on the metal surface Q_m could be obtained. Thus, the oxide voltage drops $V_{ox,i}$ can be calculated as [23]

$$V_{ox,i} = \frac{Q_m(T)}{C_{ox,i}} \quad (i = 1, 2, \text{and } 3) \tag{24}$$

where $C_{ox,i}$ is the oxide capacitance and can be calculated by

$$C_{ox1,2} = \frac{2\pi\varepsilon_{\mathrm{Si}} h_{\mathrm{TSV}}}{\ln(r_2/r_3)}, \quad \text{for signal ATSVs} \tag{25}$$

$$C_{ox3} = \frac{2\pi\varepsilon_{\mathrm{Si}} h_{\mathrm{TSV}}}{\ln(r_7/r_6)}, \quad \text{for shielding shell} \tag{26}$$

According to the conservation law of charge, one has

$$\begin{aligned} &C_{ox2}\,(V_{ox3} - V_{ox0}) \\ &\quad = -C_{ox1}\,(V_{ox1} - V_{ox0}) - C_{ox1}\,(V_{ox2} - V_{ox0})\,. \end{aligned} \tag{27}$$

Therefore, by using the method of simultaneous equations (8)-(13) and (23)-(27), the relationship of the bias voltage V_i applied to the SD-ATSV can be calculated as follows:

$$V_1 = \varphi_{s1} - \varphi_{s3} - V_{ox1} + V_{ox3} + 2V_{ox0} \tag{28}$$

$$V_2 = \varphi_{s2} - \varphi_{s3} - V_{ox2} + V_{ox3} + 2V_{ox0} \tag{29}$$

$$V_3 = \varphi_{s1} - \varphi_{s3} - V_{ox1} + V_{ox3} - 2V_{ox0} \tag{30}$$

Furthermore, the depletion capacitances can be obtained as

$$C_{dep1,2}(T) = \left.\frac{\mathrm{d}Q_s(\varphi_s, T)}{\mathrm{d}\varphi_s}\right|_{r=r_3}, \quad \text{for signal ATSVs} \tag{31}$$

$$C_{dep3}(T) = \left.\frac{\mathrm{d}Q_s(\varphi_s, T)}{\mathrm{d}\varphi_s}\right|_{r=r_6}, \quad \text{for shielding shell} \tag{32}$$

The MOS capacitances of each signal ATSV and shielding shell can be obtained by cascading the oxide capacitance of oxide and the depletion capacitance, i.e.,

$$C_i(T) = \left(\frac{1}{C_{ox,i}} + \frac{1}{C_{dep,i}(T)}\right)^{-1}, \quad i = 1, 2, \text{and } 3. \tag{33}$$

Then, the depletion widths can be calculated by

$$w_{dep1,2} = r_3\left(e^{\frac{2\pi\varepsilon_{\mathrm{Si}} h_{\mathrm{TSV}}}{C_{dep1,2}}} - 1\right), \quad \text{for signal A-TSVs} \tag{34}$$

$$w_{dep3} = r_6\left(1 - e^{-\frac{2\pi\varepsilon_{\mathrm{Si}} h_{\mathrm{TSV}}}{C_{dep3}}}\right), \quad \text{for shielding shell} \tag{35}$$

Based on the theory of multiconductor transmission line, the substrate capacitance can be obtained as [38]

$$\begin{bmatrix} L' & L'_m \\ L'_m & L' \end{bmatrix} \cdot \begin{bmatrix} C_{\mathrm{Si2}} + C_{\mathrm{Si1}} & -C_{\mathrm{Si1}} \\ -C_{\mathrm{Si1}} & C_{\mathrm{Si2}} + C_{\mathrm{Si1}} \end{bmatrix} = \mu_0\varepsilon_{\mathrm{Si}} \begin{bmatrix} 1 & 0 \\ 0 & 1 \end{bmatrix} \tag{36}$$

where C_{Si1} and C_{Si2} are the capacitance between two ATSVs and between a ATSV and shielding shell, respectively. The inductances can be calculated by

$$L' = \frac{\mu_0}{2\pi}\ln\left(\frac{r_5^2 - (p/2)^2}{r_5 r_4}\right) \tag{37}$$

$$L'_m = \frac{\mu_0}{2\pi}\ln\left(\frac{r_5^2 - (p/2)^2}{r_5 p}\right) \tag{38}$$

The substrate conductance $G_{\mathrm{Si},i}$ ($i = 1$ and 2) can be obtained as

$$G_{\mathrm{Si},i} = \frac{\sigma_{\mathrm{Si}}}{\varepsilon_{\mathrm{Si}}} C_{\mathrm{Si},i} \quad (i = 1 \text{ and } 2)\,. \tag{39}$$

where σ_{Si} is the silicon conductivity and can be calculated by

$$\sigma_{\mathrm{Si}} = qN_a\left[47.7 + \frac{477.3}{1 + \left(\frac{N_a}{6.3\times10^{16}}\right)^{0.76}}\right]\left(\frac{T}{300}\right)^{-1.5} \tag{40}$$

Therefore, the admittance of the SD-ATSV can be extracted. Here, the SD-ATSVs under two different geometrical configurations A and B are considered, and their dimensions are given in Table 2. As the annular trenches have been fabricated in [28] and [29], and the TSV aspect ratio is expected to reach 20:1 [31], it is feasible to fabricate the SD-ATSV of configuration A. The inner ATSVs can be obtained by electroplating Cu layer on the sidewalls of the vias [34]. Furthermore, the influence of the SD-ATSV scaling is considered by shrinking it to about 5 times smaller (see Column 2 in Table 2). It is worth noting that the circuit model in Fig. 2 is scalable as all the elements have physical significance.

Consider an inner ATSV of the SD-ATSV with configuration A. Fig. 3(a) plots the relationship between the surface charge density ($Q_{sd} = Q_s/(2\pi\rho_s h_{\mathrm{TSV}})$) and the surface potential. It can be seen that, at the static/low frequencies (<10 MHz), the curves of the surface charge density can be divided into three regions: accumulation, depletion, and inversion regions. The flatband and threshold voltages are introduced at the turning points of three regions. The flatband voltage can be calculated by (9), while the threshold voltage is obtained at the threshold condition, i.e., $\varphi_s = (2kT/q)\cdot\ln(N_a/n_i)$. For high frequency signals (>10 MHz), however, the surface charge density remains unchanged as the

TABLE 2. Dimensions of SD-ATSV (Unit: μm).

Configurations	A	B
h_{TSV}	100	20
p	30	6
r_0	7.8	1.3
r_1	8	1.5
r_2	10	2
r_3	10.2	2.2
r_6	59.8	11.8
r_7	60	12
r_8	65	13
r_9	65.2	13.2

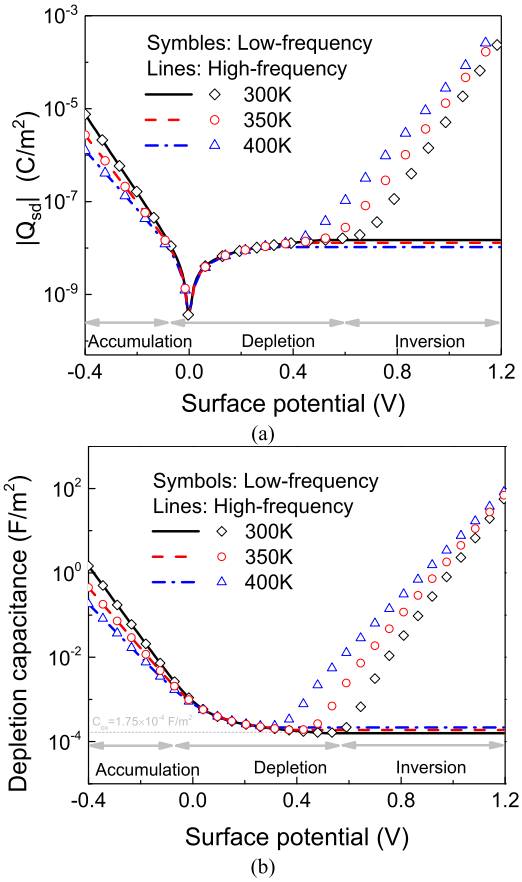

FIGURE 3. (a) Surface charge densities and (b) depletion capacitances of a signal ATSV versus surface potential for different temperatures.

bias voltage exceeds the threshold voltage. This is because the minority carrier generation rate cannot keep up with the high frequency signals, and therefore, the surface charge density increases slightly with the potential in the inversion region [23].

In order to gain insight into the relationship between the surface charge density and the depletion capacitance, Fig. 3(b) depicts the depletion capacitance versus the surface potential. Similarly, the curve of the depletion capacitance can also be divided into three regions mentioned above. The depletion capacitance decreases in both the accumulation and depletion regions. In the inversion region, it increases

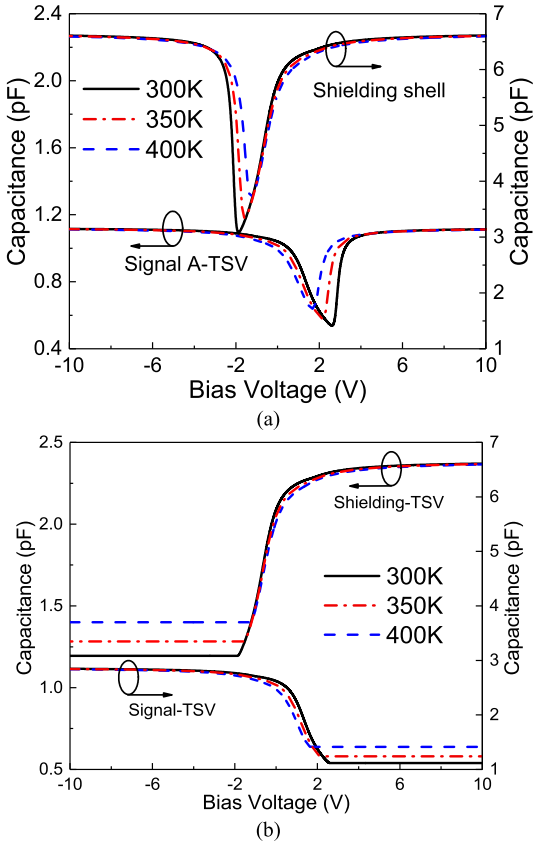

FIGURE 4. *C-V* curves of the SD-ATSV for different temperatures at (a) static/low frequency (<10 MHz) and (b) high frequency (>10 MHz).

and remains unchanged at low and high frequencies, respectively. As the temperature increases, the depletion capacitance decreases in the accumulation region and increases in the inversion region. The temperature rise leads to an increased ratio of $(\varphi_s/\rho_s)^2$ to $F(\varphi_s)$, thereby resulting in a wider inversion region and decreased threshold voltage [42]. Moreover, the oxide capacitance $C_{ox} = 1.75 \times 10^{-4}$ F/m^2 is illustrated in Fig. 3(b). It is worth noting that the depletion capacitance is much larger than the oxide capacitance in the accumulation region and the low frequency inversion region. As the TSV capacitance is a series combination of the oxide and depletion capacitances, it can be predicted that the TSV capacitance is almost unchanged in these regions.

Figs. 4(a) and (b) show the capacitance-voltage (C-V) curves of the SD-ATSV at low and high frequencies, respectively. Similarly, the C-V curves can be divided into the accumulation, depletion, and inversion regions. It can be seen from Fig. 4(a) that at static/low frequency, with the increasing bias voltage, the MOS capacitance is initially the oxide capacitance, then decreases as the bias voltage exceeds the flat-band voltage, and finally increases to the oxide capacitance as the bias voltage exceeds the threshold voltage. For high-frequency signal, the MOS capacitance is kept at its minimum value in the inversion region. The impact of temperature variation on the C-V curves of the SD-TSV is also illustrated, as shown in Fig. 4. It is evident

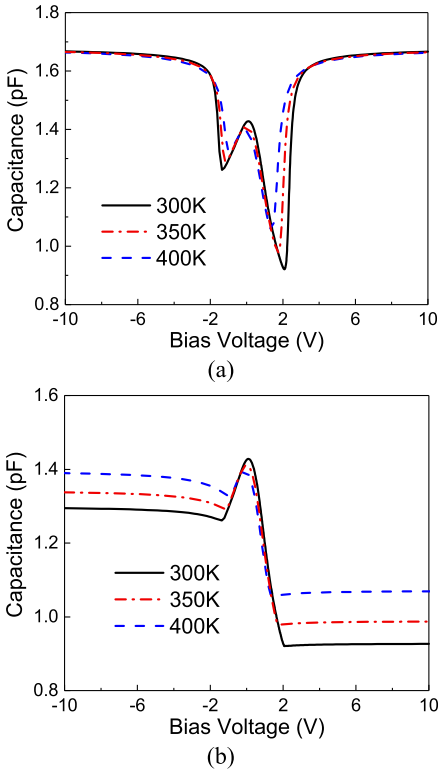

FIGURE 5. Total MOS capacitance of the SD-ATSV for different temperatures at (a) Static/low frequency (<10MHz) and (b) high frequency (>10MHz).

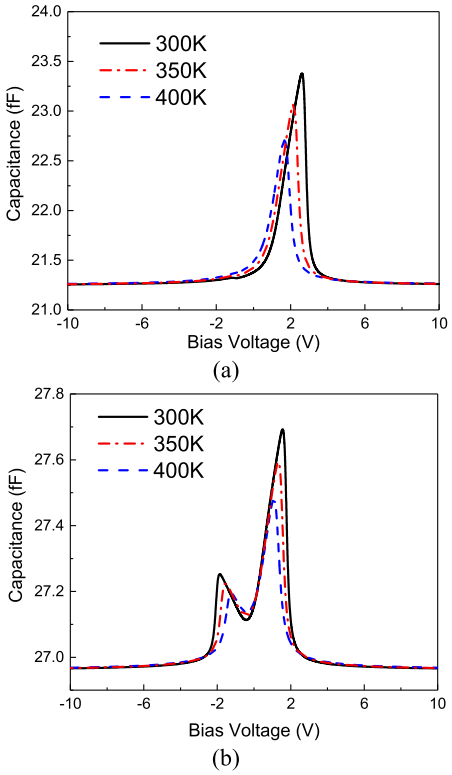

FIGURE 6. Silicon capacitance between (a) two inner ATSVs and (b) an inner ATSV and the outer shielding shell for different temperatures at low frequency (<10 MHz).

that the oxide capacitance is independent with the temperature variation, while the depletion capacitance increases with the temperature in the inversion region.

Furthermore, the total MOS capacitance of the SD-ATSV, which can be calculated by $C_{\text{Total}} = \left[(C_1 + C_2)^{-1} + (C_3)^{-1}\right]^{-1}$, is plotted in Fig. 5. It can be seen that, at low-frequency, the total MOS capacitances in the range of $|\text{V}| > 3\text{V}$ are almost unchanged as the temperature increases. This is because when $|V| > 3\text{V}$, the depletion region is not formed, and the MOS capacitance is equal to $\left[(C_{ox1} + C_{ox2})^{-1} + (C_{ox3})^{-1}\right]^{-1}$, where the oxide capacitances are independent with the temperature variation. However, as shown in Fig. 5(b), for high frequency signal, the total MOS capacitance increases with the temperature at the two end regions of the curve, and decreases around the central region.

Figs. 6(a) and (b) show the low-frequency silicon capacitances between two inner ATSVs and between an inner ATSV and the outer shielding shell, respectively. It is found that the silicon capacitance at the two end regions of the curve is kept almost unchanged with the temperature rise. The maximum value occurs around the central region, and it decreases significantly with the increasing temperature. Note that the load capacitance between signal and ground in the SD-ATSV is a series combination of the MOS capacitance and the silicon capacitance. As the silicon capacitance is much smaller than the MOS capacitance, the load capacitance is mainly determined by the silicon capacitance, and therefore is in the range of several tens of femtofarads (fF).

III. ELECTRICAL CHARACTERISTICS

A. FREQUENCY-DOMAIN ANALYSIS

For frequency-domain analysis of the SD-ATSV, a four-port single-ended model shown in Fig. 2 is employed. After extracting the four-port mixed-mode S-parameters, the differential- and common-mode S-parameters can be computed. The proposed model is validated using a commercial full-wave electromagnetic simulation tool (HFSS [43]) with the two set of geometrical configurations as listed in TABLE 2.

Figs. 7 and 8 show the magnitudes of differential- and common-mode S_{11} and S_{21} of configurations A and B for three different cases: 1) without depletion (i.e., w_{dep} equals to zero); 2) nonlinear depletion (i.e., w_{dep} is a function of bias voltage); and 3) maximum depletion (i.e., w_{dep} equals to its maximum value). In the figures, the HFSS simulation results are labeled by symbols, while the results obtained from the circuit model are plotted using lines. It is evident that the modeled and simualted results agree well with each other. Note that the case of nonlinear depletion cannot be simulated using the HFSS as the capacitance is voltage dependent. It is demonstrated that ignoring the voltage-dependent

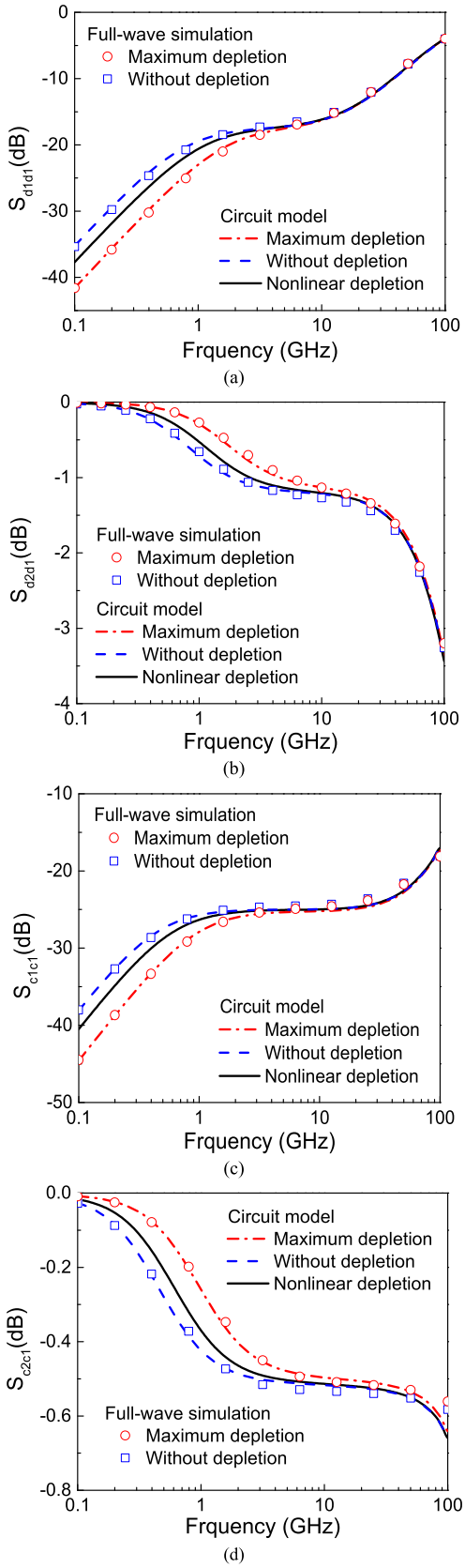

FIGURE 7. (a) S_{d1d1}, (b) S_{d2d1}, (c) S_{c1c1}, and (d) S_{c2c1} of configuration A for different cases.

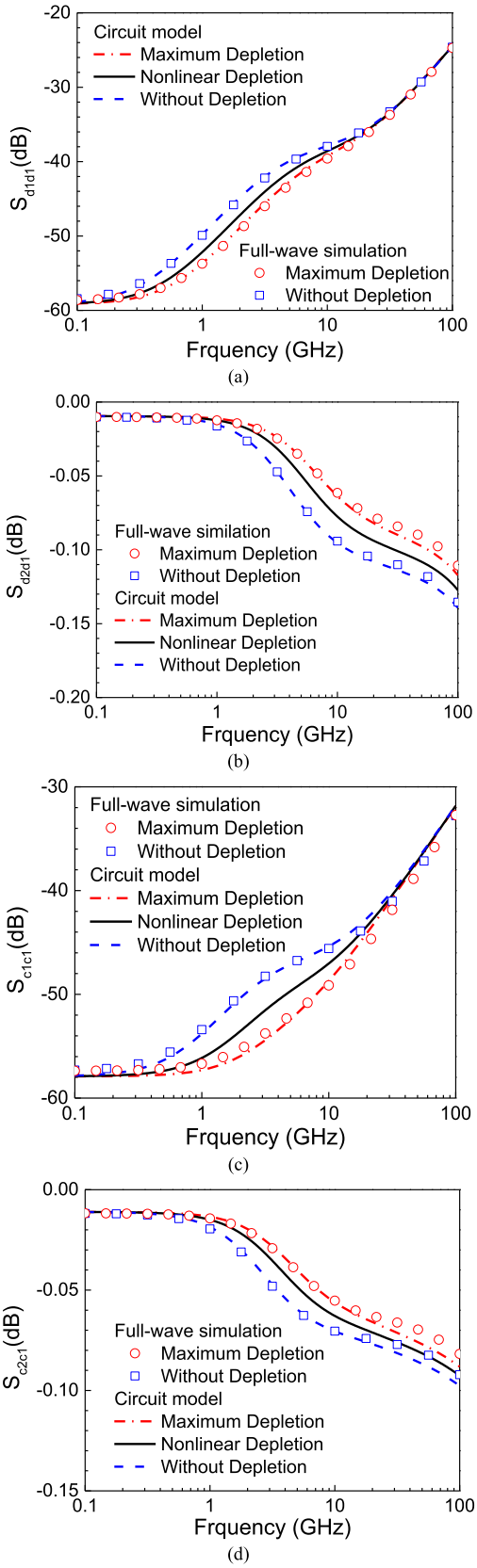

FIGURE 8. (a) S_{d1d1}, (b) S_{d2d1}, (c) S_{c1c1}, and (d) S_{c2c1} of configuration B for different cases.

MOS capacitance would lead to inaccuracy for both differential- and common-mode S-parameters.

Moreover, the impact of temperature variation on the S-parameters of the SD-ATSV with floating inner silicon is illustrated in Fig. 9. It is found that both the differential- and common-mode insertion losses are reduced with the increasing temperature, which is mainly attributed to the decreased silicon conductivity according to (40).

B. TIME-DOMAIN ANALYSIS

Taking the SD-ATSV of configuration A (see Table 2) for example, the time-domain analysis is performed in this subsection. Fig. 10(a) shows a symbolical differential transmission line model of the inner ATVs. A set of low voltage differential signal (LVDS), which is comprised of two sets of low square-wave voltage sources (V_p and V_n) with opposite polarity, is used as the input voltage. Herein, V_p is the source voltage with positive polarity. It has a fundamental frequency of 2 GHz (i.e., a period T of 500 ps), and its amplitude is from 0.45 V to 0.75 V with both rising and falling times of 50 ps. V_n is a reverse polarity voltage with respect to V_p. The output voltages (V_p' and V_n') can be captured as LVDS transmits along the two ATSVs.

The nonlinear capacitance of the inner ATSVs and the outer shielding shell C_i ($i = 1, 2, 3$) in (33) can be derived by solving the following equation:

$$i_i(t) = C_i(V_{\mathrm{TSV}}(t)) \frac{dv_i(t)}{dt}, \quad i = 1, 2, \text{and } 3. \tag{41}$$

where $i_i(t)$ is the current flowing through the oxide and depletion capacitances and $v_i(t)$ is the voltage between the ends of two capacitances. Fig. 10(b) shows the Symbolically-defined devices (SDD) block in the Keysight ADS [44], which can be used to model the nonlinear MOS capacitances of the SD-ATSV.

The transient waveforms of the SD-ATSV with electrically floating silicon substrate can be obtained by using the same method proposed in [45]. As shown in Fig. 11, the output voltage of each ATSV (V_p' and V_n') is an imperfect square-wave voltage. The different-mode voltage (V_{diff}) and the common-mode voltage (V_{comm}) are given as

$$V_{\mathrm{diff}} = V_p' - V_n', \tag{42}$$

$$V_{\mathrm{comm}} = \frac{1}{2}\left(V_p' + V_n'\right). \tag{43}$$

Fig. 12 shows the transient waveforms of the output voltages for three cases mentioned above. In order to validate the circuit model, the S-parameters from HFSS are imported into the S4P block in ADS to perform a time-domain simulation. It is evident that the results obtained from the circuit model and the S4P simulation agree well with each other. From Fig. 12, it can be seen that the voltages of three cases may lead to about 5% difference. This phenomenon can be readily explained by Fig. 13. The total MOS capacitance of the SD-ATSV with the floating inner silicon is approximately

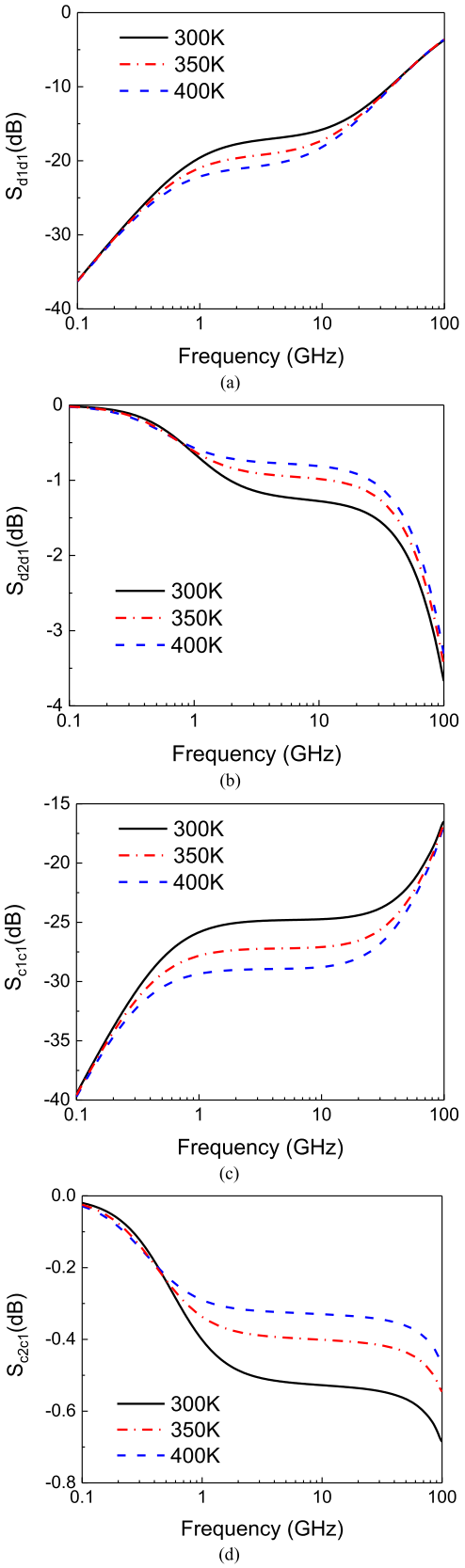

FIGURE 9. (a) S_{d1d1}, (b) S_{d2d1}, (c) S_{c1c1}, and (d) S_{c2c1} of configuration A for different temperatures.

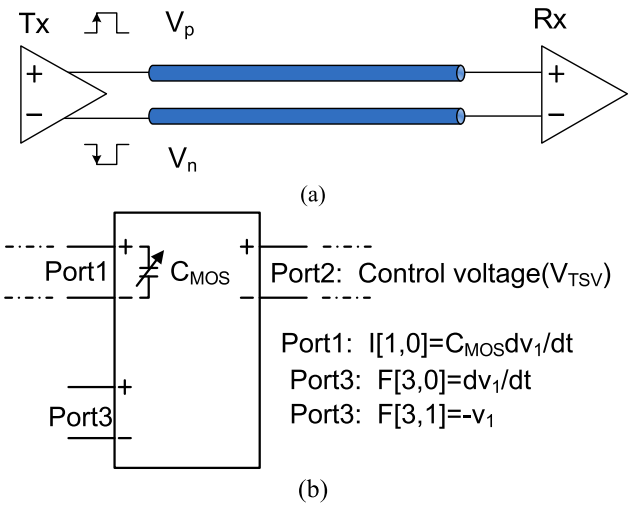

FIGURE 10. (a) Symbolical differential transmission line model. (b) SDD block used for modeling the voltage-based MOS capacitance.

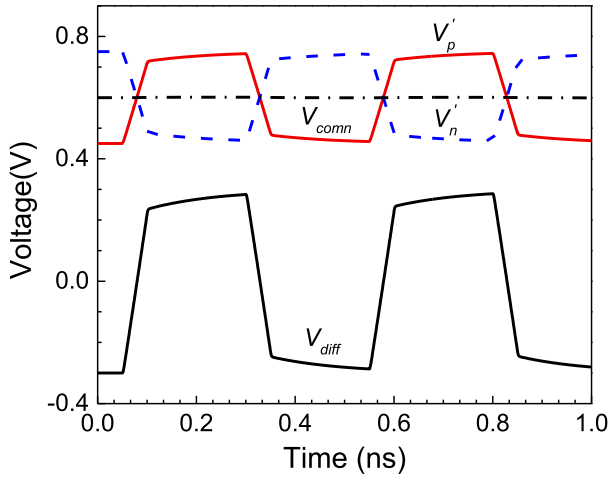

FIGURE 11. Transient waveforms of the output voltage.

located at the middle level of the maximum and minimum values.

As the number of stacking layers increases, the impacts of floating silicon substrate on the transient output voltage waveforms become more significant, as shown in Fig. 14. Moreover, Fig. 15 depicts the transient output voltage waveforms of the SD-ATSV for different temperatures. As the temperature rises, the silicon conductivity decreases, thereby leading to lower signal leakage and increased output voltage amplitude.

IV. COMPARISON WITH SD-TSV

In this section, the electrical and thermo-mechanical characteristics of the SD-ATSV are compared with those of the conventional SD-TSV.

A. ELECTRICAL PERFORMANCE

Fig. 16 compares the differential- and common-mode insertion losses of the SD-TSV and the SD-ATSV of

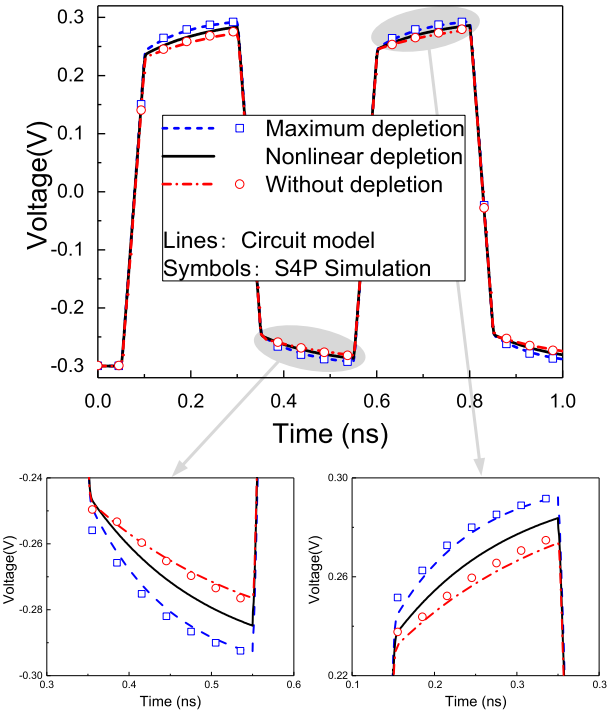

FIGURE 12. Transient output voltage waveforms of the SD-ATSV of configuration A for different cases.

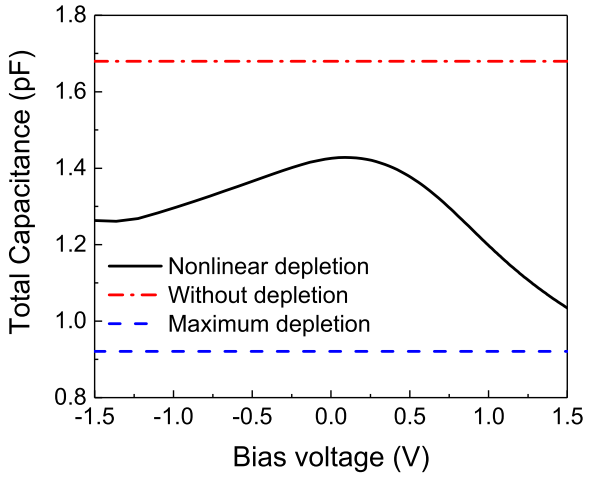

FIGURE 13. The total MOS capacitance of the SD-ATSV of configuration A for different cases.

configuration B. The geometrical parameters of the SD-TSV are the same as those of the SD-ATSV except that the inner metal radius of the ATSV is set to be zero, i.e., $r_1 = 0$. It is evident that the SD-ATSV has the comparable performance with the SD-TSV for differential- and common-mode signal propagations. On the one hand, the mutual admittance plays a major role in the signal leakage. The mutual admittances of the SD-TSV and the SD-ATSV are the same with each other as they are merely related to the outer edges of the signal vias and the inner edge of the shielding shell. On the other hand, although the internal inductance of the shielded pair

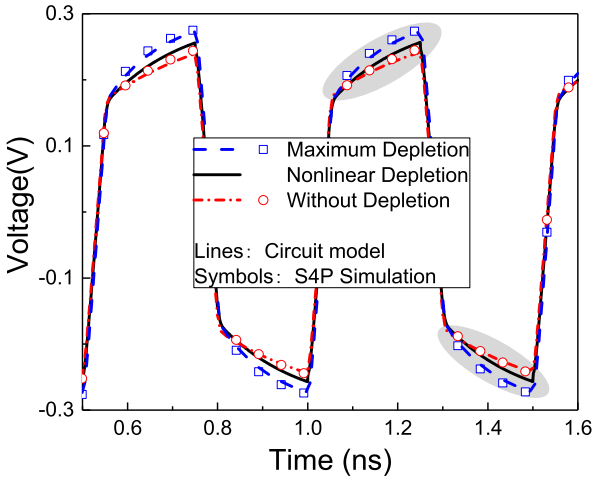

FIGURE 14. Transient output voltage waveforms of 3-stacked SD-ATSVs of configuration A for different cases.

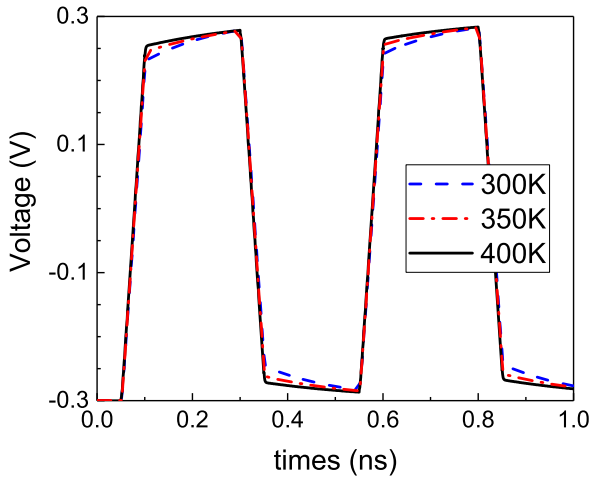

FIGURE 15. Transient output voltage waveforms of the SD-ATSV for different temperatures.

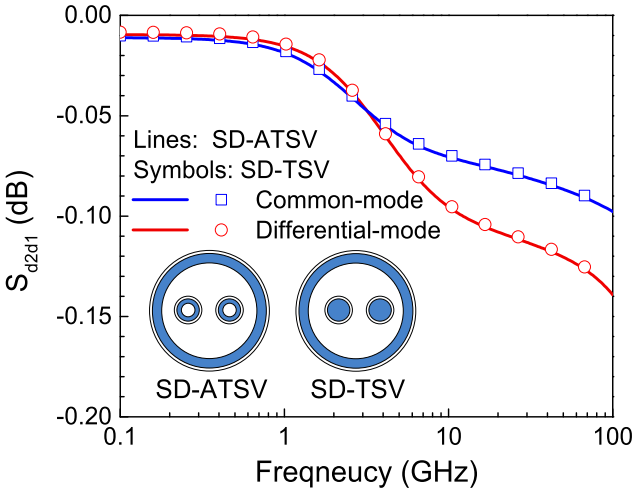

FIGURE 16. Differential- and common-mode insertion losses of the SD-TSV and SD-ATSV.

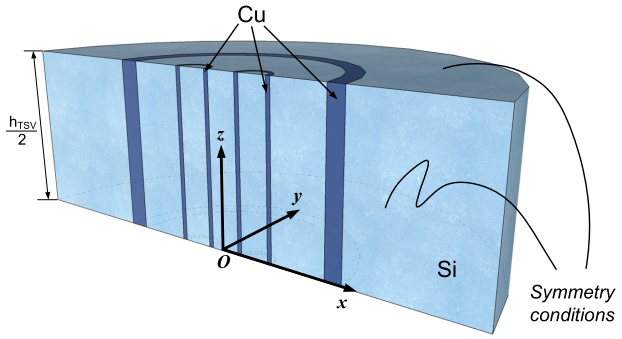

FIGURE 17. Multi-physics simulation model. A quarter of the SD-ATSV structure is adopted for simulation by setting symmetry conditions to the top and cross-sectional surfaces. So the height of the simulation model is chosen as $h_{TSV}/2$.

TABLE 3. Material parameters used in the multiphysics simulation.

Material	Cu	SiO_2	Si
Young's modulus E (GPa)	110	72	130
Poisson's ratio v	0.35	0.16	0.28
Thermal expansion coefficient α (ppm/°C)	17	0.6	2.3

vias is changed when replacing the cylindrical vias with the annular ones, it is much smaller than the external inductance and therefore can be neglected.

B. THERMO-MECHANICAL CHARACTERISTICS

During the manufacturing processes, thermal stress is induced by the mismatch of the thermal expansion coefficients of various materials employed in the fabrication [17]. The thermo-mechanical characteristics of the SD-ATSV of configuration B are captured and compared with those of the SD-TSV by using the commercial multiphysics simulation tool COMSOL [46]. For reducing the simulation time, only a quarter of the TSV structure is used for simulation, as shown in Fig. 17. The boundary conditions of "symmetry" are set for the top and front cross sections. Here, the linear elastic materials are utilized, with the material parameters listed in Table 3. A thermal load, which is used to simulate the temperature drop from the annealing temperature to the room temperature, is assumed to be −250 °C to imitate the thermal circumstance [21].

Fig. 18 shows the simulated thermal stresses of the SD-TSV and the SD-ATSV along the x-axis. The thermal stress decreases along the radial direction when away from the centers of the TSV. It is found that the thermal stress near the outer edge of the shielding shell can be reduced by 25 MPa by replacing the cylindrical vias with the annular ones. Moreover, as discussed earlier, the inner ATSVs can be fabricated by electroplating Cu layer on the sidewalls of the vias. The material inside the ATSVs is replaced with the air in this scenario. It is found that the thermal stress of such air-core SD-ATSV is almost the same as that of the original SD-ATSV (see Fig. 18), which is because the reduction in

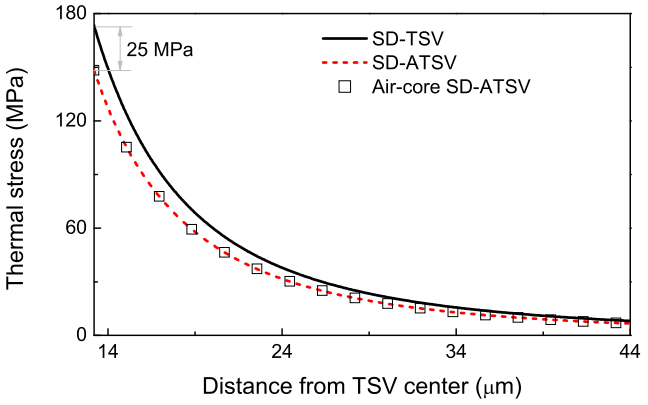

FIGURE 18. Comparison of thermal stress for SD-TSV and SD-ATSV along the x-axis. The curve is starting from the outer edge of the shielding shell, whose coordinate on the x-axis is 13.2 μm.

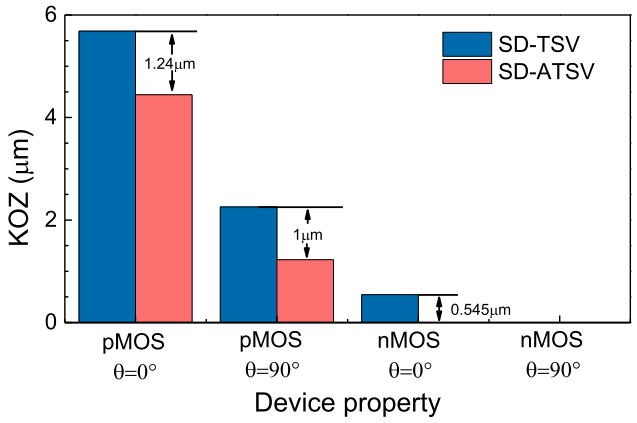

FIGURE 19. KOZs caused by TSV for different device properties.

the thermal stress is mainly attributed to the reduction in the metal ratio of the inner ATSVs [20].

As the thermal mismatch stress induced by TSVs may affect the substrate carrier mobility and thereby degrades the device performance, the keep-out zones (KOZs) of the SD-TSV and the SD-ATSV are calculated [47]. Considering the angle between the transistor and the radial stress, four kinds of device properties are studied: 1) pMOS that is parallel to the radial stress; 2) pMOS that is perpendicular to the radial stress; 3) nMOS that is parallel to the radial stress; and 4) nMOS that is perpendicular to the radial stress. The KOZ is calculated by [21]

$$\mathrm{KOZ} = r|_{|\Pi\times\sigma_{rr}(r)\times\beta(\theta)|<5\%}\,. \tag{44}$$

where σ_{rr} is the radial stress, $\beta(\theta)$ is an orientation factor, θ is the angle between transistor channel and radial stress, and Π is 71.8×10^{-11} Pa^{-1} and -31×10^{-11} Pa^{-1} for pMOS and nMOS respectively. Specifically, $\beta(0°)=1$, and $\beta(90°)$ is -0.6 and 0.5 for pMOS and nMOS respectively. As shown in Fig. 19, the KOZs induced by the SD-ATSV is about 22% smaller than that of the SD-TSV for different device properties.

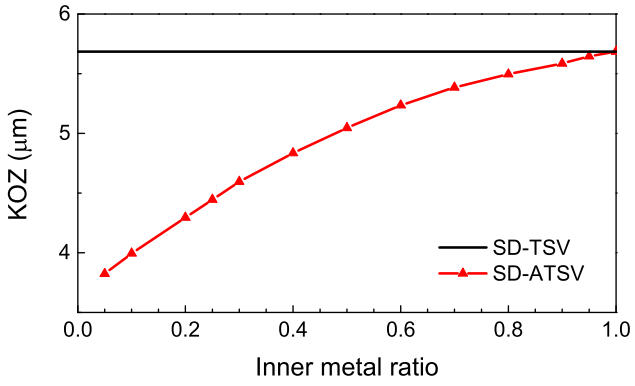

FIGURE 20. KOZ induced by the SD-ATSVs versus inner metal ratios.

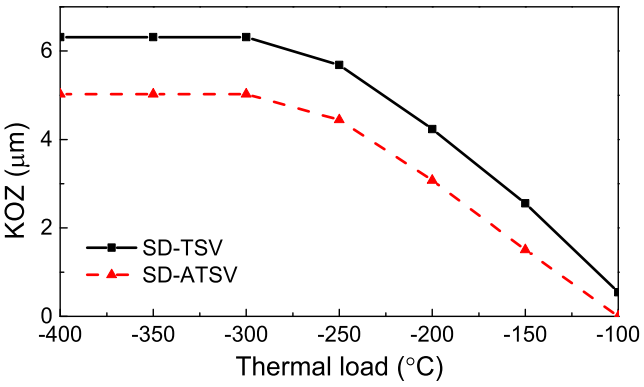

FIGURE 21. KOZs of the SD-TSV and the SD-ATSVs versus thermal load.

For the SD-ATSV, the inner metal ratio, which can be defined as $(r_2-r_1)/r_2$ of the inner ATSVs, has an impact on the KOZ. Fig. 20 shows the KOZ induced by the SD-ATSV for pMOS at $\theta=0°$ with different inner metal ratios. In the figure, the KOZ induced by the SD-TSV is also plotted for comparison. It is evident that a lower rate of metal leads to smaller KOZ. As the metal ratio increases, the KOZ of the SD-ATSV increases rapidly and tends to that of the SD-TSV. Finally, the influences of the thermal load on the KOZs of the SD-TSV and SD-ATSV are illustrated in Fig. 21. It is shown that the KOZs decrease with the increasing thermal load, and the KOZ of the SD-ATSV is always smaller than that of the SD-TSV.

V. CONCLUSION

This work proposed a SD-ATSV, which is composed of two inner signal ATSVs and an outer shielding shell. Due to its self-shielding function, the SD-ATSV has better noise immunity than the ground-signal-signal-ground differential TSVs. The fabrication feasibility of the proposed SD-ATSV was briefly discussed. Furthermore, an equivalent circuit model of the SD-ATSV was developed, with the influence of the electrically floating silicon considered. It was found that the MOS capacitance varies with the bias voltage, which is because the minority carriers flow alternatively between the signal and the ground in the floating silicon substrate.

By using the SDD block in Keysight ADS, the voltage-dependent capacitances were modeled accurately, and the frequency- and time-domain electrical characteristics of the SD-ATSV were captured and verified against the full-wave electromagnetic simulations. It was found that ignoring the impact of floating silicon substrate would lead to inaccuracy, which becomes more severe with increasing number of stacking layers. The impacts of temperature on the electrical characteristics were also studied. Finally, the electrical and thermo-mechanical characteristics of the SD-ATSV were compared with those of the SD-TSV. It was demonstrated that the SD-ATSV has comparable electrical performance as the SD-TSV for both differential- and common-mode signal propagations since they have the same mutual admittances and external inductances. However, as the metal ratio of the inner ATSVs decreases, the SD-ATSV shows smaller thermal stress and KOZ than the SD-TSV.

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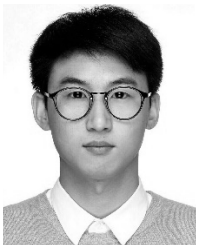

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