

Received March 25, 2018, accepted May 18, 2018, date of publication May 31, 2018, date of current version July 6, 2018. *Digital Object Identifier 10.1109/ACCESS.2018.2842199*

Morphology Evaluation of Microelectronic Packaging Substrates Using Shadow Moiré Technique

FULONG ZHU^{©[1](https://orcid.org/0000-0002-0756-9051)}, XINXIN LIN¹, WEI ZHANG², JIAJIE FAN^{©[3](https://orcid.org/0000-0001-5400-737X)}, (Senior Member, IEEE), AND SHENG LIU^{1,4}, (Fellow, IEEE)

¹School of Mechanical Science and Engineering, Institute of Microsystems, Huazhong University of Science and Technology, Wuhan 430074, China ²Department of Mechanical Engineering, Hubei University of Automotive Technology, Shiyan 442002, China ³School of Mechanical and Electrical Engineering, Hohai University, Changzhou 213022, China ⁴School of Power and Mechanical Engineering, Wuhan University, Wuhan 430072, China

Corresponding author: Fulong Zhu (zhufulong@hust.edu.cn)

This work was supported in part by the National Program on Key Basic Research Project (''973'' Program) of China under Grant 2015CB057203, in part by the National Nature Science Foundation of China under Grant 51675211, and in part by the National High Technology Research and Development Program (''863'' Program) of China under Grant 2015AA033304.

ABSTRACT The surface quality and long-term reliability of packaging substrates in microelectronic packaging processes have become subjects of increasing concern as circuit board component density increases while the pitches of these components decrease. As a result, packaging substrate morphology inspection is becoming more crucial than ever before. This paper presents a noncontact measurement technology based on a shadow moiré technique to evaluate the surface quality and morphology of microelectronic packaging substrates. Fringe pattern images of packaging substrates are acquired through the noncontact measurement technology, and the resulting images are then analyzed using the phase-shifting technique to determine the morphology and surface quality (specifically, the flatness) of the microelectronic packaging substrates. A full-field morphology measurement system with adjustable sensitivity and measurement range was developed. The measurement system was tested using three typical types of microelectronic packaging substrate, a coin and a step made from two standard gauge blocks. The measurement system proved to be both feasible and effective by the test results.

INDEX TERMS Morphology, microelectronic packaging substrate, phase-shifting, shadow moiré.

I. INTRODUCTION

As microelectronic packaging densities continue to increase while component pitches decrease, the reliability of the packaging substrates is becoming an increasingly important aspect of microelectronic packaging. The surface quality of the packaging substrate affects the overall quality of the assembly of microelectronic components and poor surface quality can lead to serious reliability problems, including misalignment and interconnection failure between the chip and the substrate. In microelectronic packaging and interconnection, the thermomechanical behavior of the packaging substrate is critical for the long-term reliability of microelectronic devices, and thermomechanical failure of microelectronic packaging is usually in connection with material failure [1]. And the coefficient of thermal expansion (CTE) mismatch can cause substrate warpage, which then affects the reliability of the

microelectronic device. These issues mean that inspection of the morphology and the surface quality of microelectronic packaging substrates is more critical than ever before, and on-line morphology measurement of these substrates will become an essential part of microelectronic package processing.

The deformation of printed circuit boards (PCB) and ceramic, silicon or metal substrates as a result of CTE mismatch is a major cause of defects and component failure in microelectronic packaging [2]. As the packaging density increases, surface morphology measurements of microelectronic packaging substrates is essential for improving package reliability and inspection of the substrate morphology should be an on-line process that is nondestructive to the microelectronic components. Many optical measurement methods are noncontact whole-field techniques, thus

making them suitable for investigation of the morphology and deformation of microelectronic packaging substrates. Since the moiré topography technique was first proposed in 1970 [3], [4], a wide range of geometric moiré techniques [5] has been developed for investigating the surface morphology, deformation and mechanical properties of chip or microelectronic packaging substrates. These moiré techniques, which include in-plane moiré interferometry [6]–[11], Fizeau interferometry [12], [13], Twyman–Green interferometry [14]–[16], shadow moiré [17]–[25], projection moiré [23], [26]–[29] and laser profilometry [30], [31], have become increasingly important in the characterization of electronic materials, components and their base substrates. The shadow moiré method is a noncontact full-field technique with high resolution that uses simple optics; these characteristics make it very suitable for on-line measurement applications, and it has been widely used in the measurement of out-of-plane displacement, surface topography, and impact deformation. When compared with laser profilometry using a laser beam scanning system, the shadow moiré method is faster for morphology and deformation measurements. However, to be suitable for use in the microelectronic packaging industry, the shadow moiré method must demonstrate high sensitivity and reliability in evaluating the surface morphologies of different types of microelectronic packaging substrates. In the sections that follow, a whole-field three-dimensional (3D) measurement system based on the shadow moiré technique with phaseshifting is proposed, and the morphology measurement of microelectronic substrates is demonstrated.

FIGURE 1. Illustration of the path of the white light in the proposed system.

II. PRINCIPLES OF SUBSTRATE MORPHOLOGY MEASUREMENT

A. SHADOW MOIRÉ TECHNIQUE

Figure 1 shows the path of the white light in the proposed measurement system. The grating placed above the substrate sample is used for reference. The white light lights up the reference grating and the substrate surface at an incidence angle α , and the reflected light scattered by the sample surface is received by a charge-coupled device (CCD) camera

located at a viewing angle $β$. When the white light comes in, the shadow of the reference grating is produced on the substrate sample; for the different heights at different points on the sample, the pitch of the substrate sample's shadow differs from that of the reference grating's shadow's and the shadow of the substrate sample thus becomes deformed; the shadows of both the substrate sample and the superimposed reference grating are received by the CCD camera. The moiré fringes can be formed through the interaction between the shadows. And through analyzing these moiré fringes, the surface morphology of the substrate sample can be determined.

The surface morphology of the microelectronic packaging substrate is obtained based on the distance, denoted by *z(x,y)*, from the reference grating, as shown in Figure 1:

$$
z(x,y) = \frac{g}{(\tan \alpha + \tan \beta)} n(x,y)
$$
 (1)

Where $z(x, y)$, the distance between the reference grating and a point (x, y) on the sample surface, is the out-of-plane displacement, *g* is the pitch of the reference grating, $n(x, y)$ is the fringe order of the point (x, y) on the sample surface, $α$ and $β$ are respectively the incidence and viewing angle. In our 3D measurement system, *g*, α , and β are constants, so $g/(tan\alpha + tan\beta)$ is also constant. If the CCD camera's view is normal to the reference grating, then the viewing angle β is 0° , and equation [\(1\)](#page-1-0) can be reduced to:

$$
z(x,y) = \frac{g}{\tan \alpha} n(x,y)
$$
 (2)

B. PHASE-SHIFTING TECHNIQUE

In optical interferometry methods (including moiré methods), phase-shifting techniques are important and effective ways to enhance measurement sensitivity [25], [28], [29], [32], [33]. In the proposed 3D morphology measurement system, a phase-shifting method based on a harmonic representation of the intensities of the moiré fringes [34] is used to achieve high testing sensitivity. A series of phase-shifted images of the substrate surface are obtained and analyzed to determine the fringe order at each point on the substrate surface. These images are obtained by moving the substrate up or down by a specific distance and capturing the resulting patterns using the CCD camera. In morphology measurements, each phaseshifted intensity image can be defined by:

$$
I(x,y) = I_b(x,y) + I_m(x,y)\cos[\varphi(x,y) + \sigma]
$$
 (3)

$$
\varphi(x,y) = 2\pi n(x,y) \tag{4}
$$

In equation (3) , $I(x, y)$ is the intensity of the image obtained using the CCD camera, $I_b(x, y)$ is the background intensity, $I_m(x, y)$ is the intensity modulation caused by the interference fringe, and φ (x, y) is the phase information obtained from the fringe pattern at point (x, y) ; σ , which can vary from 0 to 2π as the sample moves, is the phase-shift for every point (x, y) , and $N(x, y)$ is the fringe order of point (x, y) . In equations [\(1\)](#page-1-0)–(4), when the fringe order $N(x, y)$ or $\varphi(x, y)$ has been determined, the distance $z(x, y)$ between the reference grating and the substrate can also be defined.

In equation [\(3\)](#page-1-1), $I_b(x, y)$, $I_m(x, y)$ and $\varphi(x, y)$ are the three unknown quantities. Therefore, a minimum of three intensity images are required to evaluate the three unknown variables and acquire the desired $n(x, y)$ or $\varphi(x, y)$. When using phaseshifting methods, three to five intensity images should be obtained to calculate the phase and three-step and four-step phase-shifting methods are commonly used. In a three-step phase-shifting method, intensity images can be defined using equation [\(5\)](#page-2-0), and thus the phase data can be computed using equation [\(6\)](#page-2-0). In equation [\(5\)](#page-2-0), $I_n(x, y)$ denote the intensities of the images at different phase angles ($\sigma = 0$, $2\pi/3$ and $4\pi/3$). The denominator of equation [\(6\)](#page-2-0) can sometimes be zero, which is a significant disadvantage of this method, and could result in the loss of some of the phase information and reduced measurement sensitivity.

$$
I_n(x,y) = I_b(x,y) + I_m(x,y) \cos \left[\varphi(x,y) + (n-1)2\pi/3\right],
$$

\n
$$
n = 1, 2, 3 \quad (5)
$$

\n
$$
\varphi(x,y) = \tan^{-1} \left[\frac{\sqrt{3} (I_1(x,y) - I_3(x,y))}{2I_2(x,y) - I_1(x,y) - I_3(x,y)} \right]
$$
 (6)

In this work, the widely applied four-step phaseshifting method, which uses a phase increment of $\pi/2$, is adopted [32], [33]. The intensities of the four phase-shifted intensity images can be formulated as follows:

$$
I_n(x,y) = I_b(x,y) + I_m(x,y) \cos \left[\varphi(x,y) + (n-1)\pi/2\right],
$$

$$
n = 1, 2, 3, 4 \quad (7)
$$

where $I_n(x, y)$ are the intensities of the images at different phase angles $(0, \pi/2, \pi, 3\pi/2)$. Using the four intensity images, the phase information $(\varphi(x, y))$ of the fringe pattern at point (x, y) can then be described as:

$$
\varphi(x, y) = \tan^{-1} \left[\frac{I_4(x, y) - I_2(x, y)}{I_1(x, y) - I_3(x, y)} \right]
$$
(8)

FIGURE 2. Measurement process flow chart for the system.

The denominator in equation [\(8\)](#page-2-1) is always nonzero [29]. Therefore, the out-of-plane displacement $z(x, y)$ can be calculated using equations [\(1\)](#page-1-0) or [\(2\)](#page-1-2), and the substrate morphology can be evaluated via phase unwrapping processing [35]; a flow chart for the measurement process is shown in Figure 2. In the 3D measurement system, the level of each pixel in the fringe pattern intensity image is identified; there are 256 levels, ranging from dark to bright, and thus in theory, the system sensitivity can be increased by a factor of 256 using this fourstep phase-shifting method. However, the typical sensitivity improvement ranges from 10 to 100 times [24]–[26].

III. 3D MEASUREMENT SYSTEM

Figure 3 illustrates the schematic of the proposed morphology measurement system. The measurement resolution of the system is 1 μ m, the sizes of the samples to be measured range from 3 mm \times 3 mm to 80 mm \times 80 mm and the angle between the incident light and the observation point ranges from 30◦ to 75◦ . There are three sub-systems: the white light source subsystem, the position control subsystem, and the image capture subsystem. All subsystems are controlled using a central personal computer through custom software that was designed at the Institute of Microsystems, School of Mechanical Science and Engineering, HuaZhong University of Science and Technology.

The light source subsystem includes a white light source with an optical fiber guide, a collimating lens and an incident light reflector. The power of the white light source can be varied from 0 to 150 W, and the source produces steady, persistent, and uniform light. To ensure that the illumination light is a parallel beam with the appropriate spot size required to illuminate microelectronic substrates, a specially designed collimating lens is used; this lens also prevents ambient light interference. The angle of the incident light reflector can be adjusted to vary the angle of incidence α and thus change the sensitivity of the system, and the incident light reflector can also be moved to ensure that the measured object is within the measurement range. The white light subsystem ensures that the reference grating is lit with consistent soft light.

The position control subsystem has two translational stages (horizontal and vertical) that can adjust the substrate sample precisely (to within 0.1 μ m) to the optimal position required for testing. The vertical stage is used to produce the phase displacement and can achieve positioning precision of 0.125 μ m after subdivision, while the horizontal stage is used to ensure that the measured object can be removed easily. Both stages are composed of a guide rail, a ball screw, a stepping motor and movement control cards. During the morphology measurements, the microelectronic packaging substrate under test can be fixed on a sample carrier, which the horizontal translation stage can move underneath the reference grating (Ronchi rulings with 100, 250, or 500 lpi) that is located within the measurable range of the CCD camera. The vertical translation stage can be precisely stepped up and down to enable phase-shifting.

The image capture subsystem can produce the grating shadow and records the fringe image on the computer. To obtain the moiré fringe pattern of the substrate sample, a grating for reference is placed above the substrate specimen. When the collimated light beam from the white light source subsystem comes in, a shadow of the reference grating is formed on the surface of the measured object; the CCD camera (CMOS, 2560×1920 pixels) can then acquire images of the fringe pattern via the reflectors. To capture the perfect moiré image, the CCD camera is equipped with a telecentric lens. During the morphology measurements, small variations in the moiré fringes (relative to the image of the

FIGURE 3. Schematic of proposed morphology measurement system based on moiré technique.

FIGURE 4. (a) Optical image of a coin and (b) moiré fringe pattern of the same coin.

FIGURE 5. Gray scale image of the coin.

reference grating on the substrate) are analyzed so that the surface morphologies of the specimens can be determined and reconstructed using custom software that was designed at the Institute of Microsystems. In this subsystem, the locations of the CCD camera and of some of the reflectors can be modified to adjust the object distance such that it satisfies the field size requirements for the different measured objects. There are three possible locations for the CCD camera in this system but, if necessary, the position of the CCD camera can be made continuously adjustable by installing the CCD camera on a specific guide. The test range increases as the CCD camera is moved from position 1 to position 3. When the CCD camera is installed at position 3, the test range reaches its maximum (80mm \times 80 mm), and when the camera is in position 1, the minimum size of $3 \text{mm} \times 3 \text{mm}$ can be measured. In the light transmission process, losses are unavoidable and distortion is easily caused, so the object distance should be as small as possible while ensuring that the field size condition is met.

Before testing, it is necessary to adjust for the system error. The positions of the incident light reflector and the CCD camera in the system can be determined and the system error can be compensated using the software after the analysis of a standard sample. Additionally, the system must be recalibrated each time that the measured structure changes.

During testing, the 3D morphology measurement system must be mounted on a vibrationless stage to ensure that the surface inspection of the microelectronic packaging substrates is not disturbed by external vibrations. Similarly, the external ambient light should also be minimized during testing.

IV. EXPERIMENTAL RESULTS AND DISCUSSION

To validate the test results and establish the capabilities of our 3D morphology measurement system, five specimens were selected: these comprise a coin with a diameter of 19 mm, a step made from two standard gage blocks, and three typical microelectronic packaging substrates. The dimensions

FIGURE 6. Morphology of the entire back (flower) surface of the coin.

FIGURE 7. (a) Step made from two standard gage blocks with thicknesses of 1.02 and 1.04 mm and (b) complete morphology of the step.

TABLE 1. Repeated measurements of total warpage of 39mm × 39 mm microelectronic packaging substrate.

Number	2 3 4 5 6 7 8 9				- 10	Mean	Standard deviation
Warpage (μm)						524 523 512 517 522 527 521 510 516 511 518.3	5.66

of the three packaging substrates are: $39 \text{mm} \times 39 \text{mm}$, 51 mm \times 51mm and 28mm \times 25.3mm respectively. The data that were obtained from these specimens are discussed below.

We first used the morphology measurement system to examine the back ''flower'' face of the coin. Figure 4(a) shows an optical image of this face, and Figure 4(b) shows the moiré fringe patterns of the coin when the same coin face is placed within the range of the CCD camera. Through resolution and analysis of the moiré fringe patterns by

four-step phase-shifting method, the corresponding distribution of the pixel intensities (or a gray-scale distribution diagram) and the morphology of the entire sample can be obtained. Figure 5 shows the gray scale image, which provides the surface morphology information. The contour map shown in Figure 6 accurately depicts the complete morphology of the flower face of the coin.

For further testing of the 3D morphology measurement system, a step formed from two standard grade-0 gage

FIGURE 8. (a) Optical image of 39mm × 39 mm microelectronic packaging substrate and (b) moiré fringe patterns from 39mm \times 39 mm microelectronic packaging substrate.

FIGURE 9. Deformation of 39mm × 39 mm microelectronic packaging substrate.

FIGURE 10. Displacement of 39mm x 39 mm microelectronic packaging substrate measured: (a) from the top-left corner to the bottom-right corner and (b) from the bottom-left corner to the top-right corner.

blocks was measured. The thicknesses of these blocks were 1.02 and 1.04 mm, as measured to within ± 0.12 μ m. Placement of these two blocks side by side on a white flat plate that acts as the reference plane gives a 0.020-mm-high step, as shown in Figure $7(a)$. The morphology of the complete step is shown in Figure 7(b). The step height is

FIGURE 11. (a) Optical image of 51mm x 51 mm microelectronic packaging substrate and (b) moiré fringe patterns from a 35mm \times 35 mm area of the above microelectronic packaging substrate (effective coverage).

FIGURE 12. Unwrapped image of microelectronic packaging substrate with dimensions of 35 mm \times 35 mm.

FIGURE 13. 3D deformation of 35mm \times 35 mm area of 51mm \times 51 mm microelectronic packaging substrate.

clearly shown in the contour plot, thus demonstrating the micrometer-scale precision of the measurement system.

In microelectronic packaging processing, small packaging substrate deformations can greatly reduce the reliability of the microelectronic devices and components on the substrate, which means that evaluation of the surface morphology

Units:mm

FIGURE 14. Optical image of array of DBC substrates.

and the deformation of microelectronic packaging substrates is becoming indispensable. In this work, the surface morphologies and small deformations of several substrates with different dimensions were investigated to demonstrate the practicality of the proposed 3D morphology measurement system.

Figure 8(a) shows a 39mm \times 39 mm microelectronic packaging substrate; Figure 8(b) is an example moiré fringe pattern that was obtained during inspection of the surface morphology of this substrate. The pattern is very clear, which means that measurement of the morphologies of industrially used substrates is feasible when using this system. After unwrapping and image analysis [35], the morphology and the deformation of this type of packaging substrate is obtained from the four-step phase-shifted images of the moiré fringe patterns and the results are shown in Figure 9.

FIGURE 15. Complete morphology of the array of DBC substrates.

FIGURE 16. Morphology of selected DBC substrate.

The deformation of the microelectronic substrate can be easily seen. For further evaluation of this deformation, two linear paths were followed across the contour plot, from top left to bottom right and from bottom left to top right, as shown in Figure 10. The deformations and surface morphologies measured along these two paths differ significantly.

The repeatability of test results is very important for any measurement device. To assess the repeatability of the proposed measurement system, the warpage of the same 39 mm \times 39 mm substrate was measured for ten times and the results are shown in Table 1. The average of the warpage measurements was 518.3μ m, and the standard deviation was 5.66 μ m. The repetition error of the system is only 1.09%, which demonstrates the excellent repeatability and consistency of the proposed 3D morphology measurement system.

Measurement of the morphology of larger area packaging substrates requires some changes to the 3D morphology measurement system, including reduction of the angle of incidence and changing the position of the CCD camera. Measurements were performed on a 51 mm square microelectronic packaging substrate, which is shown in Figure 11(a). And an example moiré fringe pattern that was obtained by the image capture subsystem from a local area (35 mm square) of this substrate is shown in Figure 11(b); the moiré fringe patterns are very distinct, which indicates that the unwrapped image should be perfect. Figure 12 shows an image of this local area after phase-shifting and unwrapping calculations. The morphology of this large area substrate can then be reconstructed. Figure 13 shows the three-dimensional deformation of the 35mm \times 35 mm local area of the larger substrate;

FIGURE 17. The cross-section of the whole DBC substrates: (a) from top left to bottom right corner and (b) form bottom-left to top-right corner.

this local area is clearly convex, with the maximum substrate warpage reaching 720 μ m. In Figure 13, the maximum deformation is shown to be located at the center of the large area substrate; this often occurs in microelectronic packaging substrates.

Another advantage of this 3D morphology measurement system is that the test range of the 3D measurement can be adjusted. In this subsystem, the locations of the CCD camera and of some of the reflectors can be modified to adjust the object distance such that it satisfies the field size requirements for the different measured objects, which means that it can detect the whole specimen and then explore the results at a specified location on a specimen in detail. Figure 14 shows an optical image of an array of direct bonded copper (DBC), produced by directly sintering of a copper layer on an alumina substrate where one of the single DBC substrates is framed by four red lines. After measurement using the 3D morphology measurement system, the complete morphology of the DBC

substrates is shown in Figure 15 and the morphology of the specific DBC substrate is shown in Figure 16. What's more, through the analyzing of the data of the whole DBC substrates, the morphology of the specific part can also be get. And the height change of the plane along the diagonal of both the whole DBC substrates and the specific DBC substrate is shown in Figure 17 and Figure 18, from which we can see that the substrates around the whole DBC substrates warping upwards (Figure 17) and the height of the specific DBC substrate is roughly 40.5 microns (Figure 18). Therefore, it is quite convenient to obtain the details of the entire specimen using this process.

The tests described above show that the 3D morphology measurement system can reproducibly characterize the surface morphology and deformation of a substrate with micrometer-scale accuracy. Very clear moiré fringe patterns were obtained from a range of specimens, including a small area substrate, a large area substrate, a step composed of

FIGURE 18. The cross-section of the specific DBC substrate: (a) from top left to bottom right and (b) form bottom left to top right.

standard gage blocks, and a coin with a complex surface configuration. The surface morphologies and deformations of these specimens could be clearly determined from these patterns.

V. CONCLUSIONS

In this work, a 3D morphology measurement system based on the shadow moiré technique was presented. A four-step phase-shifting technique that eliminates the problem of zero denominator values that can occur in the three-step phaseshifting method is used; interference from ambient light is prevented by a collimating lens placed between the white light source and the reference grating. A telecentric lens allows the system to capture clear moiré fringe patterns. During measurement of the morphology, the positioning of the CCD camera and the angle of incidence of the white light are adjustable; this allows the system to evaluate microelectronic packaging substrates with different areas. Similarly, the sensitivity of this 3D measurement system can be varied for different applications. Test data from specimens with different areas showed excellent repeatability and consistency when evaluating the surface morphologies and deformations of different microelectronic packaging substrates.

The 3D morphology measurement system that is proposed in this work can investigate the surface morphologies and deformations of entire microelectronic packaging substrates, but can also be used to explore details of parts of the whole specimen through direct measurement or datum processing. All tests demonstrated the good performance and reliability of the proposed measurement system.

ACKNOWLEDGMENT

The authors would like to thank Prof. Xiaoyua. He and Dr Yiquan Dai from Southeast University for their help and good advice.

REFERENCES

- [1] R. Tummala, *Fundamentals of Microsystems Packaging*. Columbus, OH, USA: McGraw-Hill, 2001.
- [2] R. E. Powell and I. C. Ume, ''Development of warpage measurement system to simulate convective solder reflow process,'' *IEEE Trans. Electron. Packag. Manuf.*, vol. 31, no. 1, pp. 83–90, Jan. 2008.
- [3] D. M. Meadows, W. O. Johnson, and J. B. Allen, "Generation of surface contours by Moiré patterns,'' *Appl. Opt.*, vol. 9, no. 4, pp. 942–947, Jan. 1970.
- [4] D. Post, B. Han, and P. Ifju, ''High sensitivity Moiré,'' *Exp. Techn.*, vol. 18, no. 2, p. 43, 1994.
- [5] H. Takasaki, ''Moiré topography,'' *Appl. Opt.*, vol. 9, no. 6, pp. 1467–1472, Jan. 1970.
- [6] A. S. Voloshin, P.-H. Tsao, and R. A. Pearson, ''*In situ* evaluation of residual stresses in an organic die-attach adhesive,'' *J. Electron. Packag.*, vol. 120, no. 3, pp. 314–318, Sep. 1998.
- [7] E. A. Stout, N. R. Sottos, and A. F. Skipor, ''Mechanical characterization of plastic ball grid array package flexure using Moiré interferometry,'' *IEEE Trans. Adv. Packag.*, vol. 23, no. 4, pp. 637–645, Nov. 2000.
- [8] S. Cho and B. Han, ''Observing real-time thermal deformations in electronic packaging,'' *Exp. Techn.*, vol. 26, no. 3, pp. 25–29, 2002.
- [9] Y. Guo and C. G. Woychik, ''Thermal strain measurements of solder joints in second level interconnections using Moiré interferometry,'' *J. Electron. Packag.*, vol. 114, no. 1, pp. 88–92, Mar. 1992.
- [10] B. Han, ''Thermal stresses in microelectronics subassemblies: Quantitative characterization using photomechanics methods,'' *J. Therm. Stresses*, vol. 26, no. 6, pp. 583–613, 2003.
- [11] Y. Wen and C. Basaran, "An analytical model for thermal stress analysis of multi-layered microelectronic packaging,'' *Mech. Mater.*, vol. 36, no. 4, pp. 369–385, 2004.
- [12] K. Verma, S.-B. Park, B. Han, and W. Ackerman, "On the design parameters of flip-chip PBGA package assembly for optimum solder ball reliability,'' *IEEE Trans. Compon. Packag. Technol.*, vol. 24, no. 2, pp. 300–307, Jun. 2001.
- [13] K. Verma and B. Han, "Warpage measurement on dielectric rough surfaces of microelectronics devices by far infrared Fizeau interferometry,'' *J. Electron. Packag.*, vol. 122, no. 3, pp. 227–232, Dec. 1999.
- [14] Y. Guo and S. Liu, ''Development in optical methods for reliability analysis in electronic packaging applications,'' *J. Electron. Packag.*, vol. 120, no. 2, pp. 186–193, Jun. 1998.
- [15] B. Han, Y. Guo, C. K. Lim, and D. Caletka, "Verification of numerical models used in microelectronics packaging design by interferometric displacement measurement methods,'' *J. Electron. Packag.*, vol. 118, no. 3, pp. 157–163, Sep. 1996.
- [16] W. D. van Driel et al., "Prediction and verification of process induced warpage of electronic packages,'' *Microelectron. Rel.*, vol. 43, no. 5, pp. 765–774, Jan. 2003.
- [17] Y. Polsky, W. Sutherlin, and I. C. Ume, "A comparison of PWB warpage due to simulated infrared and wave soldering processes,'' *IEEE Trans. Electron. Packag. Manuf.*, vol. 23, no. 3, pp. 191–199, Jan. 2000.
- [18] M. R. Stiteler, I. C. Ume, and B. Leutz, ''In-process board warpage measurement in a lab scale wave soldering oven,'' *IEEE Trans. Compon., Packag., Manuf. Technol. A*, vol. 19, no. 4, pp. 562–569, Dec. 1996.
- [19] C.-H. Chien *et al.*, "Influences of the moisture absorption on PBGA package's warpage during IR reflow process,'' *Microelectron. Rel.*, vol. 43, no. 1, pp. 131–139, Jan. 2003.
- [20] D. Karalekas and A. Aggelopoulos, ''Study of shrinkage strains in a stereolithography cured acrylic photopolymer resin,'' *J. Mater. Process. Technol.*, vol. 136, nos. 1–3, pp. 146–150, Jan. 2003.
- [21] T. Y. Lin, B. Njoman, D. Crouthamel, K. H. Chua, and S. Y. Teo, ''The impact of moisture in mold compound preforms on the warpage of PBGA packages,'' in *Proc. IEEE/CPMT/SEMI 28th Int. Electron. Manuf. Technol. Symp. (IEMT)*, Jul. 2003, pp. 273–278.
- [22] S. K. Bhattacharya, I. C. Ume, and A. X. H. Dang, "Warpage measurement of large area multitilted silicon substrates at various processing conditions,'' *IEEE Trans. Compon. Packag. Technol.*, vol. 23, no. 3, pp. 497–504, Sep. 2000.
- [23] H. Ding, R. E. Powell, C. R. Hanna, and I. C. Ume, ''Warpage measurement comparison using shadow Moiré and projection Moiré methods,'' in *Proc. 52nd Electron. Compon. Technol. Conf.*, May 2002, pp. 176–182.
- [24] Y. Wang and P. Hassell, "On-line measurement of thermally induced warpage of BGAs with high sensitivity shadow Moiré,'' *Int. J. Microcircuits Electron. Packag.*, vol. 21, no. 2, pp. 191–196, 1998.
- [25] Y. Y. Wang and P. Hassell, "Measurement of thermally induced warpage of BGA packages/substrates using phase-stepping shadow Moiré,'' in *Proc. 1st Electron. Packag. Technol. Conf.*, Oct. 1997, pp. 283–289.
- [26] H. Ding, R. E. Powell, C. R. Hanna, and I. C. Ume, "Warpage measurement comparison using shadow Moiré and projection Moiré methods,'' *IEEE Trans. Compon. Packag. Technol.*, vol. 25, no. 4, pp. 714–721, Dec. 2002.
- [27] H. Ding, R. E. Powell, and I. C. Ume, "A projection Moiré system for measuring warpage with case studies,'' *Int. J. Microcircuits Electron. Packag.*, vol. 25, no. 1, pp. 15–26, 2005.
- [28] C. Quan, X. Y. He, C. F. Wang, C. J. Tay, and H. M. Shang, "Shape measurement of small objects using LCD fringe projection with phase shifting,'' *Opt. Commun.*, vol. 189, nos. 1–3, pp. 21–29, Jan. 2001.
- [29] H.-N. Yen and D.-M. Tsai, ''A fast full-field 3D measurement system for BGA coplanarity inspection,'' *Int. J. Adv. Manuf. Technol.*, vol. 24, nos. 1–2, pp. 132–139, Jul. 2004.
- [30] Y. Du, J.-H. Zhao, and P. Ho, "An optical method for measuring the two-dimensional surface curvatures of electronic packages during thermal cycling,'' *J. Electron. Packag.*, vol. 123, no. 3, pp. 196–199, Mar. 2000.
- [31] J. S. Kim, K. W. Paik, and H. S. Seo, "A quantitative analysis of the stress relaxation effect of thermoplastics in multilayer substrates,'' *IEEE Trans. Adv. Packag.*, vol. 22, no. 4, pp. 638–641, Nov. 1999.
- [32] J. E. A. Liao and A. S. Voloshin, ''Enhancement of the shadow-Moiré method through digital image processing,'' *Exp. Mech.*, vol. 33, no. 1, pp. 59–63, Mar. 1993.
- [33] H. Liu, A. N. Cartwright, and C. Basaran, "Sensitivity improvement in phase-shifted Moiré interferometry using 1-D continuous wavelet transform image processing,'' *Opt. Eng.*, vol. 42, no. 9, pp. 2646–2652, 2003.
- [34] K. Creath, ''V phase-measurement interferometry techniques,'' in *Progress in Optics*, vol. 26, E. Wolf, Ed. Amsterdam, The Netherlands: Elsevier, 1988, pp. 349–393.
- [35] D. C. Ghiglia and M. D. Pritt, *Two-Dimensional Phase Unwrapping: Theory, Algorithms, and Software*. New York, NY, USA: Wiley, 1998.

FULONG ZHU received the B.S. degree in mechanical engineering from the Wuhan University of Technology, Wuhan, China, in 1998, and the M.S. degree in engineering mechanics and the Ph.D. degree in mechanical engineering from the Huazhong University of Science and Technology, Wuhan, in 2003 and 2007, respectively. He is currently an Associate Professor with the School of Mechanical Science and Engineering, Huazhong University of Science and Technology.

He has authored over 30 technical articles in English, and holds about eight Chinese patents. His main research interests include morphology measurement technology, optical metrology, image processing, micro and nano-manufacturing, micrometer/nanometer mechanics, and reliability of micro-electronics packaging.

XINXIN LIN received the B.S. degree in mechanical engineering from Shandong Jianzhu University, Jinan, China, in 2014. She is currently pursuing the M.S. degree with the Huazhong University of Science and Technology, Wuhan, China. Her major areas of interest are morphology measurement technology, the reliability of electrical connectors, and finite-element analysis.

WEI ZHANG received the B.S. degree in mechatronic engineering from the Lanzhou University of Technology, Lanzhou, China, in 2001, the M.S. degree in mechanical engineering from Wuhan University, Wuhan, China, in 2006, and the Ph.D. degree in mechanical manufacture and automation from the Huazhong University of Science and Technology, Wuhan, in 2014. Since 2014, he has been an Associate Professor with the College of Mechanical Engineering, Hubei University

of Automotive Technology. His current research interests include optical metrology, image processing, and 3-D shape measurement.

JIAJIE FAN (S'12–M'14–SM'17) received the B.S. degree in inorganic materials science and engineering from the Nanjing University of Technology, Nanjing, China, in 2006, the M.S. degree in material science and engineering from the East China University of Science and Technology, Shanghai, China, in 2009, and the Ph.D. degree in industrial and systems engineering with The Hong Kong Polytechnic University, Hong Kong, in 2014. He is currently an Associate Professor

with the College of Mechanical and Electrical Engineering, Hohai University, Changzhou, China. He is also a Post-Doctoral Research Fellow with the Beijing Research Centre, Delft University of Technology, and the State Key Laboratory of Solid State Lighting, China. His main research interests include lifetime estimation for LEDs, failure diagnosis and prognosis for electric devices and system, prognostics and health management for LED lightings, and advanced electronic packaging and assembly. He is a registered as a certified Six Sigma Green Belt in Hong Kong Society for Quality.

SHENG LIU (F'13) received the B.S. and M.S. degrees in flight vehicle design from the Nanjing University of Aeronautics and Astronautics, Nanjing, China, in 1983 and 1986, respectively, and the Ph.D. degree in mechanical engineering from Stanford University, Stanford, CA, USA, in 1992. From 1992 to 1995, he was an Assistant Professor with the School of Mechanical and Aerospace Engineering, Florida Institute of Technology, Melbourne. In 1995, he joined the School of

Mechanical Engineering and the Institute for Manufacturing Research (joint appointment), Wayne State University, Detroit, MI, USA, as an Assistant Professor, where he became a Tenured Associate Professor in 1998. In 2006, he joined the School of Mechanical Science and Engineering, Huazhong University of Science and Technology, Wuhan, China, as a Full Professor, where he was the Director of the Institute of Microsystems. He was the Director of the Division of Micro-Opto-Electronicmechanical Systems, Wuhan National Laboratory for Optoelectronics, Wuhan. He was also the Executive Director of the Birdnest Program, initiated by Prof. G. Chen, MIT; Prof. C.-M. Ho, UCLA; Prof. Z. Suo, Harvard; and Prof. Z. Ren, University of Houston, with the aiming of recruiting and mentoring young faculty in a tenure track system similar to USA. He is currently the Dean of the School of Power and Mechanical Engineering, Wuhan University, Wuhan. His main research interests include light-emitting diodes, microelectromechanical systems, integrated circuit packaging, mechanics, and power electronics. Prof. Liu has authored over 500 technical articles in English, two books by Wiley, and holds about 300 Chinese patents. He was a recipient of the Presidential Faculty Fellow Award in 1995, the ASME Young Engineer Award in 2006, and the IEEE CPMT Excellent Technical Achievement Award in 2009. He was evaluated to be an ASME Fellow in 2009.