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A Single-Phase Single-Source 7-Level Inverter With Triple Voltage Boosting Gain

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ABSTRACT The cascaded H-bridge multilevel inverter (MLI) requires separate isolated dc sources to generate more than three voltage levels and to generate higher output voltage. This paper proposes a new MLI topology that requires only one dc source and is capable of generating seven voltage levels with triple voltage boosting gain. Three H-bridges are interconnected through two bidirectional voltage blocking switches to enable the integration of two switched-capacitors. Unlike the existing two-stage structure switched-capacitor-based MLI, the proposed MLI is a single-stage topology. It alleviates the voltage stress across switches such that low voltage stress of not more than the dc source voltage is ensured on all switches. In addition, capacitors voltage balancing is achieved automatically during operation. The operation of the proposed MLI is analyzed followed by verification through simulation and experimental test of a low power/voltage prototype.

INDEX TERMS Multilevel inverter, single-stage, switched-capacitor, voltage boosting.

I. INTRODUCTION

Multilevel inverters (MLIs) have been an emerging power electronics technology with promising developments and growing importance for dc-ac electrical energy conversion system [1], [2]. They are exceptionally popular for high/medium voltage applications and thus envisaged to continue garner continuous attention in the near future. Tremendous research works are ongoing for establishing new MLI topologies for various applications [3].

Despite the widespread popularity and recognizable maturity of cascaded H-bridge in single-phase applications, there are still intensive effort devoted to the establishment of alternative multilevel topologies specifically for single-phase system [4]. For instance, the conception of switched dc source introduced in [5] has been utilized in [6] and [7], where a multi-source multilevel dc-dc converter is connected to an H-bridge. Comparing with the cascaded H-bridge, the integrated module topologies offer a key advantage of extensively reduced number of power switches.

Besides, a different approach termed the T-type inverter [8] that was initially developed for three-phase system has recently enhanced its adaptability for single-phase applications as well. Nonetheless, a typical T-type inverter have a limitation of voltage levels up to only three levels. To address this issue, [9]–[11] have recently advocate the deployment of a half-bridge together with the T-type inverter. Parallel connection between the half-bridge and the T-type inverter can effectively increase the number of voltage level. Alternatively, [12] proposed to cascade an H-bridge to the T-type inverter. The floating capacitor connected to the H-bridge is charged to quarter of the dc source voltage and thus enable up to seven voltage levels generation.

Lately, a MLI topology developed by [13] which is referred to as a ST-type MLI exploits the T-type inverter as the basic cell. Two T-type inverters are connected back-to-back across four auxiliary power switches. An essential prerequisite for proper operation of this topology is the need of four asymmetrical dc sources to accomplish up to 17 voltage levels generation. Compared to the ST-type MLI, a similar topology called E-type MLI presented in [14] requires two less power switches, at the expense of a relatively reduced number of voltage level with only 13 voltage levels generation.

The concept of back-to-back connected T-type inverters has further inspired and initiated investigations on different improved topologies. The switch-ladder MLI, for example, expands the T-type inverter vertically by increasing the number of series-connected dc sources with additional bidirectional switches [15]. On the other hand, attempts have also been made by expanding the T-type inverter horizontally [16]. The established submultilevel MLI is essentially composed

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of multiple T-type inverters with the outer T-type inverters enclosing their inner counterparts.

All the above mentioned MLI topologies are perceived to face limitation in their gain. They are not capable of voltage boosting since their gain are confined to one. Attention should be drawn to the fact that multiple isolated dc sources are inevitable in these topologies if higher output voltage is desired. In this sense, the incorporation of the so-called switched-capacitor circuit into MLIs is recently attempted to increase the voltage boosting gain [17]–[24]. The established topologies in these literatures share one common characteristic in essence, i.e. they are constituted by two stages. The first stage which comprises a switched-capacitor dc-dc converter is dedicated to generate positive voltage levels, while the second stage which normally comprises an H-bridge is dedicated to the polarity control of output voltage. A major drawback of these topologies is the inherently high voltage stress across some power switches in the second stage since some of them are subjected to voltage stress as high as the maximum voltage level, which is highly undesirable.

The aim of this paper is to contribute to a new MLI topology which employ power switches with low voltage rating for single-phase system. With only single dc source, the proposed topology is able to generate up to seven voltage levels with a voltage boosting gain of three. The voltage stress across any power switch in the proposed topology is restricted within the dc source, which is three times lower than the achievable maximum voltage level. In addition, the proposed topology faces no difficulty in voltage balancing since charge balance of the capacitors is maintained automatically during operation.

The paper is organized as follows: Section II addresses the structure and operating principles of the proposed single-phase MLI topology. A comparison against some selected latest single-phase MLI topologies is examined. In section III, the simulation and experimental results of a low power/voltage prototype is discussed. Finally, section IV draws the conclusion.

II. PROPOSED MLI TOPOLOGY

The circuit configuration of the proposed single-phase MLI topology is depicted in Fig. 1. It consists of three H-bridges. The middle H- bridge is connected to the dc source while the front-end and rear-end H-bridges are connected respectively to a floating capacitor. Neutral terminals of the H-bridges are connected by bidirectional voltage blocking switches which comprised of two MOSFETs with their Source terminals jointly connected. In order to generate higher voltage level, the concept of switched-capacitor is integrated into this topology such that each capacitor is charged to V_{dc} when it is connected in parallel with the dc source, and discharged when it is connected in series with the dc source. Despite the mere use of a single dc source, the maximum voltage level is $3V_{dc}$, which is an excellent merit of the proposed topology.

As mentioned earlier, switches in the existing switched-capacitor based MLI topologies [23], [24] suffer from

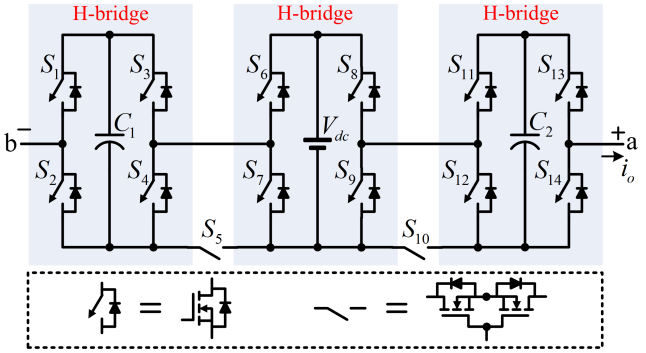

FIGURE 1. The proposed single-source 7-level inverter with triple voltage gain.

TABLE 1. Switching states of the proposed topology.

State	[0]	[+1]	[+2]	[+3]	[-1]	[-2]	[-3]
S1	0	0	0	0	1	1	1
S2	1	1	1	1	0	0	0
S3	1	1	1	1	1	0	0
S4	0	0	0	0	0	1	1
S5	1	1	1	0	1	0	0
S6	1	1	1	0	1	1	1
S7	0	0	0	1	0	0	0
S8	1	1	1	1	1	1	0
S9	0	0	0	0	0	0	1
S10	1	1	0	0	1	1	0
S11	1	1	0	0	1	1	1
S12	0	0	1	1	0	0	0
S13	0	1	1	1	0	0	0
S14	1	0	0	0	1	1	1

voltage stress as high as the maximum voltage level owing to their two-stage configurations. Voltage stress across all the switches in the proposed MLI topology are constrained to three times lower than the maximum voltage level, i.e. V_{dc}. This is an evident advantage over the two-stage switched-capacitor based MLIs. To substantiate the merit of voltage stress reduction, the corresponding equivalent circuits for all voltage levels/states are summarized in Fig. 2. The switching states are summarized in Table 1. Note that the proposed topology is also not affected when dead-time is taken into account during transition between two voltage levels/states. Though not specifically elaborated, it is not hard to analyze from Fig. 2 that the transition between voltage levels demonstrates smooth commutation with no voltage spike occurrence when dead-time is considered. Specifically, the voltage level during dead-time commutation is either equal to the current voltage level or the next voltage level, irrespective of the direction of load current.

Fig. 3 illustrates the key waveforms of the proposed MLI topology. Fundamental load current with load angle of φ is considered. The angles for output voltage level of V_{dc}, $2V_{dc}$ and $3V_{dc}$ are defined as θ_1, θ_2, and θ_3 respectively. Capacitor C_1 discharges for a shorter period during the positive half-cycle ($3V_{dc}$) than during the negative half-cycle ($-2V_{dc}$ and $-3V_{dc}$). It is worth noting that the discharging period of C_2 is

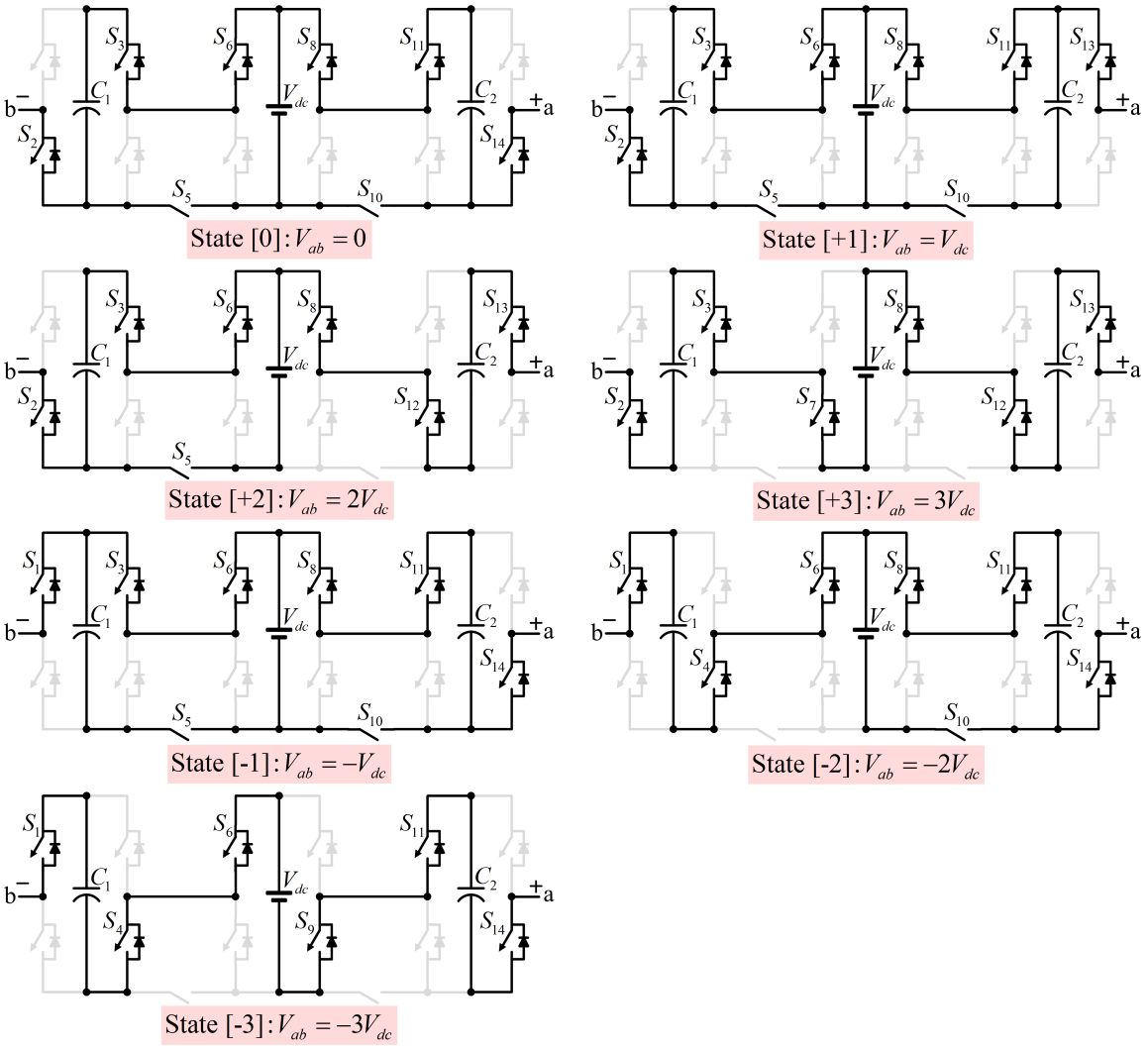

FIGURE 2. Equivalent circuits for all voltage levels / states.

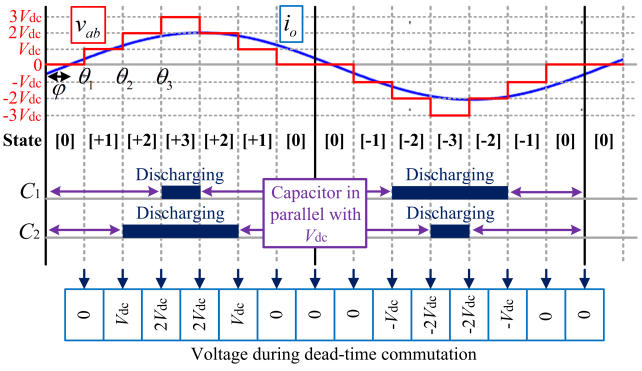

FIGURE 3. Key waveforms of the proposed single-phase MLI topology.

complementary to that of C_1, which is during $2V_{dc}$, $3V_{dc}$ and $-3V_{dc}$. With symmetrical output voltage and symmetrical load current over half of each fundamental cycle, the complementary discharging sequence of C_1 and C_2 can ensure equivalent changes of electric charges in both capacitors. Therefore, their average voltages are automatically balanced during operation.

The voltage ripples across the capacitors could be derived by considering their respective longest discharging period, i.e. from $(\pi + \theta_2)$ to $(2\pi - \theta_2)$ for C_1, and from (θ_2) to $(\pi - \theta_2)$ for C_2. In this instance, the capacitors are connected in series with the load. On that account the changes of electric charge depends on the load current and power factor. The capacitors voltage ripple is therefore written as,

$$\Delta V_C = \frac{\sqrt{2} I_o \cos\theta_2 (PF)}{\pi f_o C} \tag{1}$$

where I_o denotes the rms of load current, $PF = \cos\varphi$, f_o denotes the fundamental output frequency (50Hz), and $C = C_1 = C_2$.

A comparative assessment of the proposed single-phase MLI topology with some of the latest single-phase MLI topologies is presented to highlight their relative distinctions.

TABLE 2. Comparison between the proposed single-phase MLI topology and the latest single-phase MLI topologies.

References	(a)	(b)	(c)	(d)	(e)	(f)
[14]	4*	13	10	$6V_{dc}$	32	1
[15]	4*	17	10	$8V_{dc}$	40	1
[4]	3	7	10	$3V_{dc}$	22	1
[24]	1	9	11	$2V_{dc}$	16	2
Proposed	**1**	**7**	**16**	V_{dc}	**16**	**3**

(a): number of dc sources
(b): number of levels
(c): number of switches and diodes
(d): maximum voltage stress across switches
(e): number of switches and diodes when their maximum voltage stress are kept within V_{dc} by connecting multiple devices in series
(f): voltage gain = maximum voltage level / total dc sources voltages
*: asymmetrical dc sources

Various criteria with emphasis on the features, the maximum voltage stress sustained by switches, as well as the attainable voltage gain are tabulated in Table 2. One common drawback of the MLI topologies in [14] and [15] is the mandatory requirement of four asymmetrical dc sources in generating the great number of output voltage levels to achieve higher output voltage. Since the maximum voltage level is achieved by connecting all the dc sources in series, their gain are therefore strictly limited to unity. Moreover, the voltage stress across the switches are exceedingly high despite their merit of low switch count. More precisely, some power switches of the MLI topologies in [14] and [15] are subjected to block voltage levels as high as $6V_{dc}$ and $8V_{dc}$, respectively. As a remedy in reducing the voltage stress, multiple series-connected switches can be used, with the expense of increment in switch count. Similarly, [4] that use multiple dc sources also suffers from the abovementioned drawbacks, i.e. requires multiple dc sources, voltage gain limited to unity and high voltage stress on power switches.

Unlike the above-mentioned MLI topologies, switched-capacitor based MLI topology which features two-stage configuration faces no restriction in voltage gain. Note that the MLI topology proposed in [24] exhibit the voltage boosting capability. With the assistance of two switched-capacitors, the maximum output voltage is twice that of the dc source. However, these topologies further relieve the voltage stress endured by the switches. Essentially, switches in the H-bridges experience voltage stress equivalent to their achievable maximum voltage level, i.e. $2V_{dc}$.

While retaining the use of two switched-capacitors, the proposed MLI topology is accomplished with only single-stage configuration. It is superior in the sense that it further extends the voltage boosting gain to three, while at the same time lowers the voltage stress across all switches to only V_{dc}. Therefore, the proposed topology is no longer requiring series-connected power switches to achieve higher voltage rating, as in the other topologies. When considering voltage stress of all power switches kept within V_{dc}, the switch counts in the other topologies are apparently greater than that in the proposed topology, as shown in Table 2. In this regard, the so-called merits of low switch counts in the other topologies are void.

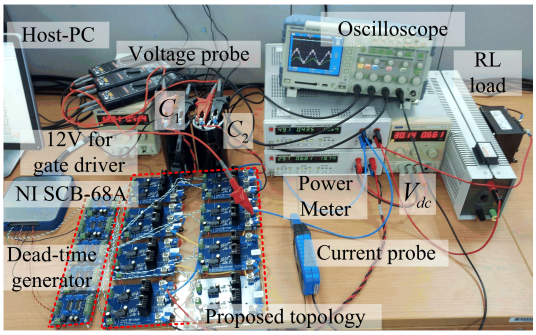

FIGURE 4. Experimental prototype.

III. SIMULATION AND EXPERIMENTAL RESULTS

A low power/voltage experimental prototype shown in Fig. 4 was tested to verify the operation of the proposed single-phase MLI topology. Sixteen Silicon Carbide power MOSFETs (Wolfspeed C2M0280120D) and two 4700 μF capacitors (KEMET ALS30A472NP400) were used in the prototype. Switching signals were computed from a host-pc running Simulink Desktop Real-Time software and generated through the data acquisition device. Switching signals were fed into the dead-time generator prior to the gate drive circuitry to control the power switches.

The experiment was first performed under a purely resistive load. With the input dc source of 30V, it is apparent from Fig. 5a that the load current is proportional to the output voltage with seven distinct levels. The magnitude of each voltage level is read as 30V with the maximum voltage level is 90V, thus signifying the voltage boosting gain of the proposed topology is three. Besides, the voltage across both the capacitors in the topology are noted balanced with their average voltage maintained at the dc source voltage, i.e. 30V.

To reinforce the observation on the capacitors voltage ripples, the oscilloscope was then set to ac coupling mode. The peak-to-peak voltage ripples illustrated in Fig. 5b is 1.6V. It was also observed that C_1 discharges during $\{3V_{dc}, -2V_{dc}, -3V_{dc}\}$ and C_2 discharges during $\{2V_{dc}, 3V_{dc}, -3V_{dc}\}$, which conform to the analysis in Fig. 2 and Fig. 3.

For further verification, the corresponding simulated results were then plotted in Fig. 5c for comparison with the measured results. The discharging periods for the capacitors are in good agreement with those obtained in the experiment. In contrast to the visible rise-time noticed in the experimental waveforms, the capacitors charged up to V_{dc} almost instantly in the simulated waveforms since ideal power switches and ideal capacitors are assumed in the simulations. Also note that the simulated capacitor voltage ripples were 1.43V, which is slightly lower than the 1.6V obtained from the experiment. The discrepancy between the simulated and measured values

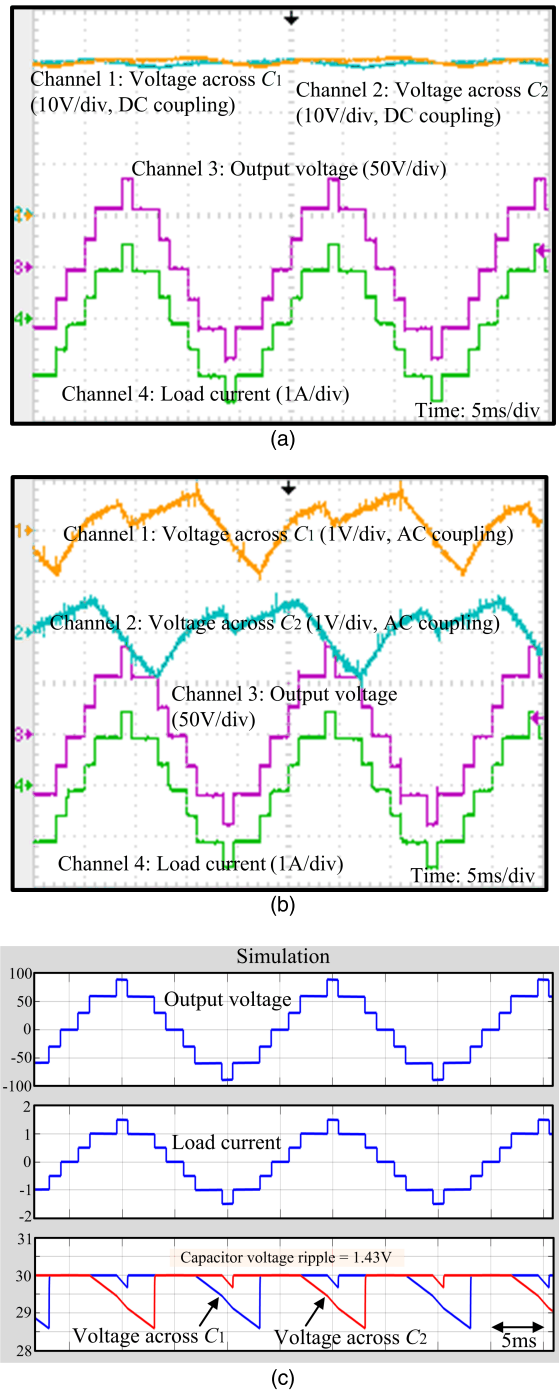

FIGURE 5. Results for purely resistive load (PF = 1), (a) measured capacitors voltages, output voltage and load current, (b) measured capacitors voltage ripples, output voltage and load current, and, (c) simulated waveforms for comparison with experimental measurements.

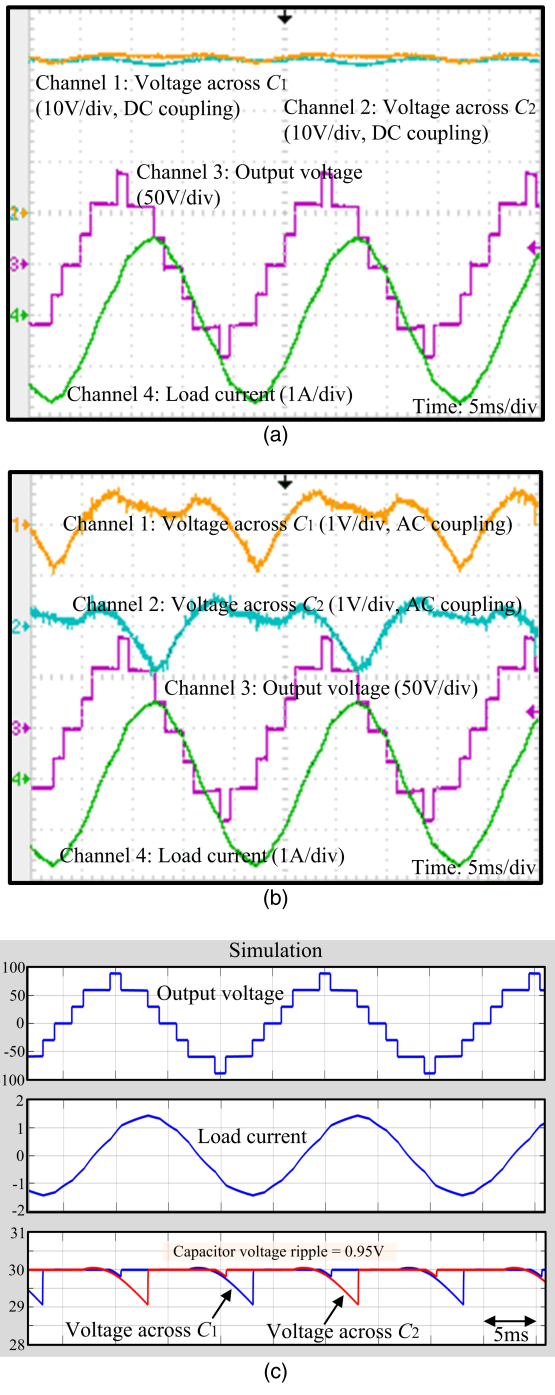

FIGURE 6. Results for resistor-inductor load (PF = 0.6), (a) measured capacitors voltages, output voltage and load current, (b) measured capacitors voltage ripples, output voltage and load current, and, (c) simulated waveforms for comparison with experimental measurements.

is insignificant and close to the estimated 1.4V calculated from (1).

The experiments and simulations were repeated for resistor-inductor load. With a power factor (*PF*) of 0.6, the capacitor voltage ripples in Fig. 6 are seen smaller than that in Fig. 5 (unity *PF*). This observation suggests that the capacitors voltage ripples decrease with lower *PF*, which agrees well with (1). For clarification, let consider the specific instant when capacitor C_2 is switched into series connection with the load at θ_2 (i.e. towards $2V_{dc}$ generation). Note that the capacitor voltage was seen increasing prior to its discharging action, which is attributed to the low power factor ($\varphi > \theta_2$).

This observation indicates that the short duration between θ_2 and φ is the charging period where load current is negative

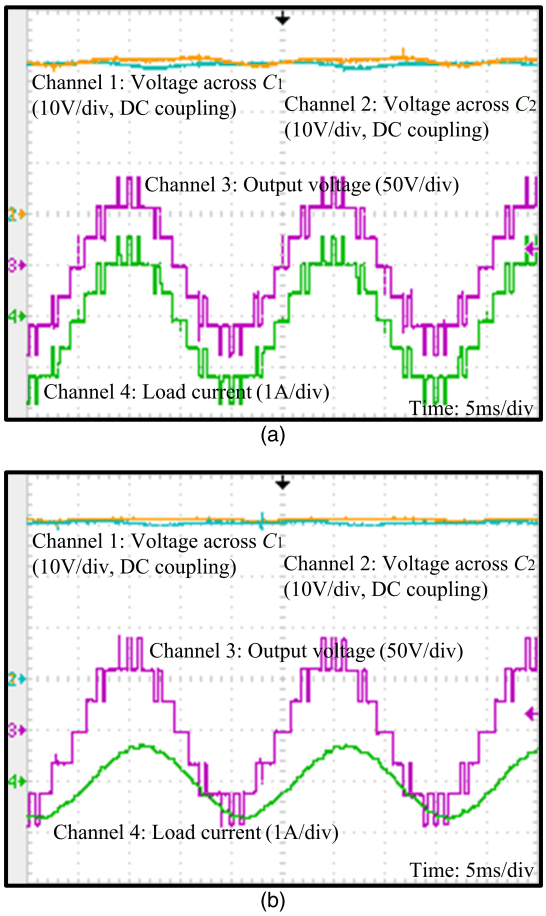

FIGURE 7. Results for the proposed MLI topology controlled by SPWM under, (a) purely resistive load (PF = 1), (b) resistor-inductor load (PF = 0.9).

and flowing into the positive terminal of C_2. The interval between φ and $(\pi - \theta_2)$ is the discharging period for C_2 when load current is positive. Similar observations and discussions are also applicable for C_1, except that it is now referred to negative half-cycle of the load current. The capacitor voltage ripples obtained in either simulation or calculation is the same, i.e. 0.95V. On the other hand, results obtained from the experimental measurement is 1.4V.

Experimental testing were then performed with the proposed single-phase MLI topology controlled by sinusoidal pulse width modulation (SPWM). The level shifted triangular carriers with frequency of 1kHz was considered. The resulting experimental waveforms under either the purely resistive load or the resistor-inductor load are captured in Fig. 7. The results confirmed that the proposed topology worked well under SPWM. It can be noticed that the average value of the capacitors voltages are balanced at 30V, which corresponds to the dc source voltage. Once again, it can be affirmed that the proposed topology exhibits the capability of seven voltage levels generation with a voltage boosting gain of three. Fig. 8 follows to demonstrate the measured efficiency of the experimental prototype. The efficiencies for output power ranges from 25W to 45W are satisfactorily well above 90%.

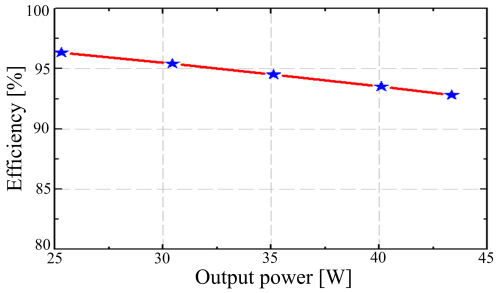

FIGURE 8. Measured efficiency of the experimental prototype.

With switch counts reduction, the proposed topology is anticipated to be more efficient than other topologies presented in Table 2. Comprehensive efficiency comparison for all the topologies implemented using the same power switches will be considered for future works.

IV. CONCLUSION

A new single-phase MLI topology integrated with the switched-capacitor concept has been established in this paper. It enables seven voltage levels generation with the maximum voltage level triple the dc source voltage. It also exhibits self-balancing capability and an interesting key feature of low voltage stress across all power switches. The proposed topology is superior over the latest single-phase MLI topologies in view of its highest voltage boosting gain, lowest voltage stress across switches, and the mere use of a single dc source. Therefore, it is an attractive alternative which open the possibility for the application in single-phase dc-ac power conversion systems. Good agreement among theoretical analysis, simulation and experimental results verified the operation and advantages of the proposed MLI topology.

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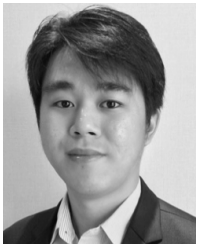

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