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VLSI Architecture for Novel Hopping Discrete Fourier Transform Computation

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ABSTRACT The hopping discrete Fourier transform (HDFT) is a new method applied for time-frequency spectral analysis of time-varying signals. In the implementation of HDFT algorithms, the updating vector transform (UVT) plays a key role, and therefore a novel recursive DFT-based UVT formula is introduced in the proposed design for a HDFT algorithm and its architecture. The perceived advantages can be summarized as: 1) the proposed algorithm reduces the number of multiplications, additions, and coefficients by 42.3%, 33.3%, and 50%, respectively, compared with Park's method under the settings of an M-sample complex input sequence ($M = 256$), and an N-point recursive DFT computation scheme ($N = 64$) for time hop L ($L = 4$); 2) by adopting the hardware-sharing scheme and the register-shifting concept, the proposed design only takes nine multipliers and 12 adders for realization. The proposed hardware accelerator can be implemented using a field-programmable gate array, which can operate at 48.33 MHz clock rate. The resource utilization of combinational logic lookup tables (LUTs) and digital signal processing (DSP) blocks reduced by 11.7% and 42.5% compared with Juang *et al.*'s work. For very-large-scale integration realizations, the proposed design would be more powerful than other existing algorithms in future applications focusing on DSP, filtering, and communications.

INDEX TERMS Hopping discrete Fourier transform (HDFT), sliding discrete Fourier transform (SDFT), recursive discrete Fourier transform (RDFT), recursive DFT-based UVT.

I. INTRODUCTION

In the field of digital signal processing (DSP), the discrete Fourier transform (DFT) is one of the most important discrete orthogonal transformations. Fourier analysis entered many applications, e.g., wireless communication and spectral analysis [1]. In recent years, several low-complexity mathematical algorithms have been developed for discrete-time signal processing [2]. The so called sliding transforms, like the sliding DFT (SDFT) [3]–[5], are applied on a sample-by-sample basis to analyze the time-frequency spectrum of the desired signals. SDFT has been used in various applications, e.g., the adaptive power-line interference canceler [6], the phase-locked loop (PLL) [7], the variable sampling frequency-based adaptive PLL [8], and the three-phase harmonic component detector [9]. The SDFT algorithm can directly use the previous DFT results to iteratively compute each new output bin. Hence, the SDFT's computational complexity is lower than that for traditional DFT. In [3] and [4], several SDFT algorithms described that the standard SDFT only takes four

real additions and four real multiplications for computing each spectral bin in next window. In addition, considering the potential problems about the instability of standard SDFT filter and its heavy computational complexity, the guaranteed-stable SDFT and the sliding Goertzel DFT were proposed to overcome these critical issues. In [5], Duda presented the so called modulated SDFT (mSDFT), which resembles to the basic DFT. This relies on circular frequency shifting to maintain the precision and the stability of the Fourier sliding transform. However, mSDFT imposes heavy computational cost, due to its hopping style. These algorithms have to perform the DFT for all of the time indices, even though the DFT output needs to be calculated only every L ($L > 0$) samples. That is, the overlap of time-window (N) is decreased from $(N-1)$ to $(N-L)$ between two subsequent local windows. Compared with SDFT, the successive outputs of DFT have L interval-samples as shown in Fig. 1. In other words, the resolution of the time-frequency representation will be how affected with different samples of L . In practical application,

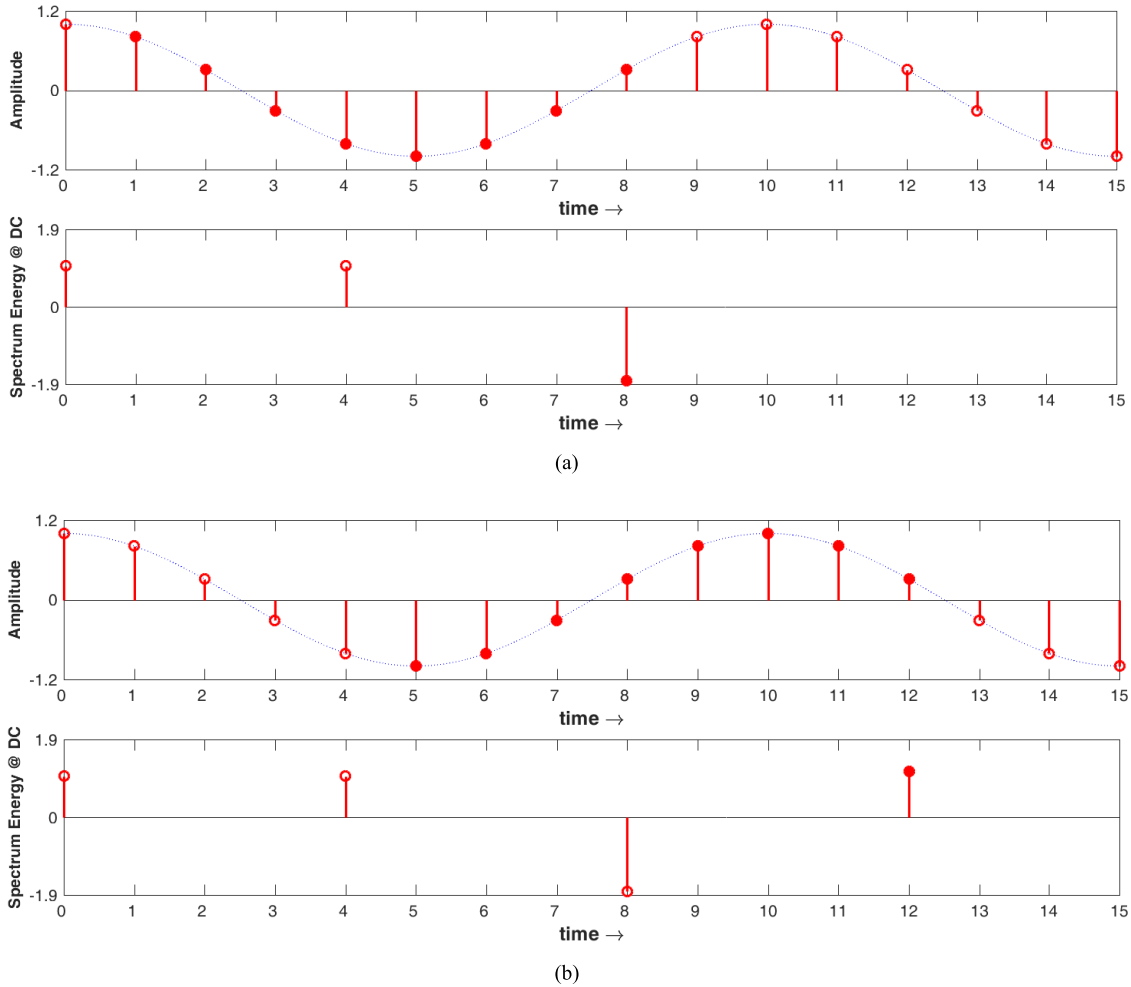


FIGURE 1. The relationship between SDFT and the successive DFT outputs with L interval samples, where N is 8 and L is 4. (a) Previous window. (b) Current window.

Park proposed the idea of time hopping to achieve less computational requirement SDFT algorithms, i.e., the generalized SDFT (gSDFT) [10] and the optimal SDFT (oSDFT) [11]. Based on the same concept, it can be combined with the adaptive DFT for performing synchrophasor measurements [12], [13]. On the other hand, the hopping DFT (HDFT) [14], [15] with the time hop is introduced to reduce the computational complexity. For the fast computation of the HDFT, Park proposed a radix-2 decimation-in-time (DIT) updating vector transform (UVT) and a UVT-based HDFT algorithm in [14]. In [15], the DFT modulation property according to mSDFT [5] was adapted to HDFT. This helped reduce the cumulative round-off errors and to ensure the pole placed on the unit circle in the complex plane. According to [14] and [15], the HDFT computation can be combined with the sliding unit, the UVT unit, and the resonators unit. Among various kinds of units, the UVT has most complexity than other units. Additionally, the increase of time hops implies that the computational complexity and hardware cost are greatly

increases. This is the major reason that a low-complexity and low-cost novel hopping DFT algorithm is needed to develop.

In this paper, we derive a novel recursive architecture for HDFT integrated with a recursive DFT-based (RDFT-based) UVT algorithm. The proposed UVT algorithm overcomes the shortcomings of Park’s UVT filter: (i) Park’s design has non-uniform architecture with arbitrary-time hopping computation; (ii) the UVT kernel of the proposed design guarantees a low-complexity and low-cost accelerator after employing a comb and a resonator cascade filter. Note that the resonator filter is implemented according to Lai’s method [16]–[18].

The rest of the paper is organized as follows. The proposed algorithm is derived in detail in Section II. Hardware accelerator mapping is displayed in Section III. Section IV compares the performance of the proposed design with that of other existing approaches. Section V presents hardware implementations for the proposed methods. Finally, conclusions and remarks are provided.

II. DERIVATION OF THE PROPOSED ALGORITHM

In this section, a HDFT is derived to be an alternative of the SDFT for the time-frequency analysis. The mathematical introduction and the properties of SDFT are given first, then an efficient and compact RDFT-based UVT design are proposed for low-complexity HDFT computation.

A. HDFT ALGORITHM

The k -th spectral bin of an N -point DFT formula at the time index m is defined as

$$X_m[k] = \sum_{n=0}^{N-1} x[\widehat{m} + n] W_N^{-nk}, \quad (1)$$

where $x[\widehat{m} + n]$ and $X_m[k]$ are, respectively, the time-domain and frequency-domain signals, $\widehat{m} = m - N + 1, k = 0, 1, \dots, N - 1$, and the twiddle factor, W_N , is denoted by

$$W_N = e^{j2\pi/N}. \quad (2)$$

As presented shown in [3] and [4], the relationship between $X_m[k]$ and $X_{m-1}[k]$ can be derived from

$$\begin{aligned} X_m[k] &= \sum_{n=0}^{N-1} x[\widehat{m} + n] W_N^{-nk} \\ &= W_N^k \sum_{n=0}^{N-1} x[\widehat{m} - 1 + n] W_N^{-nk} \\ &\quad + x[\widehat{m} + N - 1] W_N^k - x[\widehat{m} - 1] W_N^k \\ &= (X_{m-1}[k] + x[m] - x[m - N]) W_N^k. \end{aligned} \quad (3)$$

Furthermore, the solution of this difference equation [see (3)] can be expressed by z-transform. The z-domain transfer function, $H_{SDFT}(z)$, for the SDFT filter is

$$H_{SDFT}(z) = \frac{(1 - z^{-N}) W_N^k}{1 - W_N^k z^{-1}}. \quad (4)$$

This means that the SDFT algorithm can be implemented by a comb filter $(1 - z^{-N})$ cascading with a resonator. When the output data rate of the spectral bin is the same as the input data rate, the first and the last samples between the current window and the pre-window in (3) can comply with the SDFT property. This means that SDFT could be treated as DFT with time hopping ($L = 1$). Similarly, for arbitrary-time hops, the HDFT relationship between $X_m[k]$ and $X_{m-L}[k]$ – as shown in [14] and [15] – is derived by recursively substituting $X_m[k]$ into $X_{m-L}[k]$ L times in (3). The resultant formula is given by

$$\begin{aligned} X_m[k] &= \sum_{n=0}^{N-1} x[\widehat{m} + n] W_N^{-nk} \\ &= W_N^{Lk} \sum_{n=0}^{N-1} x[\widehat{m} - L + n] W_N^{-nk} \end{aligned}$$

$$\begin{aligned} &+ \sum_{n=N}^{N-1+L} x[\widehat{m} + n - L] W_N^{-(n-L)k} \\ &- \sum_{n=0}^{L-1} x[\widehat{m} + n - L] W_N^{-(n-L)k} \\ &= W_N^{Lk} \sum_{n=0}^{N-1} x[\widehat{m} - L + n] W_N^{-nk} \\ &\quad + \sum_{n=0}^{L-1} (x[\widehat{m} + n + N - L] - x[\widehat{m} + n - L]) W_N^{-(n-L)k} \\ &= (X_{m-L}[k] + D_m^L[k]) W_N^{Lk}, \end{aligned} \quad (5)$$

where $D_m^L[k]$ is defined as the k -th bin of the L -point UVT substitute.

$$D_m^L[k] = \sum_{n=0}^{L-1} d[m - n] W_N^{(n-L+1)k}, \quad (6)$$

where $d[m] = x[m] - x[m - N]$ and $k = 0, 1, \dots, N - 1$.

Equation (6) can be therefore rewritten as

$$\begin{aligned} D_m^L[k] &= W_N^k \left(\sum_{n=0}^L d[m - n] W_N^{-Lk} W_N^{nk} - d[m - L] \right) \\ &= W_N^k \left(\sum_{n=0}^L (d[m - n] W_N^{-Lk} - d[m - n - L]) W_N^{nk} \right) \\ &= W_N^k \left(\sum_{n=0}^L \widehat{d}[m - n] W_N^{nk} \right), \end{aligned} \quad (7)$$

where

$$\widehat{d}[m] = d[m] W_N^{-Lk} - d[m - L],$$

and

$$d[m - n - L] = 0|_{n \neq 0}.$$

After expanding the sigma function of the UVT filter in (7), we obtain a recursive formula as

$$\begin{aligned} D_m^L[k] &= W_N^k \left(\sum_{n=0}^L \widehat{d}[m - n] W_N^{nk} \right) \\ &= \left(\widehat{d}[m - L] W_N^k + \widehat{d}[m - L + 1] \right) W_N^k + \dots + \widehat{d}[m] W_N^k. \end{aligned} \quad (8)$$

Hence, the kernel function of the difference equation is obtained as (9).

$$D[m, k] = \left(D[m - 1, k] + \widehat{d}[m] \right) W_N^k, \quad (9)$$

where $D[-1, k] = 0$. Here, the z-domain transfer function, $H_D(z)$, is derived from the recursive difference equation (9).

$$H_D(z) = \frac{W_N^k}{1 - W_N^k z^{-1}}. \quad (10)$$

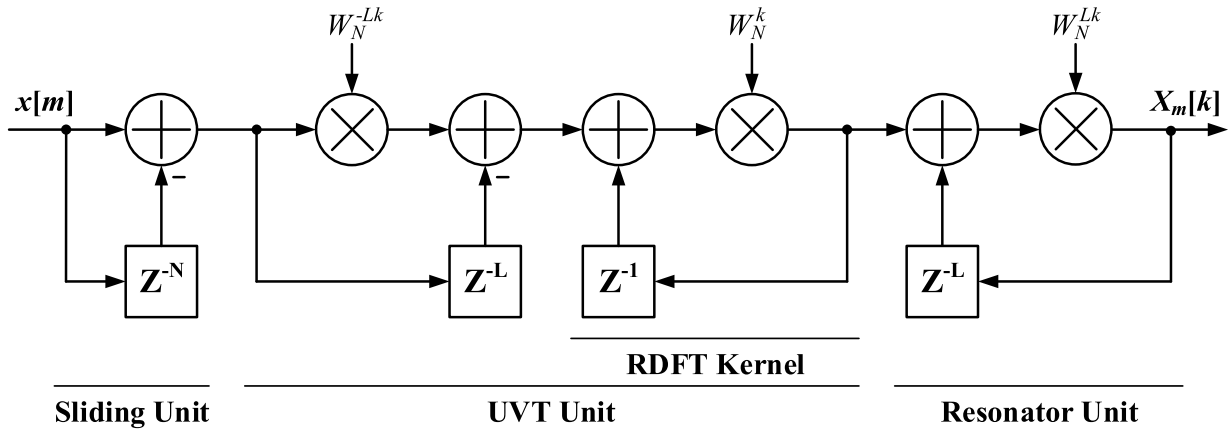


FIGURE 2. The novel hopping DFT structure with recursive computation.

According to (5) and (10), the proposed novel HDFT structure with a recursive kernel is depicted in Fig. 2.

B. NOVEL RDFT-BASED UVT FORMULA

Since equation (8) is similar to the derivation of RDFT in [16]–[18], the function, $D[L, k]$, can be derived as

$$D_m^L[k] = D[L - 1, k]. \tag{11}$$

Via (8) and (9), and taking the result of $D_m^L[k]$ at time $n = L - 1$, the coefficient of UVT can be obtained by L iterations. From [16]–[18], the transfer function $H_D(z)$ can be derived as

$$\begin{aligned} H_D(z) &= \frac{W_N^k}{1 - W_N^k z^{-1}} \\ &= \frac{W_N^k (1 - W_N^{-k} z^{-1})}{(1 - W_N^k z^{-1})(1 - W_N^{-k} z^{-1})} \\ &= \frac{W_N^k - z^{-1}}{1 - 2 \cos \theta_k z^{-1} + z^{-2}} \\ &= \frac{(\cos \theta_k - z^{-1}) + j \sin \theta_k}{1 - (2 \cos \theta_k - z^{-1}) z^{-1}}, \end{aligned} \tag{12}$$

where $\theta_k = 2\pi k/N$. Now, the proposed architecture design for the RDFT-based UVT algorithm is shown in Fig. 3.

III. VLSI ARCHITECTURE DESIGN

In the proposed design, the key indices in terms of speed, area, and power are all considered before starting VLSI implementation. In this section, we discuss how to use well-known design techniques to improve chip speed, to reduce chip area, and to achieve area efficiency for the proposed architecture.

For the purpose of explaining, the nodes of graph are named, e.g., A_m , B_m , and C_m , and are all tagged in Fig. 3. Besides, to obtain the real and the imaginary parts of the UVT filter or for a complex-number output, the functions are also built, as (13) and (14).

$$\begin{aligned} \Re_m &= \text{Re} \{ D_m^L[k] \} \\ &= \text{Re} \{ B_m \} - \text{Re} \{ C_m \} - \text{Im} \{ A_m \} \times \sin \theta_k, \end{aligned} \tag{13}$$

Function 1 Compute the Real Part of a Complex Number

Input: The results of the UVT filter, $D_m^L[k]$

Output: The real part of the UVT filter, \Re_m

1. $\dot{D}_m^L[k] = \text{conjugate}(D_m^L[k])$
2. $\Re_m = (D_m^L[k] + \dot{D}_m^L[k]) / 2$
3. return \Re_m

Function 2 Compute the Imaginary Part of a Complex Number

Input: The results of the UVT filter, $D_m^L[k]$

Output: The imaginary part of the UVT filter, \Im_m

1. $\dot{D}_m^L[k] = \text{conjugate}(D_m^L[k])$
2. $\Im_m = (D_m^L[k] - \dot{D}_m^L[k]) / 2j$
3. return \Im_m

TABLE 1. Latency analysis in various units for the proposed architecture.

Unit	Path	Latency	Worst
Sliding	In. to Out.	$1T_A$	$1T_A$
RDFT-based UVT	In. to Out. through A_m	$2T_M + 4T_A$	$2T_M + 5T_A$
	In. to Out. through B_m	$2T_M + 5T_A$	
Resonator	In. to Out.	$1T_M + 2T_A$	$1T_M + 2T_A$
Total			$3T_M + 8T_A$

$$\begin{aligned} \Im_m &= \text{Im} \{ D_m^L[k] \} \\ &= \text{Im} \{ B_m \} - \text{Im} \{ C_m \} + \text{Re} \{ A_m \} \times \sin \theta_k, \end{aligned} \tag{14}$$

where the subscript m is a time index, and the pseudo-code for $\text{Re}\{\bullet\}$ and $\text{Im}\{\bullet\}$ are shown in Function 1 and 2, respectively.

A. LATENCY ANALYSIS AND IMPROVEMENT

The latency between the input and the output of a path can be calculated in various units [see Fig. 2 and Fig. 3]. The results are listed in Table 1. The critical path of the proposed

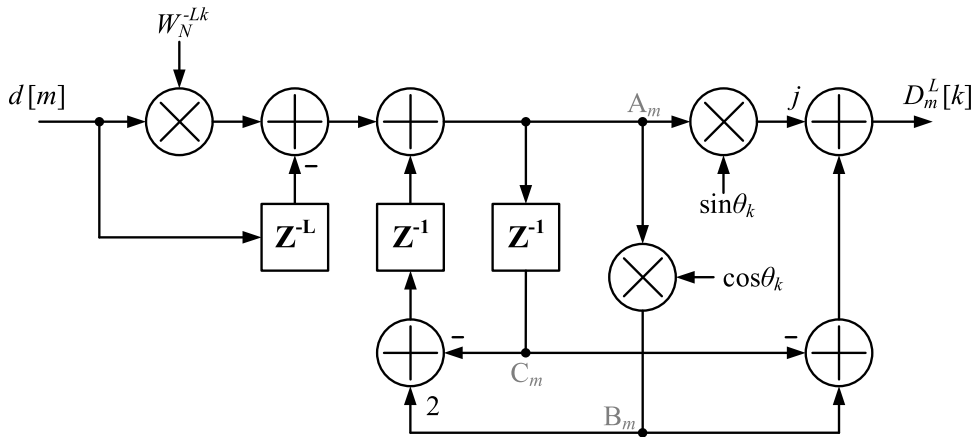


FIGURE 3. Proposed novel RDFT-based UVT design.

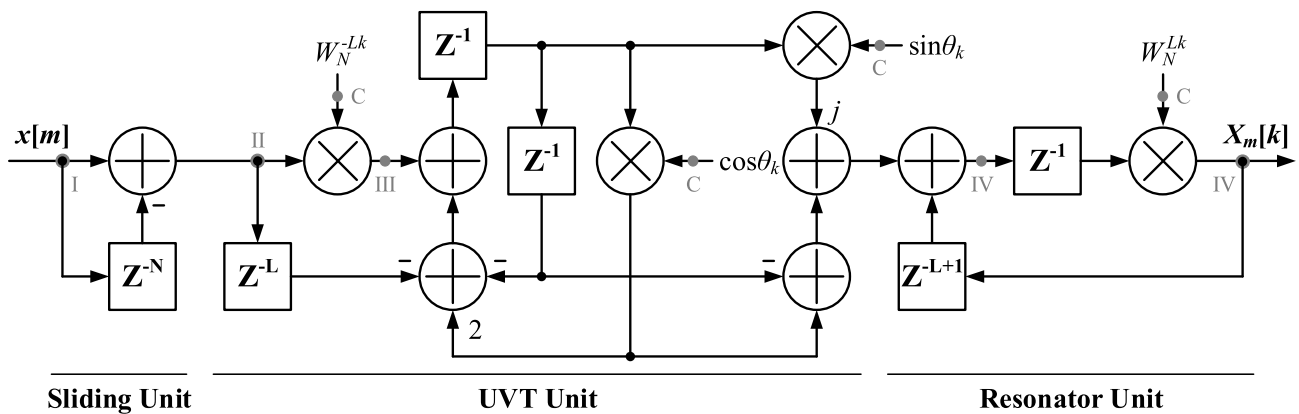


FIGURE 4. Proposed low-critical-path HDFT design.

algorithm consists of $3T_M + 8T_A$, where T_M is the time period of the real multiplier and T_A is the time period of the real adder.

Note that the time period of one complex multiplier is evaluated as $1T_M + 1T_A$ under $x[m]$ is a complex sequence. After applying basic VLSI techniques and a re-timing scheme [19] to shorten the critical path on Fig. 3, the proposed low-critical-path HDFT design is displayed in Fig. 4. There, the critical path is greatly shortened from $8T_A + 3T_M$ into $3T_A + 1T_M$.

B. HARDWARE RESOURCE SHARING SCHEME

For the property of HDFT [see (5) and (11), or Fig. 1], the output data rate of spectral bin decreased by a factor of L compared with SDFT. The hardware resource of the proposed architecture can be shared, namely, the real and the imaginary part calculation circuits can be interlaced as shown in the right side of Fig. 4. The control flow and the plan of calculations are described on a flow diagram (FD) in Fig. 5. The FD is divided into five procedures:

- Proc. 1: Calculate the real part of the UVT filter, and then accumulate the results from the previous DFT. The values of $\text{Re}\{A_m\}$, $\text{Im}\{B_m\}$, and $\text{Im}\{C_m\}$ need to be stored for use in Proc. 2.

- Proc. 2: Similar to Proc. 1, but calculate the imaginary part of the UVT filter and accumulate the results from the previous DFT.
- Proc. 3: Calculate the real part of the new DFT with L -samples.
- Proc. 4: Calculate the imaginary part of the new DFT with L -samples.
- Proc. 5: Update temporary variables Var_III, Var_VI, and Var_VII. The variables are realized using a D-type flip-flop for hardware implementation.

Fig. 6 (a) displays an example of the proposed hardware sharing scheme based on the above FD. The number of time hops (L) is set to two. The timing diagram of the overall architecture is displayed in Fig. 6 (b).

As mentioned above, the results show that the proposed method not only shortens the latency, but also uses the hardware sharing scheme to reduce the cost of the area. Moreover, the power consumption can be saved, simultaneously.

IV. DISCUSSION AND COMPARISON

For the hopping issue of various HDFT algorithms, the performance metrics in terms of numbers of multiplication, addition, and coefficient are evaluated in Table 2. For performance metrics, we set the transformation length (N) of

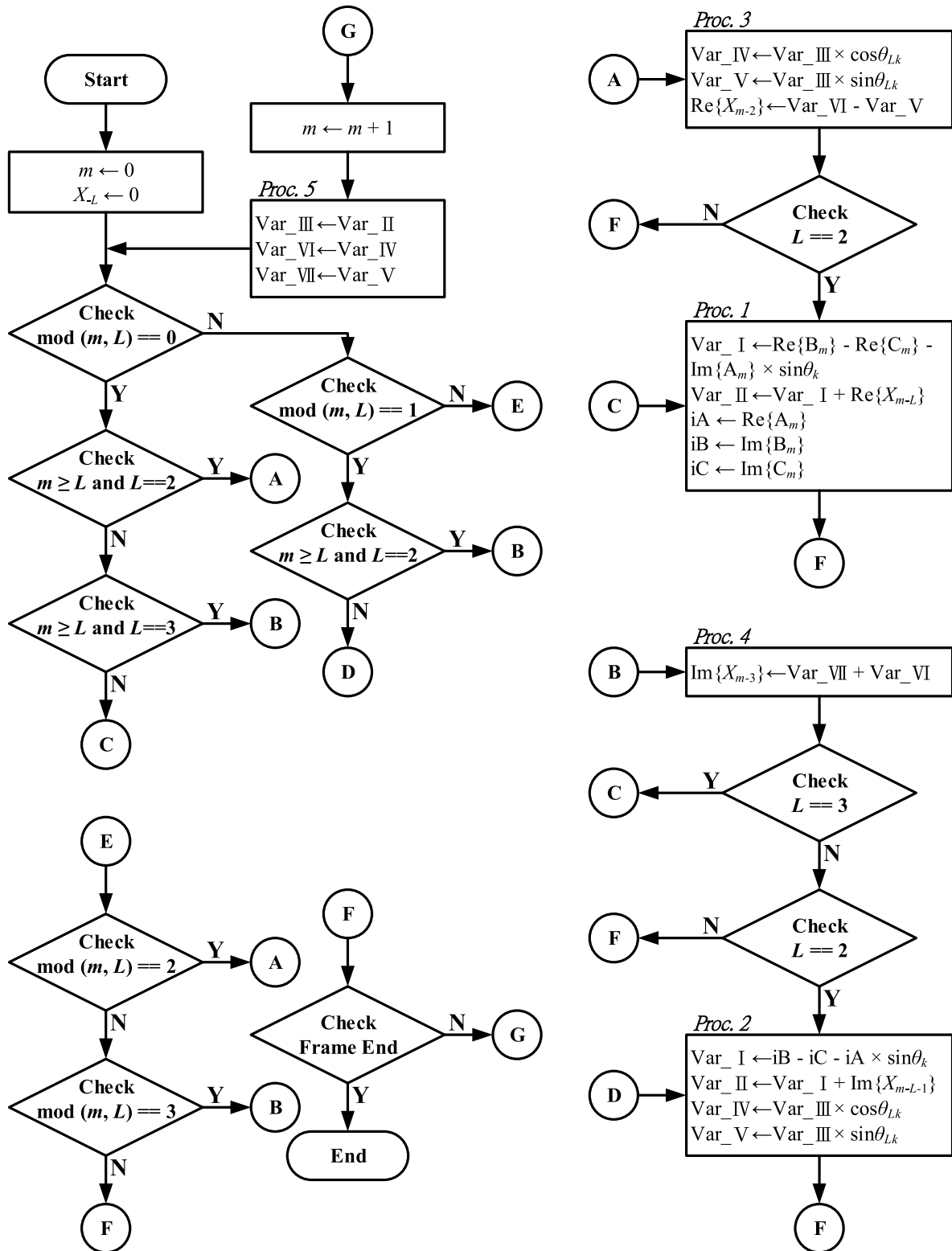


FIGURE 5. Flow diagram of the control and the plan of calculations.

DFT to 64, the time-domain frame size (M) to 256, the number of time hops (L) to 4, and the input signal to complex numbers for k -th spectral bin of the single-bin. Note that one complex multiplication involves four real multipli-

cations and two real additions. The evaluation results show that although Wang's [15] method is more accurate than Park's [14], it has greater computational complexity, i.e., 3,840 multiplications and 4,096 additions. In this paper, the

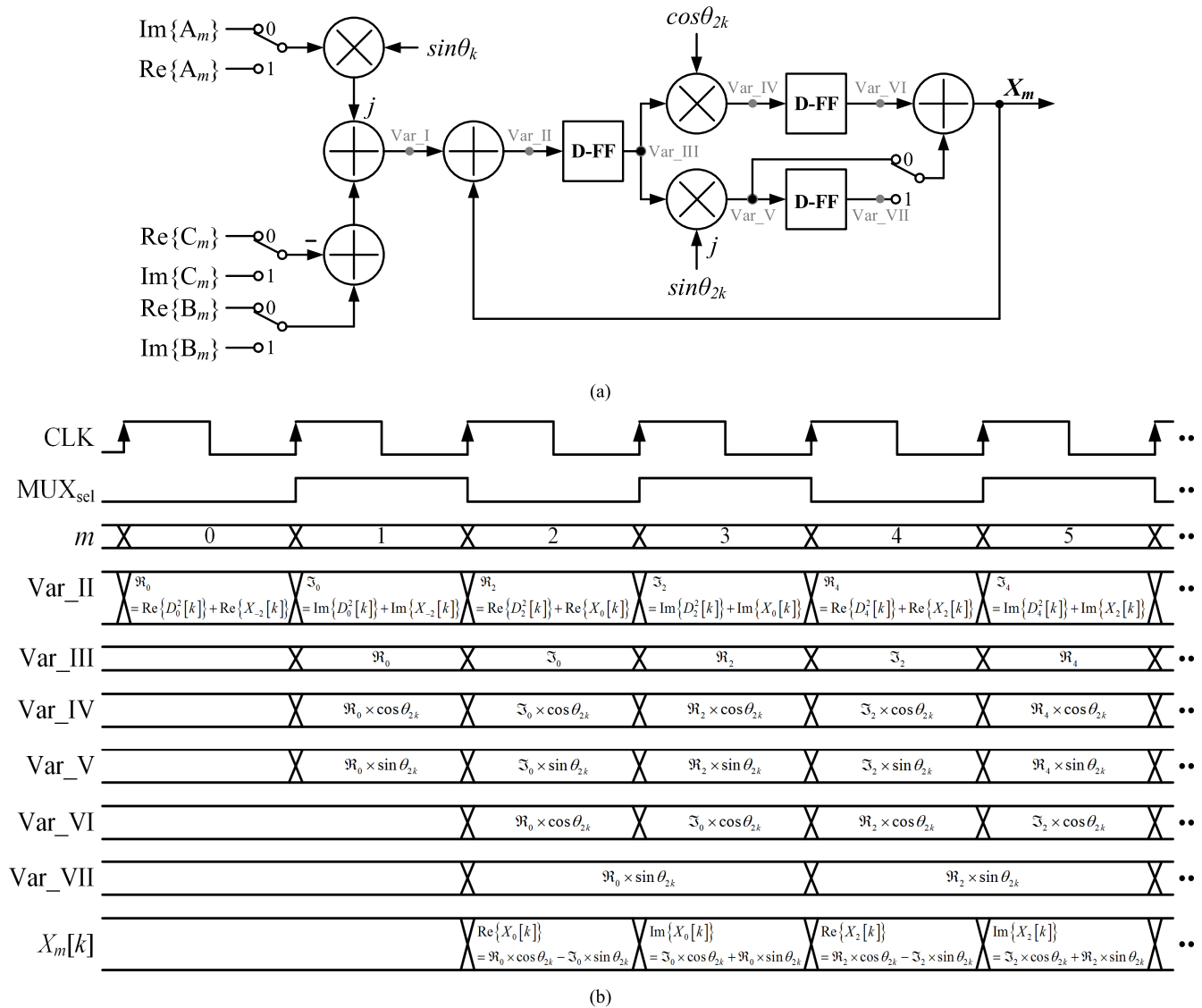


FIGURE 6. Hardware design for proposed HDFT structure. (a) Hardware architecture design with sharing scheme. (b) Timing diagram of the hardware sharing scheme.

TABLE 2. Computational complexity comparison of N -point HDFT algorithms for hopping applications.

Metrics	2014 [14]	2015 [15]	Previous work [20]	Proposed
Multiplication	$4M * (L - 1) + (4M / L)$	$4M * (L - 1) + (12M / L)$	$8M + (4M / L)$	$6M + (6M / L)$
Addition	$4M * (2L - 1) + (4M / L)$	$2M * (2L - 1) + (8M / L)$	$10M + (4M / L)$	$8M + (8M / L)$
Coefficient	$2L$	$4N + 2L - 2$	4	4
Cri. Path (a) (T_A, T_M)	$(L + 2, 2)$	$(L + 3, 3)$	$(3, 1)$	$(3, 1)$
Cpt. Cycle (b)	M	M	$M + 2$	$M + 2$
Cpt. Time	(a) * (b)			

RDFT-based computation with a recursive kernel for the UVT filter, and it not only takes fewer computational complexity than previous works [20] but also reduces the number of multiplications, additions, and coefficients by 42.3%,

33.3%, and 50%, respectively, compared with Park's [14] method.

Table 3 shows the comparison of the hardware resources for HDFT algorithms. Hardware resources include

TABLE 3. Hardware cost comparison of N-point HDFT architecture designs for hopping applications.

Metrics	2014 [14]	2015 [15]	Pre-work [20]	Proposed
Multiplier	4L	4L + 8	12	9
Adder	4L + 2	4L + 6	14	12
Register	N + 2L - 1	N + 3L - 1	N + 2L + 1	N + 2L + 2
Coefficient	2L	2L	4	4

multipliers, adders, registers, and coefficient-ROM. Here, it should be noticed that one complex multiplier requires four real multipliers and two real adders for the hardware evaluation. The hardware need of the proposed design is lower than that of other designs [14], [15]. There are only nine real multipliers, 12 real adders, 74 registers, and four coefficients in our implementation. Compared with previous works [20], we saved 25% on multipliers and 14.3% on adders.

Overall, the advantages of the proposed design are low complexity and area efficiency, and it would be more suitable for real-time time-frequency spectral applications.

V. IMPLEMENTATION AND RESULTS

A. FPGA IMPLEMENTATION

Before mapping HDFT algorithm into FPGA, a detailed and completed analysis is made to the word-length of each node for the proposed architecture through mathematical software, and then the available precision selected according to the simulation reports. We assume the test signal is influenced by complex Gaussian noise. It has zero-mean, and its variance equals one. First we feed the test signal in 16-format, until each node [see Fig. 4] is recorded at each time slot using fixed-point arithmetic in Q-format, as listed in Table 4. The node quality of recursive DFT is evaluated through the signal-to-quantization-noise ratio (SQNR) as

$$\epsilon_m = X_{mDFT}^k - X_{mHDFT}^k \tag{15}$$

$$SQNR = 10 \log \left(X_{mDFT}^{k2} / \epsilon_m^2 \right), \tag{16}$$

where X_{mDFT}^k denotes the standard DFT bin output from the batch data of length N, and X_{mHDFT}^k stands for the recursive computations of the proposed algorithm. The simulation results are shown in Fig. 7, and the selected optimization set reports that the proposed hardware has approximate 100 dB SQNR as well as previous work [20] does, since we select the finite-word representation of fractional numbers are 24 bits and 27 bits on the coefficients of twiddle factors and internal each node, respectively.

For hardware implementation, the proposed architecture was coded by the Verilog-2001 hardware description language (HDL), and converted from HDL into an SRAM Object File (SOF) or Programmer Object File (POF) using Quartus II software. Table 5 displays the comparison between the proposed design and previous works [20] after FPGA implementations. We used Altera Cyclone IV, an FPGA device,

TABLE 4. Fixed point word-length analysis at each node of the proposed (low-critical-path) HDFT design.

Node	Word-length	
	Format	Total bits
I	Q1.15	16
II	Q2.15	17
III	Q2. ΔL ₁	2+ ΔL ₁
IV	Q7. ΔL ₁	7+ ΔL ₁
C	Q1. ΔL ₂	1+ ΔL ₂
Other	Q4. ΔL ₁	4+ ΔL ₁

TABLE 5. FPGA implementation and resource utilization.

Hardware Cost	Hardware Block (Cyclone IV E EP4CE115F29C7)	
	Previous work [20]	Proposed
LC Combinations	1634	1443
LC Registers	465	560
DSP Elements	80	46
DSP 18x18	40	23
Mem.	RAM	64 * 32 bits
	ROM	4 * 25 bits
Dyn. Power (mW)	Unlist	23.33
Max Speed (MHz)	47.26	48.33
Norm. Power (mW/MHz)	Unlist	0.48

TABLE 6. Physical chip results.

Technology	TSMC 0.18μm 1P6M CMOS
Word Lengths (Max Inter. / Coeff.)	34 bits / 25 bits
Supplied Voltage / Clock Rate	1.8 V / 25 MHz
Data Memory (RAM)	64 * 32 bits
DFT-Length (N) / Time Hop (L)	64 / 4
Power Consumption (Chip / Core)	49.8 mW / 23.2 mW
Chip Size / Core Size	2.0737 mm ² / 0.7937 mm ²
Gate Count	133,161

which can be operated at 48.33 MHz. The realization results show that the resource utilization of combinational logic lookup tables (LUTs) and DSP blocks reduced by 11.7% and 42.5%, respectively, compared with previous works [20]. The dynamic power consumption based on the test signal is shown in Fig. 8. The normalized power metrics are given in Table 5. Overall, the advantages of the proposed design has low complexity and area efficiency, although the utilization

TABLE 7. Implementation of cell-based design for the proposed HDFT accelerator.

Unit	Power (mW)	Percentage (%)	Area (um ²)	Percentage (%)	Power norm. to area (mW / mm ²)
Sliding	9.92	42.76	359,600	45.3	27.59
UVT (RDFT-based)	11.2	48.28	313,225	39.46	35.76
Resonator	1.89	8.15	110,880	13.97	17.05
Other	0.19	0.81	10,045	1.27	18.91

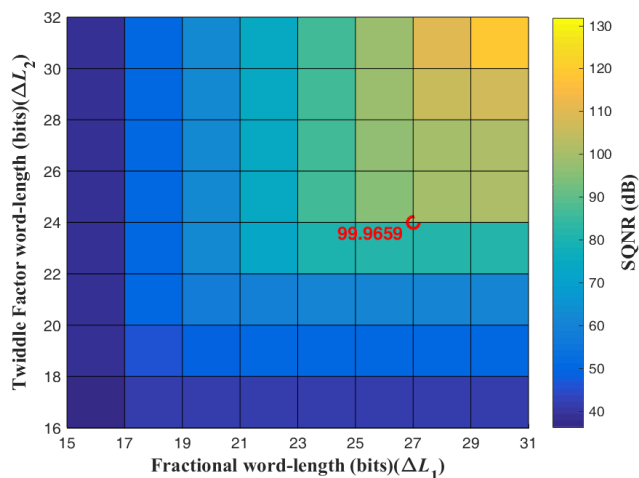


FIGURE 7. Bit-level SQNR simulation for the proposed (low-critical-path) HDFT design.

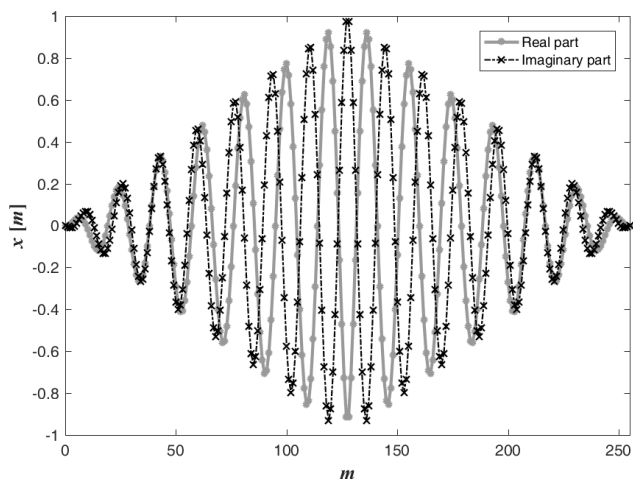


FIGURE 8. A test signal with complex Gaussian distribution for power analysis.

of registers are increased for saving the derived values that are generated in the calculation.

B. ASIC PHYSICAL RESULTS

The proposed architecture was implemented using an application specific integrated circuits (ASIC) chip with 0.18-um technology. The Taiwan Semiconductor Manufacturing Company Limited (TSMC) 0.18-um 1P6M CMOS

standard-cell library was used, and then the verilog code synthesized using the Synopsys Design Compiler and place-and-route for layout using Cadence SOC Encounter. The specifications and the chip results of the implementation are listed in Table 6. The total pad count of the design is 130. It is packaged in a ceramic quad flat pack (CQFP) package. The chip size is 1780 um × 1165 um and the core size is 1250 um × 635 um. The power consumption is 49.8 mW at 25 MHz as simulated by the Synopsys PrimePower tool. For analysis of the core size and the power consumption, the proposed design can be divided into four sub-blocks, as listed in Table 7. In the sliding unit, the function z^{-N} is realized by a two-port memory, which dominates the metrics. In the UVT unit, the percentages of the power and the area use are 48.28% and 39.26%, respectively. This confirms that the proposed RDFT-based UVT filter is greatly involved in the reduction of computational and hardware cost. The resonator unit has small portion of the power consumption and the area compared with other units, because it only takes a light workload and employs resource sharing. In Table 7, the power consumption is normalized to the corresponding area. According to the result, the UVT filter plays a crucial role that decides the complexity and the performance of chip.

VI. CONCLUSION

This paper presented a low-complexity, low-cost, RDFT-based architecture design for HDFT computation. The proposed HDFT algorithm employs a unified recursive kernel for arbitrary length time hops. The results show that the proposed method has lower hardware requirements compared with previous works. It would be a more powerful element for a VLSI realization in future applications focusing on digital signal processing, filtering, and communications.

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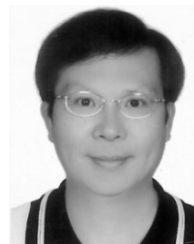
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