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A Three-Level Modular DC/DC Converter Applied in High Voltage DC Grid

HONGCHENG YOU AND XU CAI
Wind Power Research Center, School of Electronic Information and Electrical Engineering, Shanghai Jiao Tong University, Shanghai 200240, China
Corresponding author: Xu Cai (xucai@sjtu.edu.cn)

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ABSTRACT Modular dc/dc converter (MDCC) based on cascaded submodules (SMs) has been an attractive converter topology for the interconnection of high voltage dc (HVDC) grids for its low cost and high efficiency; however, the quite large filter inductor implemented at lower voltage side significantly increases the system volume. In this paper, a buck three-level type MDCC (Buck-TL-MDCC) is derived from the classic buck three-level converter (Buck-TLC) by replacing the switches and blocking capacitor with cascaded SMs for HVDC application. Just like the major merit of the Buck-TLC, the filter inductance of the Buck-TL-MDCC can be reduced, and the high voltage blocking capacitor is eliminated by the cascaded SMs. Instead of the sine-wave modulation employed by prior arts of MDCCs, the stepped two-level modulation is adopted; it offers the following merits: 1) smaller SM capacitance requirement; 2) smaller ac circulating current; 3) the switching frequency is equal to the fundamental frequency, which avoids extra switching actions; 4) the computation burden is dramatically reduced. Finally, the simulation and experimental results verify the effectiveness of the proposed Buck-TL-MDCC.

INDEX TERMS Dc/dc power conversion, high voltage direct current (HVDC) transmission, modular multilevel converter (MMC), dc grid.

I. INTRODUCTION

Multi-terminal high voltage direct current (HVDC) transmission technology and dc grid technology are the efficient methods to resolve the problems of renewable energy integration, however, high voltage dc transformer is required to interconnect the apart HVDC systems with different voltage levels like the function of the ac transformer in the ac grid [1]–[4]. Traditional dc/dc topologies (e.g. buck converter) are not applicable here because the voltage levels of the HVDC systems are typically hundreds of kilovolts, so that a series connection of hundreds of IGBTs is required, which brings additional snubber circuits and makes the driving units quite complicated [5]. What's more, the series connection of power switches produces extremely high dv/dt stress, which results in the serious electromagnetic interference (EMI) [6].

Dual-active-bridge (DAB) with input-series-output-series (ISOS) configuration [7] can realize high voltage dc/dc power conversion, but the main disadvantage is the requirement of a large number of isolation transformers, which have high potential differences between the windings [8].

Modular multilevel converter (MMC) [9] based on cascaded submodules (SMs) has become the preferable topology in high voltage dc/ac conversion, and the MMC based dc/ac/dc converter can effectively achieve high voltage dc/dc power conversion [6], [10], [11]. As a transformer is employed in the intermediate ac link to perform voltage stepping and achieve electric isolation, the MMC based dc/ac/dc converter is suitable for high voltage stepping ratio (>5) application, e.g., to interconnect dc based offshore wind farm (30kV) and HVDC transmission system (300kV). But the two dc/ac conversion stages and full-rated ac transformer result in large system volume and high cost.

Auto transformer has been the preferable choice in ultra-high voltage ac grid due to its high efficiency and low cost [12], though it loses the ability of electric isolation. Similarly, electric isolation may not be necessary in the interconnection of HVDC systems, and a so-called dc/dc autotransformer (DC AUTO) was developed in [13] and [14]. DC AUTO reduces the required capabilities of the ac transformer and MMCs, but the ac transformer is still indispensable. Since the MMC operating with power frequency results

in large system volume due to the quite large SM capacitance [15], medium ac frequency is recommended to reduce the SM capacitance. However, the manufacture of medium-frequency ac transformer for HVDC application is difficult now [16], this may limit the application of the converters requiring ac transformers.

Later, [17] presented a non-isolated modular dc/dc converter (MDCC) based on two chains of SMs, where sine-wave modulated ac circulating current is generated to ensure the charge balance of the SM capacitors. Thanks to one stage conversion, it requires the reduced SMs, and gets rid of the ac transformer. Thus, the MDCC provides a low-cost solution for the interconnection of HVDC systems with low or medium voltage stepping ratio [18]–[21]. The major technical challenge of the MDCC is that the filter inductor implemented at lower-voltage side reaches almost one thousand millihenries [19] at hundreds of kilovolts, this is mainly due to the switching speed of state-of-the-art high voltage power switches is not expected to exceed hundreds of Hertz [6]. Though a buck type MDCC (Buck-MDCC) with the stepped 2-level modulation was reported in [22] to lower the ac circulating current and reduce the SM capacitance, the bulk filter inductor is still required. The MDCCs with high voltage stepping ratio are reported in [8] and [23], but the peak-to-peak value of the inner ac voltage is equal to a single SM capacitor voltage, which means the ac circulating current must be quite large to achieve the charge balance of the SM capacitors according to the principle of orthogonal power flow presented in [17]. Thus, these converters are restricted to medium voltage range. Reference [24] proposed the MDCC employing the active filter to substitute for the filter inductor, but the additional full-bridge SMs bring relatively large conduction and switching losses. The MDCC with cross-connected configuration [25] can also eliminate the filter inductor, but the inner high voltage blocking capacitor limits the converter to medium voltage range [24], [26].

In this paper, a buck three-level type MDCC (Buck-TL-MDCC) is derived from the classic buck three-level converter (Buck-TLC) [27] by replacing the switches and blocking capacitor with cascaded SMs (abbreviated as chain-links) [28]. The Buck-TL-MDCC, which was first presented in [28], dramatically reduces the filter inductance with comparison to the MDCCs proposed in [17]–[22], and eliminates the high voltage capacitor required in [25], so that it is suitable for ultra-high voltage dc/dc power conversion.

Generally, sine-wave modulation, including the carrier phase shifted pulse width modulation (CPS-PWM) [24], [25] and the nearest level modulation (NLM) [19]–[21], is adopted in the existing MDCCs. The CPS-PWM requires an additional controller in each SM to balance the capacitor voltages, which significantly increases the economic costs and system complexity. The NLM with a sorting and selection algorithm to balance the SM capacitor voltages is usually preferred in the sine-wave modulated MMC or MDCC because it is easy to be implemented and extended with hundreds-level staircase output voltage [29], however, the high frequency sorting of hundreds of SM capacitor voltages has been a real burden in the MMC operating with 50/60 Hz fundamental frequency [29], [30], the problem will become even worse for the MDCC operating with medium frequency [19]–[21], [24], [25]. To resolve the aforementioned problem, the stepped 2-level modulation [22] is employed by the Buck-TL-MDCC, it offers the following merits: 1) smaller SM capacitance requirements; 2) smaller ac circulating current; 3) the switching frequency is equal to the fundamental frequency, which avoids the extra switching actions existing in the sine-wave modulation; 4) the SM capacitor voltages need only to be sorted twice a period, which poses a significant reduction of the computation burden, especially for ultra-high voltage power conversion requiring hundreds of SMs.

The paper is organized as follows. Firstly, the circuit configuration and the operation principle of the Buck-TL-MDCC is illustrated in Section II, followed by the analysis of the control strategy in Section III. The design principles of the Buck-TL-MDCC are discussed in Section IV. Section V compares the Buck-TL-MDCC and the prior arts of MDCCs through a study case. In Sections VI and VII, the simulation and experimental results verify the effectiveness of the Buck-TL-MDCC. Finally, Section VIII concludes this paper.

II. BUCK THREE-LEVEL TYPE MODULAR DC/DC CONVERTER

A. CIRCUIT CONFIGURATION OF BUCK-TL-MDCC

Fig. 1 shows two basic submodules (SMs), i.e., the half-bridge SM (HBSM) and the full-bridge SM (FBSM). The output voltage of the HBSM is either equal to its capacitor voltage V_C (inserted state) or zero (bypassed state). The output voltage of the FBSM has three levels, i.e., $+V_C$ (positive inserted state), $-V_C$ (negative inserted state) and zero (bypassed state). The cost of the converter based on the FBSMs is significantly higher than that based on the HBSMs because the number of switches is doubled, however, the FBSM provides dc-fault blocking capability because of the negative voltage level [19].

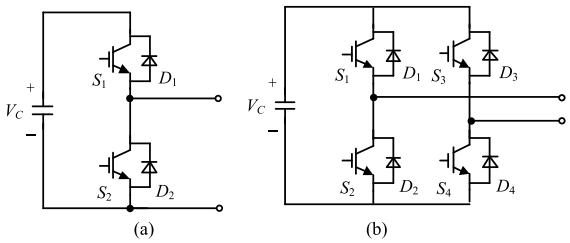

FIGURE 1. Two basic SMs. (a) HBSM. (b) FBSM.

The classic bidirectional buck three-level converter (Buck-TLC) [27] is depicted in Fig. 2. It consists of two pairs of complementary switches, i.e., (S_{1a}, S_{1b}) and (S_{2a}, S_{2b}), a blocking capacitor C_{block}, and a filter inductor L_f. The synthesis methodology of modular dc/dc converters (MDCCs), i.e., replacing the complementary switches in classic dc/dc

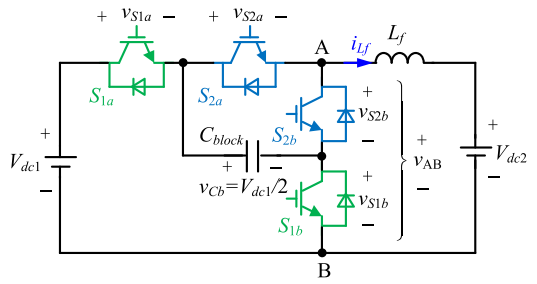

FIGURE 2. Circuit configuration of Buck-TLC.

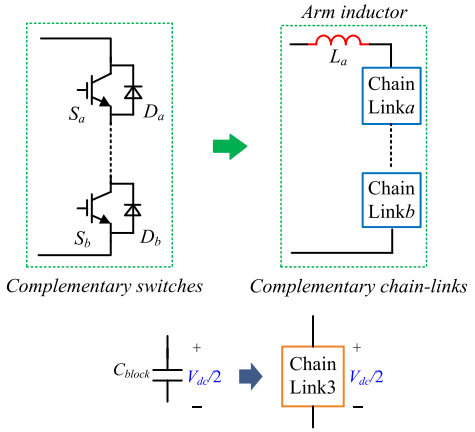

FIGURE 3. Synthesis methodology of MDCCs.

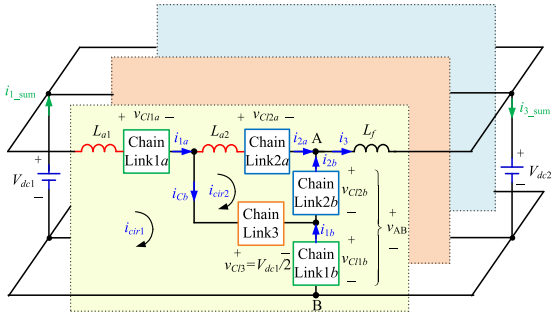

FIGURE 4. Circuit configuration of Buck-TL-MDCC.

converters with two chains of cascaded SMs (abbreviated as complementary chain-links) and an arm inductor as shown in Fig. 3, was proposed in [22]. With that, the Buck-TL type MDCC (Buck-TL-MDCC) [28] can be derived by replacing the two pairs of complementary switches in the Buck-TLC with two pairs of complementary chain-links, i.e., (chain-link 1a, chain-link 1b) and (chain-link 2a, chain-link 2b), and two arm inductors, i.e., L_{a1} and L_{a2}, as shown in Fig. 4, where each chain-link comprises n SMs. The rated voltage of the blocking capacitor C_{block} is half that of the input voltage ($V_{dc1}/2$), which is typically rated for hundreds of kilovolts for ultra-high voltage power conversion. However, the manufacture of the capacitor rated for hundreds of kilovolts may be challenging because it requires the series and parallel connections of hundreds of capacitor units [26], which brings the new problem of the voltage balance of the capacitor units. To resolve the problem, the blocking capacitor (C_{block}) is replaced by the cascaded HBSMs (abbreviated as blocking chain-link) which output dc voltage $V_{dc1}/2$, as shown in Fig. 4.

B. OPERATION PRINCIPLE OF BUCK-TL-MDCC

The Buck-TL-MDDC can functionally converse power with the HBSMs, while to achieve the dc-fault blocking capability, partial SMs should adopt the FBSM [19]. It is assumed that all SMs adopt the HBSM to simplify the analysis. To clearly illustrate the operation principle of the Buck-TL-MDCC, two operation states of chain-link are primarily defined. If total n SMs in the chain-link work in the inserted state, the output voltage of the chain-link is nV_C, it is called the high-level state of the chain-link. If total n SMs in the chain-link work in the bypassed state, the output voltage of the chain-link is 0, it is called the low-level state of the chain-link. Suppose the SM capacitor voltage V_C satisfies

$$nV_C = \frac{V_{dc1}}{2}. \tag{1}$$

The basic waveforms of the Buck-TLC when $V_{dc2} < V_{dc1}/2$ and $V_{dc2} > V_{dc1}/2$ are respectively shown in Figs. 5(a) and 7(a). The voltages across (S_{1a}, S_{1b}) and (S_{2a}, S_{2b}), i.e., (v_{S1a}, v_{S1b}) and (v_{S2a}, v_{S2b}), are complementary 2-level PWM waves. v_{S2a} and v_{S2b} respectively lag v_{S1a} and v_{S1b} 180°, so that a new voltage level, i.e., $V_{dc1}/2$, can be obtained and the equivalent switching frequency is doubled [27]. Similar with the voltage waveforms across (S_{1a}, S_{1b}) and (S_{2a}, S_{2b}) in the Buck-TLC, the output voltages of chain-links 1a, 1b, 2a and 2b in the Buck-TL-MDCC, i.e., v_{Cl1a}, v_{Cl1b}, v_{Cl2a} and v_{Cl2b}, are also 2-level PWM waves as shown in Figs. 5(b) and 7(b), and the duty-ratios of v_{Cl1a}, v_{Cl1b}, v_{Cl2a}, v_{Cl2b} are $(1-d_1)$, d_1, $(1-d_2)$, d_2 respectively. In addition, to keep the charge balance of the SM capacitors [17], the shifted-phases respectively exist between (v_{Cl1a} and v_{Cl1b}), (v_{Cl2a} and v_{Cl2b}), so that the trapezoidal ac circulating currents, i.e., i_{cir1} and i_{cir2}, can be generated between the two pairs of complimentary chain-links as shown in Fig. 4. The waveforms of i_{cir1} and i_{cir2} are exhibited in Fig. 6. The phase-shifted duty ratio between v_{Cl1a} and v_{Cl1b} is d_{s1}, and that between v_{Cl2a} and v_{Cl2b} is d_{s2}. Just the same as the voltages across the switches in the Buck-TLC, v_{Cl2a} and v_{Cl2b} respectively lag v_{Cl1a} and v_{Cl1b} 180°.

To conveniently describe the operation principle of the Buck-TL-MDCC, the following assumptions are supposed to be satisfied:

1) The voltage ripples of the SM capacitors are ignored, i.e., the SM capacitor voltages are V_C.
2) The inductances of L_{a1} and L_{a2} are the same, i.e., $L_{a1} = L_{a2} = L_a$.

The basic waveforms of the Buck-TL-MDCC when $V_{dc2} < V_{dc1}/2$ are given in Fig. 5(b), and it has 8 stages at the steady state in a switching period T:

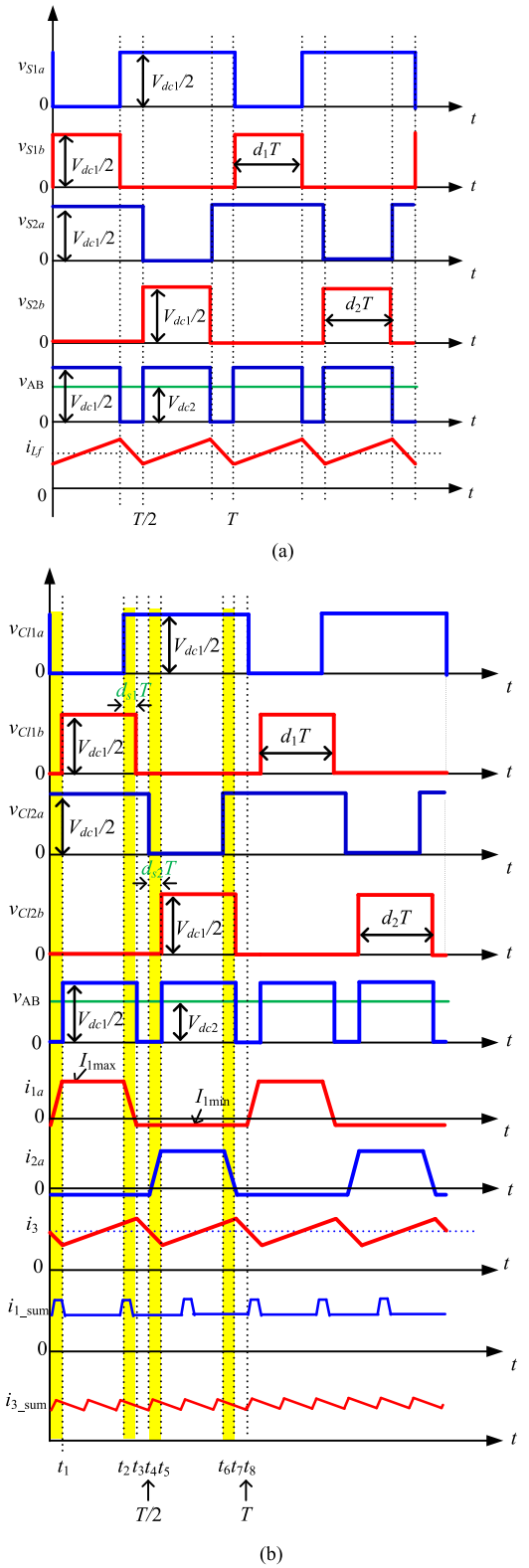

FIGURE 5. Basic waveforms when $V_{dc2} < V_{dc1}/2$. (a) Buck-TLC. (b) Buck-TL-MDCC.

1) *Stage 1 [0, t_1]:* Chain-links $1a$, $1b$, $2b$ work in the low level state, and chain-link $2a$ works in the high level state. The voltages across L_{a1}, L_{a2} and L_f can be respectively expressed as

$$v_{La1}(t) = \frac{V_{dc1}}{2} - (v_{Cl1a} + v_{Cl1b}) = \frac{V_{dc1}}{2} \quad (2)$$

$$v_{La2}(t) = \frac{V_{dc1}}{2} - (v_{Cl2a} + v_{Cl2b}) = 0 \quad (3)$$

$$v_{Lf}(t) = (v_{Cl1b} + v_{Cl2b}) - V_{dc2} = -V_{dc2}. \quad (4)$$

According to the above equations, it is easy to obtain the expressions of i_{1a}, i_{2a} and i_3 as

$$i_{1a}(t) = I_{1a}(0) + \frac{V_{dc1}}{2L_a}t \quad (5)$$

$$i_{2a}(t) = I_{2a}(0) \quad (6)$$

$$i_3(t) = I_3(0) - \frac{V_{dc2}}{L_f}t. \quad (7)$$

2) *Stage 2 [t_1, t_2]:* Chain-links $1a$, $2b$ work in the low level state, and chain-links $1b$, $2a$ work in the high level state. The voltages across L_{a1}, L_{a2} and L_f can be respectively obtained as 0, 0 and $V_{dc1}/2 - V_{dc2}$. Thus, i_{1a} and i_{2a} remain unchanged, i_3 increases linearly.
3) *Stage 3 [t_2, t_3]:* Chain-link $2b$ works in the low level state, and chain-links $1a$, $1b$, $2a$ work in the high level state. The voltages across L_{a1}, L_{a2} and L_f can be respectively obtained as $-V_{dc1}/2$, 0 and $V_{dc1}/2 - V_{dc2}$. Thus, i_{1a} decreases linearly, i_{2a} remains unchanged, i_3 increases linearly.
4) *Stage 4 [t_3, $t_4(T/2)$]:* Chain-links $1b$, $2b$ work in the low level state, and chain-links $1a$, $2a$ work in the high level state. The voltages across L_{a1}, L_{a2} and L_f can be respectively obtained as 0, 0 and $-V_{dc2}$. Thus, i_{1a} and i_{2a} remain unchanged, i_3 decreases linearly.

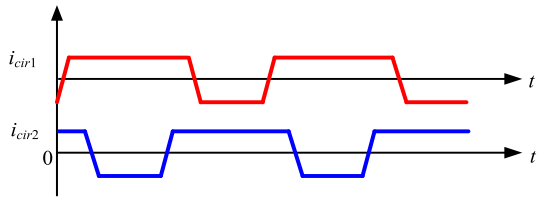

FIGURE 6. Ac circulating currents.

As stages 5-8 are similar to stages 1-4, they are not discussed here for simplification. The waveforms of i_{1a}, i_{2a} and i_3 can be obtained, and the total input and output currents (i_{1_sum} and i_{3_sum}) of the three-phase Buck-TL-MDCC can also be exhibited in Fig. 5(b). It can be observed that fluctuation still exists in the total input and output currents, however, referring to the analysis in [6], the distributed capacitance and inductance of a dc cable can bypass the current ripple to acceptable limit.

Summing v_{Cl1b} and v_{Cl2b}, we can get the voltage across point A and B (v_{AB}) in the Buck-TL-MDCC as shown in Fig. 5(b). It is clear that when $V_{dc2} < V_{dc1}/2$, the voltage levels of v_{AB} are 0 and $V_{dc1}/2$.

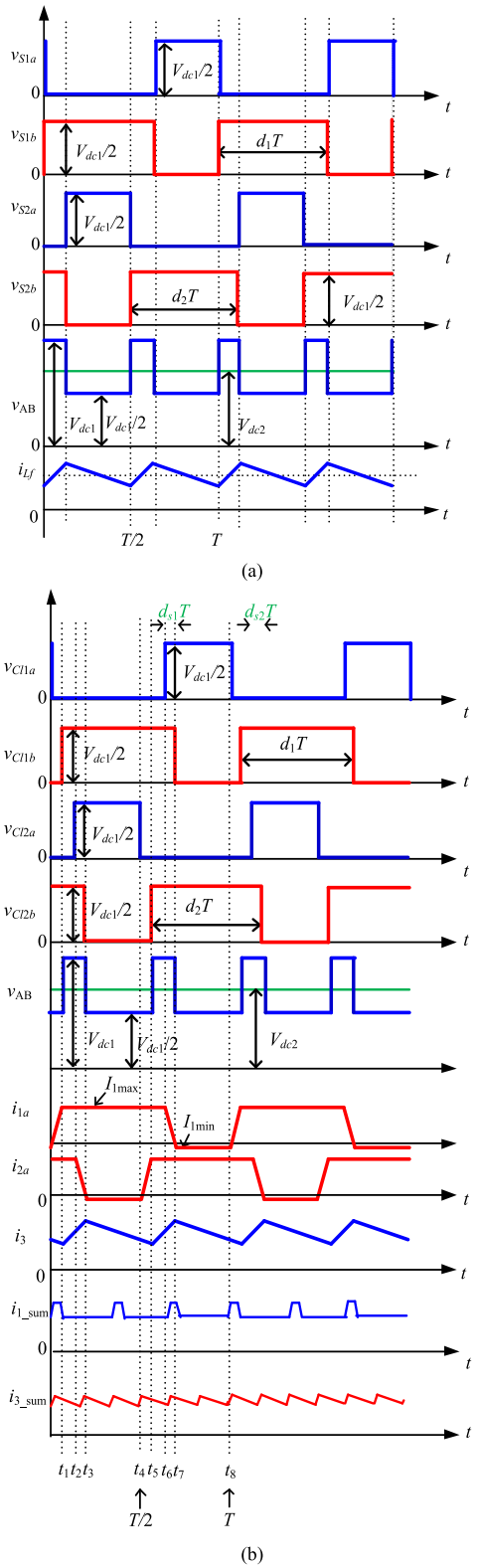

FIGURE 7. Basic waveforms when $V_{dc2} \geq V_{dc1}/2$. (a) Buck-TLC. (b) Buck-TL-MDCC.

Likewise, when $V_{dc2} \geq V_{dc1}/2$, the basic waveforms of the Buck-TLC and the Buck-TL-MDCC are respectively given in Figs. 7(a) and 7(b), where the voltage levels of v_{AB} are $V_{dc1}/2$ and V_{dc1}. As the frequency of v_{AB} is twice the fundamental frequency, and the fluctuation range of v_{AB} is only half of the input voltage ($V_{dc1}/2$), a smaller filter inductance is required in the Buck-TL-MDCC with comparison to the Buck-MDCC proposed in [22].

C. STEADY-STATE ANALYSIS

As $L_{a1} = L_{a2}$, at steady state, d_1 and d_{s1} are equal to d_2 and d_{s2}, respectively. Assume that

$$d_1 = d_2 = D \tag{8}$$

$$d_{s1} = d_{s2} = D_s \tag{9}$$

where D and D_s are the steady value of d_1, d_2 and d_{s1}, d_{s2}, respectively.

To achieve the voltage-second balance of L_f, it is easy to obtain

$$V_{dc2}\,(1-D)\,T = (V_{dc1} - V_{dc2})\,DT. \tag{10}$$

Manipulating the above equation yields

$$D = \frac{V_{dc2}}{V_{dc1}}. \tag{11}$$

As seen from Figs. 5(b) and 7(b), the waveform of i_{1a} is the trapezoidal-wave whose maximum and minimum values are $I_{1\max}$ and $I_{1\min}$, respectively. Referring to (5), the relationship between $I_{1\max}$ and $I_{1\min}$ is

$$I_{1\,\max} - \frac{V_{dc1}}{2L_a} D_s T = I_{1\,\min}. \tag{12}$$

If the transferred power of the converter is P, the average value of i_{1a} is

$$\frac{1}{T}\int_0^T i_1(t)\,dt = I_{1\,\max} D + I_{1\,\min}(1-D) = \frac{P}{V_{dc1}}. \tag{13}$$

Combining (12) and (13), $I_{1\max}$ and $I_{1\min}$ can be respectively expressed as

$$I_{1\,\max} = \frac{P}{V_{dc1}} + \frac{V_{dc1}}{2L_a}(1-D)\,D_s T \tag{14}$$

$$I_{1\,\min} = \frac{P}{V_{dc1}} - \frac{V_{dc1}}{2L_a} D D_s T. \tag{15}$$

With reference to the waveforms of v_{Cl1a} and i_{1a} exhibited in Fig. 5(b), the energy absorbed by chain-link $1a$ in a period can be obtained as

$$W_{Cl1a} = \int_0^T v_{Cl1a}(t)\,i_{1a}(t)dt = \frac{I_{1\,\max} + I_{1\,\min}}{4} V_{dc1} D_s T + \frac{I_{1\,\min}}{2} V_{dc1}(1-D-D_s)\,T \tag{16}$$

where W_{Cl1a} is the energy absorbed by chain-link $1a$ in a period.

Substituting (14) and (15) into the above equation yields

$$W_{Cl1a} = \frac{P(1-D)\,T}{2} + \frac{V_{dc1}^2 T^2}{4L_a}\left[\frac{1}{2}D_s^2 - (1-D)\,DD_s\right]. \tag{17}$$

Likewise, the energy absorbed by chain-links 1b can be obtained as

$$W_{Cl1b} = -\frac{P(1-D)T}{2} - \frac{V_{dc1}^2 T^2}{4L_a}\left[\frac{1}{2}D_s^2 - (1-D)DD_s\right]. \tag{18}$$

To achieve the charge balance of the SM capacitors, the energy absorbed by the chain-links in a period should be zero, which yields

$$D_s = (1-D)D - \sqrt{(1-D)^2 D^2 - 4P(1-D)L_a \Big/ \left(V_{dc1}^2 T\right)} \tag{19}$$

where the steady state value of shifted-phase duty ratio is D_s.

The power analysis of chain-links 2a and 2b are similar and not detailed here. It should be noted that the proposed Buck-TL-MDCC has bi-directional power transferring capability. If power is delivered from V_{dc2} to V_{dc1}, d_{s1} and d_{s2} should be negative values, i.e., v_{Cl1a} and v_{Cl2a} should respectively lag v_{Cl1b} and v_{Cl2b}. In this case, the steady state value D_s can also be calculated by (19), provided that P is set negative value.

Comparing Figs. 5(a) and 5(b), we can find that the main difference between the basic waveforms of the Buck-TLC and the Buck-TL-MDCC is the transition periods of i_{1a}, i_{1b}, i_{2a} and i_{2b} existing in the Buck-TL-MDCC, i.e., the yellow area as shown in Fig. 5(b). i_{1a} is taken as an example to analyze the transition period. If L_a tends to zero, the transition time of i_{1a}, i.e., D_sT, also tends to zero in terms of (19). Meanwhile, the waveform of i_{1a} is transformed from the trapezoidal-wave to a 2-level square-wave. Manipulating (14), (15) and (19), the maximum and minimum values of the square-wave can be respectively obtained as

$$I_{1\max} = \frac{P}{V_{dc1}} + V_{dc1}(1-D)T \cdot \lim_{L_a \to 0}\frac{D_s}{2L_a} = \frac{P}{V_{dc2}} \tag{20}$$

$$I_{1\min} = \frac{P}{V_{dc1}} - V_{dc1}DT \cdot \lim_{L_a \to 0}\frac{D_s}{2L_a} = 0. \tag{21}$$

Interestingly, we can find that the operation waveforms of the Buck-TL-MDCC in this case are the same as that of the Buck-TLC if ignoring the ripple of i_3. Thus, the RMS value of the ac circulating current, i.e., I_{acS2}, can be obtained as

$$I_{ac\_S2} = \frac{P}{V_{dc2}}\sqrt{D(1-D)}. \tag{22}$$

As for the sine-wave modulated MDCCs, if $V_{dc2} > 0.5V_{dc1}$ ($D > 0.5$), the maximum inner ac voltage is limited by the upper chain-link, and if $V_{dc2} < 0.5V_{dc1}$ ($D < 0.5$), the maximum inner ac voltage is limited by the lower chain-link [20], thus, the minimum RMS value of the ac circulating current, i.e., I_{ac_sin}, can be obtained as [20]

$$I_{ac\_\sin} = \begin{cases} \sqrt{2}\dfrac{P}{V_{dc2}}(1-D) & D < 0.5 \\ \sqrt{2}\dfrac{P}{V_{dc2}} \cdot D & D > 0.5. \end{cases} \tag{23}$$

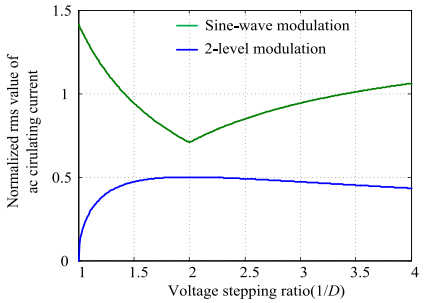

FIGURE 8. Normalized RMS value of the ac circulating current.

According to (22) and (23), the normalized RMS values of the ac circulating currents in these two modulation methods can be plotted in Fig. 8. Obviously, the RMS value of the ac circulating current in the Buck-TL-MDCC is smaller than that in the sine-wave modulated MDCCs, which poses smaller conduction loss.

According to (21), it can be observed that the smaller L_a is, the closer $I_{1\min}$ is to zero, which poses smaller circulating current. Nevertheless, the inductance of L_a cannot be too small for the requirement to limit the rising velocity of the fault current when the V_{dc1}-side dc fault occurs, and the detailed design principle of L_a will be discussed in Section IV-B.

III. CONTROL STRATEGY OF BUCK-TL-MDCC

A. GENERAL CONTROL SCHEME

Fig. 9 shows the general control scheme of the Buck-TL-MDCC, which is composed by four major parts including feedback control, feedforward control, phase-shifted control and voltage balancing control. The phase-shifted control intends to redistribute the power between chain-links 1 and 2, meanwhile, the SM capacitor voltages in the same chain link can be balanced by the voltage balancing control. The feedback control aims to regulate the output current or voltage, and current feedback control is adopted in Fig. 9. The function of the feedforward control is to ensure the blocking

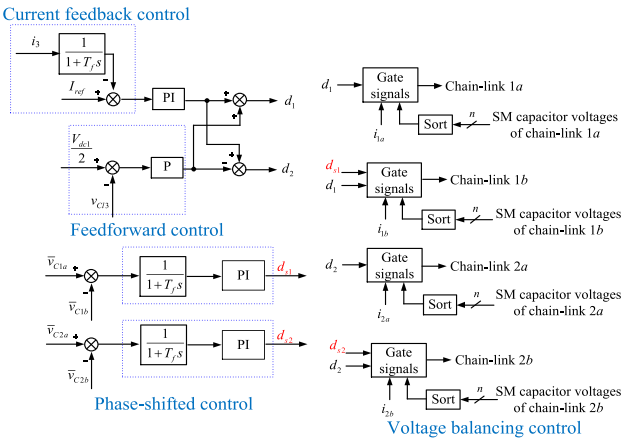

FIGURE 9. Complete control scheme of Buck-TL-MDCC.

chain-link voltage to be half of the input voltage without affecting the current feedback control [31].

B. VOLTAGE BALANCE OF SMS

In practice, the stepped 2-level modulation is introduced [22] to achieve the voltage balance of the SM capacitors and alleviate the dv/dt stress. The output voltage of the chain-link is given in Fig. 10, where the voltage transition period exists in the switching process between the high-level and low-level states. During the voltage rising or descending transition period, the chain-link inserts or bypasses a SM capacitor every T_d second. Generally, $nT_d \ll T$ should be satisfied so that the voltage transition period won't affect the basic operation principle described in Section II-B.

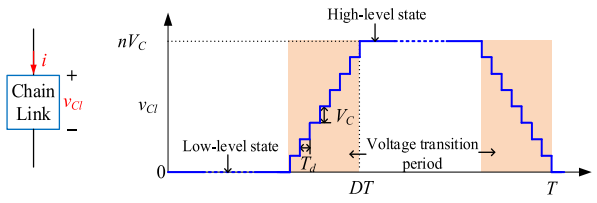

FIGURE 10. Stepped 2-level modulation.

During the voltage rising or descending transition period, the chain-link inserts or bypasses the proper SM capacitor based on the sorting result of the SM capacitor voltages and the polarity of the arm current i as discussed in [22], so that the voltage balance of the SM capacitors can be achieved. To reduce the switching frequency of the switches, each SM capacitor is inserted or bypassed once during the voltage rising or descending transition periods. As the stepping time T_d is small and all SM capacitances are designed to be the same, the voltage rankings of the un-inserted SMs during the voltage rising transition period keep unchanged, and that of the un-bypassed SMs during the voltage descending transition period also keep unchanged. Therefore, the SM capacitor voltages are not necessary to be sorted during the voltage transition period, so that the sorting algorithm needs only to be executed twice in a period. As for the sine-wave modulated converters, the carrier phase-shifted pulse width modulation (CPS-PWM) requires additional controller in each SM [24], [25], and the nearest level modulation (NLM) requires high-frequency sorting of the SM capacitor voltages [19]–[21]. Thus, the stepped 2-level modulation provides a significant reduction of the computation burden with comparison to the sine-wave modulated MDCCs, especially for ultra-high voltage power conversion requiring hundreds of SMs. Moreover, the stepped 2-level modulation allows fundamental switching frequency, which avoids the extra switching actions existing in the sine-wave modulation [19], [20].

It should be noted that the concept of the stepped 2-level modulation was first presented in [6] for the MMC based dc/ac/dc topology, however, the control method, the requirements of the SM capacitance and arm inductance are totally different in the proposed converter. The output voltages of the complementary chain-links in [6] are completely complementary, which is similar with the traditional 2-level converters. According to [6], the commutation of the current is achieved by the oscillation of the arm inductors and SM capacitors. However, the arm inductance and SM capacitance should be sufficient small to produce short current oscillations, and 5 μH arm inductance (may be the stray inductance of the converter) is adopted in [6]. But when dc short fault occurs near to the converter (transmission line parameter can be ignored), the quite small arm inductor will cause disastrous di/dt of the fault current even up to tens of kA/μs. This requires the converter to detect the fault and block IGBTs in 1 μs to avoid overcurrent, which is impractical for the control system and the available IGBTs now. Unlike the complementary 2-level modulation presented in [6], the shifted phase exists between the output voltages of the complementary chain-links in the proposed Buck-TL-MDCC, as discussed in Section II, so that the arm inductance can be designed to a reasonable value (e.g., several or tens of millihenrys), which can limit the rising velocity of the fault current. To sum up, the proposed stepped 2-level modulation provides more flexible design of the arm inductance, which is quite important in the interconnection of HVDC systems where all dc fault cases should be considered to ensure high reliability.

As for the blocking chain-link, if the rated voltage of the SM capacitors is V_C, the number of the inserted SM capacitors in chain-link 3, i.e., n_3, is always

$$n_3 = \frac{V_{dc1}}{2V_C}. \tag{24}$$

Practically, one SM should be added, so that the SM capacitors can be sorted and then rotated to achieve their voltage balance. Concretely, chain-link 3 bypasses the SM capacitor with the highest voltage when the current flowing through it (i_{Cb}) is negative, and bypasses the SM capacitor with the lowest voltage when i_{Cb} is positive. The sorting algorithm of the SM capacitor voltages in chain-link 3 is also executed twice every period, and at most two SMs need to switch IGBTs a period, which means the average switching frequency of the SMs in chain-link 3 is much lower than the fundamental frequency.

C. CLOSED-LOOP CONTROL

According to (17) and (18), when the phase-shifted duty ratio d_{s1} is larger than its steady-state value D_s, it is easy to get $W_{Cl1a} > 0$ and $W_{Cl1b} < 0$. That is to say chain-link $1a$ absorbs active power while chain-link $1b$ releases active power, which means the SM capacitor voltages in chain-link $1a$ will increase and that in chain-link $1b$ will decrease. Therefore, the average voltages of the SM capacitors in chain-links $1a$ and $1b$($\bar{v}_{C1a}$ and $\bar{v}_{C1b}$) can be balanced by modifying d_{s1}, as shown in Fig.9. In case that the fluctuation of the SM capacitor voltage affects the control loop, a low-pass filter is added to bypass the inherent fluctuations of $\bar{v}_{C1a}$ and $\bar{v}_{C1b}$. Likewise, the average voltages of the SM capacitors

in chain-links 2a and 2b can also be balanced by modifying d_{s2}. Note that if power is delivered from V_{dc2} to V_{dc1}, the phase-shifted control given in Fig. 9 is still applicable, however, d_{s1} and d_{s2} should be negative as discussed in Section II-C.

The feedback and feedforward controls of the Buck-TLC, which were presented in [31], can be directly applied to the Buck-TL-MDCC. If the Buck-TL-MDCC is interfacing a dc source and a passive load, the output voltage should be regulated. While if the Buck-TL-MDCC is interfacing two dc sources, the output current should be regulated. Suppose the Buck-TL-MDCC is interfacing two dc sources, and the complete control scheme of the Buck-TL-MDCC is shown in Fig. 9, where v_{Cl3} is the blocking chain-link voltage, $\bar{v}_{C1a}$, $\bar{v}_{C1b}$, $\bar{v}_{C2a}$ and $\bar{v}_{C2b}$ are the average voltages of the SM capacitors in chain-links 1a, 1b, 2a and 2b, respectively.

IV. DESIGN PRINCIPLES OF BUCK-TL-MDCC

A. DESIGN OF ARM INDUCTANCE

When a V_{dc1}-side dc fault occurs, smaller arm inductor will lead to faster rising velocity of the fault current. Therefore, the arm inductor in the Buck-TL-MDCC has a lower limit value to suppress the rising velocity of the fault current. Considering the worst case, i.e., chain-links 1a and 1b both work in the high-level state, we have

$$v_{La1} = -\left(v_{Cl1a} + v_{Cl1b} + \frac{V_{dc1}}{2}\right) = -\frac{3}{2}V_{dc1}. \quad (25)$$

The rising velocity of the fault current i_f can be expressed as

$$\alpha = \frac{di_f}{dt} = \frac{3V_{dc1}}{2L_a} \quad (26)$$

where α is the rising velocity of i_f.

If the upper limit of the rising velocity of i_f is α_0, it is required that

$$L_a \geq \frac{3V_{dc1}}{2\alpha_0}. \quad (27)$$

Note that the Buck-TL-MDCC can achieve bidirectional dc fault blocking capability if the full-bridge SMs are employed, as discussed in [19].

B. DESIGN OF SM CAPACITANCE

The choice of the SM capacitance depends on the fluctuation requirement of the SM capacitor voltage. Chain-link 1a is taken as an example to analyze the fluctuation of the SM capacitor voltage, the result can be extended to chain-links 1b, 2a and 2b. With reference to the waveforms of i_{1a} and v_{Cl1a} exhibited in Fig. 6(b), the waveform of the instantaneous power of chain-link 1a(p_{Cl1a}) can be depicted in Fig. 11. Assume the zero crossing point of p_{Cl1a} is t_0. It is easy to obtain the expression of t_0 as

$$t_0 = DT + \frac{2L_aI_{1\,\max}}{V_{dc1}}. \quad (28)$$

As seen from Fig. 11, p_{Cl1} is zero during [0, DT], positive during [DT, t_0], and negative during [t_0, T]. Thus, the energy

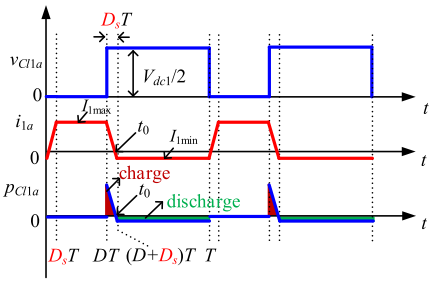

FIGURE 11. Charge and discharge of chain-link 1a.

fluctuation of chain-link 1 during a period, i.e., ΔW, is

$$\Delta W = \int_{DT}^{t_0} p_{Cl1}(t)\,dt = \frac{L_aI_{1\,\max}^2}{2}. \quad (29)$$

If the fluctuation coefficient of the SM capacitor voltage is ε_v, the energy fluctuation of chain-link 1 during a period can also be expressed as

$$\begin{aligned}\Delta W &= \frac{1}{2}nC_{sm}[(V_C + \varepsilon_v V_C)^2 - (V_C - \varepsilon_v V_C)^2] \\ &= 2nC_{sm}\varepsilon_v V_C^2. \end{aligned} \quad (30)$$

Combining (33) and (34), the relationship between C_{sm} and ε_v can be obtained as

$$C_{sm} = \frac{L_aI_{1\,\max}^2}{4\varepsilon_v nV_C^2} \quad (31)$$

where $I_{1\max}$ can be obtained in (14).

Note that the theoretical analysis are based on the 2-level modulation, the practical fluctuation of the SM capacitor voltage may slightly larger than the theoretical value for the stepped 2-level modulation. Eq. (35) indicates that the smaller arm inductance is, the smaller SM capacitance C_{sm} is. This is because the charge time of the chain-link is short and the discharge current of the chain-link is small when L_a is small, as shown in Fig. 11. Generally, the designed arm inductance is relatively small (e.g., several or tens of millihenrys), which can limit the rising velocity of the current and also achieve much smaller SM capacitance requirement with comparison to the sine-wave modulated MDCCs.

As for the blocking chain-link, the current flowing it when $D > 0.5$ and $D < 0.5$ can be respectively exhibited in Fig. 12. Ignoring the current transition period (D_sT), we can easily express the SM capacitance as

$$C_{sm} = \begin{cases} \dfrac{(I_{1\,\max} - I_{1\,\min})\,D}{2\varepsilon_v V_{Cf}} & D < 0.5 \\ \dfrac{(I_{1\,\max} - I_{1\,\min})\,(1-D)}{2\varepsilon_v V_{Cf}} & D > 0.5 \end{cases} \quad (32)$$

C. DESIGN OF FILTER INDUCTOR

According to the voltage waveform across the filter inductor, which can be obtained by (v_{AB}–V_{dc2}) as shown in Figs. 5(b) and 7(b), the filter inductance can

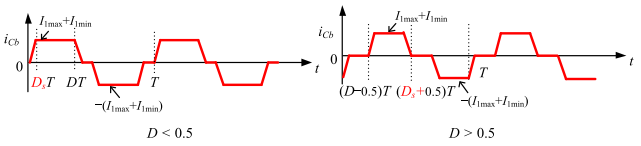

FIGURE 12. Current flowing through the blocking chain-link.

be expressed as

$$L_f = \begin{cases} \dfrac{(1-2D)\,DV_{dc1}}{2I_r f} & D < 0.5 \\ \dfrac{(2D-1)\,(1-D)\,V_{dc1}}{2I_r f} & D > 0.5 \end{cases} \tag{33}$$

where I_r is the current ripple of filter inductor current.

The filter inductance of the Buck-MDCC presented in [22] can be obtained as

$$L_f = \frac{(1-D)\,DV_{dc1}}{I_r f} \tag{34}$$

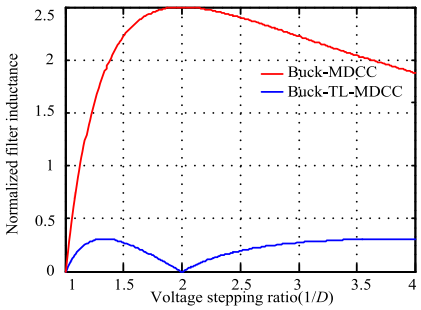

FIGURE 13. Normalized filter inductance.

If the power ratings and the current ripple requirements are the same, the normalized filter inductances of two MDCCs can be plotted in Fig. 13. Obviously, the Buck-TL-MDCC has much lower filter inductance requirement than the Buck-MDCC, especially when the voltage stepping ratio is near to 2. Referring to [14], in most cases of interconnecting HVDC systems, the voltage stepping ratio will fall within the low and medium voltage stepping ratio, thus, the weight and cost of the filter inductor in the Buck-TL-MDCC can be reduced.

V. BRIEF COMPARISON WITH OTHER DC/DC CONVERTERS

This section compares the proposed Buck-TL-MDCC with the MDCCs that also do not require large filter inductors, including the DC AUTO reported in [13], the MDCC with the active filter reported in [24] (abbreviated as A-MDCC), and the cross connected MDCC with the sine-wave modulation reported in [25] (abbreviated as C-MDCC). The circuit configurations of the DC AUTO, A-MDCC and C-MDCC are shown in Figs. 14(a), 14(b) and 14(c), respectively. As the ultra-high voltage blocking capacitor also exists in the C-MDCC, it is replaced by the active blocking chain-link just like the Buck-TL-MDCC.

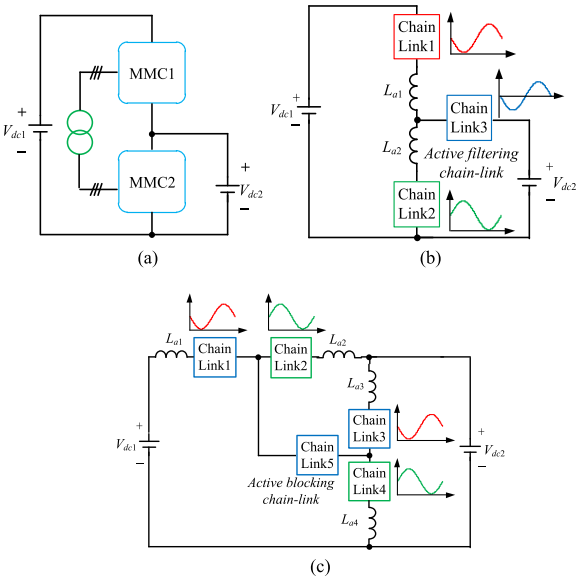

FIGURE 14. Prior arts of MDCCs (one-phase). (a) DC AUTO. (b) A-MDCC. (c) C-MDCC.

TABLE 1. Parameters of study case.

Rated power	P	450MW
Input voltage	V_{dc1}	320kV
Output voltage	V_{dc2}	150kV
Fundamental ac frequency	f	200Hz
SM capacitor voltage	V_C	10kV

A typical study case is given to compare the four converters, the voltage and power ratings are listed in Table 1. To fairly compare the four converters, all converters adopt three-phase configuration, and the fundamental ac frequencies are all 200Hz. The switches in the SMs employ 5SNA1000N330300 IGBT module manufactured by ABB corporation, and five IGBTs are connected in series for each switch to sustain 10kV SM capacitor voltage.

The power losses of the sine-wave modulated converters are calculated by the model presented in [33]. Generally, the switching frequencies of the sine-wave modulated converters are 2 $\sim$ 3 times the fundamental frequency to well balance the SM capacitor voltages [29], [34], and the switching frequencies of the DC AUTO, S-MDCC and C-MDCC are supposed to be twice the fundamental frequency, i.e., 400Hz. The efficiency of the ac transformer employed by the DC AUTO is supposed to be 99.4%. Coupled filter inductors with 0.5 mutual induction coefficient are employed by the Buck-TL-MDCC to increase the equivalent inductance and cancel the dc flux (coupled inductor can be installed in bipolar converter or unipolar converter with even phase legs [19]). Air-core inductor with current density of 2A/mm^2 is used for the inductor design, and the inductor losses are mainly composed by the winding conduction loss [15], [16]. The SM capacitance designs of the sine-wave modulated converters are referred to [21], and when the voltage stepping ratio is

TABLE 2. Comparisons of MDCCs.

Electrical parameters	DC AUTO	A-MDCC	C-MDCC	Buck-TL-MDCC
No. of HBSMs	192	186	234	240
No. of FBSMs	0	48	0	0
No. of IGBTs	1920	2820	2340	2400
SM capacitance (No.)	1.6mF(192) **Total**:307.2mF	1.6mF(186) 3.2mF(48) **Total**:451.2mF	1.6mF(186) 6mF(48) **Total**:585.6mF	0.2mF(192) 5mF(48) **Total**:278.4mF
SM capacitor voltage ripple	≈±2%	≈±2%	≈±2%	≈±2%
No. and inductances of arm inductors	20mH(12)	20mH(6)	20mH(12)	20mH(6)
Filter inductor	—	—	—	60mH(3)
Transformer	Required	—	—	—
Computation burden	Large	Large	Large	Medium
RMS value of ac circulating current	0.9kA	0.9kA	0.9kA	0.5kA
Switching frequency	≈400Hz	≈400Hz	≈400Hz	200Hz
Transformer loss	1.44MW	—	—	—
Inductor loss	0.12MW	0.08MW	0.12MW	0.15MW
Switching loss	1.42MW	2.28MW	1.42MW	0.48MW
Conduction loss	1.78MW	2.44MW	2.69MW	1.62MW
Efficiency	98.95%	98.93%	99.06%	99.50%

close to 2 (which is in accordance with the study case), the SM capacitance designs are similar with the MMC [35], i.e.,

$$C_{sm} = \frac{P}{2\pi f n V_C^2 g \varepsilon_v \cos\varphi} \sqrt{\left[1 - \left(\frac{g\cos\varphi}{2}\right)^2\right]^3} \quad (35)$$

where P is the transferred power per phase, g is the voltage ratio of ac voltage (ac component divides dc component), φ is the phase angle between ac voltage and ac current, and ε_v is the fluctuation coefficient of the SM capacitor voltage.

Assume $g = 0.9$ and $\cos\varphi = 0.95$, the SM capacitance can be obtained as 1.6mF, and the designed value will be larger than the theoretical value, due to the fact that non-ideal voltage balancing is achieved for the sorting and selection algorithm [34]. Finally, the results are listed in Table 2.

Thanks to the stepped 2-level modulation, the RMS value of the ac circulating current in the Buck-TL-MDCC is smaller with comparison to the C-MDCC, and extra switching actions are avoided so that the switching frequency is equal to the fundamental frequency, this poses smaller switching and conduction losses as seen from Table 2. The C-MDCC does not require filter inductors, but the Buck-TL-MDCC requires half the amount of the arm inductors in the C-MDCC, and the total SM capacitance requirement of the Buck-TL-MDCC is about half that of the C-MDCC. Note that the 60mH filter inductor employed by the Buck-TL-MDCC is a reasonable value in HVDC application [36], furthermore, it can limit the rising velocity of the fault current when V_{dc2}-side fault occurs, which functions like the dc limiting inductor in MMC [37]. According to the analysis in Section III-B, the sorting algorithm needs only to be executed twice a period for the stepped 2-level modulation, which poses reduced computation burden with comparison to the sine-wave modulation employed by the C-MDCC. In a word, the stepped 2-level modulation provides higher efficiency, smaller SM capacitance requirement and reduced computation burden with comparison to the sin-wave modulation.

A-MDCC needs 48 FBSMs to act as the active filter inductor (active filtering chain-link, i.e., chain-link 3 in Fig. 15(a)), C-MDCC and Buck-TL-MDCC both require 48 HBSMs to act as the active blocking chain-link, thus, A-MDCC requires more IGBTs than the C-MDCC and Buck-TL-MDCC. Moreover, the equal switching frequencies of the blocking chain-links are far smaller than the fundamental frequency (as discussed in Section III-B), while the IGBTs of the FBSMs in the filtering chain-link need to be switched every period to generate ac waveform, which leads to larger switching loss.

DC AUTO needs the least SMs, but ac transformer is required to connect the ac terminals of two MMCs. According to [13], the power flowing through the transformer is $P(1-V_{dc2}/V_{dc1})$, which means only partial rated power flowing through the transformer and MMC. But the power loss of the ac transformer with the reduced capability (1.44MW) is still larger than the power losses of the blocking chain-links in the C-MDCC and Buck-TL-MDCC (0.91 MW and 0.54 MW, respectively), moreover, the manufacture of the high voltage medium frequency transformer is difficult now [16], which may limit the medium operation of the DC AUTO.

To sum up, in this study case, the Buck-TL-MDCC provides at least 0.44% higher efficiency than the other three converters, and the computation burden is dramatically reduced because high frequency sorting is avoided. Efficiency may be the most important criterion to evaluate the performance of the dc/dc converter in HVDC grid for the large transferred power rated at hundreds or even thousands of megawatts, and 0.44% is a huge promotion of the efficiency, which means the Buck-TL-MDCC may be the promising topology to interconnect HVDC systems.

The efficiencies of these four converters under different voltage stepping ratios are also evaluated in Fig. 15. It is

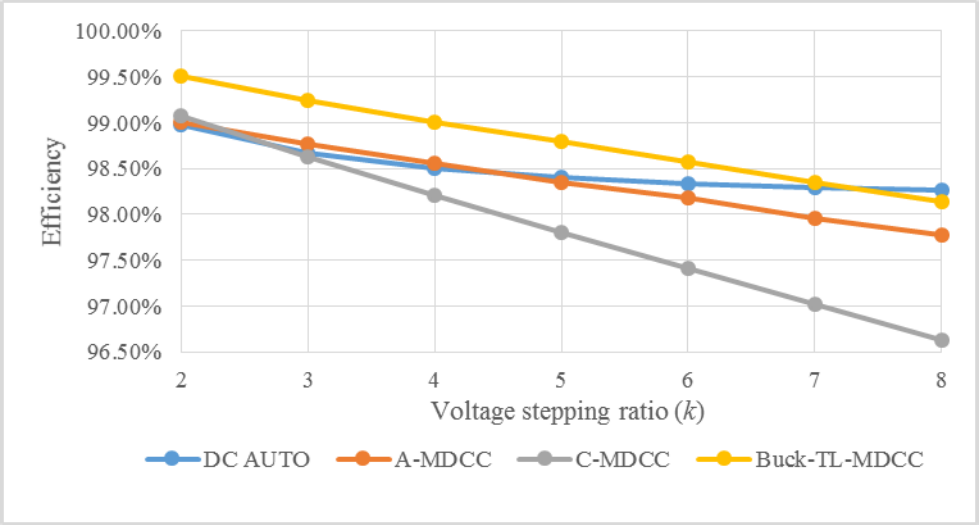

FIGURE 15. Efficiencies under different voltage stepping ratio.

assumed that V_{dc1} keeps 320kV, V_{dc2} is 320kV/k, and the transferred power is 450MW/k, where k is the voltage stepping ratio. It can be observed that as k increases, the efficiencies of the A-MDCC, C-MDCC and Buck-TL-MDCC decrease much faster than that of the DC AUTO. This is because the inner ac voltages of the transformer-less converters are limited by the lower chain-links (e.g., chain-link 2 in the A-MDCC), which leads to large ac circulating current with comparison to the input dc current [20]. The efficiency of the Buck-TL-MDCC decreases slower than that of the C-MDCC because its ac circulating current increases slower as shown in Fig. 16, so that the voltage ratio range of the Buck-TL-MDCC is wider.

As seen from Fig. 15, the Buck-TL-MDCC can only cope with the low or medium voltage stepping ratio application (e.g., $k < 5$), and the best application scenario is around 2:1 for the dramatically reduced filter inductance according to Fig. 13. As for the converters employing ac transformers, including the DC AUTO and isolated converters [6], [10], will be the better choices in high voltage stepping ratio application. According to [14], typical dc voltage ratings of HVDC system are 800kV, 640kV, 500kV, 320kV, 150kV, so that in most cases of interconnecting HVDC systems, the voltage stepping ratio will fall within the low or medium voltage stepping ratio. This means the Buck-TL-MDCC can cope with most cases of interconnecting HVDC systems, but for other applications like interconnecting the wind farm and HVDC transmission line where the voltage stepping ratio exceeds 10, the DC AUTO and isolated converters are the better choices.

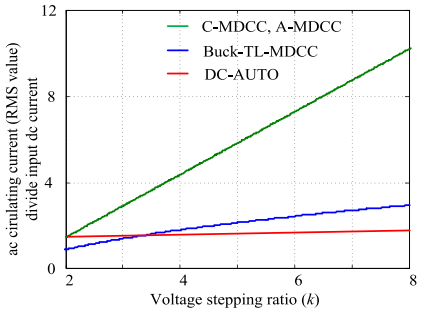

FIGURE 16. Ac circulating current divide input current.

VI. SIMULATION RESULTS

The proposed Buck-TL-MDCC is simulated in Matlab/Simulink to verify its effectiveness. The Buck-TL-MDCC is suitable for HVDC applications, typically rated for hundreds of kilovolts and hundreds of megawatts. Due to too large amount of SMs will dramatically increase the computation complexity, the rated voltage of SM capacitor is set 10kV to make the simulation practical.

A. STEADY-STATE PERFORMANCE

The simulation parameters of the Buck-TL-MDCC are listed in Table 3, chain-links 1a, 1b, 2a and 2b all employ 16 SMs. Fig. 17 shows the steady-state waveforms at rated power, where $v_{C1a(j)}$, $v_{C1b(j)}$, $v_{C2a(j)}$ and $v_{C2b(j)}$ are the capacitor

TABLE 3. Parameters of three-phase Buck-TL-MDCC.

Rated power	P	450MW
Input voltage	V_{dc1}	320kV
Output voltage	V_{dc2}	150kV
Switching frequency	f	200Hz
Arm inductors	L_{a1}, L_{a2}	20mH
Filter inductor	L_f	60mH
SM capacitance in chain-links 1a-2b	C	200μF
SM capacitor voltage	V_C	10kV
Stepped time during voltage transition period	T_d	2.5μs

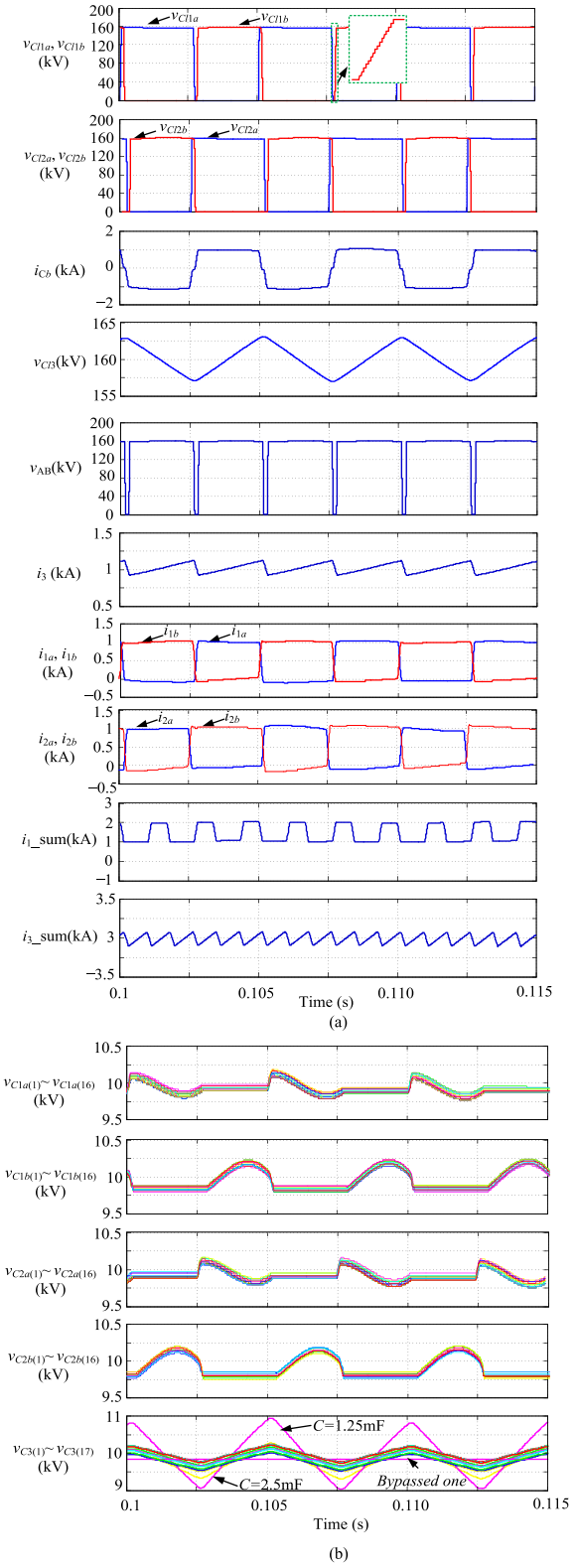

FIGURE 17. Steady-state waveforms of Buck-TL-MDCC with $L_f = 100$ mH. (a) Basic waveforms. (b) SM capacitor voltages.

voltages of the SMs numbered j ($1 \sim 16$) in chain-links $1a$, $1b$, $2a$ and $2b$, respectively. The symbols of the operation parameters are labeled in Fig. 4.

The enlarged waveform of the voltage rising transition period of v_{Cl1b} is given in the dotted box, from which we can see that the output voltages of four chain-links are all stepped 2-level waves. During the voltage transition period, the chain-links insert or bypass a SM every 2.5μs, so that the dv/dt stress of the converter can be alleviated. Similar with the operation of the Buck-TLC, v_{Cl2a} and v_{Cl2b} respectively lag v_{Cl1a} and v_{Cl1b} 180°, so that a new level, i.e., $V_{dc1}/2$, can be obtained and the equivalent switching frequency is doubled. Though the relatively small output filter inductance (60mH) is adopted, the output current ripple is only 100A, which validates the discussion in Section V.

As seen from Fig. 17(b), the SM capacitor voltages in chain-links $1a$-$2b$ are well balanced and the ripples are about $\pm$ 2 % though the small SM capacitance (0.2mF) is adopted. Obviously, the SM capacitance requirement is dramatically reduced with comparison to the sine-wave modulated MDCCs. This validates the analysis in Section V.

As for the blocking chain-link, i.e., chain-link 3, 16 SMs are employed to output dc voltage, and one SM is added to achieve their voltage balance. The rated voltage of the SMs in chain-link 3 is also 10kV, and the SM capacitance in chain-link 3 is 5 mF. While to validate the voltage balance algorithm, two of the SM capacitors are respectively set 2.5 mF and 1.25 mF, otherwise, the switching actions of the SMs are not required. Chain-link 3 bypasses the SM capacitor with the highest voltage when the current flowing through it (i_{Cb}) is negative, and bypasses the SM capacitor with the lowest voltage when i_{Cb} is positive. As shown in Fig. 18, the switching action does not occur every period, this is because the bypassed SM capacitor is always the same one. Thus, the equal switching frequency of the SMs in chain-link 3 is much lower than the fundamental frequency.

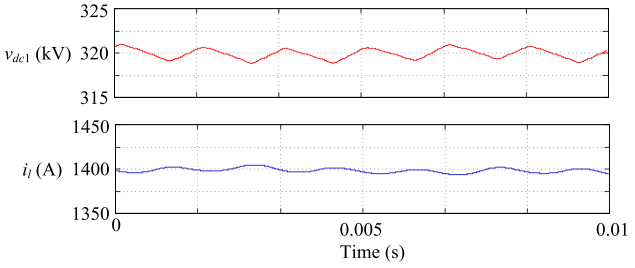

FIGURE 18. DC voltage and current waveforms of Buck-TL-MDCC connected to overhead line.

The total input and output currents of the three-phase Buck-TL-MDCC are given in Fig. 17(a). Obviously, the fluctuation frequency of the total current is tripled. Nevertheless, relatively large current ripple still exists in $i_{1_{\rm sum}}$. According to the simulation results in [5], the distributed capacitance and inductance of 100-km dc cable may be enough to bypass such current ripple to acceptable limit. While if the MDCC is connected to low-capacitance dc line (e.g., overhead HVDC lines), discrete dc-link filter is needed. The simulation results of the converter connected to 500-km overhead HVDC line ($L_{dc} = 4.1$mH/km, $R_{dc} = 22$mΩ/km, $C_{dc} = 9$nF/km) and

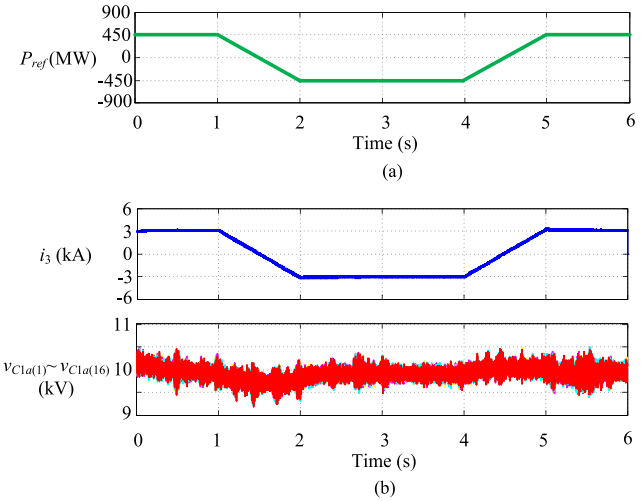

FIGURE 19. Dynamic-state waveforms of Buck-TL-MDCC under power changing condition. (a) Power reference. (b) Output current and SM capacitor voltages of Buck-TL-MDCC.

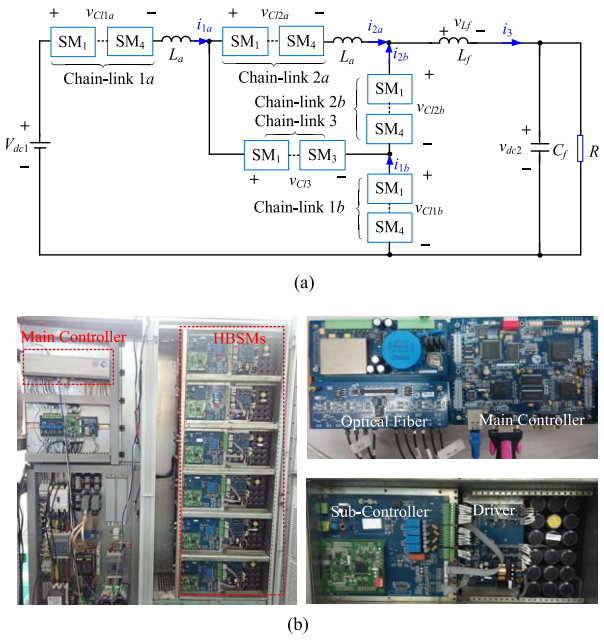

FIGURE 20. Circuit configuration and photograph of the prototype. (a) Circuit configuration of the prototype. (b) Photograph of the prototype.

100μF discrete dc capacitor are given in Fig. 18, where i_l is the terminal current of the transmission line and v_{dc1} is the high-voltage side terminal voltage of the converter. It can be seen that the dc current ripple can be damped to low value along the transmission line, and the terminal voltage ripple of the converter is also within acceptable value.

B. PERFORMANCE UNDER POWER CHANGE

Fig. 19 shows the dynamic responses of the Buck-TL-MDCC under the power changing condition. The dc power reference P_{ref} remains 450MW during 0-1s, reversed linearly to −450MW during 1s-2s, and then reversed again to 450MW during 4s-5s, as shown in Fig. 19 (a).

As seen from Figs. 19(b), the transferred power of the Buck-TL-MDCC follows its order. The waveforms of the SM

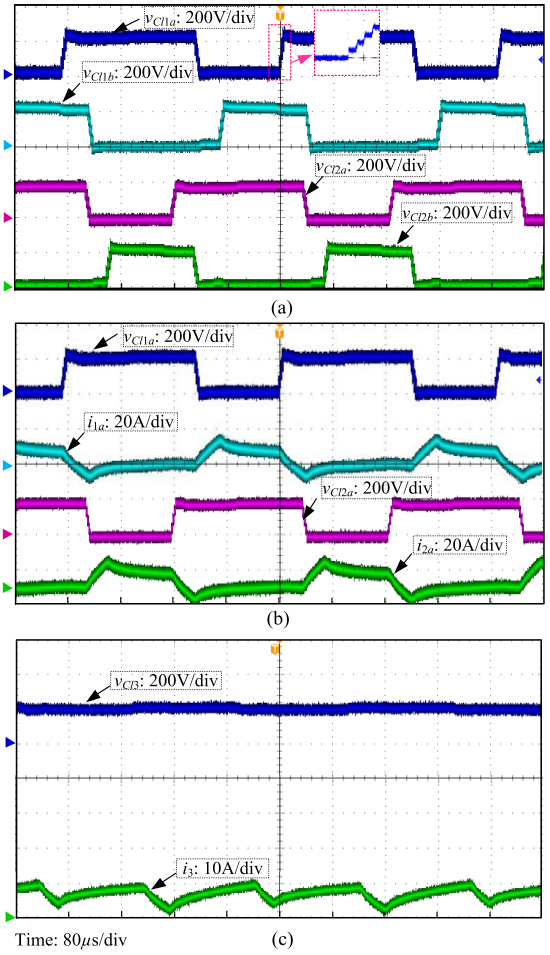

FIGURE 21. Steady-state waveforms of Buck-TL-MDCC.

capacitor voltages show that they are well balanced at steady and dynamic states, which proves the effectiveness of the voltage balancing strategy.

VII. EXPERIMENTAL RESULTS

A laboratory prototype of the Buck-TL-MDCC has been built as shown in Fig. 20. Chain-links 1a, 1b, 2a and 2b all contain four HBSMs, chain-link 3 contains three HBSMs and two HBSMs are inserted to provide the constant voltage. Main parameters are listed in Table 4. The circuit configuration of the prototype is shown in Fig. 20(a), as a passive load is adopted, a filter capacitor C_f is paralleled at lower voltage side, and the voltage feedback control is employed.

A. STEADY-STATE PERFORMANCE

The steady-state waveforms of the Buck-TL-MDCC are given in Fig. 21, from which it can be observed that chain-links 1a, 1b, 2a and 2b output stepped 2-level waveforms. During the voltage transition period, the chain-link inserts or bypasses a SM every 2μs. As seen from Fig. 21(a), v_{Cl2a} and v_{Cl2b} respectively lag v_{Cl1a} and v_{Cl1b} 180°, so that v_{AB} can obtain an additional voltage level $V_{dc1}/2$ (200V), and the equivalent switching frequency

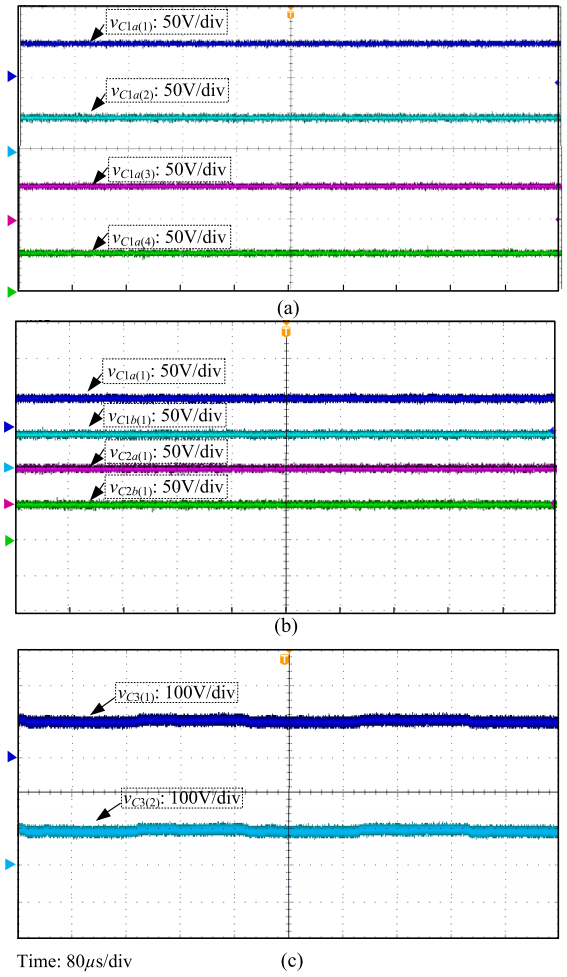

FIGURE 22. SM capacitor voltages.

TABLE 4. Parameters of Buck-TL-MDCC.

Input voltage	V_{dc1}	400V
Output voltage	V_{dc2}	160V
Passive load	R	25Ω
Switching frequency	f	3kHz
Arm inductors	L_{a1},L_{a2}	0.5mH
Filter inductor	L_f	1mH
Filter capacitor	C_f	3.3mF
SM capacitance	C	2mF
SM capacitor voltage	V_C	50V
Stepped time during voltage transition period	T_d	2μs

is twice the fundamental frequency (6 kHz), as shown in Fig. 21(c). Figs. 22(a) and 22(b) respectively show the four SM capacitor voltages in chain-link 1a and the capacitor voltages of the first SM in chain-links 1a-2b. Fig. 22(c) shows the capacitor voltages of two inserted SMs in the blocking chain-link. It can be observed that the SM capacitor voltages are well balanced, which validates the voltage balancing control discussed in Section III.

The efficiency of the experiment at rated power is about 90.2%. As four SMs are employed per chain-link to

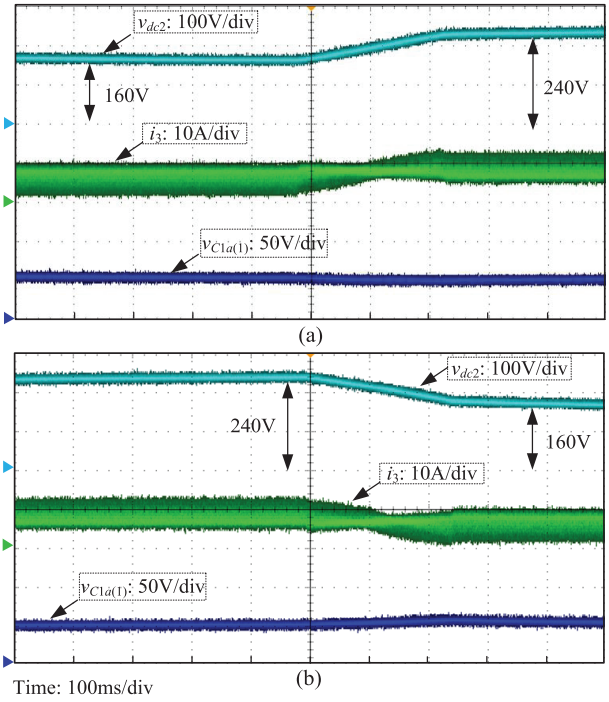

FIGURE 23. Dynamic-state waveforms of Buck-TL-MDCC.

verify the voltage balancing control, and maximum input voltage is only 400 V (restricted by the dc sources in the lab), the SM capacitor voltage is much smaller than the rated voltage of the IGBT module we used, which results in large conduction loss. Furthermore, the switching frequency is selected as 3 kHz to facilitate the design of inductors. Therefore, the efficiency of the experiment is much lower than the calculated value in Section V. If the input voltage is increased and the switching frequency is lowered, the efficiency will be improved.

B. DYNAMIC-STATE PERFORMANCE

To test the dynamic performance of the Buck-TL-MDCC, two transient cases are considered. As seen from Fig. 23(a), initially, the output voltage v_{dc2} is set 160V, then its reference is increased from 160V to 240V. As the passive load is not changed, the average value of the output current i_3 is increased from 6.4 A to 9.6 A simultaneously. During the transient state, the output voltage follows its order and the SM capacitor voltages remain almost unchanged. Similarly, when the output voltage reference is decreased from 240 V to 160 V, the output voltage follows its order and the SM capacitor voltages keep balanced, as shown in Fig. 23(b).

VIII. CONCLUSION

A novel Buck-TL-MDCC is derived from the classic Buck-TLC by replacing the switches and blocking capacitor with cascaded SMs for HVDC application. Compared with the prior arts of MDCCs, the Buck-TL-MDCC reduces the SM capacitance requirement, and provides higher efficiency, due to the smaller ac circulating current and lower

switching frequency. Moreover, the computation burden can be dramatically reduced because the high-frequency sorting of the SM capacitor voltages can be avoided. The simulation and experimental results validate the performance of the Buck-TL-MDCC.

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HONGCHENG YOU received the B.Eng. and M.Sc. degrees in hydropower engineering and electrical engineering from the Huazhong University of Science and Technology. He is currently pursuing the Ph.D. degree in electrical engineering with Shanghai Jiao Tong University.

His current research interests include modular multilevel converter and high voltage dc/dc converter.

XU CAI received the B.Eng. degree in electrical engineering from Southeast University, Nanjing, China, in 1983, and the M.Sc. and Ph.D. degrees from the China University of Mining and Technology, Beijing, China, in 1988 and 2000, respectively.

He was with the Department of Electrical Engineering, China University of Mining and Technology, as an Associate Professor, from 1989 to 2001. He joined Shanghai Jiao Tong University, as a Professor, in 2002, where he has been the Director of the Wind Power Research Center, since 2008. His special fields of interest lie in power electronics and renewable energy exploitation and utilization.