

Received February 2, 2018, accepted March 18, 2018, date of publication April 12, 2018, date of current version May 2, 2018.

Digital Object Identifier 10.1109/ACCESS.2018.2818323

High Frequency Buffer-Feedback Oscillator With an RF Negative-Resistance Circuit

KANG-UN CHOI¹, THANH DAT NGUYEN¹, SEONG-GON CHOI², AND JONG-PHIL HONG¹

¹School of Electrical Engineering, Chungbuk National University, Cheongju 28644, South Korea

²School of Information and Communication Engineering, Chungbuk National University, Cheongju 28644, South Korea

Corresponding author: Jong-Phil Hong (jphong@cbnu.ac.kr)

This work was supported in part by the Basic Science Research Program through the National Research Foundation of Korea funded by the Ministry of Education under Grant NRF-2015R1D1A1A01057788 and in part by the Human Resources Program in Energy Technology of the Korea Institute of Energy Technology Evaluation and Planning through financial resource from the Ministry of Trade, Industry & Energy, Republic of Korea, under Grant 20164030201330.

ABSTRACT This paper presents a millimeter-wave oscillator using frequency-boosting techniques to increase the oscillation frequency. In the proposed oscillator, a buffer-feedback oscillator and an RF negative-resistance circuit reduce the parasitic load capacitance and effective inductance, respectively. As a result, the proposed topology operates at a higher oscillation frequency than the conventional oscillators. The proposed oscillator is fabricated in a 65-nm CMOS process. The measured oscillation frequency is 82.4 GHz, and the output power is -3.9 dBm. The power consumption is 10.9 mW at a supply voltage of 1.8 V, excluding output buffers.

INDEX TERMS CMOS, buffer-feedback, RF negative resistance tank, millimeter-wave (mm-wave), oscillator.

I. INTRODUCTION

In recent years, the millimeter-wave (mm-wave) frequency band has attracted attention for wireless communication because large available bandwidth at mm-wave band can lead to higher speed for communication [1]–[3]. The oscillator is one of the key elements involved in implementing a communication system. Among several device technologies, the CMOS process is a good candidate in mm-wave applications because of its low cost and high integration capability [4]–[6]. The maximum oscillation frequency (f_{\max}) of the 65-nm CMOS process is 300GHz, which is a rough estimate and can vary from transistor to transistor and layout to layout [7]–[9]. However, the practical operating frequency of the oscillator is significantly decreased by parasitic capacitances, which are generated by the inductor and buffer transistor [8], [10]. In addition, the transconductance of the transistor decreases with increasing frequency. As a result, the transconductance is insufficient to compensate for the loss and begin the oscillation at the high frequency.

The push-push oscillator [11]–[19] method is a common approach to generating high-frequency signals using the second harmonic frequency. However, it has only a single-ended output and a low output power. For differential output, the push-push oscillator requires a balun to transform

the single-ended signal to a differential signal, which generally decreases the output power and occupies a large area. Instead of increasing the operating frequency using harmonics, the admittance-transforming technique in [20] enhances the fundamental oscillation frequency of a conventional cross-coupled oscillator (XCO), but the transmission lines that transform the admittance occupy a large chip area.

In this paper, a buffer-feedback oscillator (BFO) combined with an RF negative-resistance (RFNR) circuit is proposed. Using both RFNR and BFO structures in the design, the proposed oscillator effectively reduces the effective inductance of the LC-tank and the parasitic capacitance of the buffer transistor, which are inversely proportional to determining the oscillation frequency. As a result, the proposed structure increases the oscillation frequency. Furthermore, the RFNR circuit adds negative transconductance to the oscillator, which improves the startup condition for oscillation.

Compared to the conventional XCO and BFO topologies, the proposed structure achieves a higher oscillation frequency and better start-up condition with differential output and still has a small chip area. In Section II, the oscillation frequency and start-up conditions of the proposed oscillator are analyzed and verified using simulation. The measurement results

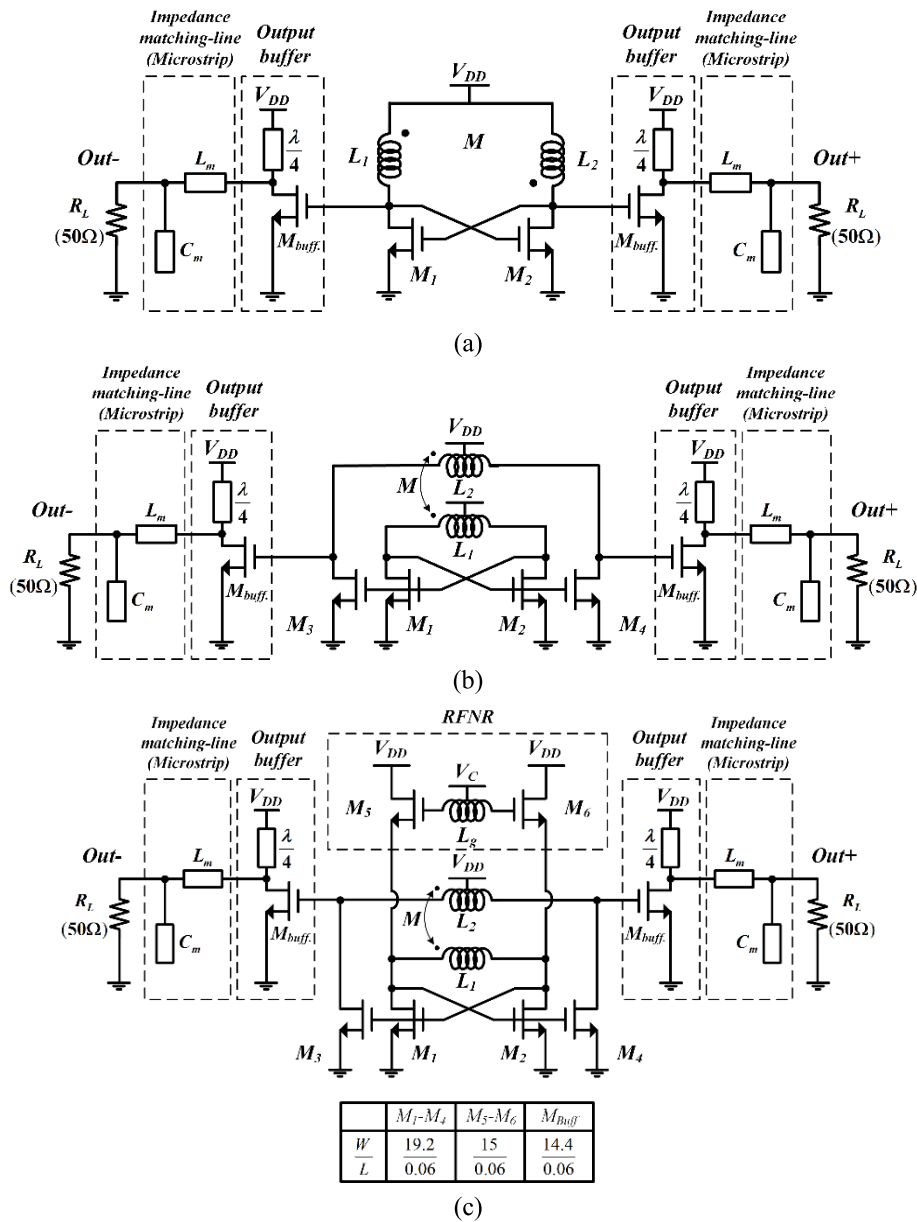


FIGURE 1. Schematic of (a) conventional cross-coupled oscillator, (b) buffer-feedback oscillator, and (c) proposed oscillator.

are presented in Section III. Finally, Section IV summarizes and concludes this paper.

II. PROPOSED OSCILLATOR TOPOLOGY

Figure 1 (a) shows the conventional cross-coupled oscillator topology, which consists of the transistor pairs (M_1-M_2), inductors (L_1 and L_2), and buffer transistors (M_{buff}) directly connecting to the oscillator tank. Therefore, the oscillation frequency decreases because the parasitic capacitance, C_{GS} , of buffer stage directly adds to the oscillator tank. Figure 1 (b) shows the BFO topology, which consists of the transistor pairs (M_1-M_4) and transformer (L_1 and L_2). The BFO reduces the parasitic capacitances of the buffer transistors

(M_{buff}) and inductor (L_1) by one quarter and one half, respectively, compared to those of the conventional XCO [8]. Figure 1 (c) shows the proposed BFO with the RFNR circuit. The differential RFNR circuit, which consists of two transistors (M_5-M_6) and a center tapped inductor (L_3), is connected in parallel with the LC-tank of the BFO. With the proper selection of the transistor width, the impedance of the RFNR circuit becomes the inductive reactance, which decreases the overall effective inductance of the LC-tank through its parallel connection with the BFO. As a result, the oscillation frequency of the proposed oscillator can be further increased in comparison to the conventional BFO. In addition, the negative conductance

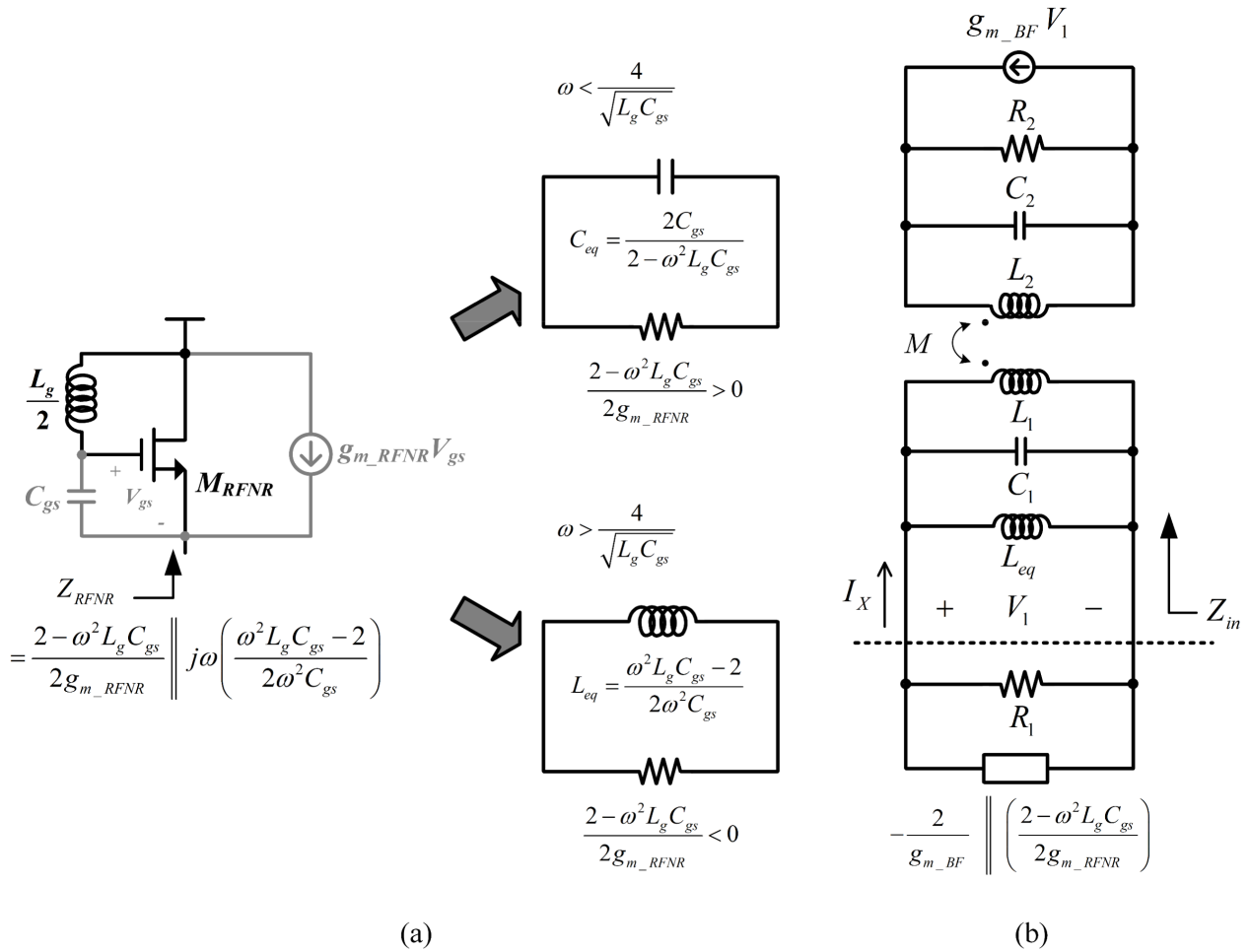


FIGURE 2. Equivalent circuit of (a) RFNR and (b) proposed oscillator.

of the RFNR circuit improves the start-up conditions of the BFO.

Figure 2 (a) shows the equivalent half circuit of the RFNR shown in Fig. 1 (c), where C_{gs} and g_{m_RFNR} are the gate-source parasitic capacitance and the transconductance of the transistor (M_5 or M_6), respectively. The impedance Z_{RFNR} looking into the source of the RFNR in Fig. 2 (a) becomes an inductive reactance (L_{eq}) with negative resistance or a capacitive reactance (C_{eq}) with positive resistance depending on the values of L_g and C_{gs} . To improve the oscillation frequency and start-up condition, in the proposed topology, the RFNR circuit is designed to become an inductive reactance with negative resistance and connected in parallel with the BFO

$$-\frac{2}{g_{m_BF}} \parallel \left(\frac{2 - \omega^2 L_g C_{gs}}{2 g_{m_RFNR}} \right) = R_1. \quad (1)$$

Figure 2 (b) shows the equivalent circuit of the proposed oscillator in Fig. 1 (b), where R_1 and C_1 are the resistance and parasitic capacitance of the primary LC-tank, R_2 and C_2 are those of the secondary LC-tank, and g_{m_BF} is the transconductance of the buffer-feedback transistors (M_1 - M_4).

From Fig. 2 (b), the start-up condition for the primary tank is Compared with the conventional buffer-feedback oscillator ($-2/g_{m_BF}$) [8], the start-up condition for the primary tank is improved by adding the negative resistance to the RFNR circuit in the proposed oscillator. Furthermore, from equation (1), the increase in the parallel resistance of the proposed topology (R_1) leads to a higher oscillation amplitude at the same power dissipation. Therefore, the phase noise of proposed oscillator can be lower than that of the conventional oscillator.

Assuming that the transformer impedances of the primary and secondary windings are identical ($L_1 = L_2 = L$, $C_1 = C_2 = C$), the tank impedance (Z_{in}) is given by equation (2), as shown at the bottom of the next page. By solving equation (2), the two resonant frequencies can be derived as equation (3), as shown at the bottom of the next page, and the minimum g_{m_BF} required for the second tank to resonate is, Figure 3 (a) shows the simulation results of equation (4), shown at the bottom of the next page, as a function of L_{eq} , where $L = 100$ pH, $M = 60$ pH, $C = 35$ fF, and $R_2 = 500 \Omega$. As shown in Fig. 3 (a), the proposed topology only oscillates at the lower resonant frequency (ω_1) because the minus value of g_{m_BF}

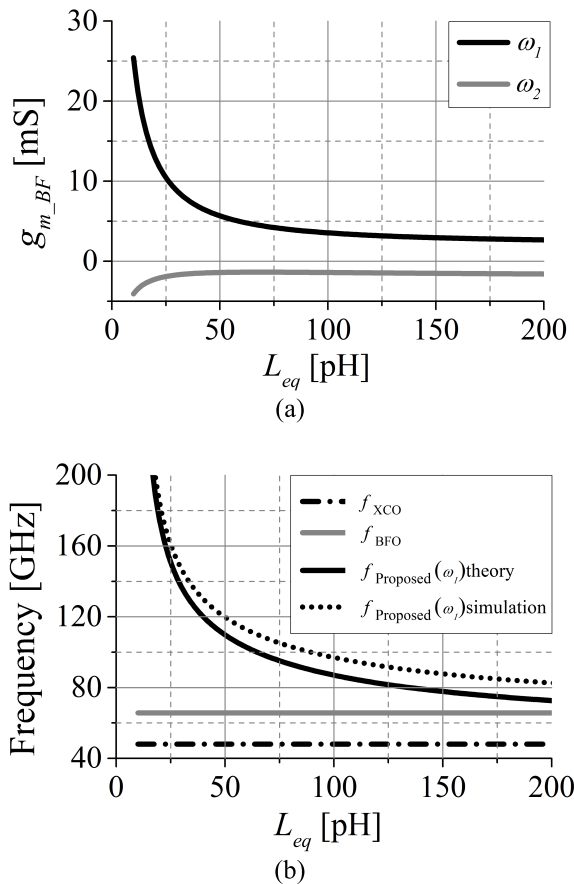


FIGURE 3. (a) Magnitude of the required g_{m_BF} at resonant frequencies and (b) oscillation frequency of three oscillators as a function of L_{eq} .

at the higher resonant frequency (ω_2) is infeasible to realize. Figure 3 (b) shows the calculated oscillation frequency of the proposed topology at ω_1 of equation (3) in comparison with those of the conventional XCO and BFO oscillators using the equations in [8]. With the decrease in L_{eq} , the proposed topology at ω_1 achieves a much higher oscillation frequency than the calculated oscillation frequencies of the XCO and BFO.

Figure 4 shows the tank impedance of the three oscillators in the simulated circuit to verify the analysis. In Fig. 1,

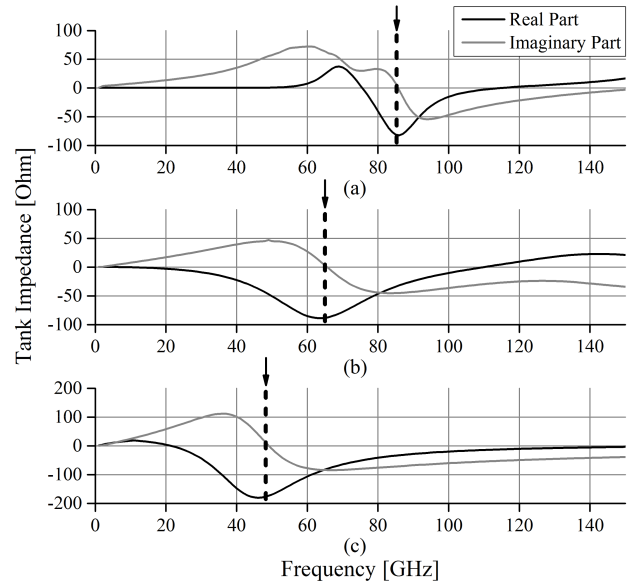


FIGURE 4. Simulated tank impedance of the (a) proposed oscillator, (b) BFO and (c) XCO.

the proposed oscillator uses the standard transformer in the process and has the smallest inductance value. The three oscillators have identical values of L_1 (=100 pH), L_2 (=100 pH), M (=60 pH) and transistor sizes. To generate a practical value of g_{m_BF} , as shown in Fig. 3 (a), the inductance, L_g , of the RFNR circuit is selected to be 400 pH to obtain 100 pH of L_{eq} . From the circuit simulation results in Fig. 4, the oscillation frequency of the proposed oscillator is 86 GHz, which is 79.2% and 26.5% higher than those of the conventional XCO (48 GHz) and BFO (68 GHz), respectively.

III. MEASUREMENT RESULTS

The proposed oscillator is fabricated in a 65-nm CMOS process. Figure 5 shows the die photograph with a size of $0.27 \times 0.7 \text{ mm}^2$ including the pads. This chip is measured via on-wafer probing with a signal analyzer R&S@FSW85. Figure 6 shows the frequency spectrum measurement setup. The output signal is probed using GGB model 110H probes. Then, the signal is transferred to the signal analyzer using

$$Z_{in}(s) \frac{V_1}{I_X} = \frac{(L^2 - M^2) Cs^3 + \frac{1}{R_2} (L^2 - M^2) s^2 + Ls}{(L^2 - M^2) C^2 s^4 + (L^2 - M^2) \frac{C}{R_2} s^3 + \left(2L + \frac{(L^2 - M^2)}{L_{eq}}\right) Cs^2 + \left(\frac{L(L + L_{eq}) - M^2}{R_2 L_{eq}} - g_{m_BF} M\right) s + \left(1 + \frac{L}{L_{eq}}\right)} \quad (2)$$

$$\omega_{1,2} = \sqrt{\frac{2LL_{eq} + (L^2 - M^2) \mp \sqrt{L^2(L^2 - 2M^2) + M^2(4L_{eq}^2 + M^2)}}{2L_{eq}(L^2 - M^2)C}} \quad (3)$$

$$g_{m_BF} = \frac{1}{2R_2 L_{eq} M} \cdot \left((L^2 - M^2) \pm \sqrt{L^2(L^2 - M^2) + M^2(4L_{eq}^2 + M^2)} \right) \quad (4)$$

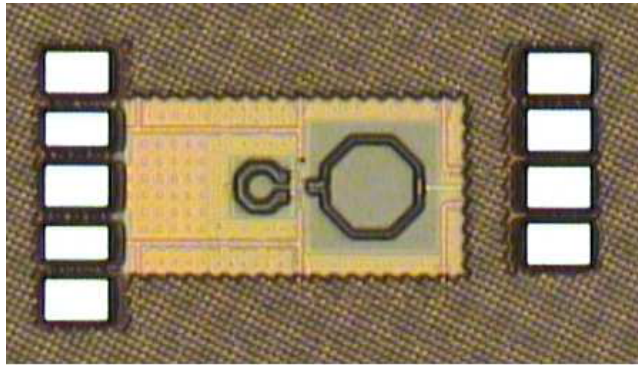


FIGURE 5. Die photograph of the proposed oscillator.

TABLE 1. Performance comparison of mm-Wave oscillators.

Ref.	[20]	[21]	[22]	[23]	This work
Technology	0.18μm CMOS	0.18μm CMOS	65nm CMOS	65nm CMOS	65nm CMOS
Supply (V)	1.8	2.5	1.2	1.2	1.8
Freq. (GHz)	62.9	69	105	73.8	82.4
Phase Noise (dBc/Hz)	-89 @1MHz	-76 @1MHz	-100 @10MHz	-112 @10MHz	-112 @10MHz
P _{out} (dBm)	-15	-18.5	4.5	-10	-3.9
P _{DC} (mW)	74	27.5	54	8.4	10.9
FOM (dBc/Hz)	-166 @1MHz	-158 @1MHz	-163.1 @10MHz	-180 @10MHz	-180 @10MHz
DC-to-RF Efficiency* (%)	N/A	0.05	5.2	0.12	3.74
Tuning range (%)	1.06	4.5	9.5	32.6	3.9
Core area (mm ²) (with pad)	0.6716	0.207	0.228	-	0.189
Core area (mm ²) (without pad)	-	0.134	-	0.03	0.046

$$* P_{eff} = \frac{P_{out}}{P_{DC}} \times 100\%$$

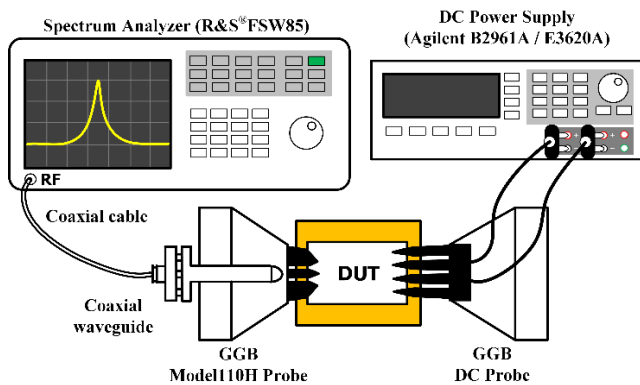


FIGURE 6. Spectrum measurement setup.



FIGURE 8. Measured phase noise at 82.4 GHz from a 1.8 V supply.

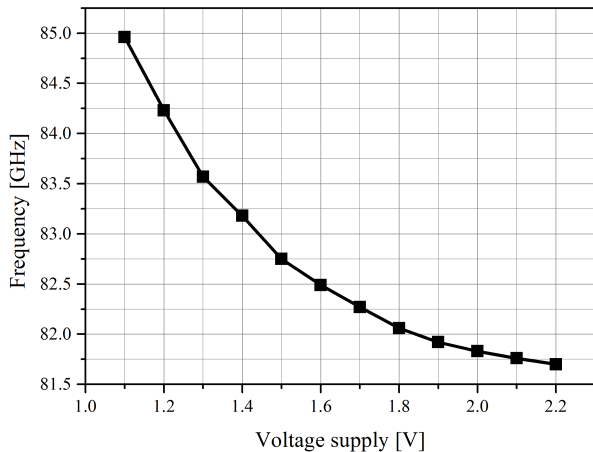


FIGURE 7. Measured tuning range with increase in supply voltage.

1-mm coaxial cables. In this measurement, two 1-mm coaxial cables were used due to the long distance between the probes and the signal analyzer. Figure 7 shows that the measured oscillation frequency varies from 81.7 GHz to 84.96 GHz over the supply voltage of 1.1-2.2 V. In Fig. 8, the measured phase noise at 82.4 GHz center frequency shows -112 dBc/Hz at 10 MHz offset frequency. Figure 9 shows the measured output spectrum of the proposed oscillator

at 82.4 GHz. The measurement shows an uncalibrated output power of -6.8 dBm. The extracted losses of the probe tip and coaxial-waveguide adapter with cables are 2.1 dB and 0.8 dB, respectively, so the calibrated output power is -3.9 dBm. The implemented oscillator consumes 6.05 mA from the 1.8 V supply excluding the output buffers. Table I shows the performance summary and comparison with other mm-wave oscillators.

The applied figure of merit FOM, in this comparison table is:

$$FOM = L\{\Delta\omega\} - 20 \log \left(\frac{\omega_0}{\Delta\omega} \right) + 10 \log \left(\frac{P_{DC}}{1mW} \right) \quad (5)$$

where $L\{\Delta\omega\}$ is phase noise at $\Delta\omega$ offset, ω_0 is the center frequency, and PDC is DC power consumption. The proposed oscillator in this work shows highest FOM. The proposed oscillator also shows good output power, DC-to-RF efficiency, and phase noise compared with the previous state-of-the-art oscillators with an oscillation frequency of approximately 80 GHz.

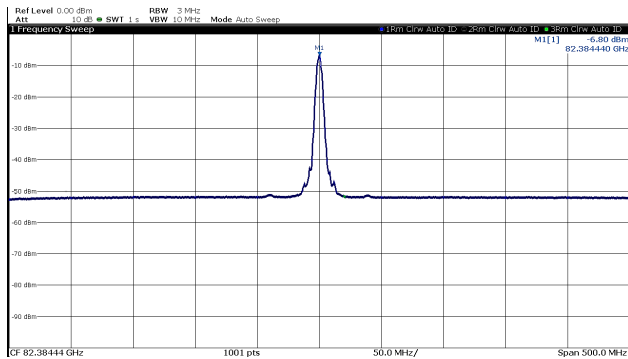


FIGURE 9. Spectrum of the proposed oscillator before calibrating the probe and adapter losses of 2.9 dB.

IV. CONCLUSION

In this paper, a mm-wave oscillator is proposed to increase the fundamental oscillation frequency. By combining the BFO with the RFNR circuit, the proposed structure reduces the effective value of the inductance into the LC-tank and parasitic capacitance. The tendency and accuracy of the proposed equations and analysis are verified using circuit simulations. The simulation results show that the proposed oscillator significantly increases the oscillation frequency compared to the conventional XCO and BFO. The measured calibrated output power is -3.9 dBm at an oscillation frequency of 82.4 GHz, while consuming a current of 6.05mA from a 1.8 V supply excluding output buffers.

REFERENCES

- [1] Z. Wang, P.-Y. Chiang, P. Nazari, C.-C. Wang, Z. Chen, and P. Heydari, "A CMOS 210-GHz fundamental transceiver with OOK modulation," *IEEE J. Solid-State Circuits*, vol. 49, no. 3, pp. 564–580, Mar. 2014.
- [2] J.-D. Park, S. Kang, and A. M. Niknejad, "A 0.38 THz fully integrated transceiver utilizing a quadrature push-push harmonic circuitry in SiGe BiCMOS," *IEEE J. Solid-State Circuits*, vol. 47, no. 10, pp. 2344–2354, Oct. 2012.
- [3] K. B. Cooper *et al.*, "A high-resolution imaging radar at 580 GHz," *IEEE Microw. Wireless Compon. Lett.*, vol. 18, no. 1, pp. 64–66, Jan. 2008.
- [4] H. Koo, C.-Y. Kim, and S. Hong, "Design and analysis of 239 GHz CMOS push-push transformer-based VCO with high efficiency and wide tuning range," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 62, no. 7, pp. 1883–1893, Jul. 2015.
- [5] Z. Ahmad, M. Lee, and K. K. O., "1.4 THz, -13 dBm-EIRP frequency multiplier chain using symmetric- and asymmetric-CV varactors in 65 nm CMOS," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2016, pp. 350–351.
- [6] N. Sharma, W. Choi, and K. K. O., "160–310 GHz frequency doubler in 65-nm CMOS with 3-dBm peak output power for rotational spectroscopy," in *Proc. IEEE Radio Freq. Integr. Circuits Symp. (RFIC)*, Jun. 2016, pp. 186–189.
- [7] H. Bamer and O. Momeni, "A high-gain mm-Wave amplifier design: An analytical approach to power gain boosting," *IEEE J. Solid-State Circuits*, vol. 52, no. 2, pp. 357–370, Feb. 2017.
- [8] B. Razavi, "A 300-GHz fundamental oscillator in 65-nm CMOS technology," *IEEE J. Solid-State Circuits*, vol. 46, no. 4, pp. 894–903, Apr. 2011.
- [9] R. Kananizadeh and O. Momeni, "High-power and high-efficiency millimeter-wave harmonic oscillator design, exploiting harmonic positive feedback in CMOS," *IEEE Trans. Microw. Theory Techn.*, vol. 65, no. 10, pp. 3922–3936, Oct. 2017.
- [10] C.-W. Kim, D. Nguyen, and J.-P. Hong, "A low power buffer-feedback oscillator with current reused structure," *IEICE Trans. Electron.*, vol. E99.C, no. 12, pp. 1335–1338, Dec. 2016.

- [11] O. Momeni and E. Afshari, "High power terahertz and millimeter-wave oscillator design: A systematic approach," *IEEE J. Solid-State Circuits*, vol. 46, no. 3, pp. 583–597, Mar. 2011.
- [12] M. Adnan and E. Afshari, "A 247-to-263.5 GHz VCO with 2.6 mW peak output power and 1.14% DC-to-RF efficiency in 65 nm bulk CMOS," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2014, pp. 262–263.
- [13] R. Kananizadeh and O. Momeni, "A 190.5 GHz mode-switching VCO with 20.7% continuous tuning range and maximum power of -2.1 dBm in $0.13 \mu\text{m}$ BiCMOS," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Jan./Feb. 2016, pp. 46–47.
- [14] J. Grzyb, Y. Zhao, and U. R. Pfeiffer, "A 288-GHz lens-integrated balanced triple-push source in a 65-nm CMOS technology," *IEEE J. Solid-State Circuits*, vol. 48, no. 7, pp. 1751–1761, Jul. 2013.
- [15] C.-H. Li, C.-L. Ko, C.-N. Kuo, M.-C. Kuo, and D.-C. Chang, "A 340 GHz triple-push oscillator with differential output in 40 nm CMOS," *IEEE Microw. Wireless Compon. Lett.*, vol. 24, no. 12, pp. 863–865, Dec. 2014.
- [16] E. Seok *et al.*, "A 410 GHz CMOS push-push oscillator with an on-chip patch antenna," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2008, pp. 627–629.
- [17] D. Shim, D. Koukis, D. J. Arenas, D. B. Tanner, and K. K. O., "553-GHz signal generation in CMOS using a quadruple-push oscillator," in *Proc. Symp. VLSI Circuits (VLSIC)*, 2011, pp. 154–155.
- [18] S.-C. Yen and T.-H. Chu, "An Nth-harmonic oscillator using an N-push coupled oscillator array with voltage-clamping circuits," in *IEEE MTT-S Int. Microw. Symp. Dig.*, vol. 3, Jun. 2003, pp. 2169–2172.
- [19] R. Han and E. Afshari, "A CMOS high-power broadband 260-GHz radiator array for spectroscopy," *IEEE J. Solid-State Circuits*, vol. 48, no. 12, pp. 3090–3104, Dec. 2013.
- [20] H. H. Hsieh and L. H. Lu, "A V-band CMOS VCO with an admittance-transforming cross-coupled pair," *IEEE J. Solid-State Circuits*, vol. 44, no. 6, pp. 1689–1696, Jun. 2009.
- [21] H.-C. Chiu and C.-P. Kao, "A wide tuning range 69 GHz push-push VCO using $0.18 \mu\text{m}$ CMOS technology," *IEEE Microw. Wireless Compon. Lett.*, vol. 20, no. 2, pp. 97–99, Feb. 2010.
- [22] M. Adnan and E. Afshari, "A 105-GHz VCO with 9.5% tuning range and 2.8-mW peak output power in a 65-nm bulk CMOS process," *IEEE Trans. Microw. Theory Techn.*, vol. 62, no. 4, pp. 753–762, Apr. 2014.
- [23] J. Yin and H. C. Luong, "A 57.5–90.1-GHz magnetically tuned multimode CMOS VCO," *IEEE J. Solid-State Circuits*, vol. 48, no. 8, pp. 1851–1861, Aug. 2013.



KANG-UN CHOI received the B.S. degree in electronic and electrical engineering from Chungbuk National University, Cheongju, South Korea, in 2015, and the M.S. degree from the Department of electrical engineering, Chungbuk National University, Cheongju, South Korea, in 2017, where he is currently pursuing the Ph.D. degree in electrical engineering. His research interests include IoT security device and THz and sub-THz integrated circuits such as oscillator for source generator based on CMOS technology.



THANH DAT NGUYEN received the B.S. degree in electronic and electrical engineering from the Hanoi University of Science and Technology, Hanoi, Vietnam, in 2015. He is currently pursuing the Ph.D. degree in electrical engineering with Chungbuk National University, Cheongju, South Korea. His research interests include THz and sub-THz integrated circuits such as oscillator for source generator based on CMOS technology.



SEONG-GON CHOI received the B.S. degree in electronics engineering from Kyeongbuk National University in 1990, and the M.S. and Ph.D. degrees from KAIST, South Korea, in 1999 and 2004, respectively. He is currently a Professor with the School of Information and Communication Engineering, Chungbuk National University. His research interests include smart grid, IoT, mobile communication, and high-speed network architecture and protocol.



JONG-PHIL HONG received the B.Sc. degree in electronic engineering from Korea Aerospace University, Seoul, South Korea, in 2005, the M.S. and Ph. D degrees from the Department of Information and Communications Engineering, Korea Advanced Institute of Science and Technology, Daejeon, South Korea, in 2007 and 2010, respectively. In 2010, he joined Samsung Electronics, Giheung, South Korea, as a Senior Engineer in the mixed-signal circuit design team. Since 2012, he has been with the Department of Electrical Engineering, Chungbuk National University, Cheongju, South Korea, as an Associate Professor. His main research interests include RF integrated circuits such as LNA, Mixer, VCO, and frequency synthesizer for wireless and wire-line communication systems. His current research interests include high frequency (THz) circuit design, and integrated security chip based on CMOS technology.

• • •