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Predictive Direct Power Control Technique for Voltage Source Converter With High Efficiency

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ABSTRACT A predictive direct power control (PDPC) technique to decrease switching loss by injecting offset voltage is proposed for three-phase voltage source converters. The active and reactive power elements of the converter are directly controlled by using three-phase future converter input voltages, which are modified for lowering switching losses by injecting a future offset voltage. Switching operations, generated by the developed PDPC algorithm with modified converter voltage, stop switching operation in one of the converter phases exposed to the highest input current. The non-switching period and the non-switching phase in the proposed technique is automatically adjusted by the reactive power reference, which leads to high efficiency, irrespective of varying input power factor angle condition. The proposed algorithm chooses one optimal voltage vector enabling future active and reactive power to approach closest to the future power references and prohibiting switching of one converter phase conducting the highest current at each step. Therefore, the developed technique can directly control power components and increase converter efficiency, which is proven by simulation and experimental verification.

INDEX TERMS Voltage source converter, predictive control, converter efficiency, direct power control, switching losses.

I. INTRODUCTION

Three-phase voltage source converters to produce input ac voltage with dc output voltage can synthesize input currents in sinusoidal form with controllable input power factor angle preferred with unity power factor, which solve harmonic problems in grids caused by diode rectifiers [1]–[5]. Adjusting the converter currents or the power at the input terminal enables the converter to regulate the dc-link voltage with smaller dc-link capacitor size compared with the diode rectifier [7]–[9]. Well-known operation principles for the voltage source rectifiers are the voltage oriented control (VOC) or direct power control (DPC) methods [1], [2]. The VOC strategy decouples the converter input currents into real and reactive elements and then individually regulates the components by current controllers and pulse-width modulated (PWM) blocks. In the meantime, in the DPC method, the active and reactive power elements of the converter are directly controlled to realize constant dc voltage regulation and unity power factor operation [5]–[7], [21], [24].

The finite set predictive control schemes have been widely studied in recent years, because of low implementation complexity with no pulse-width modulation process and no linear controller, easiness to consider system nonlinearities in intuitive ways, and advanced dynamics [8]–[15]. The predictive control method with a finite control set, considering discrete nature of power converters, have been used to control output currents in voltage source inverters, voltage source rectifier, multilevel converters, and direct ac-ac converters. Besides of the current control methods, direct power control and torque control approaches have also been realized with the finite set predictive control schemes. In the voltage source converters, the finite set predictive direct power control method, hereafter referred to as PDPC method, utilizes a limited number of switching states for the purpose of independently regulating the real and the reactive power components [10], [16], [22], [23]. The PDPC algorithm uses a predefined cost function to evaluate future behaviors of the two power components in the next interval. An optimal voltage vector is chosen from possible vectors to minimize power errors, other than switching lookup tables in traditional direct power control methods [11]–[14].

On the other hand, increasing efficiency by reducing switching losses has been studied as an important subject for the voltage source converter, because it is more utilized in

areas of medium- or high-power systems in general, due to its higher cost than the diode rectifier [17]. One effective approach to decrease the switching losses in the voltage source converters is the addition of offset signals to the reference voltages produced by the VOC strategy, which results in discontinuous PWMs (DPWMs) [17]–[19]. Connecting one converter phase to the upper or the lower dc-bus of the dc-link capacitor with a proper offset signal, the DPWM method realized with distinct PWM blocks using voltage references can decrease the losses at varying input power factor angles [18], [19]. However, the PDPC scheme is based on evaluating future real and reactive power components with their future references through a cost function, without employing PWM blocks and voltage references. As a result, it is not straightforward in the platform of the PDPC method to decide the clamping leg and the clamping region without switching operation in the area of highest value of input current. The switching loss reduction algorithm for the PWM rectifiers with the model predictive control method has been proposed by the same authors [24]. In [24], four voltage vectors to reduce switching losses are preselected on the basis of the magnitudes of the input voltages and the input currents of the PWM rectifiers. As a result, an optimal voltage vector to be selected for input active and reactive power control of the PWM rectifiers is determined among one of the four preselected voltage vectors. Preselecting voltage vectors for the purpose of switching loss reduction leads to the reduced number of candidate vectors when an optimal vector is selected by a predetermined cost function. It has been well known that one of major advantages of the model predictive control method is that several control targets and constraints can be included in a single cost function with several objectives by means of weighting factors. Considering this fact, the reduced number of vectors by the preselection for the purpose of switching loss reduction can limit the best choice for an optimal vector, in cases that other control targets and constraints are included in a cost function.

This paper proposes a switching loss reduction technique for a PDPC method using future offset voltage injection, which can effectively decrease the switching losses of the voltage source converters. The developed method directly controls real and reactive power of the converter based on the PDPC technique using a finite set of future converter input voltages, which are modified by injecting the three-phase future offset voltage. In this scheme, switching operations to directly control the future real and reactive power of the converter are generated with future converter input voltages, which are produced by injecting future offset signal. This proposed scheme has no switching operation in one phase with the highest input current, leading to decreased switching losses of the converter. Because the proposed technique produces the future converter input voltages with the future real and reactive power references, the clamping periods automatically varies according to the input power factor determined by the reactive power reference. The proposed PDPC scheme selects one optimal switching status enabling future active and reactive power to approach closest to the future power references, using a predefined cost function. Therefore, the proposed PDPC method can execute direct power control and can connect one converter phase with the highest input current to the positive or negative dc-bus of the dc-link capacitor, to reduce the switching losses. The switching loss reduction method in this paper is realized by injecting an offset voltage into the converter reference voltage vector, instead of vector preselection method in [24]. Therefore, an optimal voltage vector to be selected for input active and reactive power control of the PWM rectifiers is determined among all possible voltage vectors in the developed method. The simulation and experimental verifications are included to validate the developed technique.

The contents of this paper are as follows. First, Section II describes the conventional method of the finite set PDPC method for three-phase voltage source converters. The proposed switching loss reduction algorithm using the offset voltage injection is presented in Section III. Section IV and Section V shows the simulation and experiment results with comparisons between the conventional method and the proposed method, respectively. Finally, Section VI contains conclusions of this paper.

II. FINITE SET PDPC METHOD FOR THREE-PHASE VOLTAGE SOURCE CONVERTERS

Fig. 1 illustrates the topology of a three-phase voltage source converter, in which L_s and R_s are the input filter inductances and resistances, respectively. The three-phase source voltages and input currents are defined, respectively, as

$$\boldsymbol{u}_s = \frac{2}{3}\left(u_{sa} + u_{sb}e^{j(2\pi/3)} + u_{sc}e^{j(4\pi/3)}\right) \tag{1}$$

$$\boldsymbol{i}_s = \frac{2}{3}\left(i_{sa} + i_{sb}e^{j(2\pi/3)} + i_{sc}e^{j(4\pi/3)}\right). \tag{2}$$

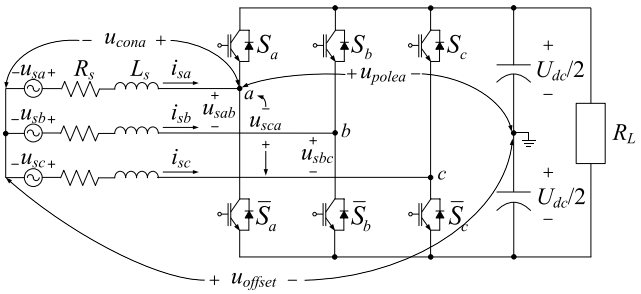


FIGURE 1. Three-phase voltage source converter.

The voltage source converter can only change input power dynamics by a finite number of voltage sets produced by a finite number of switching status, which leads to the PDPC method based on the finite-set-concept.

Eight voltage vectors and corresponding switching operations can provide constant dc voltage regulation and decoupled power control, leading to sinusoidal input current synthesis [16]. Dynamic relationship between the input current vector, $\boldsymbol{i}_s$, and the converter voltage vector, $\boldsymbol{u}_{con}$, at the

input terminal of the converter is written as

$$L_s \frac{di_s}{dt} = \boldsymbol{u}_s - \boldsymbol{u}_{con} - R\boldsymbol{i}_s. \tag{3}$$

The input current dynamics in (3) is written in the discrete-time domain by using approximation in (4) with a sampling interval T_s.

$$\frac{d\boldsymbol{i}_s}{dt} \approx \frac{\boldsymbol{i}_s(n+1) - \boldsymbol{i}_s(n)}{T_s}. \tag{4}$$

Shifting the current vector at the $(n+1)$th instant, obtained by (3) and (4), by one step forward leads to the current vector at the one-step ahead, $\boldsymbol{i}_s(n+2)$, is expressed by [20]

$$\boldsymbol{i}_s(n+2) = \left(1 - \frac{R_s T_s}{L_s}\right)\boldsymbol{i}_s(n+1) + \frac{T_s}{L_s}\left[\boldsymbol{u}_s(n+1) - \boldsymbol{u}_{con}(n+1)\right]. \tag{5}$$

As seen from (5), the current vector $\boldsymbol{i}_s(n+1)$ is constructed from the input current vector $\boldsymbol{i}_s(n)$ and the source voltage vector $\boldsymbol{u}_s(n)$ obtained at the nth instant. Furthermore, the source voltage $\boldsymbol{u}_s(n+1)$ in (5) is also expressed by

$$\boldsymbol{u}_s(n+1) = \boldsymbol{u}_s(n)\, e^{j\Delta\theta}, \tag{6}$$

where $\Delta\theta = \omega T_s$ is the angle variation of the source voltage vector during one sampling step. Using the future converter input current and the future source voltage vectors, the future input real and reactive power components are calculated by

$$\begin{aligned} P(n+2) &= \mathrm{Re}\left\{\boldsymbol{u}_s(n+2)\,\bar{\boldsymbol{i}}_s(n+2)\right\} \\ &= u_{s\alpha}(n+2)i_{s\alpha}(n+2) + u_{s\beta}(n+2)i_{s\beta}(n+2) \end{aligned} \tag{7}$$

$$\begin{aligned} Q(n+2) &= \mathrm{Im}\left\{\boldsymbol{u}_s(n+2)\,\bar{\boldsymbol{i}}_s(n+2)\right\} \\ &= u_{s\beta}(n+2)i_{s\alpha}(n+2) - u_{s\alpha}(n+2)i_{s\beta}(n+2) \end{aligned} \tag{8}$$

where $i_{s\alpha}(n+2)$, $i_{s\beta}(n+2)$, $u_{s\alpha}(n+2)$, and $u_{s\beta}(n+2)$ are the $\alpha\beta$ components of the converter input current and the source voltage vectors at the $(n+2)$th step. The source voltage values in (7) and (8) are calculated by shifting (6) one-step ahead. A cost function is defined with a difference between power reference values and predicted power components as

$$g = \left|P^* - P(n+2)\right| + \left|Q^* - Q(n+2)\right|. \tag{9}$$

Finally, one optimal switching state corresponding to an optimal converter input voltage vector is chosen in such a way to minimize the cost function.

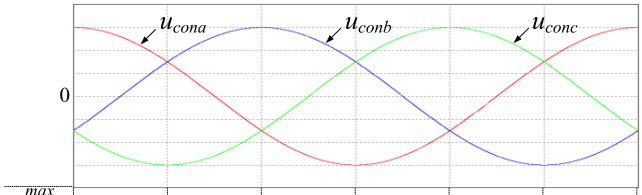
III. PROPOSED SWITCHING LOSS REDUCTION TECHNIQUE FOR THE PDPC METHOD BASED ON FUTURE OFFSET VOLTAGE INJECTION

Because high current amplitude carried through switches result in high switching losses at switching moments, stopping the switching of switches conducting the highest current can reduce switching losses. This proposed method produces the future offset voltage in such a way that the converter input voltages with the future offset voltage injection connect one phase with the highest converter input current to the upper or lower dc-bus bar. The three-phase pole voltages of the converter (u_{polea}, u_{poleb}, u_{polec}), the converter input voltages (u_{cona}, u_{conb}, u_{conc}), and the offset voltage (u_{offset}) as shown in Fig. 1 are related with

$$\boldsymbol{u}_{pole}(n+1) = \boldsymbol{u}_{con}(n+1) + u_{offset}(n+1). \tag{10}$$

The converter input voltage can be achieved by rearranging (5) as

$$\boldsymbol{u}_{con}(n+1) = \boldsymbol{u}_s(n+1) + \frac{L_s}{T_s}\left\{\left(1 - \frac{R_s T_s}{L_s}\right)\boldsymbol{i}_s(n+1) - \boldsymbol{i}_s(n+2)\right\}. \tag{11}$$



u_{con}^{max}	u_{cona}	u_{conb}	u_{conb}	u_{conc}	u_{conc}	u_{cona}
u_{con}^{mid}	u_{conb}	u_{cona}	u_{conc}	u_{conb}	u_{cona}	u_{conc}
u_{con}^{min}	u_{conc}	u_{conc}	u_{cona}	u_{cona}	u_{conb}	u_{conb}

FIGURE 2. Classification of the converter input voltages.

Fig. 2 illustrates the future converter input voltages calculated by (11), $u_{cona}(n+1)$, $u_{conb}(n+1)$ and $u_{conc}(n+1)$, which are classified to $u_{con}^{\max}(n+1)$, $u_{con}^{mid}(n+1)$, and $u_{con}^{\min}(n+1)$, depending on their magnitudes. A restrictive converter leg, which should not stop the switching for linear operation of the converter, can be chosen on the basis of the three classified voltages shown in Fig. 2, which is a converter phase assigned to medium voltage $u_{con}^{mid}(n+1)$. Clamping a prohibitive phase may result in over-modulated operation of at least another phase in the voltage source converter, and thus, the converter may not control its input current [19]. Therefore, one of the two remaining phases with $u_{con}^{\max}(n+1)$ and $u_{con}^{\min}(n+1)$ is forced to stop switching by the proposed method, whereas the converter leg associated with the voltage $u_{con}^{mid}(n+1)$ continues to switch. One converter phase with larger input current than the other one, between the two converter phases, is connected to either the upper or lower dc-bus bar. Among three input currents, $i_{sa}(n+1)$, $i_{sb}(n+1)$, and $i_{sc}(n+1)$, the input currents of the converter associated with $u_{con}^{\max}(n+1)$ and $u_{con}^{\min}(n+1)$ are assigned to $i_{con}^{\max}(n+1)$ and $i_{con}^{\min}(n+1)$, respectively. One phase of the converter with a higher input current magnitude, between the two phases related to $u_{con}^{\max}(n+1)$ and $u_{con}^{\min}(n+1)$, is required to stop the switching to reduce the switching losses. If an absolute magnitude of the input current $i_{con}^{\max}(n+1)$ is larger than that of $i_{con}^{\min}(n+1)$, the leg with $u_{con}^{\max}(n+1)$ should be connected to the upper dc-bus bar at $(n+1)$th instant, because $u_{con}^{\max}(n+1)$ is positive. On the other hand, the leg assigned to $u_{con}^{\min}(n+1)$, that is negative,

is connected to the negative dc-link at $(n+1)$th instant, in the case that the leg is exposed to the input current with larger absolute magnitude. The proposed method produces the offset voltage at $(n+1)$th instant in such a way that the upper or the lower switching device with the larger input current stops switching operation in the legs with $u_{con}^{\max}(n+1)$ or $u_{con}^{\min}(n+1)$. Therefore, the one-step future offset voltage can be obtained from the future converter input voltage in (11) as

$$u_{offset}(n+1) = \begin{cases} \dfrac{U_{dc}}{2} - u_{con}^{\max}(n+1), \\ \quad if \ \left|i_{con}^{\max}(n+1)\right| > \left|i_{con}^{\min}(n+1)\right| \\ -\dfrac{U_{dc}}{2} - u_{con}^{\min}(n+1), \\ \quad if \ \left|i_{con}^{\min}(n+1)\right| > \left|i_{con}^{\max}(n+1)\right|. \end{cases} \tag{12}$$

From (11) and (12), it can be noted that the one-step and the two-step future input current vectors are necessary to achieve the offset voltage to stop switching operation. Instead of the two actual current values $\boldsymbol{i}_s(n+1)$ and $\boldsymbol{i}_s(n+2)$, the reference values are used by assuming that the converter actual currents accurately track the references at both the $(n+1)$th and the $(n+2)$th steps. Utilizing the reference current vectors to obtain the converter voltage vectors can avoid a delay of one sampling step and reduce the effect of current ripples on deciding the clamping phase. The reference current values of the a- and b- phases at the $(n+2)$th step are calculated by the real and reactive power references in (7) and (8) by

$$i_{sa}^{*}(n+2) = \frac{\sqrt{3}u_{sa}(n+2)P^{*} + \{u_{sa}(n+2)+2u_{sb}(n+2)\}Q^{*}}{2\sqrt{3}\{u_{sa}(n+2)^2 + u_{sa}(n+2)u_{sb}(n+2) + u_{sb}(n+2)^2\}} \tag{13}$$

$$i_{sb}^{*}(n+2) = \frac{\sqrt{3}u_{sb}(n+2)P^{*} - \{2u_{sa}(n+2) + u_{sb}(n+2)\}Q^{*}}{2\sqrt{3}\{u_{sa}(n+2)^2 + u_{sa}(n+2)u_{sb}(n+2) + u_{sb}(n+2)^2\}}. \tag{14}$$

Note that the c-phase reference input current can be calculated with (13) and (14). In addition, delaying one-step the reference currents calculated by (13) and (14) yields reference current values $\boldsymbol{i}_s^{*}(n+1)$. Thus, the offset voltage in (12) can be achieved by (6), (11), (13), and (14). Furthermore, the converter input voltage adjusted with the offset voltage injection, $\boldsymbol{u}_{con}^{\mathrm{mod}}(n+1)$, is generated with the pole voltages $\boldsymbol{u}_{pole}(n+1)$ and the offset voltage $u_{offset}(n+1)$ as

$$\boldsymbol{u}_{con}^{\mathrm{mod}}(n+1) = \boldsymbol{u}_{pole}(n+1) - u_{offset}(n+1) \tag{15}$$

where, the future pole voltage $u_{pole}(n+1)$ can take $U_{dc}/2$ and $-U_{dc}/2$ in the case that the switch S_i $(i = a, b, c)$ is closed and open, respectively, as illustrated in Table 1.

The future active and reactive power components $P(n+2)$ and $Q(n+2)$ in the proposed PDPC method can be calculated from (5), (7), and (8) with the modified converter input voltages $\boldsymbol{u}_{con}^{\mathrm{mod}}(n+1)$ as

$$\begin{aligned} P(n+2) &= u_{sa}(n+2)\left(i_{sa}(n+1) + \frac{T_s}{L_s}U_{La}^{\mathrm{mod}}(n+1)\right) \\ &\quad + u_{sb}(n+2)\left(i_{sb}(n+1) + \frac{T_s}{L_s}U_{Lb}^{\mathrm{mod}}(n+1)\right) \\ &\quad + u_{sc}(n+2)\left(i_{sc}(n+1) + \frac{T_s}{L_s}U_{Lc}^{\mathrm{mod}}(n+1)\right) \end{aligned} \tag{16}$$

$$\begin{aligned} Q(n+2) &= \frac{u_{sbc}(n+2)}{\sqrt{3}}\left(i_{sa}(n+1) + \frac{T_s}{L_s}U_{La}^{\mathrm{mod}}(n+1)\right) \\ &\quad + \frac{u_{sca}(n+2)}{\sqrt{3}}\left(i_{sb}(n+1) + \frac{T_s}{L_s}U_{Lb}^{\mathrm{mod}}(n+1)\right) \\ &\quad + \frac{u_{sab}(n+2)}{\sqrt{3}}\left(i_{sc}(n+1) + \frac{T_s}{L_s}U_{Lc}^{\mathrm{mod}}(n+1)\right) \end{aligned} \tag{17}$$

where,

$$U_{Lj}^{\mathrm{mod}}(n+1) = u_{sj}(n+1) - u_{conj}^{\mathrm{mod}}(n+1) - R_s i_{sj}(n+1), \quad j = a, b, c.$$

In addition, $u_{sbc}(n+2)$, $u_{sca}(n+2)$, and $u_{sab}(n+2)$ are the three-phase input line-to-line voltages, respectively defined by

$$\begin{aligned} u_{sbc}(n+2) &= u_{sb}(n+2) - u_{sc}(n+2), \\ u_{sca}(n+2) &= u_{sc}(n+2) - u_{sa}(n+2), \\ u_{sab}(n+2) &= u_{sa}(n+2) - u_{sb}(n+2). \end{aligned} \tag{18}$$

By the cost function in (9), one optimal switching state, yielding the smallest power errors between the power components and the future power references among the eight possible future power components produced by the modified converter input voltages, is selected. Note that the future real and reactive power in (16) and (17) are generated with the future offset voltage injection, which forces the one leg with the largest input current to stop switching operation. As a result, the proposed method can not only perform direct power control to follow the power references, but also achieve high efficiency by decreasing switching loss.

The proposed method connects one converter phase exposed to the highest input current, unless it is the prohibitive leg, to the positive or negative terminal of the dc-link, whereas the other two phases are switched. This clamping

TABLE 1. Switching states and pole voltages.

Converter switching states			Three-phase pole voltages of converter		
S_a	S_b	S_c	u_{polea}	u_{poleb}	u_{polec}
0	0	0	$-U_{dc}/2$	$-U_{dc}/2$	$-U_{dc}/2$
0	0	1	$-U_{dc}/2$	$-U_{dc}/2$	$U_{dc}/2$
0	1	0	$-U_{dc}/2$	$U_{dc}/2$	$-U_{dc}/2$
0	1	1	$-U_{dc}/2$	$U_{dc}/2$	$U_{dc}/2$
1	0	0	$U_{dc}/2$	$-U_{dc}/2$	$-U_{dc}/2$
1	0	1	$U_{dc}/2$	$-U_{dc}/2$	$U_{dc}/2$
1	1	0	$U_{dc}/2$	$U_{dc}/2$	$-U_{dc}/2$
1	1	1	$U_{dc}/2$	$U_{dc}/2$	$U_{dc}/2$

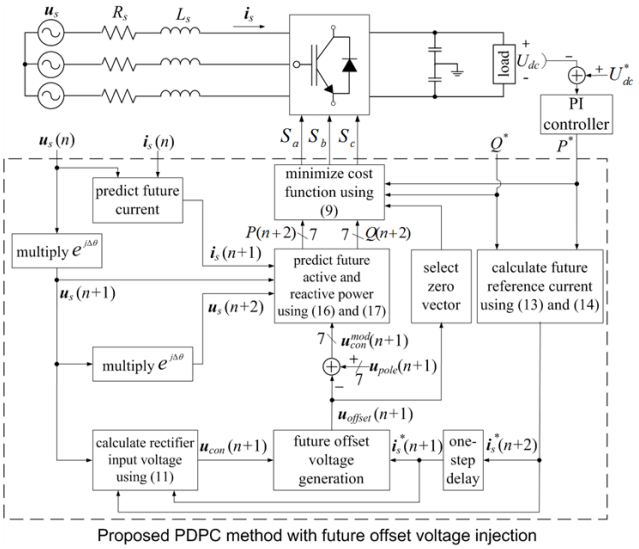


FIGURE 3. Block diagram of the proposed PDPC method.

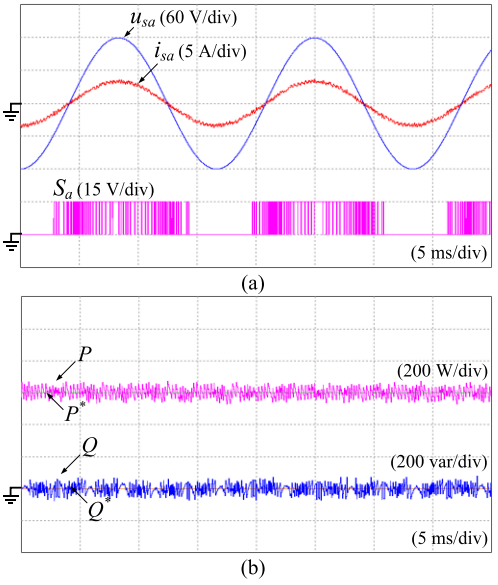


FIGURE 4. Simulation results of the conventional method (a) source voltage, input current, and switching waveform of S_a (b) real and reactive power.

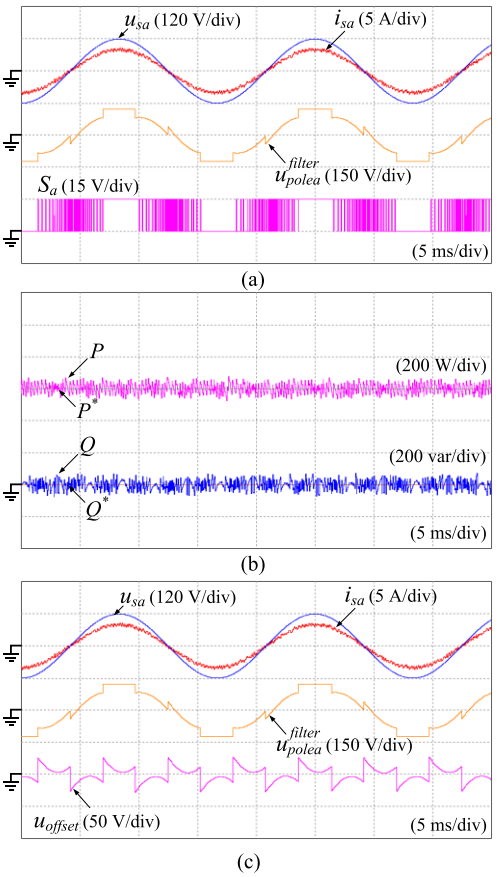


FIGURE 5. Simulation results of the proposed PDPC technique (a) source voltage, input current, *a*-phase filtered pole voltage, and switching waveform of S_a (b) real and reactive power (c) source voltage, input current, *a*-phase filtered pole voltage, and offset voltage.

operation should not be disturbed by unwanted switching of the zero vectors. Because the cost function in (9) selects an optimal voltage vector based on the power errors with no consideration of switching operation, arbitrary choice of one between two zero vectors might yield undesirable switching during the clamping period. Thus, selecting a proper vector between the two zero vectors is required when the cost function selects the zero vector as the optimal vector. This proposed algorithm chooses the zero voltage vector depending on the polarity of the future offset voltage, to keep the clamping interval without switching operation. In the case that the future offset voltage is greater than zero, the vector $\boldsymbol{V}_7$ is utilized. On the contrary, the vector $\boldsymbol{V}_0$ is used when the offset voltage is less than zero.

Fig. 3 illustrates the block diagram of the proposed PDPC method, where it is seen that the proposed method does not require any extra measurement. Moreover, the future offset voltage to determine the non-switching phase and the non-switching interval is built using the reactive power reference Q^* as shown in Fig. 3. Thus, the clamping operation without the switching operation in the proposed method is automatically varied according to the reactive power reference, although Q^* is set to zero for unity power factor in general. Thus, the proposed PDPC method can decrease the switching losses both at the unity power factor operation and at any input power factor angle with arbitrary reactive power reference.

IV. SIMULATION RESULTS

The developed PDPC technique based on the future offset voltage injection was simulated for a voltage source converter connected with the source voltage with the amplitude of $u_{sa} = 120$ V. In addition, the line impedance was set to $R_s = 0.8\ \Omega$ and $L_s = 12$ mH. The 1100 μF output capacitor and the 100 Ω load resistor were used with the 245 V output voltage reference and the 50 μs sampling step. The simulation results obtained by the conventional PDPC algorithm are also obtained with the same condition for comparison.

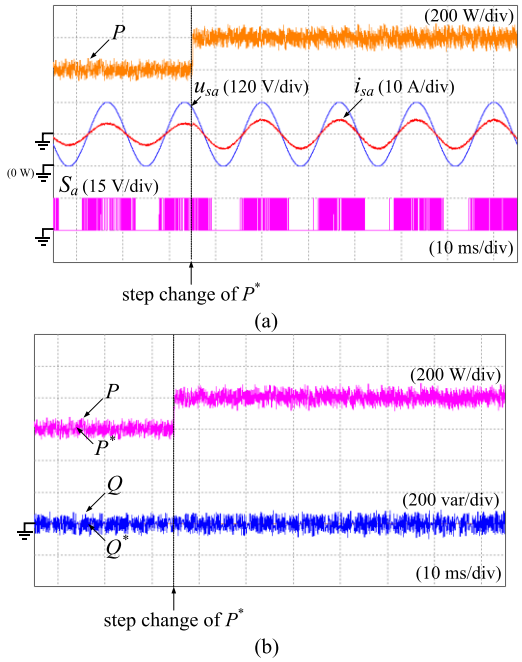


FIGURE 6. Simulation results of the conventional method with the sudden-change of P^* (a) active power, source voltage, input current, and switching waveform of S_a (b) real and reactive power.

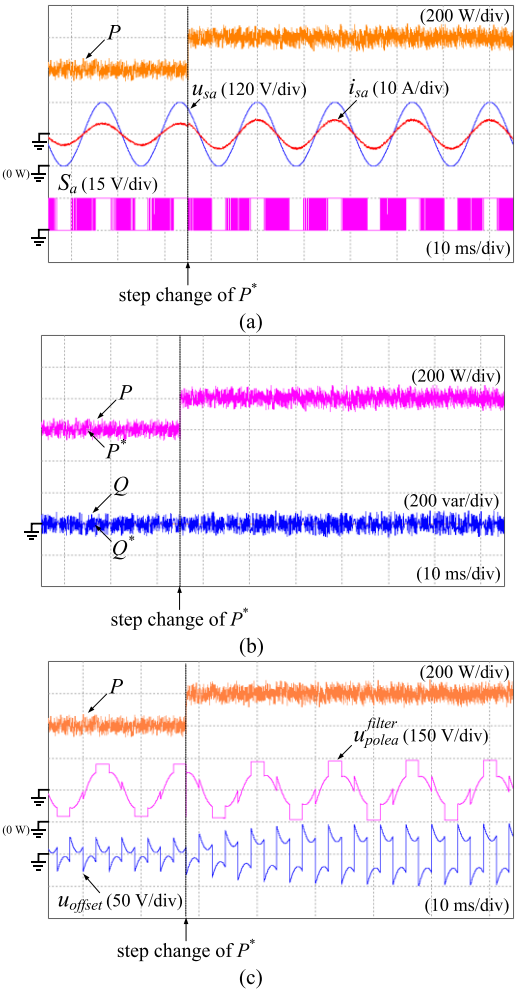


FIGURE 7. Simulation results of the proposed PDPC technique under the step-change of P^* (a) real power, source voltage, input current, and switching waveform of S_a (b) real and reactive power (c) active power, a-phase filtered pole voltage, and offset voltage.

Fig. 4 illustrates the simulation results obtained by the conventional method including the source voltage and current, the switch signal of S_a, and active and reactive power components. The active and reactive power accurately follow their references by the conventional PDPC method. Simulation waveforms obtained by the proposed PDPC method with the future offset voltage injection are shown in Fig. 5. Unlike the switching waveform of S_a in the conventional method in Fig. 4(a), the proposed method prevents the switch S_a from commutating in the region of positive and negative peak input currents in Fig. 5(a). It is seen from the low-pass filtered pole voltage at the a-phase, $u_{polea}^{filter}(n+1)$, that the middle of the non-switching period of the switching pattern is aligned with the peak of the input current, because of the future offset voltage and the converter input voltage modified by the offset voltage injection. The waveform of $u_{polea}^{filter}(n+1)$ was obtained by filtering out the high-frequency components of the pole voltage with a cut-off frequency at 1 kHz. In addition, it is clearly seen that the proposed technique synthesizes sinusoidal input currents with unity power factor, same as the conventional method. Moreover, the proposed algorithm leads to no steady-state error between the actual and the reference power components.

Figures 6 and 7 show the transient responses of the conventional and proposed PDPC techniques under sudden variation in P^* from 600 W to 800 W, whereas Q^* is kept to 0 var. As shown in Figs. 6 and 7, the power tracking capability and the transient response of both the developed and the conventional PDPC techniques is the same. Furthermore, both the methods result in no coupling effect in the real and reactive power elements. The switch S_a, in the proposed PDPC method with the future offset voltage injection, has no switching in the 60° periods of the positive and negative peak input currents, under the transient circumstance. It is seen that the future offset voltage u_{offset} and the a-phase filtered pole voltage u_{polea}^{filter} in Fig. 7(c) experience no waveform change in the case of the step-change of the active power command, where only the amplitudes of the two waveforms are increased with the increased P^*. As a result of the same waveforms of the future offset voltage, the clamping region to stop the switching operation of the switch S_a does not change because the reactive power command Q^* is unchanged. Thus, the middle of the no-switching region of the switching pattern is aligned with the peak of the input current both before and after the step-change of P^*.

Figures 8 and 9 illustrate the simulated waveforms of the transient response under sudden variation in Q^* from 0 to 200 var for the conventional and developed PDPC algorithms. The real power command is kept to $P^* = 600$ W. It can

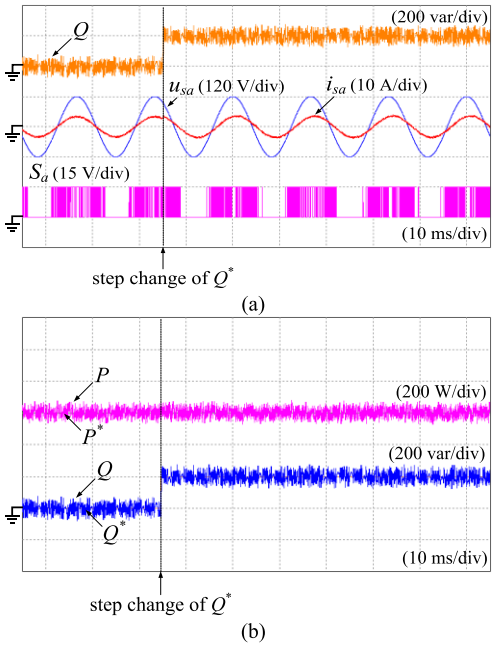


FIGURE 8. Simulation results of the conventional method under the transient response of Q* (a) active power, source voltage, input current, and switching waveform of S_a (b) real and reactive power.

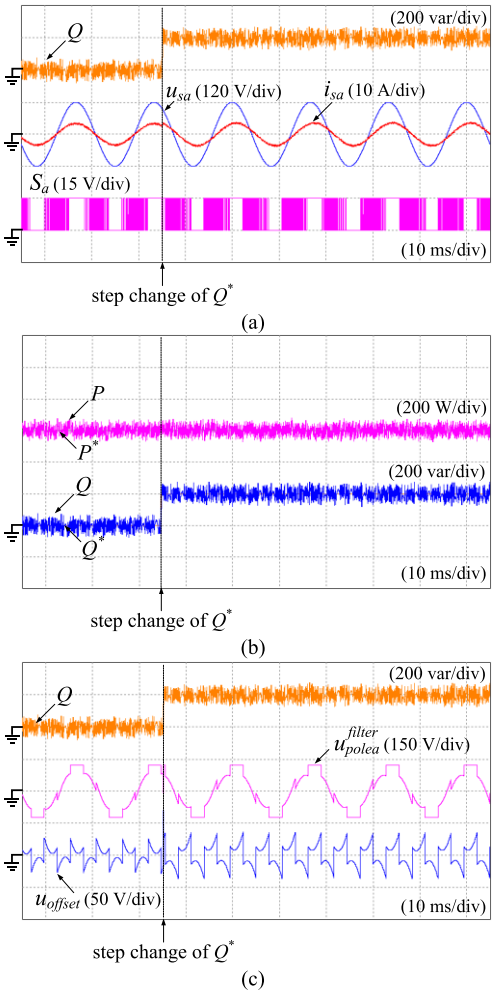


FIGURE 9. Simulation results of the proposed PDPC technique under the transient response of Q* (a) reactive power, source voltage, input current, and switching waveform of S_a (b) real and reactive power (c) reactive power, a-phase filtered pole voltage, and offset voltage.

be seen that the source voltage and current alters from the in-phase operation to the out-of-phase operation, according to change of the reactive power reference. Fig. 9(c) shows that the shapes of the future offset voltage u_{offset} and the a-phase filtered pole voltage u^{filter}_{polea} are changed because of the sudden change in Q^*. Accordingly, the clamping period generated by the proposed PDPC method moves, according to the phase difference of the source voltage and current. Therefore, the proposed technique yields switching loss reduction, regardless of the input power factor condition.

V. EXPERIMENTAL RESULTS

The experimental setup to prove the developed PDPC technique was built with a voltage source converter with an Insulated Gate Bipolar Transistor (IGBT) module, a 12 mH input inductor, a 0.8 Ω input resistor, and a 1100-μF output capacitor. The 120 V amplitude of the source voltage was used and the dc output voltage command was fixed to 245 V. In addition, a 100 Ω resistor was employed for the output load. The entire control algorithm was implemented in a Digital Signal Processor (DSP) board (TMS320F28335) with a sampling interval $T_{sp} = 50$ μs. Fig. 10 provides a photograph of the experiment setup. Fig. 11 shows the experimental waveforms achieved by the conventional algorithm. In addition, the experimental results of the developed PDPC method are shown in Fig. 12, where the shape of the a-phase filtered pole voltage, u^{filter}_{polea}, the offset voltage u_{offset}, and the pulse pattern of S_a in the proposed technique are the same as those in the simulated waveforms of Fig. 5. It can be seen that the conventional and proposed algorithms

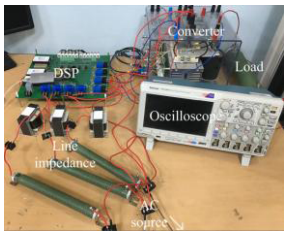


FIGURE 10. Photograph of the experimental setup.

generate sinusoidal source currents in phase with the source voltages with $Q^* = 0$. Moreover, the two techniques lead to no steady-state errors in the real and the reactive power components. The proposed PDPC technique clearly produces the switching patterns to stop the switching in the area of the highest input currents to reduce the switching losses, as shown in Fig. 12(a).

Experimental results with transient response by the proposed PDPC technique along with the conventional algorithm are depicted in Figs. 13 and 14 under the condition

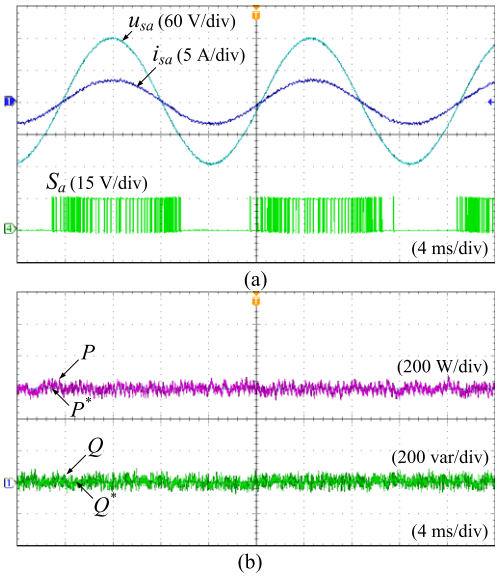


FIGURE 11. Experimental results of the conventional method (a) source voltage, input current, and switching waveform of S_a (b) real and reactive power.

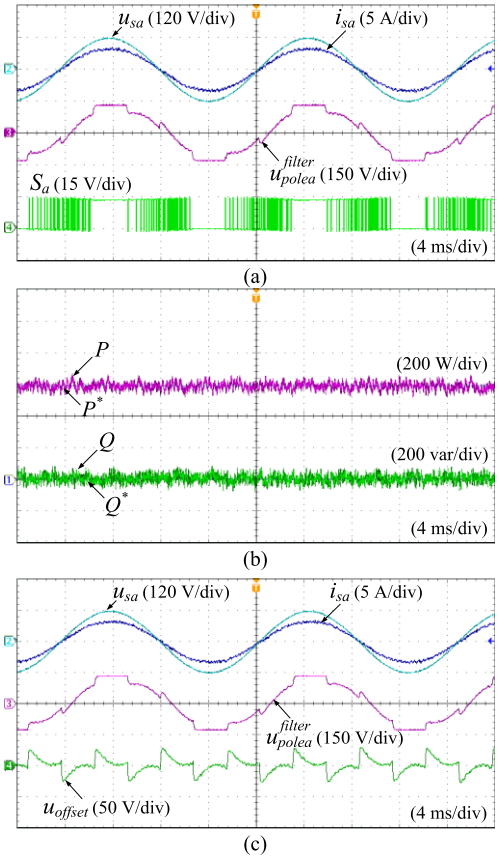


FIGURE 12. Experimental waveforms of the proposed PDPC technique (a) source voltage, input current, *a*-phase filtered pole voltage, and switching waveform of S_a (b) real and reactive power (c) source voltage, input current, *a*-phase filtered pole voltage, and offset voltage.

of the sudden change in P^* from 600 W to 800 W, whereas Q^* is fixed to zero. Experimental waveforms, including the offset voltage and the *a*-phase filtered pole

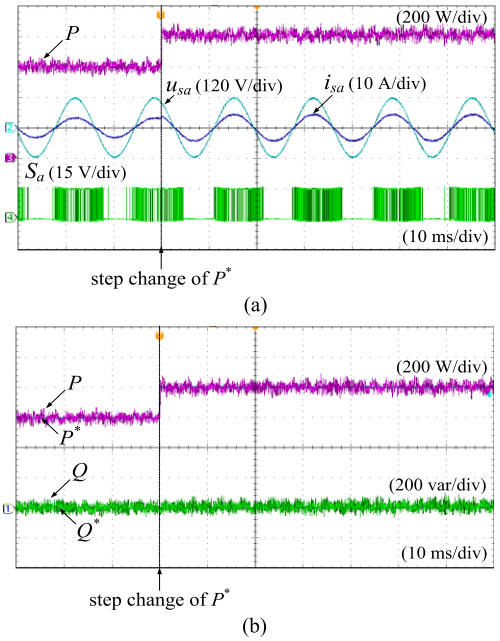


FIGURE 13. Transient waveforms of the conventional method with the step-change of P^* (a) real power, source voltage, input current, and pulse waveform of S_a (b) real and reactive power.

voltage of the proposed method, are the same as simulation waveforms in Figs. 6 and 7. As shown in Figs. 13 and 14, the active power component in the developed PDPC technique shows fast reference tracking, same as the conventional algorithm. It is seen from Fig. 14(a) that the pulse pattern of S_a that resulted from the proposed technique leads to no switching in the area of the peak of i_{sa} irrespective of the step-change of P^*.

Figures 15 and 16 illustrate that the experimental waveforms under the sudden change in Q^* from 0 to 200 var for both the techniques, where the real power reference is kept to 600 W. In the experimental waveforms in Fig. 16(c), which are identical to the simulated waveforms of Fig. 9(c), the shapes of the future offset voltage u_{offset} and the a-phase filtered pole voltage u_{polea}^{filter} are changed depending on the reactive power command. Thus, the experimental results in Fig. 16 verify that the proposed PDPC method generates the switching patterns with the clamping period moving according to the input displacement power factor angle of the source voltage and input current obtained by the reactive power command, to reduce the switching losses.

Figs. 6, 8, 13, and 15 show the simulation and the experimental waveforms of the conventional methods in cases of the step-changes of the real and the reactive power, respectively. It is seen that the real and the reactive power obtained by the conventional method follow the reference values with the step-changes. In addition, Figs. 7, 9, 14 and 16 show the simulation and the experimental waveforms of the proposed methods in cases of the step-changes of the real and the reactive power, respectively. It is clearly seen that the real and the reactive power obtained by the proposed method

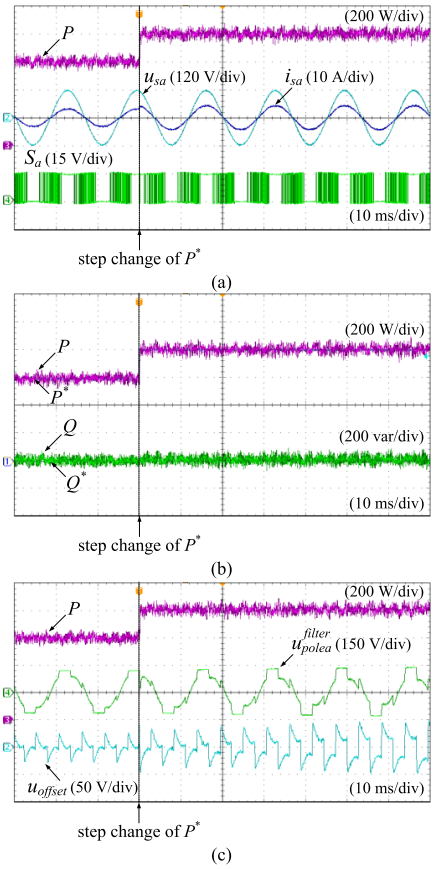


FIGURE 14. Transient waveforms of the proposed PDPC technique under the step-change in P^* (a) real power, source voltage, input current, and switching waveform of S_a (b) real and reactive power (c) real power, a-phase filtered pole voltage, and offset voltage.

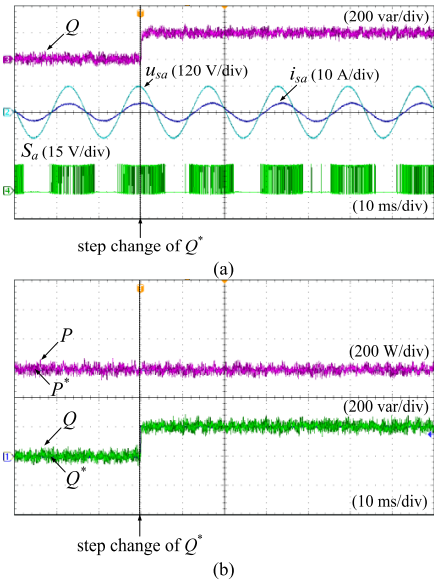


FIGURE 15. Transient waveforms of the conventional method under the sudden change in Q^* (a) reactive power, source voltage, input current, and switching waveform of S_a (b) real and reactive power.

follow the reference values with the step-changes. However, the switching waveforms obtained by the proposed method in the figures have no switching operation in the 60° periods

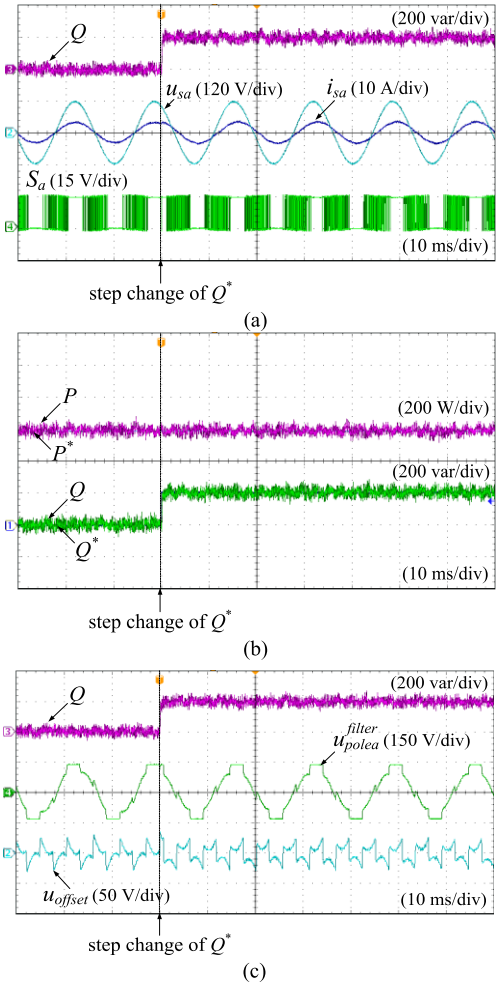


FIGURE 16. Transient waveforms of the developed PDPC technique under the step-change of Q^* (a) reactive power, source voltage, input current, and pulse patterns of S_a (b) real and reactive power (c) reactive power, a-phase filtered pole voltage, and offset voltage.

of the positive and negative peak of the input currents for switching loss reduction, even when the transient state occurs. On the other hand, the periods of no switching operation of the conventional method have no relationship with input current peak regions, as shown in the figures. Therefore, the figures can show that the proposed method can reduce the switching loss compared to the conventional method, whereas both the methods can force satisfactory direct power control performance in cases of the step-change of the power references.

Figure 17 depicts the comparison achieved by the both techniques with $P = 10$ kW in simulation. The proposed PDPC algorithm with the future offset voltage injection produces reduced losses than those of the conventional technique, whereas the total harmonic distortion (THD) values of the input currents as well as the power error are almost the same. Fig. 18 illustrates the frequency spectra of the load currents produced by the two techniques. Note that the effects of the loss reduction of the proposed method would be increased with increasing sampling frequency and increasing

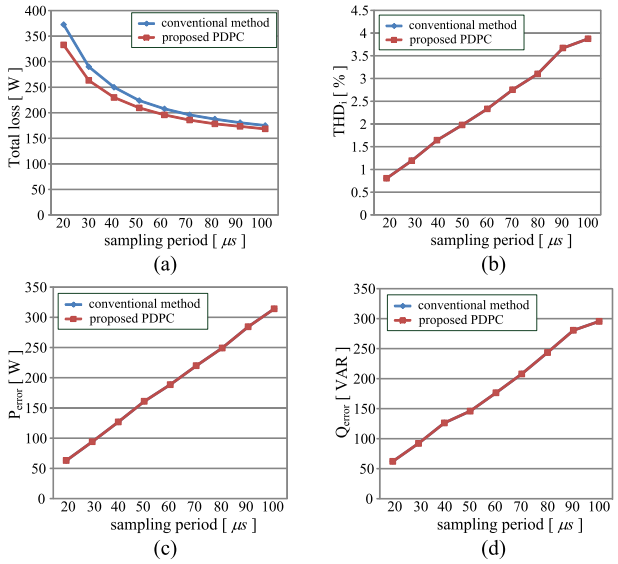


FIGURE 17. Comparison of the conventional and proposed techniques according to the sampling interval: (a) total loss (b) THD_i of the input current (c) real power error (d) reactive power error.

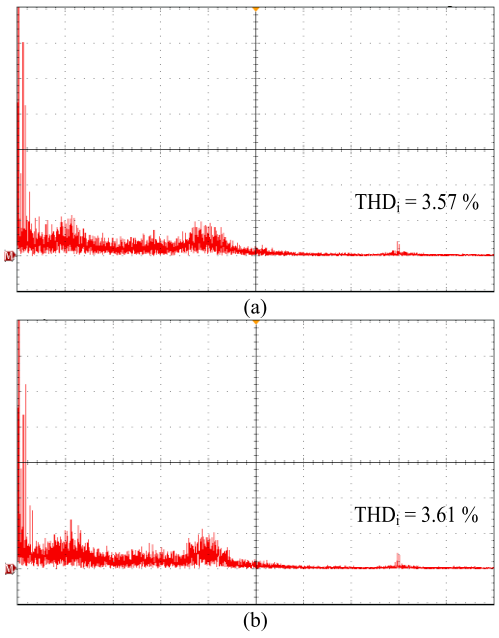


FIGURE 18. Frequency spectrum of the load current (i_{sa}) (2500 Hz/div and 10 mA/div) produced by the (a) conventional and (b) proposed algorithms.

output power. Fig. 17 illustrates that the proposed method can lead to lower total losses than the conventional method, due to the reduced switching losses by stop switching operation in one of the converter phases exposed to the highest input current, which are proved by the simulation and experimental results in Figs. 7, 9, 14, and 16. Those figures show that the switching waveforms obtained by the proposed method can successfully stop the switching operations in the 60° periods of the positive and negative peak of the input currents.

VI. CONCLUSION

This paper has developed a switching loss reduction technique for the PDPC method for the three-phase voltage source converter using offset signal injection. In the proposed method, the active and reactive power elements of the converter are directly controlled in a platform of the PDPC algorithm using future converter input voltages, which are modified by injecting a future offset voltage. The proposed method can stop switching operation of one of the three converter phases exposed to the highest input current to reduce the switching losses, while it performs independent control of the active and reactive power. Because the proposed method builds the future offset voltage on-line based on the future active and reactive power references at every sampling period, the clamping periods to stop switching operations in one converter phase with largest input currents are optimally varied depending on the input power factor angle. As a result, the developed PDPC algorithm can decrease switching losses of the converter even under conditions of varying input power factor.

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