IEEE Access
Multidisciplinary | Rapid Review | Open Access Journal

SPECIAL SECTION ON NOVEL LEARNING APPLICATIONS AND SERVICES FOR SMART CAMPUS

Received February 27, 2018, accepted March 25, 2018, date of publication April 3, 2018, date of current version May 16, 2018.

Digital Object Identifier 10.1109/ACCESS.2018.2822699

Research on High Performance Frequency Synthesizer in Radio Frequency Integrated Circuits

ZHANG WEIJIA

College of Electronic Information and Automation, Tianjin University of Science and Technology, Tianjin 300457, China

e-mail: zwj035@163.com

This work was supported by the Tianjin Municipal Education Commission Scientific Research Project under Grant 2017KJ036.

ABSTRACT With the popularization of broadcasting networks, telecommunication networks, and Internet triple play services, broadband requirements have been proposed for transceivers in wireless communication systems. Frequency source is an important part of the RF transceiver, which is usually chosen as the source of the transceiver frequency reference source. Therefore, the development of ultra-wideband, high stability, low phase noise, and low spurious performance of the frequency synthesizer is of great significance. This paper firstly analyzed the transmission process of noise in phase-locked loop by establishing a linear mathematical model of phase locking loop (PLL), and then studied the main factors affecting the phase noise and spurious performance in the application design. In order to meet the demand of triple-miniaturized RF front end, an integrated phase-locked chip is used to design a frequency synthesizer, where the output frequency of the two channels ranges from 137.5 MHz to 4.4 GHz. In order to meet the engineering application requirements, the frequency synthesizer is designed with a host computer to achieve the programmable control of the output frequency and output power. Finally, the optimized design of a wideband frequency synthesizer is provided to make up for the lack of performance of the integrated phase-locked chip design, of which the output frequency range is 31.25 MHz ∼8 GHz, including basic PLL module circuit, power control module circuit, and frequency expansion module circuit.

INDEX TERMS Wideband frequency synthesizer, PLL (phase locking loop), radio frequency integrated circuits.

I. INTRODUCTION

In recent years, with the rapid development of network Internet application technology, the convergence of technology and business has emerged in the three major networks of radio, television, telecommunications and the Internet [1]. As a typical information fusion phenomenon, triple play arises in the context of the convergence. As a key RF technology in the evolution of network convergence and evolution, radio frequency reconfigurable and broadband miniaturized multi-antenna integration technologies have been the research hotspots [2]. As the source of the frequency reference that is essential for triple-play tele-transmitters, the frequency synthesizer has not caught the eye. The antenna receives the RF signal through the preselection filter, low noise amplifier, image rejection filter and local oscillator signal mixing, resulting in the intermediate frequency signal amplification filter. Throughout the receiver, the frequency source is considered as the reference frequency of the entire system, of which spectral purity, frequency accuracy, spurious levels directly affect the receiver's demodulation performance [3]. In recent years, with increasing applications of converged services, spectrum resources are increasingly crowded. In order to be able to modulate data to an accurate channel without interfering with adjacent channels, it requires that the frequency synthesizer can provide a reference for a broadband frequency source [4]. In addition, the diversity of applications makes the system increasingly large, which also provides a precise and stable frequency source to increase the difficulty [5]. Therefore, the design of wideband frequency synthesizer becomes more and more difficult.

Frequency synthesis technology originated in the 1930s, which has been widely used and developed in subsequent decades. Frequency synthesis is a reference source for stable, high-precision and low-phase noise of birds [6], and it is processed by signal processing such as frequency division, frequency multiplication and mixing to generate a large

number of signals with the same precision, which can provide smaller frequencies for modern communication system transceivers. According to the development history, the frequency synthesis technology can be divided into direct frequency synthesis, phase-locked frequency synthesis and direct digital synthesis technology [7].

Frequency coverage is one of the most important indicators of frequency synthesizer design. In recent years, with the rapid development of communication technology, the demand for wideband frequency synthesizers and higher frequency synthesizers has been increasingly increased [9]. Frequency resolution port is equipped with the ability to separate two adjacent peaks. In practice, the traditional direct frequency synthesis technology has a large frequency resolution, which is generally equal to the frequency of the reference source [10]. In addition, it is noted that owing to the fractional frequency division technique used in modern PLLs, the typical frequency resolution is less than 1 Hz [11]. The part II and part III describe the circuit design scheme of high performance frequency synthesizer in 31.25 MHz ∼8 GHz. The test results of the circuit are analyzed in the part IV. Finally, the conclusion of the research is expounded in part V.

Based on the aforementioned research background, this paper mainly studies the frequency synthesizer design in the broadband communication system. The subject stems from the network integration project, devoted to design the highly integrated frequency synthesizer to meet the demand of ''miniaturization''. Based on this target, this paper attempts to optimize the frequency synthesizer design to improve the circuit performances including the output frequency coverage, frequency resolution and other expansion.

TABLE 1. Main Indicators of triple play frequency synthesizer.

Parameters		Indicators
Frequency coverage		137.5 MHz ~ 4.4 GHz
Frequency step		200 kHz
Spurious performance		Better than -70 dBc
Phase noise	@1 kHz	Better than -85 dBc
	@10 kHz	Better than -90 dBc
	@100 kHz	Better than -90 dBc
	@1 MHz	Better than -120 dBc
Reference source		10 MHz

II. 137.5 MHZ∼4.4 GHZ FREQUENCY SYNTHESIZER DESIGN

In the triple play broadband communication system, the synthesizer is expected to meet the requirements of systematic application as shown in Table 1.

In this system application, it is expected to design a miniaturized frequency synthesizer subjected to the strict limits on receiver and transmitter size. Therefore, in terms of chip choice, other than the performance requirements to meet the system application needs, it also requires to choose integrated circuits, peripheral circuits and simple chips. To this end, the frequency synthesizer of PLL circuit is considered to use the highly integrated PLL chip ADF4350, which is built in three independent broadband VCO with a different VCO output fundamental frequency ranging from 2.2 GH ∼4.4 GHz. In the application of triple play ''miniaturized'' broadband frequency synthesizer design, the ADF4350 chip with the fundamental output frequency range of 2.2 GHz ∼4.4 GHz built in 16-division circuit can produce RF output as low as 137.5 MHz. In addition, by modifying the host computer software, the chip can directly generate different power output, of which the maximum output power is 5 dBm, the minimum power is −4dBm, and the power step value is 3 dBm

A. REFERENCE SOURCE SELECTION

In the application of the triple play project, the strict size requirement is proposed for the prototype machine used for communication (12cm ∗ 9cm), so the use of zero IF transceiver structure based on the requirements of each component size is expected to be as small as possible [12]. Therefore, in this communication system, the reference source of the frequency synthesizer is FOX Corporation product TCXO-FOX924. FOX924 temperature compensation crystal oscillator is equipped with the output frequency of 10 MHz, and a high degree of frequency stability, which can work in a smaller operating current drive, and therefore it is widely used in mobile communications systems.

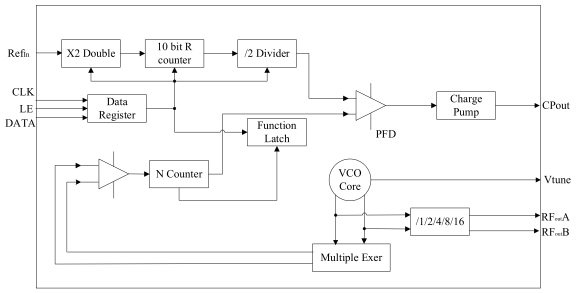

FIGURE 1. Functional block diagram of ADF4350.

B. CIRCUIT DESIGN AND ANALYSIS

In the application of triple-play ''miniaturized'' 137.5 MHz ∼4.4 GHz frequency synthesizer design, the highly integrated PLL chip ADF4350 is chosen. The chip RF output ranges from 137.5 MHz ∼4.4 GHz, which has many advantages such as low noise, low spurious performance, the ability to support for fractional frequency and low price, thus it is especially suitable for miniaturization circuit design. The functional block diagram of ADF4350 is shown in Figure 1.

The ADF4350 consists of a precision charge-dump, a low noise phase detector, a variable input reference divider, a programmable N-divider, three independent wideband VCOs, and an output programmable 16-divider [13]. Table 2 shows the main performance specifications of the ADF4350.

TABLE 2. The Main performance indicators of ADF4350.

Parameters	Indicators
Output frequency range	137.5 MHz ~ 4.4 GHz
Programmable output power	-4 dBm ~ 5 dBm
Maximum phase frequency	32 MHz
Dual-mode prescaler	Divide by 4/5 or Divide by 8/9
voltage	3.0V ~ 3.6V Supply Voltage
Divider mode	Support fractional and integer division
Remote phase noise	-140 dBc/Hz @1 MHz

The Phase Frequency Counter (PFD) accepts the inputs of the R and N counters, producing an output that is proportional to the phase and frequency difference. The PFD incorporates a fixed delay element to set backlash, backlash, and pulse width [14]. This pulse ensures no dead zone in the PFD transfer function, providing a consistent reference level [15].

The relationship of ADF4350 frequency synthesizer output frequency setting is:

$$RF_{out} = \left[INT + \frac{FRAC}{MOD}\right] \cdot f_{PFD} \tag{1}$$

Where RF_{out} is output frequency; INT is integer frequency division factor; $FRAC$ is decimal; MOD is modulus and f_{PFD} is phase detector frequency.

$$f_{PFD} = REF_{in} \cdot \frac{1+D}{R \cdot (1+T)} \tag{2}$$

Where RF_{in} is input reference frequency; D is input reference frequency multiplication factor; T is baseline two frequency division; R is RF reference frequency division factor.

Communication system applications are expected to satisfy the channel resolution requirements. For example, a UMTS system requires 2112.6 MHz frequency output, while providing 200 kHz channel resolution; the VCO frequency resolution is 400 kHz, and the use of l0 MHz temperature compensation crystal is most reference input conditions. The input reference is directly acted as the phase detector frequency, and the register configuration is calculated as follows:

$$MOD = \frac{REF_{in}}{f_{RES}} = \frac{10\text{MHz}}{400\text{kHz}} = 50 \tag{3}$$

In the ADF4350 register configuration design, it should be noted that the input reference can be directly used as the phase detector phase frequency while meeting the same channel resolution, and can also be used as the phase detector by inputting the reference frequency doubling. Then the corresponding modulo value MOD should be multiples of (1 + D), so that the theoretical phase noise can be improved by 3 dB under the same input reference and channel resolution.

C. PASSIVE LOOP FILTER DESIGN

Phase-locked loop design loop filter is a linear circuit composed of resistors, capacitors or operational amplifiers, which is a low-pass filter. Its role is to filter out the PLL circuit from the phase detector output voltage $V_D(t)$ in the frequency component and noise components, get a control voltage $V_C(t)$ to control the voltage-controlled oscillator frequency output [17]. Loop filters include an active loop filter and a passive loop filter that determines the form of the loop filter based on the phase-locked loop chip and voltage-controlled oscillator of choice. In this ADF4350 phase-locked loop design, the charge-system output voltage passes the passive loop filter directly as the VCO control voltage.

Loop filter main indicators include: loop bandwidth, lock time, DC gain, high-frequency gain and damping coefficient. Its parameters are based on the loop in the VCO gain, charge gain heart and phase detector phase ratio design [18]. The most important parameters in loop parameter design are the loop bandwidth, the loop bandwidth and the reference frequency, and the PFD is proportional to the phase noise of the LP loop. It is inversely proportional to the phase noise, lock time and resolution of the VCO.

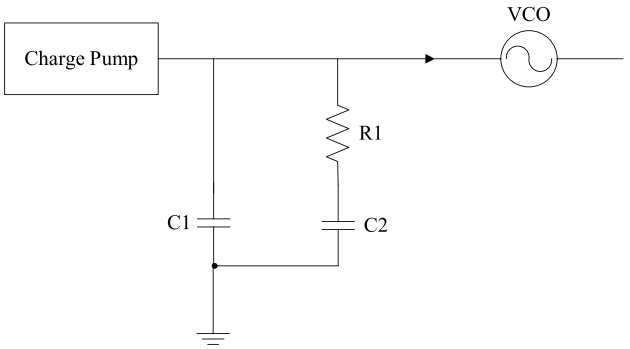

FIGURE 2. Passive Second order filter.

Passive loop filter topology. Passive second-order loop filter is the simplest application of loop filter, of which bridge structure is shown in Figure 2. The noise source introduced by the passive second-order loop filter usually comes from the resistor R2, and due to the simple transfer function of the second-order loop filter, it is convenient to design a smaller resistance value, thereby reducing the effect of the thermal resistance of the medium resistance on the total phase noise of the loop.

The impedance of the second-order passive loop filter can be calculated as:

$$\begin{cases} Z(s) = \dfrac{1+s \cdot T_2}{C_{tol} \cdot (1+s \cdot T_1)} \\ T_2 = R_2 \cdot C_2;\ T_1 = \frac{T_2}{C_{tol}};\ C_{tol} = C_1 + C_{t2} \end{cases} \tag{4}$$

The phase margin of PLL for second order passive loop filter can be calculated as:

$$\Phi = 180 + \arctan(2\pi \cdot f_C \cdot T_2) - \arctan(2\pi \cdot f_C \cdot T_1) \tag{5}$$

The third-order loop filter can better suppress the interference ripple more than tenfold of the loop bandwidth frequency by increasing the medium of the loop QCM, and

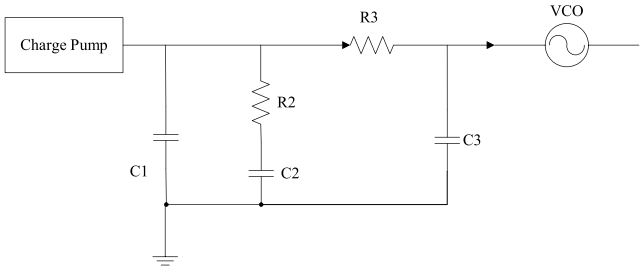

FIGURE 3. Passive third-order loop filter.

the basic topology of the third-order loop filter is as shown in Fig.3.

Different from the second-order loop filter, the component parameters of the third-order passive loop filter cannot be solved numerically. However, the loop parameters are still directly related to the time constant.

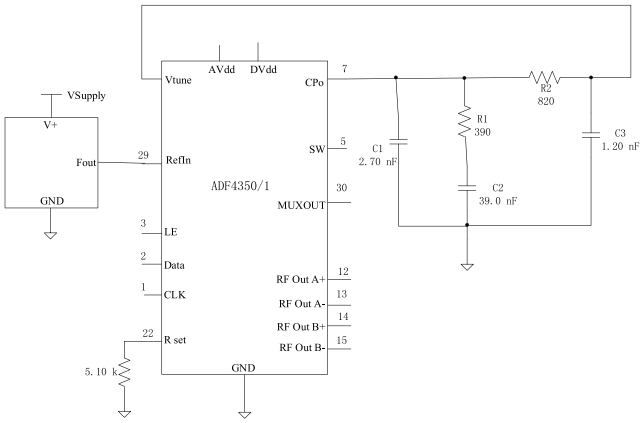

FIGURE 4. ADF4350 simulation circuit diagram.

ADIsimPL simulation software has a powerful simulation capabilities, which can be used for simulation design, fast and convenient, accurate and reasonable design of a stable loop filter, reducing the amount of computation in the design process, thus greatly improving the design efficiency. The third-order passive loop filter is used in this study, to obtain the simulation circuit as shown in Fig.4:

D. PC SOFTWARE AND CONTROL CIRCUIT DESIGN

In the frequency synthesizer design based on ADF4350, the interactive application software is divided into MFC host computer software and the lower computer hardware design based on C8051F320 single chip microcomputer. The adopted PC MFC software programming environment includes visual studio2010 and the C++ programming language. Based on the API application functions and the USB communication protocol to communicate with the microcontroller, the workflow is shown in the Fig.5.

PC software design. Host computer software refers to the computer that provides the service to send control instructions directly. In the design of frequency synthesizer from 137.5 MHz to 4.4 GHz, the host computer uses MFC

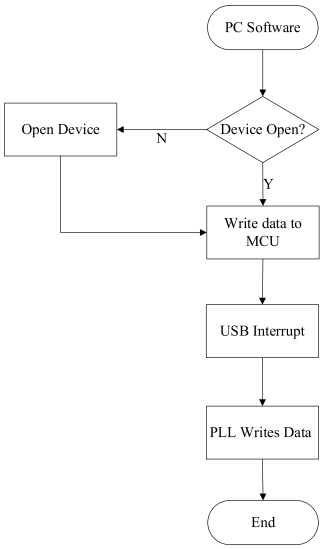

FIGURE 5. Interactive Application Design Flow Chart.

developed under Visual Studio 2010 programming environment, and mainly implements the following functions:

Reference Source Switching: Switching between internal 10MHz TCXO reference and external signal source reference via HMC544,

PLL Operating Modes: The ADF4350's optimal low noise and optimal low spurious mode selection can be achieved by setting the value of the ADF4350's internal registers.

Output Frequency Control: The ADF4350 fundamental output frequency range is 2.2 GHz ∼4.4 GHz, which can provide 137.5MHz minimum internal programmable output divider frequency output.

Output Power Control: The ADF4350 supports dual programmable power outputs that deliver −4 dBm, −1 dBm, 2 dBm and 5 dBm power levels for applications that require different power levels for good output matching.

Host computer application software is conducted as a control interface, and its important communication method is to call the Windows API function to meet the application requirements of real-time data transmission. The main working process of the host computer is presented as follows: in the initialization process, Windows firstly calls SI_Open () function to open the serial port and successfully open the handle. The user writes the control word such as frequency and power to the register setting function through the window response function. The register setting function sets the user set to convert the corresponding register value, the register value through SI_Write () write serial communication through the single chip. Once the data is written, the buffer would be empty, and the SI_Close() function would be implemented to close the operation handle to complete the host computer communication at the same time.

E. CONTROL CIRCUIT DESIGN

Control circuit design includes synthesizer control signal control design and lower computer design. In the frequency

synthesizer design, the lower computer is designed based on C8051F320 single chip microcomputer, which is a miniature on-chip system (Soc) with a 1K-sized USB buffer memory, and the instruction execution speed is up to 25 MIPS.

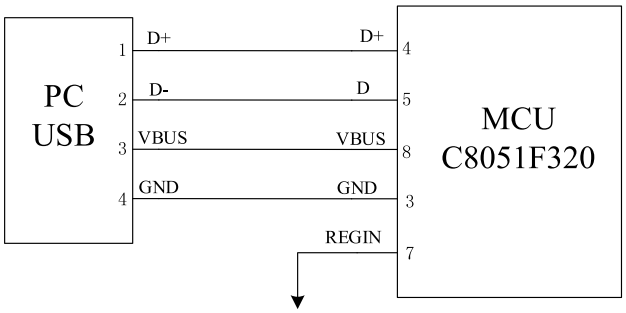

FIGURE 6. C8051F320 USB Communication Interface Design.

C8051F320 USB communication interface circuit design is shown in Figure 6, in which D + and D- is the data transfer pin; VBUS is the master (PC) and slave (microcontroller) status flag.

The process that the lower computer receives the data from the host computer is presented as follows: firstly, check the host computer sends the flag, and flag = 1 means that the host computer has sent data to the next bit machine, then turn off the USB interrupt into the microcontroller interrupt processing; and if MCU has completed the application function processing, the flag would be set to 0 to restart the USB interrupt, and then enter the new event loop. The process of receiving data from the next crew can be seen through a continuous cycle interrupt function to complete the host computer data in real time update operation.

The microcontroller pin output can generate PIX control signal to avoid the introduction of noise source due to the control line, and the control signal needs to be fully filtered in two ways: the majority of the noise signal can be filtered out based on RC filter network access control line; or the final output control signal can be generated through the AND gate, both of which can enhance the anti-interference ability of the control circuit.

III. 31.25 MHz~8 GHz FREQUENCY SYNTHESIZER DESIGN

In order to make up for the ''miniaturized'' performance of wideband frequency synthesizers, this chapter attempts to optimize the frequency synthesizer design. The frequency synthesizer HMC704 is used in the PLL basic module circuit, and the 10 MHz thermostatic oscillator OCXO is considered to be the system reference, and the basic frequency of 2 GHz ~4 GHz is generated through the PLL basic module. In the power control module, a digital attenuator and a gain amplifier are used to design a gain amplifier. The dynamic range of the broadband VCO output power is negotiated and switched by a 1 dB compression point switch with low insertion loss, which is

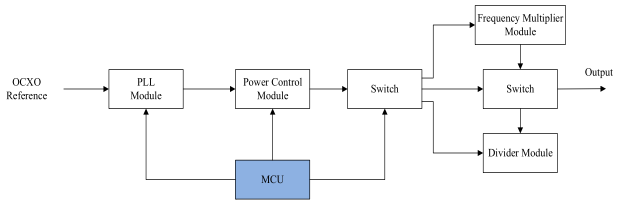

FIGURE 7. Frequency synthesizer design block Diagram Based on MHC704.

TABLE 3. Main indicators of crystal oscillator OCXO-023B [13].

Parameters	Indicators
Output frequency	10 MHz
Output waveform	Square wave
Output Power	13 dBm
Spurious clever system	Harmonic suppression is less than -50 dBc; Spurious suppression is less than -80 dBc
Power consumption	Start power is 5 W; Stable power consumption 2 W

acted as the input of the frequency expansion module. Frequency expansion module consists of two frequency divider circuits and a frequency multiplier circuit.

The frequency multiplier module selected in this study is the passive multiplier, of which input power requirement is 10 dBm~15dBm, and the output frequency is 4GHz~8GHz. In the frequency divider circuit, the low-noise active digital programmable divider is used. The single-stage divider ratio programmable cascaded /1, /2, /4, /8 divider circuit is considered to generate output frequency of 31.25 MHz~2 GHz, and the entire frequency synthesizer system can generate output frequency of 31.25 MHz~8 GHz. The overall system block diagram is shown in Figure 7.

A. REFERENCE SOURCE SELECTION

In 31.25 MHz ~8 GHz frequency synthesizer system design, the input reference as the only system frequency reference, its performance will directly determine the output performance of the entire system. At present, the crystal oscillator is widely used as a reference of a frequency source. According to the frequency control method and the temperature compensation method, the crystal oscillator is mainly divided into an ordinary crystal oscillator (SPXO), a temperature compensated crystal oscillator (TCXO), a voltage controlled crystal oscillator (VCXO) and temperature controlled crystal oscillator supply (OCXO).

SPXO has lower frequency stability and frequency accuracy, which lacks temperature control and temperature compensation measures and usually acts as a microprocessor clock device. VCXO through the external control voltage, the crystal oscillator output frequency control. TCXO through the application of temperature compensation circuit, which in terms of frequency stability than the average

quartz crystal oscillator 1-3 orders of magnitude, and has the advantages of small size, low power consumption, usually used in civil electronic equipment. VCXO in the broadband communication system has good frequency stability, usually used in satellite communications systems. The OCXO utilizes a thermostat to maintain the crystal oscillator temperature constant, greatly reducing the amount of frequency change due to temperature. OCXO has excellent performance in terms of slow aging rate, good temperature stability and high frequency accuracy, and is widely used as a precision reference source in microwave electronic instruments.

In the basic PLL loop design, HMC704 chip phase detector for the input reference input power 6dBm, phase detector operating frequency 0∼200 MHz, the required input reference slew rate greater than 0.5 V/ns. Considering the crystal oscillator performance, the 10 MHz crystal oscillator OCXO-023B is chosen, of which main indicators are presented as follows:

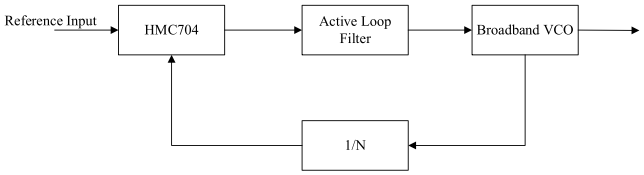

FIGURE 8. PLL Module Design Diagram.

B. PLL MODULE DESIGN

In the PLL module, the 10 MHz temperature crystal OCXO-023B is designed as a reference input, and the use of broadband VCO output frequency covering 1.9 GHz ∼4.1 GHz. The module includes a PLL chip HMC704, active loop filter, broadband VCO. The specific block diagram is shown in Figure 8.

PLL module is the frequency of the frequency synthesizer core module, and its output signal through the frequency expansion circuit, covering the entire frequency range; the output signal of the module performance indicators determine the output signal of the entire frequency synthesizer index. According to the final frequency synthetic indicators and programs, it is can be calculated that the PLL module can achieve the following indicators:

The output frequency coverage is guaranteed by the wideband VCO. The output frequency resolution is guaranteed by the PLL fractional-division mode of the PLL chip. The output near-phase noise is guaranteed by the reference source and the PLL chip. The far-end phase noise is guaranteed by the wideband VCO chip.

C. ACTIVE LOOP FITER DESIGN

In this scheme, the charge of HMC704 electric charge is 5 V and the wide-band VCO tuning voltage is up to 16 V, which is much higher than the output voltage of the charge system. Therefore, the design of the active loop filter circuit is required.

TABLE 4. Main indicators of PLL module [15].

Parameters	Indicators
Frequency Range	2 GHz ~ 4 GHz□□
Output Power	Greater than -10 dBm
Phase Noise	Better than -100 dBc/Hz @1 KHz; Better than -120 dBc/Hz @1 MHz
Spurious Suppression	Better than -70 dBc/Hz

According to the optimal design principle of the phase noise of the loop filter, choose the best loop bandwidth. To study the phase noise output by the PLL, we must consider the perturbation of the reference source, voltage-controlled oscillator, and phase detector introduced, and neglect the additional noise of the circuit which has little effect on the phase noise. Active filters are mainly simple gain type, standard feedback alternative to feedback network agencies. Active filter op-amp design, op amp noise performance parameters are many, but the most important two parameters are; voltage noise and current noise. Voltage noise refers to the voltage fluctuation at the output when the op amp input is shorted without any other noise.

Current noise refers to the current fluctuations at the output when the op amp input is open without any other noise. A typical indicator of amplifier noise is noise density. Voltage noise density unit is nV/JHz, and the current noise density unit is usually expressed as pv/JHz. These parameters can be found in the low noise op amp data sheet, and typically give values for two frequencies: one is flicker noise below 200 Hz and the other is noise within the 1 kHz passband. Based on the design considerations, the final choice of the TI op amp chip THS4041, the chip has a very low current noise and high speed of the conversion library to meet the design and application.

This design uses a standard feedback structure active loop filter, of which the circuit topology is shown in Figure 9:

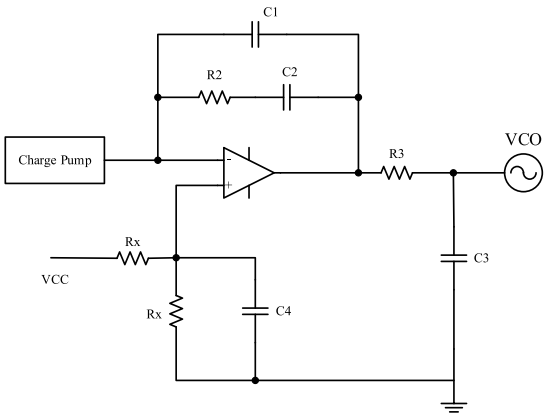

FIGURE 9. Standard feedback active loop filter.

In the standard feedback active filter structure, there will be a resistor R2 and capacitor C1 and capacitor C2 filter network is located in the op amp THS4031 feedback path, which can

achieve the low-pass filter loop function, in addition to the output of the op amp by A filter network consisting of resistor R3 and capacitor C3 further adds loop filtering.

Standard feedback active filter structure has smaller ripple noise, the role of the op-amp will be charged out of the compulsory output charge and charge Spring half, that is, through the Rx op amp in series the partial pressure of the input of the op amp. The voltage is set at half the charge-accumulated voltage. In the design, the small value of the decoupling resistor Rx will result in a large current consumption; a larger value of Rx will introduce additional resistance thermal noise, which can be shunted in parallel by a series resistor of Rx in series with a bypass capacitor Rc method to reduce the thermal noise generated by the resistance.

In the standard feedback active filter structure, there will be a resistor R2 and capacitor C1 and capacitor C2 filter network located in the op amp THS4031 feedback path, so that the loop can be achieved low-pass filtering, in addition, through the operational amplifier output increases The filter network consisting of resistor R3 and capacitor C3 further adds the filter function of the loop.

Standard feedback active filter structure with smaller ripple noise, the role of the op-amp will be charged out of the compulsory output charge and charge Spring half, that is, through the Rx op amp in series the partial pressure of the input of the op amp. The voltage is set at half the charge-accumulated voltage. In the design, the small value of the decoupling resistor Rx will result in large current consumption. The larger value of Rx will introduce additional thermal resistance noise, which can be bypassed in parallel with the Rx series resistor in the design Capacitance Rc method to reduce the thermal noise generated by the resistance.

The impedance of standard feedback active filter is calculated as follows:

$$Z(s) = \frac{1 + s \cdot T_2}{s \cdot C_x} \cdot \frac{-A}{(1 + s \cdot T_1) \cdot (1 + s \cdot T_3)} \tag{6}$$

The parameters of the loop filter can be uniquely determined by the time constant, while the time constant of the loop filter is determined by the loop bandwidth and the phase margin. This is consistent with the way of solving the parameter of the passive filter.

In the above standard feedback active power filter design, the solution of C_x is the key to solving the loop filter parameter. C_x can be solved by the open-loop gain in the loop bandwidth of 1 and the C_x is calculated as:

$$C_x = \frac{\kappa_d \cdot \kappa_{VCO} \cdot A}{\omega_n^2 \cdot T_1} \sqrt{\frac{1 + \omega_n^2 \cdot T_2}{\left(1 + \omega_n^2 \cdot T_1\right) \cdot \left(1 + \omega_n^2 \cdot T_3\right)}} \tag{7}$$

Where $T_1 \sim T_3$ is time constant; ω_n is inherent oscillation angle frequency; k_d and k_{VCO} are the gain of the phase detector and the VCO.

D. POWER CONTROL MODULE DESIGN

In the frequency synthesizer design, part of the output power of the VCO is pin-connected to the PLL RF input end to perform the phase-frequency detection and phase-demodulation operation through the network, and the other part is input as the frequency expansion module through the network. Because the flatness of the broadband VCO output power is relatively poor and the frequency expansion module circuit is sensitive to the input power level, careful gain control circuit design is needed between the output stage of the broadband VCO and the input stage of the frequency synthesizer module.

Gain control circuit design methods are mainly three under W: The first is by changing the transistor's static operating point to change the gain amplifier gain characteristics; the second is by changing the transistor AC operating conditions to change the gain characteristics; the third is to insert a programmable control attenuator in a fixed gain amplifier block to achieve gain control by controlling the amount of attenuation.

In the change of the transistor static operating point way to achieve a gain of smart circuit design, the detector can be taken from the output signal of a DC signal through the filter and the DC gain amplifier to generate a control voltage, thereby changing the controlled gain amplifier DC bias Set and work current, in order to achieve the amplifier gain control. This kind of gain control circuit is widely used ingenuity. The disadvantage is that the characteristic parameters of the transistor vary with the static operating point, which may cause problems such as output frequency offset, frequency band change and signal distortion. At the same time, this method of changing the static operating point of the transistor has a narrow range of gain control and is suitable for occasions with small dynamic range and high accuracy.

Change the exchange of working conditions to achieve the gain control circuit design, including changing the load resistance and change the feedback network in two ways. Because the amplifier's voltage gain is linear with the load impedance, changing the load impedance allows for amplified gain control. Fixed gain module into the attenuator to achieve gain control is the most commonly used gain control circuit design. Attenuators are usually electronic attenuator or programmable digital attenuator, which is the core device of the gain control circuit design. Controlled attenuator needs a larger attenuation variation range, stable input and output impedance, smaller insertion loss, flat frequency response, accurate gain step and so on. In this gain control circuit design, VCO output frequency coverage of 2∼4 GHz, the output power varies greatly with the frequency, so by inserting a controlled attenuator gain control is particularly suitable for such circuit applications.

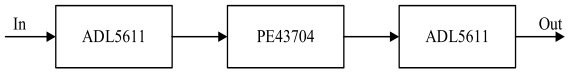

FIGURE 10. Gain control circuit design.

This circuit design uses two fixed-gain RF amplifier into a digital control attenuator way to achieve gain control, and the link design is shown in Figure 10.

In this study, the fixed gain amplifier is considered to be the ADI's dynamic module RF amplifier ADL5611, which is equipped with the operating frequency range of 30 MHz ∼6 GHz, the fixed gain of 22 dB, and the typical output of 1dB compression point.

E. FREQUENCY EXPANSION MODULE DESIGN

As a frequency expansion module input, the broadband VCO is adopted in gain control circuit, of which the output power of the dynamic range is 0∼15 dBm, and the output frequency coverage is 2-4 GHZ, which can also be divided into two signals: one signal is considered as the input of divider module and the another one is considered to be the input of double frequency module.

Multiplier circuit design. In 31.25 MHz ∼8 GHz frequency synthesizer design, the frequency multiplier circuit design is going through the gain control of the 2 GHz ∼4 GHz signal through the frequency multiplier output 4 GH ∼8 GHz. The fundamental theory of multiplier design is the non-linear effect of the circuit. By inputting the single tone signal, nonlinear components produce multiple harmonic components. The harmonic components are separated by the filter circuit to complete the frequency doubling operation. I follow the law of conservation of energy under the premise of I input signal power is assigned to the harmonic components, so there is a multiplier multiplier frequency multiplication. In the analysis of frequency multiplication circuit, the nonlinear transformation function is introduced / used to describe the nonlinear characteristic of frequency multiplier circuit, that is, the nonlinearity of frequency multiplier is expressed as:

$$i_o = f(v_i) \tag{8}$$

The Eq.(8) can be expanded in accordance with Taylor series expansion:

$$i_o = f(0) + f'(0) \cdot v_i + \frac{1}{2!} f''(0) \cdot v_i^2 + \frac{1}{3!} f'''(0) \cdot v_i^3 + \ldots \tag{9}$$

Where the input tone signal can be expressed as $v_i = A \cdot \cos(\omega_i \cdot t)$, and the Eq.(9) can be expressed as follows:

$$i_o = \left[f(0) + \frac{1}{4} \right] + f'(0) \cdot v_i + \frac{1}{2!} f''(0) \cdot v_i^2 + \frac{1}{3!} f'''(0) \cdot v_i^3 + \ldots \tag{10}$$

From Eq.(10), it can be seen that the output signal includes many harmonic components in addition to the DC component and the fundamental component after the input monophonic RF signal undergoes the nonlinear effect of the circuit. Frequency multiplier is based on the fundamental to achieve the desired (n) harmonic extraction, suppression of fundamental components, to achieve the purpose of frequency doubling. The ideal frequency doubler block diagram is shown in Figure.11.

FIGURE 11. Ideal frequency doubler block diagram.

In the signal phase noise analysis, it is known that when the monophonic signal is subjected to random modulation of phase and amplitude, it can be expressed by the following formula:

$$V_i = V_i \cdot [1 + \alpha(t)] \approx V_i \cdot \cos\omega_i + \alpha(t) \cdot V_i \cdot \cos(\omega_i t) - \varphi(t) \cdot V_i \cdot \sin(\omega_i t) \tag{11}$$

Where $V_i \cdot \cos\omega_i$ is the carrier voltage; $\alpha(t) \cdot V_i \cdot \cos(\omega_i t)$ is the degree of noise voltage, which can be used to measure the amplitude of the integrated power spectral density $S_\varphi(f)$; $V_i \cdot \sin(\omega_i t)$ is the phase noise voltage, which can be used unilateral integrated power spectrum density $S_N(f)$.

The phase noise introduced by $\varphi(t)$ can be expressed by the unilateral phase fluctuation power spectrum $S_\varphi(f)$, and the relationship between it and the baseband unilateral power spectral density is presented as follows:

$$S_\varphi(f) = \frac{1}{2} S_\varphi(\Delta f) \tag{12}$$

The phase noise of the frequency multiplier is directly related to the amplitude of the input signal. However, in an ideal frequency multiplier application, the influence of the amplitude and the phase fluctuation of the input signal on the entire frequency multiplier is small. The relationship between the output phase noise power spectral density of the frequency multiplier and the phase noise power spectral density of the input signal is presented as:

$$S_{\varphi^n}(f) = n^2 \cdot S_\varphi(f) \tag{13}$$

Divide circuit design. Frequency divider module input signal frequency coverage is 2 ∼4 GHz, the output frequency is divided into two bands, single-stage frequency divider circuit output frequency coverage of 250 MHz ∼2 GHz, two cascaded divider circuit output frequency coverage of 31.25 MHz ∼250 MHz, Typical output power −2dBm ∼3dBm.

By using a frequency-divided output, the phase noise at the same frequency offset has a 36dB improvement. We calculate that the output of the frequency synthesizer is dominated by the far-end phase noise of the VCO at −120 dBc/Hz@lMHz, The output phase noise at 31.25 MHz RF output is −156 dBc/Hz @lMHz. The analysis shows that to avoid noise introduced by the divider's base noise, the divider's base noise is at least −156 dBc/Hz@1 MHz. Therefore, in the choice of divider, in addition to frequency coverage, another important indicator is the divider's base noise

After the crossover frequency and output performance comparison, the final choice of divider HMC862.

TABLE 5. HMC862 Division ratio truth table.

S0	S1	S2	Divide Ratio
0	0	0	1
1	0	0	2
1	1	0	4
1	1	1	8`

0=Logical low level; 1=Logical high level

HMC862 operating frequency coverage of 100 MHz ∼15 GHz, the input RF power −10 dBm ∼10 dBm, frequency division output power −2 dBm ∼ 3 dBm. The frequency divider uses H terminal 3 ∼ 5 V CMOS control level, the frequency division ratio is 1, 2, 4 and 8. The HMC8 beat frequency output logic control truth table as shown in Table 5.

IV. TEST RESULTS AND ANALYSIS

The basic PLL is the key to the frequency synthesizer design. As the reference source of the frequency synthesizer, its performance will directly determine the performance of the entire frequency synthesizer. In this chapter, the detailed output tests would be conducted based on the ADF4350 integrated phase-locked loop design and the HMC704 phase-locked loop design.

A. 137.5 MHZ∼ 4.4 GHZ FREQUENCY SYNTHESIZER TEST RESULTS

The ADF4350 basic loop output frequency ranges from 2.2 GHz–4.4 GHz, based on the built-in frequency divider output as low as 137.5 MHz. Figure 12(a) shows the ADF4350 output phase measurement results at the frequency of 2.4 GHz; Figure 12(b) gives the ADF4350 output phase noise measurements a at the frequency of 1.2 GHz through the built-in divider.

Owing to the poor accuracy and phase noise of TCXO crystal used in the circuit system, the output phase noise has a certain gap compared with the data sheet. From the test results, it can be seen that the phase noise at the output frequency of 2.4 GHz is about −84.9 dBc/Hz@1kHz, −93.1dBc/Hz@10kHz, −105.5dBc/Hz@100kHz, −135dBc/Hz @lMHz, and it can be concluded that the spurious performance has been effectively suppressed due to the low spurious integer division mode. From the test results, it can be seen that compared with the phase noise results at frequency of 2.4 GHz, the latter basically meets the relationship of 6dB difference.

Table 6 and Table 7 show the other frequency and crossover test results. It can be seen from the table test results that in the ADF4350 fundamental output frequency band of 2.2 GHz ∼4.4 GHz, the phase noise at the frequency offset of 1KHz is about −85 dBc/Hz, the phase noise at the frequency offset of 10kHz is about −90 dBc/Hz, and the phase noise at 100kHz is about −103 dBc/Hz. As a result, it concludes that the phase noise performance would worsen less as frequency increases, which can meet the local oscillator phase noise requirements for broadband wireless communication systems.

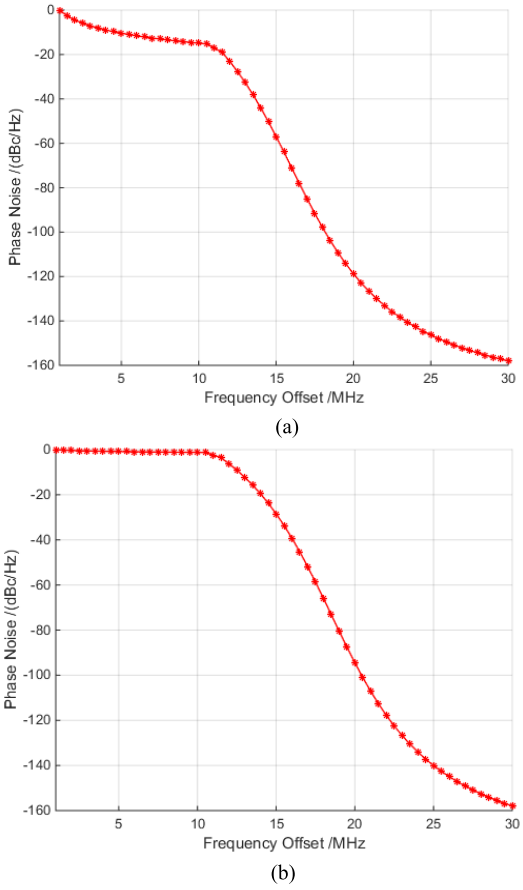

FIGURE 12. ADF4350 frequency synthesizer output test. a) Phase noise measurement results @2.4 GHz. b) phase noise measurement results @1.2 GHz.

TABLE 6. Phase noise test results at fundamental wave of 3.3GHz.

Frequency\Frequency Deviation	@l KHz(dBc/Hz)	@l0 KHz(dBc/Hz)	@l00 KHz(dBc/Hz)
Fundamental wave (3300MHz)	-85.2	-89.8	-103.1
Two divided-frequency (1650 MHz)	-91.1	-96.1	-109.4
Four divided-frequency (825 MHz)	-95.3	-102.1	-116.2
Eight divided-frequency (421.5 MHz)	-103.5	-108.9	-121.5

B. 31.25 MHz∼8 GHz FREQUENCY SYNTHESIZER TEST RESULTS

Based on the HMC704 frequency synthesis design, the basic loop output frequency range is 2 GHz ∼4 GHz, and the output phase noise measurement results at output frequency of 2.5 GHz and 3.5 GHz are shown in Figure 13.

TABLE 7. Phase noise test results at fundamental wave of 4 GHz.

Frequency\Frequency Deviation	@1 KHz(dBc/Hz)	@10 KHz(dBc/Hz)	@100 KHz(dBc/Hz)
Fundamental wave (4000MHz)	-84.7	-88.9	-103.3
Two divided-frequency (2000 MHz)	-90.5	-94.4	-111.6
Four divided-frequency (1000 MHz)	-95.1	-99.3	-116.7
Eight divided-frequency (500 MHz)	-101.5	-105.7	-121.2

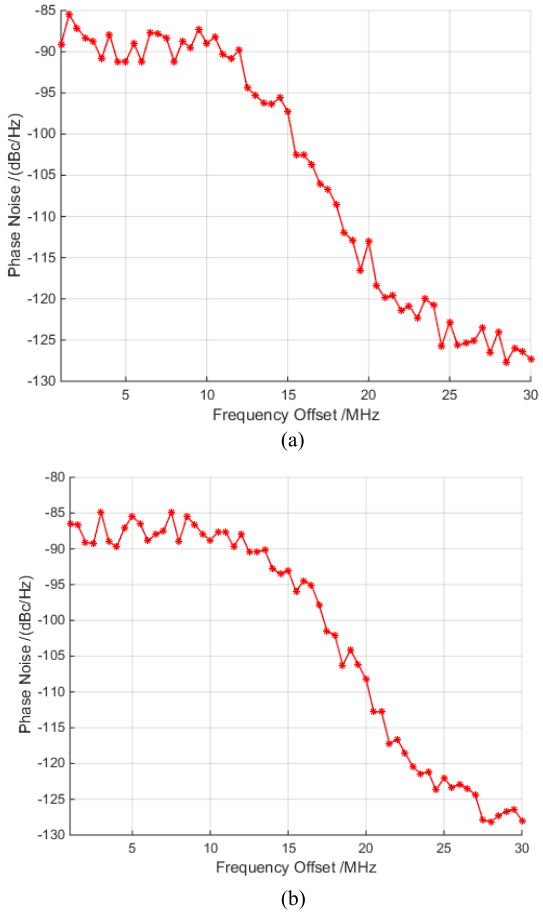

FIGURE 13. Single-stage frequency division circuit output test. a) phase noise ,measurement results @2.5 GHz. b) phase noise measurement results @3.5 GHz.

The results of the frequency synthesizer basic loop output test show that the typical phase noise at the output frequency of 2.5GHz is: −96.8 dBc/Hz@100Hz, −104.8 dBc/Hz@lkHZ, −106 dBc/Hz@10kHz, −127.8 dBc/Hz@lMHz; The typical output phase noise at the output frequency of 3.5GHz is: −93.3 dBc/Hz@100Hz, −102.2 dBc/Hz@1kHz, −102.3 dBc/Hz @10kHz, −124.8 dBc/Hz@1MHz. The basic loop output frequency

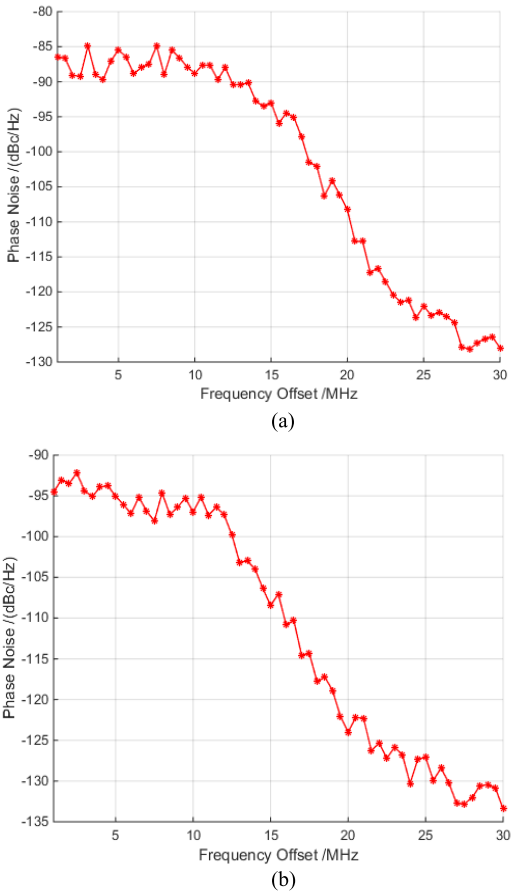

FIGURE 14. Double-stage frequency division circuit output test. a) phase noise measurement results @5 GHz. b) phase noise ,measurement results @7 GHz.

range is 2 GHz ∼4 GHz. Through the gain control circuit, the input power is adjusted to 13dBm, and the frequency multiplication output frequency coverage is set to 4GHz∼8GHz. In order to facilitate the analysis and comparison, the basic loop output test frequency points of 5GHz and 7GHz are selected, to obtain the output test results as shown in Figure 14.

The detailed test results of the crossover circuit are shown in Table 8 and Table 9. The results show that the phase synthesizer output phase noise meets the 6 dB attenuation relationship with the doubled frequency.

C. TEST RESULTS ANALYSIS

Based on the above two kinds of measurement results, it can be seen that in the phase-locked loop frequency synthesizer design based on ADF4350, the phase noise at the frequency of 1GHz is −95.5 dBc/Hz @ 1 KHz, −95.5 dBc/Hz @ 10 KHz, −116.7 dBc/Hz @ 100 KHz, −142.5 dBc/Hz @ 1 MHz. In the design of the HMC704 frequency-based integrator, the 1GHz phase noise output from the divider is −102.01dBc/Hz@ 100 Hz, −114.01 dBc/Hz@1 KHz, −115.35 dBc/Hz@10K Hz, −112.00 dBc/Hz@100 KHz, −131.29 dBc/Hz@1 MHz. Each of aforementioned designs

TABLE 8. Single-stage frequency division circuit phase noise test results.

Frequency\ Frequency Deviation	@l00 Hz (dBc/Hz)	@l KHz (dBc/Hz)	@l0KHz (dBc/Hz)	@lMHz (dBc/Hz)
1500 MHz	-100.58	-109.7	-110.63	-134.7
750 MHz	-107.46	-115.53	-116.43	-140.14
375 MHz	-111.93	-120.89	-122.33	-145.05

TABLE 9. Double-stage frequency division circuit phase noise test results.

Frequency\ Frequency Deviation	@l00 Hz (dBc/Hz)	@l KHz (dBc/Hz)	@l0KHz (dBc/Hz)	@lMHz (dBc/Hz)
125 MHz	-125.7	-131.1	-132.9	-148.2
62.5 MHz	-129.6	-136.9	-138.6	-151.6
31.25MHz	-137.25	-143.8	-146.4	-158.6

has its advantages and disadvantages in terms of performance of frequency coverage, near-end phase noise and far-end phase noise, and the specific analysis is presented as follows:

Frequency coverage. In the design of the frequency synthesizer based on the ADF4350, the internal frequency division output frequency is programmed to cover a frequency range of 137.5 MHz to 4.4 GHz, of which the maximum output power is 5 MHz. Based on the HMC704 frequency synthesizer design, the frequency expansion module circuit output frequency coverage is 31.25 MHZ∼8 GHZ.

Near-end phase noise: Near-end phase noise is primarily determined by the phase detector, reference source, N-divider and loop filter performance. On the one hand, the ADF4350 frequency synthesizer design is subjected to the strict size constraints on the circuit, reference source selection, and the temperature stability of the crystal oscillator OCXO. On the other hand, the normalized substrate phase noise level of ADF4350 chip is higher than that of HMC704 chip. As a result, it can be seen that the near-end phase noise in the HMC704 frequency synthesizer design is much better than that based on the ADF4350 frequency synthesizer device design.

V. CONCLUSION

As the frequency reference of electronic system, the frequency source is an important part of modern transceivers, and the development of the frequency synthesizer is inevitably faced with many new challenges. In this paper, the frequency synthesizer technology in broadband wireless communication system is studied, involved with the frequency synthesizer design and implementation.

First of all, in view of the demand of miniaturization module of ''triple play'', the frequency synthesizer design based on on-chip integrated VCO phase-locked loop chip was implemented. In this study, the frequency coverage of PLL frequency divider is considered as 137.5 MHz ∼4.4 GHz, and the PLL module design, passive filter design and topology of passive filter are analyzed in detail.

Secondly, in order to make up for the lack of miniaturized frequency synthesizer performance in the ''triple play'' system, the article optimizes the design of the wideband frequency synthesizer, where the optimized broadband frequency synthesizer is acted as the PLL basic phase-locked loop output, which is also the frequency expansion module input through the power control circuit. In this section, the frequency expansion module is divided into frequency divider module and frequency multiplier module, of which output frequency range is 31.25 MHz ∼8 GHz, and the theoretical frequency resolution is 0.6 Hz through the use of fractional divider.

Finally, the frequency synthesizer designed based on ADF4350 and the design scheme based on HMC704 frequency synthesizer were tested and analyzed. The test results show that the design of highly integrated VCO ADF4350 with the output frequency range of 137.5 MHz ∼4.4 GHz is less demanding on the circuit size restrictions. However, based on the HMC704 program, the performances of designed synthesizer including design complexity, frequency output coverage, frequency resolution and phase noise are better than the frequency synthesizer designed on ADF4350. As a result, the detailed comparing analysis made for advantages and disadvantage between the two schemes is conducted at the end of this chapter, to provide a reference for the subsequent circuit designers.

REFERENCES

[1] S.-J. Han, A. V. Garcia, S. Oida, K. A. Jenkins, and W. Haensch, ''Graphene radio frequency receiver integrated circuit,'' *Nature Commun.*, vol. 5, Jan. 2014, Art. no. 3086.
[2] Z. Zhang, Y. Xu, J. Yang, X. Li, and D. Zhang, ''A survey of sparse representation: Algorithms and applications,'' *IEEE Access*, vol. 3, pp. 490–530, 2015.
[3] A. Sanne *et al.*, ''Radio frequency transistors and circuits based on CVD MoS_2,'' *Nano Lett.*, vol. 15, no. 8, pp. 5039–5045, 2015.
[4] P. Ghelfi *et al.*, ''A fully photonics-based coherent radar system,'' *Nature*, vol. 507, no. 7492, pp. 341–345, Mar. 2014.
[5] H. Liu *et al.*, ''Phosphorene: An unexplored 2D semiconductor with a high hole mobility,'' vol. 8, no. 4, pp. 4033–4041, 2014.
[6] G. W. Burr *et al.*, ''Experimental demonstration and tolerancing of a large-scale neural network (165 000 synapses) using phase-change memory as the synaptic weight element,'' *IEEE Trans. Electron Devices*, vol. 62, no. 11, pp. 3498–3507, Nov. 2015.
[7] A. H. M. Shirazi *et al.*, ''On the design of mm-Wave self-mixing-VCO architecture for high tuning-range and low phase noise,'' *IEEE J. Solid-State Circuits*, vol. 51, no. 5, pp. 1210–1222, May 2016.
[8] G. Fiori *et al.*, ''Electronics based on two-dimensional materials,'' *Nature Nanotechnol.*, vol. 9, pp. 768–779, Oct. 2014.
[9] C. Venerus and I. Galton, ''A TDC-free mostly-digital FDC-PLL frequency synthesizer with a 2.8-3.5 GHz DCO,'' *IEEE J. Solid-State Circuits*, vol. 50, no. 2, pp. 450–463, Feb. 2015.
[10] W.-J. Yu *et al.*, ''Differential evolution with two-level parameter adaptation,'' *IEEE Trans. Cybern.*, vol. 44, no. 7, pp. 1080–1099, Jul. 2014.
[11] D. Puiu *et al.*, ''CityPulse: Large scale data analytics framework for smart cities,'' *IEEE Access*, vol. 4, pp. 1086–1108, 2016.
[12] J. Wang *et al.*, ''Reconfigurable radio-frequency arbitrary waveforms synthesized in a silicon photonic chip,'' *Nature Commun.*, vol. 6, Jan. 2015, Art. no. 5957.

[13] A. Sajid, H. Abbas, and K. Saleem, "Cloud-assisted IoT-based SCADA systems security: A review of the state of the art and future challenges," *IEEE Access*, vol. 4, pp. 1375–1384, 2016.
[14] K. Raczkowski, N. Markulic, B. Hershberg, and J. Craninckx, "A 9.2–12.7 GHz wideband fractional-N subsampling PLL in 28 nm CMOS with 280 fs RMS jitter," *IEEE J. Solid-State Circuits*, vol. 50, no. 5, pp. 1203–1213, May 2015.
[15] Y. Wu et al., "200 GHz maximum oscillation frequency in CVD graphene radio frequency transistors," *ACS Appl. Mater. Interfaces*, vol. 8, no. 39, pp. 25645–25649, Sep. 2016.
[16] D. Akinwande, N. Petrone, and J. Hone, "Two-dimensional flexible nanoelectronics," *Nature Commun.*, vol. 5, Dec. 2014, Art. no. 5678.
[17] F. S. Stinner *et al.*, "Flexible, high-speed CdSe nanocrystal integrated circuits," *Nano Lett.*, vol. 15, no. 10, pp. 7155–7160, 2015.
[18] Y. Sun, H. Song, A. J. Jara, and R. Bie, "Internet of Things and big data analytics for smart and connected communities," *IEEE Access*, vol. 4, pp. 766–773, 2016.

ZHANG WEIJIA was born in Binhai New Area, Tianjin, China, in 1984. He received the B.S. and M.S. degrees in physical electronics from the Hebei University of Technology, Tianjin, in 2007 and 2010, respectively. He is currently pursuing the Ph.D. degree in microelectronics and solid-state electronics with Tianjin University, Tianjin.

Since 2013, he has been a Lecturer with the College of Electronic Information and Automation, Tianjin University of Science and Technology. He has authored one book and over three patents. He participates in several research projects in the field of information technology. His research interests include RFIC design, communication system design, electromagnetic fields and microwaves, and microwave photonics.