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Active DC Link Capacitance Reduction in Grid-Connected Power Conversion Systems by Direct Voltage Regulation

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ABSTRACT In this paper, an unconventional method of dc link bulk capacitance active reduction without ripple increase in mains-connected power conversion systems is proposed. Even though the adopted power circuitry (a bidirectional dc–dc converter, terminated by a much smaller capacitance) is analogous to solutions proposed up to date, the concept of operation is quite different. Rather than controlling the current, flowing into the dc link (i.e., operating as a current controlled current sink, similarly to an active power filter), suggested solution regulates the ripple by controlling the dc link voltage (i.e., operating as a voltage controlled current sink) thus letting the grid-interfacing converter OFF the task. This allows widening of the dc link voltage loop bandwidth and, as a result, reducing the ripple for the same capacitance utilized or reducing the capacitance while maintaining the same ripple without trading off the power factor. In order to validate the proposed methodology experimentally, it is successfully applied to a single-phase off-the-shelf power factor correction pre-converter.

INDEX TERMS Mains-interfacing power converters, dc link capacitance reduction, control systems.

NOMENCLATURE

$v_1(t)$	instantaneous grid voltage;
$i_1(t)$	instantaneous grid current;
$p_1(t)$	instantaneous grid power;
$v_x(t)$	instantaneous load-side voltage of x-th converter;
$i_x(t)$	instantaneous load-side current of x-th converter;
$p_x(t)$	instantaneous power of x-th converter;
P_x	average power of x-th converter;
$\Delta p_x(t)$	instantaneous zero-average pulsating power component of x-th converter;
$v_{DC}(t)$	instantaneous DC link voltage;
$v_{DC}^{ss}(t)$	instantaneous DC link voltage in steady state;
V_{DC}	DC link voltage set point;
$\Delta v_{DC}(t)$	instantaneous DC link voltage ripple;
v_{DC}^{MAX}	upper instantaneous DC link voltage limit in steady state;
v_{DC}^{MIN}	lower instantaneous DC link voltage limit in steady state;
$P_{CB}(t)$	instantaneous DC link power;
$p_{CB}^{ss}(t)$	instantaneous DC link power in steady state;
C_B	bulk DC link capacitance;
$v_A(t)$	instantaneous auxiliary capacitor voltage;
$v_A^{ss}(t)$	instantaneous auxiliary capacitor voltage in steady state;
V_A	auxiliary capacitor voltage set point;
$\Delta v_{DC}(t)$	instantaneous auxiliary capacitor voltage ripple;
v_A^{MAX}	upper instantaneous auxiliary capacitor voltage limit in steady state;
v_A^{MIN}	lower instantaneous auxiliary capacitor voltage limit in steady state;
C_A	auxiliary DC link capacitance;

I. INTRODUCTION

In order to meet tight power quality requirements of modern mains codes, grid-connected converters exchange current with predetermined shapes with the utility [1], [2]. This forces the instantaneous grid power to contain both DC and pulsating components. In general, instantaneous power with similar decomposition flows through all terminals of the power conversion system. In order to preserve energy balance, instantaneous power DC components sum up to zero in steady state. On the other hand, pulsating power constituents differ according to functionality of each source/load, connected to the power conversion system. Therefore, pulsating power balancing component is needed to cope with the nonzero sum of all pulsating components. Bulk capacitor, connected across the DC link of the power conversion system is typically utilized for this purpose stages [3]. Pulsating power flow component creates DC link voltage ripple, directly related to the power conversion system rating and inversely related to the value of the bulk capacitance. DC link ripple should remain between determined limits, usually dictated by both power conversion system functionality and voltage rating of the bulk capacitor. As a result, electrolytic capacitors are typically utilized in systems rated above several tens of watts. Regrettably, widely recognized reliability problems associated with electrolytic capacitors [4], [5] in addition to significant weight and volume [6], [7] often become system bottleneck.

Numerous approaches intended to cure the above-mentioned shortcomings were suggested in the literature. In [8], a passive solution was proposed by the authors. There, an properly tuned resonant filter formed by a series connected capacitor-inductor combination, placed across the DC link, was shown to be capable of suppressing the pulsating power constituent. Nevertheless, comparatively low base frequency of the grid yields a bulky resonant filter. Moreover, in case multiple grid-frequency pulsating power components exist, the system requires a capacitor-inductor couple for each significant frequency. In addition, capacitor voltage drop may be higher than the DC-link voltage (depending on the filter quality factor), calling for increased voltage rating of the capacitor.

DC link capacitance reduction was achieved in [9] and [10] by distorting the input current while pushing the power factor from near towards the lowermost tolerable bound. Nevertheless, apart from being cumbersome and computationally demanding, adding harmonic content to mains current may be potentially incompatible with grid codes. Hence, the solution cannot be considered universal. Moreover, the resultant capacitance reduction is relatively insignificant.

A group of active capacitance reduction approaches allowing to emulate large capacitance with a much smaller one [11], [12] utilizes controlled converter based circuits to keep the ripple of the DC link voltage within the desired limits [13]–[23]. It may be divided into two main subgroups: topology integrated or additional hardware enhanced [13]. The former subgroup [14]–[16] consists of topologies specially designed to cope with the pulsating power components (mainly differentially). In the latter subcategory [17]–[23], active energy buffer is added to existing topologies. The principle of the second subgroup operation is based on the following observation: the energy required to achieve pulsating power matching is actually a small fraction of the total energy stored in the bulk capacitor. Consequently, significantly lower capacitance may be sufficient to cope with the pulsating power constituent. Hence, high capacitance value is mainly necessary to satisfy the tight DC link ripple requirements. Consequently, decoupling energy and ripple requirements would allow releasing bulk capacitor from ripple limitation constraints thus reducing its value considerably. This may be accomplished by decoupling the power matching capacitance and the DC link by a bidirectional power converter. The auxiliary converter-capacitor unit may be inserted either in parallel to the DC link [14]–[23] or in series with it [24]. While the parallel-connected units operate similarly to active power filters (minimizing the DC link capacitor current), series-connected units operate similarly to voltage compensators (creating voltage opposite-phase to DC link ripple).

The method proposed in the paper belongs to parallel-connected active solutions group. Even though the adopted power circuitry is analogous to solutions proposed up to date, the concept of operation is quite different. Instead of drawing the pulsating DC link current component into the auxiliary circuit by first measuring all the currents flowing into the DC link and then extracting the non-DC part (as performed by typical solutions), the proposed system attains the same result by directly regulating the DC link voltage. No information regarding any of the DC link currents is therefore required. As a result, the auxiliary circuit resembles a voltage rather than current controlled current sink from the DC link point of view. On the other hand, the following drawback appears: once the auxiliary unit gains control over the DC link voltage, the latter no longer serves as the system power balance indicator. Grid-interfacing converters typically use average value of the DC link voltage to determine the magnitude of active current component drawn from the grid and consequently set the amount of active power drawn/injected from/to the grid. This creates coupling between input power factor and DC link voltage quality (it is well known that voltage loop crossover frequency of grid interfacing converters should be kept well below the double-base-frequency in order to preserve a predetermined shape of the input current [3]). However, the pulsating power component as well as any other input-output power mismatch are shifted to the auxiliary capacitance in the proposed solution; the above-mentioned shortcoming is cured by utilizing the average value of the voltage across auxiliary capacitor (rather than that of the DC link voltage) to the power-balancing controller. This action also eliminates the trade-off between the input power factor and DC link voltage quality. This is because the power balancing controller no longer regulates the DC link voltage, which is a significant advantage. Thus, magnitude of the DC link ripple becomes

reliant solely on control capabilities of the auxiliary unit, limited by switching / sampling frequency and the control approach utilized.

To conclude, the main contribution of the manuscript is introducing direct voltage DC regulation concept, allowing DC link capacitance reduction without any DC link current sensing as an alternative to the commonly adopted active-power-filter-like operation, requiring multiple invasive current sensing.

II. PULSATING POWER MISMATCH PROBLEM

A common mains-connected power conversion system, consisting of a grid interfacing converter (GIC) and N downstream converters (DSC_1– DSC_N), is shown in Fig. 1.

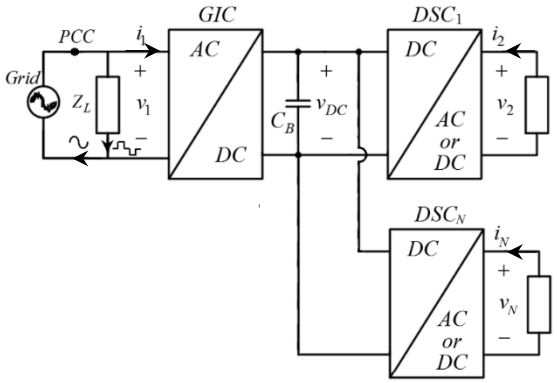

FIGURE 1. Generalized grid-connected power conversion system.

The grid voltage may be distorted in general, given by

$$v_1(t) = V_{10} + \sum_{n=1}^{\infty} V_{1n} \sin(n\omega_1 t + \theta_{1n}). \tag{1}$$

Moreover, GIC may be utilized as either active power filter or reactive power compensator, connected parallel with a local load Z_L in order to correct the power factor at the point of common connection (PCC). Thus, GIC current may be distorted as well, given by

$$i_1(t) = I_{10} + \sum_{n=1}^{\infty} I_{1n} \sin(n\omega_1 t + \varphi_{1n}). \tag{2}$$

Likewise, voltage and current of the downstream converters (DSC_x) terminals may be generally described by

$$\begin{aligned} v_x(t) &= V_{x0} + \sum_{n=1}^{\infty} V_{xn} \sin(n\omega_x t + \theta_{xn}) \\ i_x(t) &= I_{x0} + \sum_{n=1}^{\infty} I_{xn} \sin(n\omega_x t + \varphi_{xn}) \end{aligned} \tag{3}$$

with $x = 2 \ldots N$. Instantaneous terminals and DC link power (valid for either direction of power flow) are given by

$$p'_x(t) = v_x(t) i_x(t) = P'_x + \Delta p'_x(t) \tag{4}$$

and

$$p_{CB}(t) = p'_1(t)\eta_1 + \sum_{x=2}^{N} p'_x(t)\eta_x^{-1} = \sum_{x=1}^{N} P_x + \sum_{x=1}^{N} \Delta p_x(t), \tag{5}$$

respectively, as shown in Fig. 2 with η_1 and η_x denoting GIC and DSC_x efficiencies, respectively. Typically, GIC voltage regulator performs system active power balancing (i.e. $\sum_{x=1}^{N} P_x = 0$ holds in steady state) by forcing the DC link voltage average value to follow a predetermined set point V_{DC}.

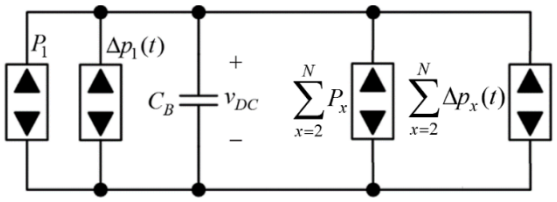

FIGURE 2. DC Link power level diagram.

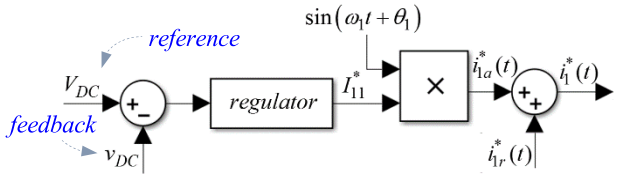

FIGURE 3. Typical GIC voltage control structure for sinusoidal grid voltage with i^*_{1a} and i^*_{1r} symbolizing active and reactive reference current components (the latter is determined by dedicated control loop).

GIC voltage control structure for a particular yet common case of sinusoidal grid voltage (i.e. $V_{10} = 0$ and $V_{1n} = 0$, $n > 1$ in (1)) is given in Fig. 3, where $i^*_1(t)$ is the reference input to the current control structure. Note that DC link voltage loop crossover frequency ω^v_{CO} must satisfy

$$\omega^v_{CO} << \min(2\omega_x),\ x = 1 \ldots N \tag{6}$$

to leave the frequency content of pulsating power components beyond GIC voltage loop bandwidth thus avoiding grid current distortion [3]. Consequently, steady state instantaneous power of the DC link capacitor is

$$p^{ss}_{CB}(t) = \sum_{x=1}^{N} \Delta p_x(t). \tag{7}$$

Steady-state value of the DC link voltage is hence given by

$$v^{ss}_{DC}(t) \approx V_{DC} + \underbrace{\frac{1}{C_B V_{DC}} \int_0^t \sum_{x=1}^{N} \Delta p_x(\tau) d\tau}_{\Delta v_{DC}(t)} \tag{8}$$

under small ripple assumption ($\Delta v_{DC}(t) \ll V_{DC}$). Since (7) denotes a zero-average finite-energy signal, instantaneous

DC link voltage resides in steady state within the following bounds,

$$V_{DC} + \min(\Delta v_{DC}) < v_{DC}^{ss}(t) < V_{DC} + \max(\Delta v_{DC}). \quad (9)$$

Observing (8), DC link voltage ripple is inversely related to DC link capacitance and average voltage values. In single-phase applications, V_{DC} is constant (380V – 400V) and typical allowed ripple is 1-2% of V_{DC}, i.e. C_B is the only design variable affecting DC link instantaneous voltage bounds. In case minimum and maximum allowed values of the DC link voltage ripple value in steady state are denoted as Δv_{DC}^{MIN} and Δv_{DC}^{MAX}, respectively, the required capacitance is determined from

$$C_B = \frac{1}{V_{DC}} \max \left(\frac{\max\limits_t \sum\limits_{x=1}^{N} \Delta p_x(t)}{\Delta v_{DC}^{MAX}}, \frac{\min\limits_t \sum\limits_{x=1}^{N} \Delta p_x(t)}{\Delta v_{DC}^{MIN}} \right). \quad (10)$$

Hence, electrolytic capacitors are typically utilized in systems rated above several tens of watts due to of physical size and price restrictions.

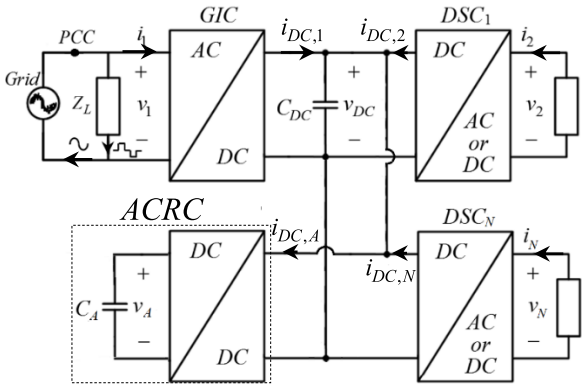

FIGURE 4. Replacing bulk DC link capacitance by ACRC.

III. ACTIVE CAPACITANCE REDUCTION

A. GENERAL CONCEPT

The idea behind parallel-connected active capacitance reduction circuits (ACRC) is eliminating the coupling between the capacitance and voltage ripple, given by (8). Note that steady-state bulk DC link capacitance energy utilization is around 6%; hence much lower capacitance may be used once the above mention coupling is eliminated. Thus, a DC-DC converter terminated by an auxiliary power-matching capacitance C_A substitutes the bulk capacitor C_B, as shown in Fig. 4, i.e. DC link and power-matching device are now decoupled while the pulsating power component (7) is transferred to the auxiliary capacitance C_A. In practice, small capacitance C_{DC} should remain connected across the DC link in order to absorb switching-frequency-current-components generated by power conversion system operation and cope with high frequency residuals of pulsating power component, residing beyond ACRC control system bandwidth. Denoting the part of pulsating power constituent (in frequency domain) processed by the ACRC as

$$\Delta p_A(\omega) = T(\omega) \sum_{x=1}^{N} \Delta p_x(\omega) \quad (11)$$

with $T(\omega)$ denoting the complimentary sensitivity function of ACRC control loop, then capacitor C_{DC} has to cope with

$$\Delta p_{DC}(\omega) = (1 - T(\omega)) \sum_{x=1}^{N} \Delta p_x(\omega). \quad (12)$$

Once C_A absorbs the pulsating power component (11), corresponding steady-state voltage may be described by

$$v_A^{ss}(t) \approx V_A + \underbrace{\frac{1}{C_A V_A} \int_0^t \Delta p_A(\tau) d\tau}_{\Delta v_A(t)} \quad (13)$$

with V_A denoting constant reference valu for $v_A(t)$ average. Since C_A is decoupled from the DC link, constraints specified in (9) are no longer relevant. Instead, theoretical operational limits of v_A as well as the value of V_A are dictated by the ACRC converter topology. In case of boost converter, v_A may vary between 0 and V_{DC}. For buck converter, v_A is limited by V_{DC} and the rated voltage of ACRC hardware. Buck-boost topology allows variation of v_A between 0 and the ACRC hardware rated voltage. Hold-up abilities and efficiency considerations pose additional restrictions to the above limits. If auxiliary capacitance voltage is required to be bounded as

$$v_A^{MIN} = V_A + \Delta v_A^{MIN} < v_A^{ss}(t) < V_A + \Delta v_A^{MAX} = v_A^{MAX}, \quad (14)$$

the auxiliary capacitance value is given by

$$C_A = \frac{1}{V_A} \max \left(\frac{\max\limits_t \Delta p_A(t)}{\Delta v_A^{MAX}}, \frac{\min\limits_t \Delta p_A(t)}{\Delta v_A^{MIN}} \right). \quad (15)$$

On the other hand, in case C_{DC} absorbs the pulsating power component residual given by (14), steady-state DC link voltage would be given by (8) with

$$\Delta v_{DC}(t) = \frac{1}{C_{DC} V_{DC}} \int_0^t \Delta p_{DC}(\tau) d\tau. \quad (16)$$

Ideally, $\Delta p_A \to \Delta p$ and $\Delta p_{DC} \to 0$. Then, $\Delta v_{DC} = 0$ and the ACRC would resemble an infinite capacitor [25].

B. TYPICAL CONTROL STRUCTURE

Operation of conventional ACRC mimics active power filtering as follows. Note that DC link currents supplied by GIC and DSCs (cf. Fig. 4) may be split into DC and pulsating components as

$$i_{DC,x}(t) = I_{DC,x} + \Delta i_{DC,x}(t), \quad x = 1...N. \quad (17)$$

Typical control structure senses and sums these currents. Then, DC component is eliminated and the remaining pulsating component is summed with small DC current i_0, reflecting internal ACRC losses (obtained by an additional voltage

control loop, forcing the average value of v_A to follow a predefined reference V_A) to form ACRC input current reference $i^*_{DC,A}$ (see Fig. 5a with *DCE*, VC_A and *CC* standing for DC eliminator, voltage controller and current controller, respectively). Inner current loop is further responsible for ensuring correct tracking. Hence, such an ACRC resembles a current controlled current source connected across the DC link, see Fig. 5b. The task of DC link voltage regulation is still carried out by the GIC in this case.

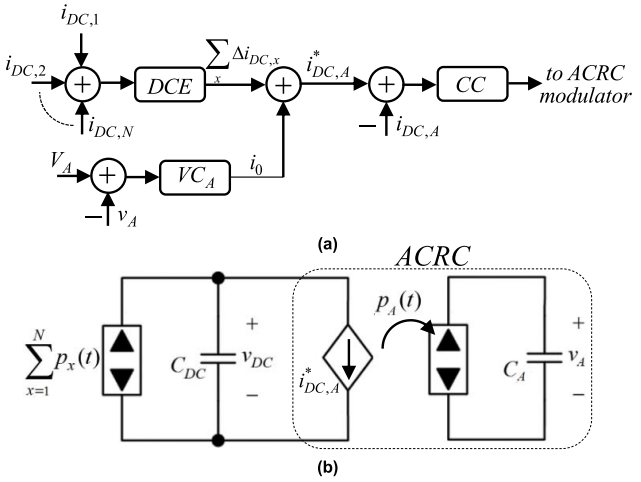

FIGURE 5. Typical solution. (a) typical ACRC control structure. (b) power level diagram.

The main drawback of the approach is hence the necessity of N current sensors installation at different locations [26]. Moreover, DCE action adds unwanted dynamics and delay into the control loop. It should also be emphasized that parameters of GIC voltage regulator (cf. Fig. 3) must be tuned taking into account C_{DC} as DC link capacitance since v_{DC} reflects system active power balance. Moreover, in case sharp load transients are expected, the value of C_{DC} must be selected taking into account the required hold up energy to withstand projected load variations. This point is usually disregarded in the literature, demonstrating steady-state performance only.

C. THE PROPOSED CONTROL STRUCTURE

The proposed control structure operates the ACRC in voltage regulation mode as follows. Instead of sensing all the DC link side currents, only DC link voltage v_{DC} is measured an regulated to the reference V_{DC} by a voltage controller *VC* as shown in Fig. 6a. Upon successful task completion, the total pulsating current component $\sum_{x=1}^{N} \Delta i_{DC,x}$ is absorbed by the ACRC without the need of measuring DC link currents. Hence, such an ACRC resembles a voltage controlled current source, connected across the DC link. While the resulting power level diagram is similar to that of Fig. 5b, the current sink variable $i^*_{DC,A}$ is indirectly generated so that there is no need for multiple currents measurements and additional processing.

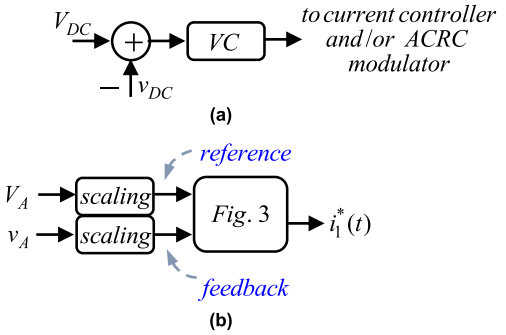

FIGURE 6. Proposed ACRC control structure. (a) proposed ACRC control structure. (b) GIC controller modification.

Nevertheless, there is an implication. According to Fig. 3, GIC voltage loop regulates the DC link voltage to achieve active power balance. However, once the ACRC gains control over the DC link voltage, the latter stops reflecting the active power balance of the system. Upon load transient, active power balance is violated, i.e. $\sum_{x=1}^{N} P_x \neq 0$ and instantaneous DC link power contains DC term. Then, C_A must absorb/supply the majority of active power difference, reflected by drift in average value of v_A. Hence, in the proposed method the average value of the auxiliary capacitance voltage reflects the system power balance. Consequently, v_A rather than v_{DC} should be regulated by GIC voltage controller (cf. Fig. 3) to assure system active power balance while satisfying (6), of course. Therefore, it is proposed to feed V_A and v_A instead of V_{DC} and v_{DC} as reference and feedback signals into existing GIC controller, respectively. It must be emphasized that in order to keep the voltage loop bandwidth unaltered to comply with (6), both V_A and v_A signals must be scaled accordingly, as shown in Fig. 6b.

Under the proposed control structure, the task of DC link voltage regulation is carried out by ACRC, while GIC is still responsible for maintaining system power balance by regulating the auxiliary voltage, i.e. the diagram of Fig. 2 is valid if C_B is replaced by C_A. Consequently, the proposed approach allows broadening of the DC voltage control loop bandwidth (i.e. achieving ripple reduction for the same capacitance utilized or keeping the ripple while decreasing the capacitance value) without trading the input power factor since DC link voltage regulation task is not related anymore to GIC voltage loop bandwidth. In other words, while GIC voltage loop must remain slow to satisfy (6), ACRC voltage loop bandwidth should be as high as possible to allow tight regulation of DC link voltage.

Apparently, obvious disadvantage of the proposed method is coupling between ACRC and GIC. However, both converters may be designed as a single entity and hence the controllers may be unified into a single IC.

IV. CASE STUDY: DC POWER SUPPLY WITH PFC FRONT END

Typical DC power supply contains a PFC front end optionally terminated by a downstream DC-DC converter.

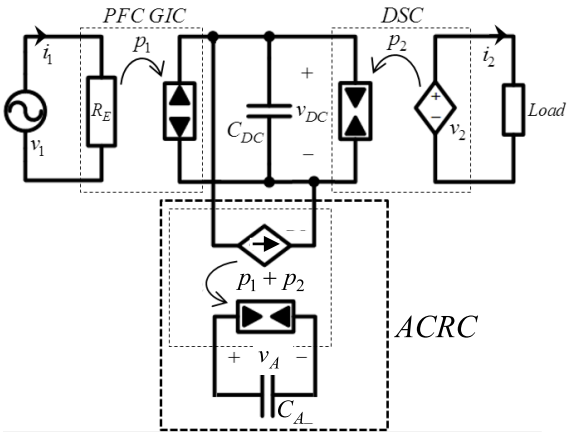

FIGURE 7. Functional power level diagram of a typical DC power supply with the proposed ACRC.

The functional diagram of such system is depicted in Fig. 7. First, consider conventional off-grid operation without RE ($C_{DC} = C_B$), assuming non-distorted sinusoidal grid and lossless conversion. At the load side,

$$v_2(t) = V_2 = const, \quad i_2(t) = I_2 = const \tag{18}$$

in steady state, i.e.

$$p_2(t) = -V_2 I_2 = -P_2 = const \tag{19}$$

and $\Delta p_2(t) = 0$. At the grid side,

$$v_1(t) = V_M \sin(\omega t), \quad i_1(t) = I_M \sin(\omega t) \tag{20}$$

in steady state, i.e. $R_E = V_M / I_M$ is the loss-free resistor [27] in Fig. 7. Thus,

$$p_1(t) = 0.5 V_M I_M - 0.5 V_M I_M \cos(2\omega t) = P_1 + \Delta p_1 \tag{21}$$

in steady state [28]. In case active power balance is preserved,

$$P_1 + (-P_2) = 0 \Rightarrow P_1 = 0.5 V_M I_M = V_2 I_2 = P_2 \tag{22}$$

and the bulk capacitance absorbs pulsating power component $\Delta p(t) = \Delta p_1(t) = -P_2 \cos(2\omega t)$ in steady state. In case the average value of DC link voltage is V_{DC}, then

$$v_{DC}^{ss}(t) \approx V_{DC} - \frac{P_2}{2\omega C_B V_{DC}} \sin(2\omega t) \tag{23}$$

according to (8), i.e.

$$C_B = \frac{P_2}{2\omega V_{DC}} \max\left(\frac{1}{\Delta v_{DC}^{MIN}}, \frac{1}{\Delta v_{DC}^{MAX}}\right). \tag{24}$$

Now, consider the proposed ACRC-based operation. Once $v_{DC} \to V_{DC}$, the majority of pulsating power is transferred to C_A. In case the average value of auxiliary capacitor voltage is V_A, there is

$$v_A^{ss}(t) = V_A \sqrt{1 + \frac{P_2}{\omega C_A V_A^2} \sin(2\omega t)} \tag{25}$$

according to (18). Assuming ACRC converter of boost topology and selecting $V_A = \sqrt{\frac{1}{2}\left(v_{A,MAX}^2 + v_{A,MIN}^2\right)}$ (to split the available capacitor energy into two equal parts above and below V_A) gives

$$C_A = \frac{P_2}{\omega\left(V_A^2 - v_{A,MIN}^2\right)} = \frac{P_2}{\omega\left(v_{A,MAX}^2 - V_A^2\right)}, \tag{26}$$

minimized for $v_{A,MIN} = 0$ and $v_{A,MAX} = V_{DC}$ as

$$C_A^{MIN} = \frac{2P_2}{\omega V_{DC}^2} \tag{27}$$

for $V_A = V_{DC} / \sqrt{2}$ [29]. Assuming $\Delta v_{DC}^{MIN} \cong \Delta v_{DC}^{MAX} = \Delta v_{DC}$, the capacitance reduction ratio is then given by

$$\frac{C_B}{C_A} = \frac{V_A^2 - v_{A,MIN}^2}{2V_{DC}\Delta v_{DC}} = \frac{v_{A,MAX}^2 - V_A^2}{2V_{DC}\Delta v_{DC}}, \tag{28}$$

maximized as

$$\max\left(\frac{C_B}{C_A}\right) = \frac{C_B}{C_A^{MIN}} = \frac{V_{DC}}{4\Delta v_{DC}}. \tag{29}$$

It is important to emphasize that according to (27), the value of C_A^{MIN} does not rely on the quality of DC link voltage regulation. As revealed in the next Section, the latter only affects $T(\omega)$ and hence the frequency content of the DC link voltage ripple. Moreover, it ought to be stated that it is possible to regulate maximum or minimum value of v_A instead of its average. The reader is referred to [26] for a discussion on pros and cons of each method.

V. VERIFICATION

For the purpose of the proposed DC link capacitance reduction and ripple mitigation approach verification, Texas Instruments UCC28180EVM-573 360[W] active PFC pre-converter evaluation board [30] was considered. Basic schematics of UCC28180EVM-573 (not including EMI filter) is shown in Fig. 8.The evaluation board includes a full bridge diode rectifier, followed by a bulk DC link electrolytic capacitor ($C_B = 270[\mu F]$) terminated boost converter, operating at switching frequency of 120 kHz. During experimental study, the evaluation board was fed from 230[V], 50[Hz] single-phase grid.

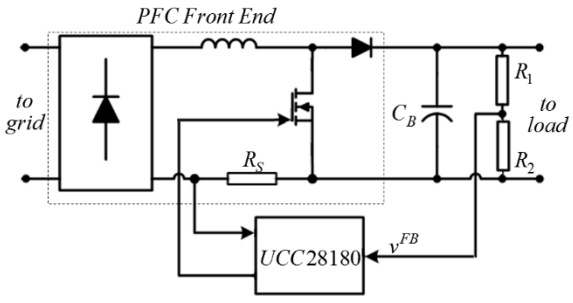

FIGURE 8. Texas Instruments UCC28180EVM-573 basic schematics.

The UCC28180EVM-573 principle of operation is as follows. The value of DC link voltage v_{DC} is measured via a 1/80 voltage divider (R_1, R_2). The resulting feedback signal v^{FB} is fed to the UCC28180 IC and subtracted from $5[V]$ internal reference. The difference is processed by type-II controller, designed to yield nominal voltage loop bandwidth of 8Hz. Thus, the DC link voltage is regulated to $V_{DC} = 400[V]$ in steady state. PFC pre-converter draws current of sinusoidal shape and is phase with the grid voltage (i.e. only $i^*_{1a}(t)$ forms the reference current $i^*_1(t)$ (cf. Fig. 3)).

Inductor current is measured via voltage across the shunt resistor R_S and the resulting feedback signal is fed to the UCC28180 IC.

TABLE 1. ACRC parameter values.

Parameter	Value	Units
Switching frequency, F_S	50	kHz
Inductance, L_A	320	μH
Capacitance, C_A	22	μF
Capacitance, C_{R2}	2.2	μF
Reference voltage, V_A	270	V

In order to realize the proposed direct-voltage-regulated (DVR) ACRC-based functionality, C_B was substituted by a $4.7[\mu F]$ ceramic capacitor C_{R1} (cf. Fig. 9(a)) and the 1/80 voltage divider (R_1, R_2) output was detached from the UCC28180 IC (i.e. v_{DC} is no longer fed back to the PFC controller). In its place, a 1/140 divider (R_X, R_Y) was connected across the DC link voltage to sense its value. The resulting feedback signal v^{FB}_{DC} was then connected to an A/D input of TMS320F28332 digital signal processor (DSP). The ACRC was realized by a bidirectional buck/boost DC-DC converter (cf. Fig. 9(b)). ACRC parameters are summarized in Table 1. Additional ceramic capacitor C_{R2} was connected across ACRC converter terminals for switching ripple filtration. Converter switches S_1 and S_2 were realized by Infineon 20N60C3 MOSFETs, driven by two DSP PWM output ports via an International Rectifier IR 2113 driver. ACRC inductor current was measured using a LEM Ltsr-15 Hall sensor; voltage across auxiliary capacitor v_A was sensed using 1/125 voltage divider (R_A, R_B). Corresponding feedback signals were then fed to the DSP via corresponding A/D (see Fig. 9(a)). Voltage feedback signal v^{FB} fed into the UCC28180 IC was created in the DSP, modulated by 50 kHz PWM and transferred through an analog auxiliary network (AN) to create filtered, scaled and shifted version of v_A (cf. Fig. 6b). The main DSP functionality is therefore executing the control algorithm given in Fig. 6a and creating scaled version of v_A, required in Fig. 6b. Complete experimental circuitry is depicted in Fig. 9(c).

The overall control diagram is given in Fig. 10. Each triangle denotes a linear transformation x-to-y of the form $y = ax + b$ with constant a and b. In particular, k_{HS} symbolizes the Hall sensor, k_{AD} and k_{PWM} denote linearized action of A/D and PWM ports, k_v and k_i scale the two sampled ACRC variables to reconstruct real world variables v_A and i_A, respectively.

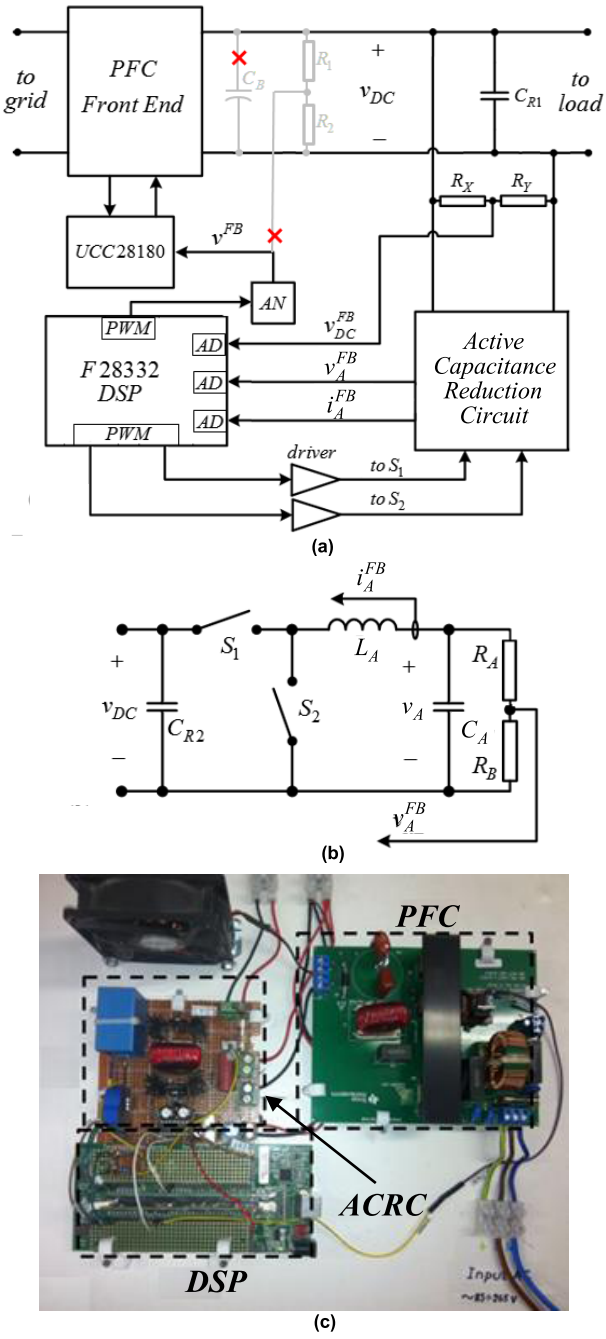

FIGURE 9. Experimental setup. (a) schematic diagram; (b) ACRC subcircuit; (c) prototype pictured.

Cascaded dual-loop control structure was used to operate the ACRC for regulating the DC link voltage to $V_{DC} = 400[V]$.

For the purpose of keeping the average value of the voltage across auxiliary capacitor at $V_A = 270[V]$, measured instantaneous voltage v_A was notch-filtered (NF) around 100Hz to attenuate the ripple and then scaled by k_A to match the range of internal PWM generator. Notch filtering is required to avoid triggering over-voltage and under-voltage protection circuitry of the UCC28180 IC. Generated PWM signal is then

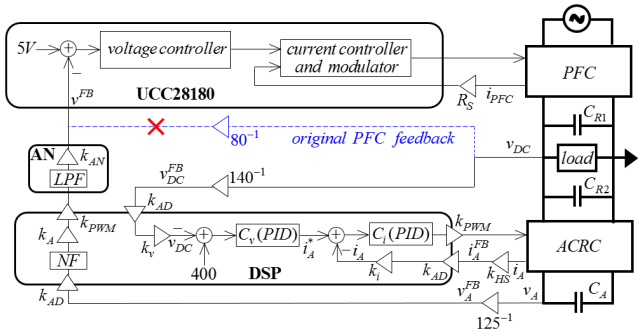

FIGURE 10. Overall control diagram.

first low-pass filtered (LPF) in the AN to eliminate PWM switching ripple and then scaled by k_{AN} so that $v_A = 270[V]$ yields $v^{FB} = 5[V]$. Moreover, the gain of v_A-to-v^{FB} loop is set to $\frac{5}{400} \cdot \frac{22}{270} = \frac{1}{981}$ to account for 1/80 original voltage feedback gain of UCC28180 and 22μF capacitance utilized instead of 270μF, according to which the parameters of UCC28180 voltage compensator are tuned. This ensures that PFC voltage loop bandwidth remains unaltered, as required. Consequently,

$$v^{FB} = 981^{-1}\left(\langle v_A \rangle_{10ms} - 270\right) \tag{30}$$

with $\langle v_A \rangle_{10ms}$ denoting average value of v_A in 10[ms] period. The sampling frequency of the DSP-executed control algorithm was chosen as 50[kHz] (the same as the switching frequency).

Parameters of controllers C_i and C_v were set according to design guidelines in [31], yielding 4.1[kHz] bandwidth with 45^o phase margin in the current loop and 794 [Hz] with 45^o phase margin in the voltage loop for nominal plants.

Recalling that in the original system, DC link voltage loop bandwidth was ~8Hz, it may be concluded that ~100 times voltage loop bandwidth increase was achieved by the proposed system.

In the first experiment, operation of UCC28180EVM-573 with original 270[μF] electrolytic capacitor was inspected under rated load. Following (23), such an operation should yield DC link voltage ripple of ~11[Vpp] for $V_{DC} = 400[V]$ in case conversion losses are neglected. Corresponding waveforms are depicted in Fig. 11(a). As expected, the ripple is nearly sinusoidal and slightly higher than 11[Vpp] due to circuit losses and un-modeled parasitics. Then, electrolytic capacitor was replaced by 22μF DVR-ACRC and rated load operation was again examined. The results are depicted in Fig. 11(b). It may be concluded that the DC link voltage is well regulated to $V_{DC} = 400[V]$, as desired. Moreover, the ripple magnitude value is slightly below that of 270[μF] electrolytic capacitor based system. Yet, the resulting ripple is periodic yet non-sinusoidal due to the nonlinearity of ACRC converter operation and non-sinusoidal v_A.

Efficiency of 92.5% was attained by the combined system under rated load operation, corresponding to ~95%

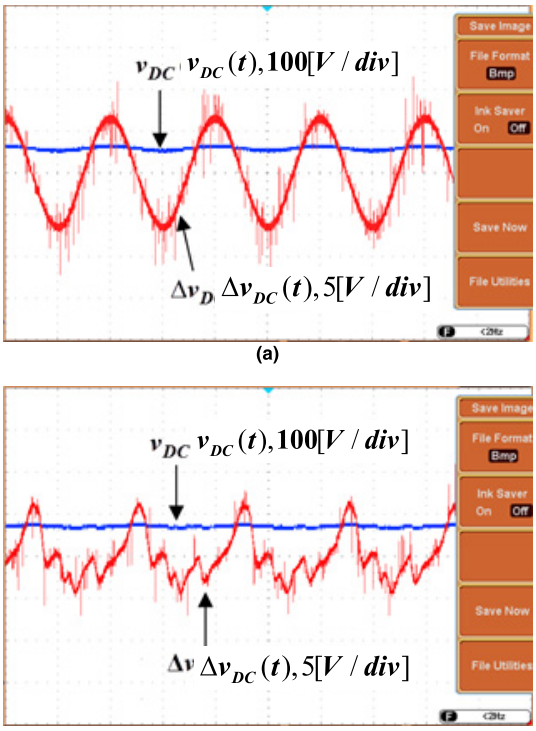

FIGURE 11. Experimental results. PFC front end DC link voltage and ripple under rated loading. (a) with electrolytic capacitor, $C_B = 270$ [μF]; (b) with DVR-ACRC, $C_A = 22$[μF].

efficiency of the ACRC (manufacturer-declared full rating PFC efficiency is 97.3%). It must be emphasized that the ACRC prototype was not optimized for efficiency, i.e. the losses may be further decreased.

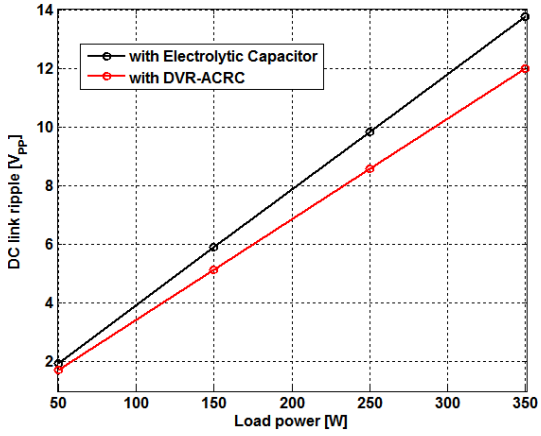

FIGURE 12. Experimental results. DC link peak-to-peak ripple values comparison for different load ratings.

Peak-to-peak values of DC link voltage ripple in both original and DVR-ACRC-based configurations are compared in Fig. 12 for 50W-350W loading range. It may be concluded that DVR-ACRC-based configuration possesses slightly lower ripple magnitude than the original one.

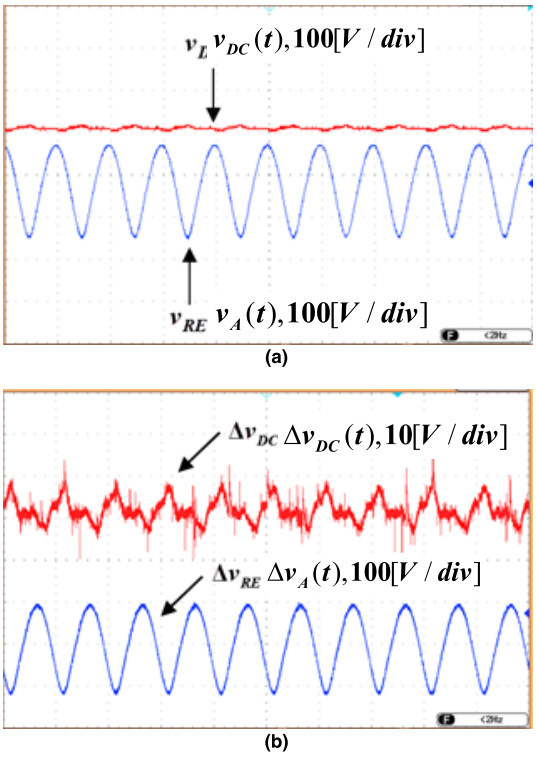

FIGURE 13. Experimental results. ACRC-based PFC front end DC link and auxiliary capacitors voltages and ripples under rated loading. (a) DC link and ACRC voltages; (b) DC link and ACRC voltage ripples.

Fig. 13 demonstrates instantaneous values of the voltage across DC link and auxiliary capacitors along with their respective ripples. Following (25), rated loading for $V_A = 270[V]$ and $C_A = 22[\mu\text{F}]$ is expected to produce auxiliary capacitor voltage ripple ideally ranging between $145[V]$–$354[V]$. This is validated by experimental results (once more, ideality assumptions cause slight underestimation).

In order to observe the pulsation power component absorbing effect, ACRC inductor current (instantaneous and switching free) is given in Fig. 14 for rated load operation.

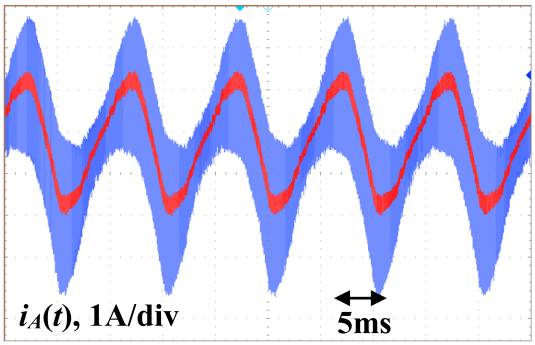

FIGURE 14. Experimental results. ACRC inductor current for rated load operation.

Dynamic behavior of the voltage across DC link and auxiliary capacitors are depicted in Fig. 15 upon abrupt

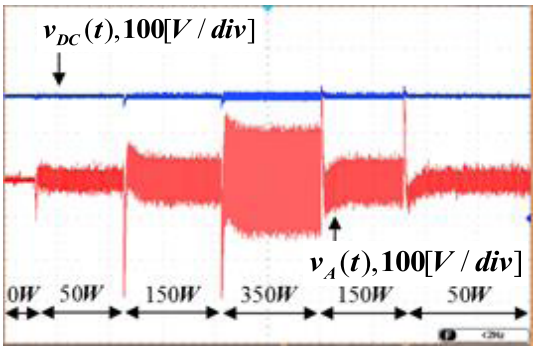

FIGURE 15. Experimental results. DC link and auxiliary capacitor voltages responses to load transients.

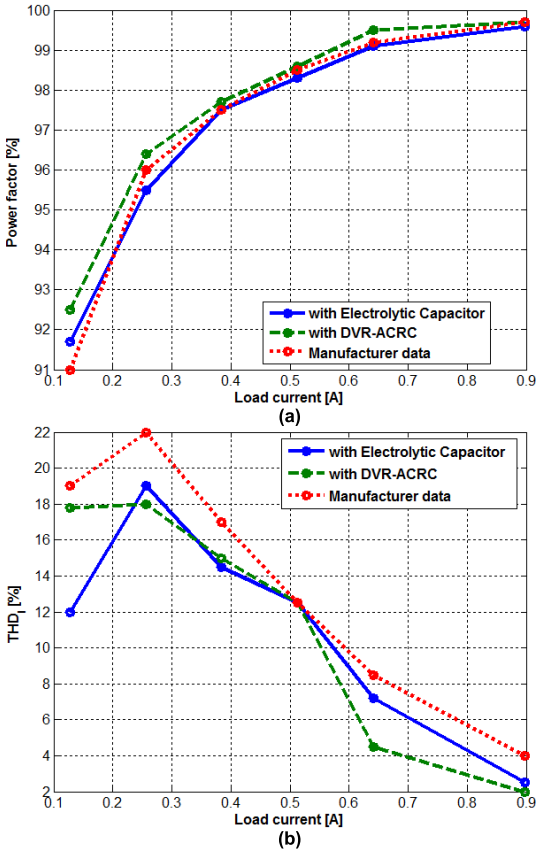

FIGURE 16. Experimental results. Power quality comparison for different load currents. (a) power factor; (b) total harmonic distortion.

load changes. Apparently, auxiliary voltage transients are relatively slow, corresponding to low bandwidth of the PFC voltage loop control. Then again, DC link voltage recovers much faster owing to the wide bandwidth of ACRC voltage loop control. Moreover, since the hold-up energy ability of the auxiliary capacitor is significantly inferior to that of the original electrolytic capacitor, auxiliary voltage experiences collapse upon sharp load increase and peaking upon sudden load decrease. It should be noted that such behavior is common to all ACRC-based systems. Improving transient response is therefore one of the most important future work directions.

In order to verify that replacing the electrolytic capacitor by the ACRC does not alter the power quality performance of the PFC front end, both power factor (PF) and current total harmonic distortion (THD_I) were measured in both original and DVR-ACRC-based configurations for the whole load range and compared to the manufacturer provided curves (related to operation with electrolytic capacitor). The results are shown in Fig. 16, validating that the DVR-ACRC -based operation does not affect the grid-side performance of the PFC front end. The outcome is supported by comparison of low-frequency harmonic content of grid-side current, normalized to the first harmonic magnitude (cf. Fig. 17).

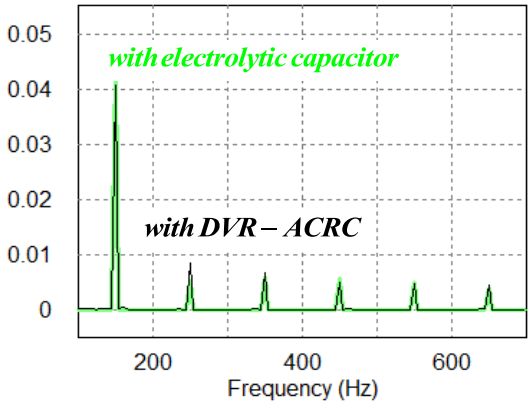

FIGURE 17. Normalized grid-side current harmonic content.

The THD_I is mainly formed by the third harmonic [32], which is nearly the same in both cases.

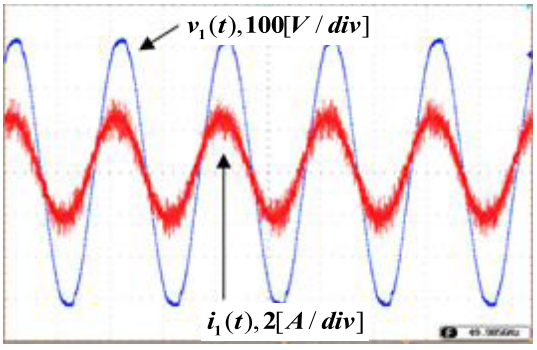

FIGURE 18. Experimental results. Mains voltage and current under rated loading.

As an example, grid voltage and input current of the PFC pre-converter under DVR-ACRC operation are depicted in Fig. 18. It may be concluded that around unity power factor is preserved, similarly to the case with electrolytic capacitor.

VI. REMARK

An significant point to be emphasized is volume/cost comparison of electrolytic capacitor and ACRC based systems. A recent study (involving a 1.6kW classical ACRC) reported 44% volume reduction (neglecting space between components) and 12% cost decrease (taking into account addition components prices only) in case ACRC is utilized [33]. Further rating increase may lead to further cost/volume reduction.

VII. CONCLUSION

An alternative approach to improving the reliability of mains interfacing power conversion systems by active DC link capacitance reduction was proposed in the paper. As in previously suggested methods, the bulk DC link capacitance is replaced by a DC-DC converter, relocating the pulsating power constituent to a much lower auxiliary capacitance. Nevertheless, the suggested control structure is different from the previously proposed in the literature. Instead of operating as an active power filter, the DC-DC converter gains control over the DC link voltage. This eliminates the need for multiple current sensors, typically required in active-power-filter-like solutions. The main shortcoming of the proposed technique is the fact that once tightly regulated by the auxiliary DC-DC converter, the DC link voltage no longer serves as the system active power balance indicator, solved by utilizing the voltage across the auxiliary capacitance in the power balance controller instead. On the other hand, DC link voltage loop bandwidth may now be increased and decoupled from the input current quality. Feasibility of the proposed methodology was validated by experimental results.

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