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An Improved Three-Phase Voltage Source Converter With High-Performance Operation Under Unbalanced Conditions

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ABSTRACT The unbalance of the three-phase grid-voltages/loads can cause double-frequency power ripples in the voltage source converter (VSC) system. Such power ripples can further lead to current and/or voltage ripples on the dc link, which may create instability of the system, lower its efficiency and shorten the lifetime of dc sources (e.g., batteries). Existing control solutions cannot well solve this issue and even bring collateral damage. Several hardware solutions have recently been proposed to tackle these issues, but these methods suffer from large size, high cost, and reduced system reliability. Instead, this paper proposed an improved topology to handle the problems faced by the VSC under unbalanced conditions. Although, hardware modification is also needed, it will not increase the size and cost of the system, since only one connecting line is added, which can be easily made on the power-stage printed circuit board. Moreover, the improved topology can also be used to reduce the leakage current in transformerless photovoltaic system and to eliminate the high frequency circulating current in multiple parallel converters. Theoretical analysis, simulation, and experimental results are provided to explain the principle and to validate the effectiveness of the improved topology.

INDEX TERMS Grid-connected, islanded, power ripple, three-phase unbalance, voltage source converter.

I. INTRODUCTION

Three-phase Voltage-Source Converters (VSC) have been widely adopted as the key interfaces between power sources and loads in distribution systems. However, different types of grid/load disturbances and faults exist in practice, which pose great challenges to the normal operation of the VSC. Grid/load unbalance is one of such abnormal conditions, which may lead to large double-frequency current/voltage ripples on the DC link [1], [2]. The presence of such ripples is detrimental to the system since it can reduce the MPPT efficiency of photovoltaic (PV) panels [3], lead to overheating of batteries [4] and shorten the lifetime of fuel cells [5]. In light of the operation of VSC under unbalanced conditions, many solutions have been developed, which can be divided into two categories as shown in Fig. 1, depending on whether hardware configuration is changed or not.

The control solution contains three types distinct by the control objectives: balanced current/voltage control, constant active and reactive power control and flexible power control [6]–[20]. The first one aims to feed balanced current to the unbalanced grid (or balanced voltage to the unbalanced load) [6]–[8]. However, the presence of the negative-sequence components in grid voltage (or load current) results in power ripples and thus the undesired current and/or voltage ripples will appear on the DC link. In comparison, the constant power control aims directly at mitigation of the current and voltage ripples on the DC link, which is realized by regulating the positive-sequence and negative-sequence current independently [9]–[13]. Its drawback is that an unbalanced and distorted AC current has to be produced, which may further deteriorate the unbalanced condition and trigger overcurrent protection. Although other flexible power control strategies were also proposed to get a tradeoff between the two objectives, they cannot resolve the problems ultimately [14]–[20]. So far, there is still not a control method in the literature that can achieve these two objectives at the same time.

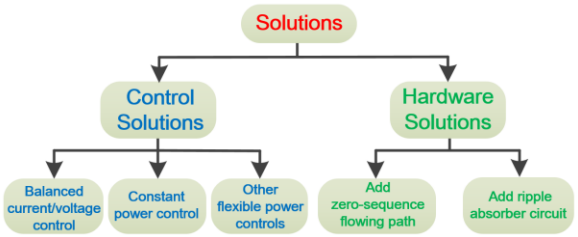

FIGURE 1. Operation solution of the VSC under unbalanced condition.

On the other hand, it is also possible to handle the three-phase unbalanced issue by adding hardware components. For instance, a neutral line is added between the grid transformer and VSC in [21], which introduces an additional current control freedom for the zero-sequence current and thus can achieve better control performance. However, this method cannot realize the balanced AC current and ripple-free DC current/voltage simultaneously and long cables have to be used if the transformer is far from the VSC. Besides, it cannot be used for the transformerless PV systems. To overcome the drawback, another topology was proposed in [22], where additional power semiconductors and passive components were added to the DC link in order to absorb the ripple power. While this method is feasible, it requires extra hardware which will greatly increase the size and cost of the system, and thus are not preferred as well.

To tackle these issues, this paper proposed an improved VSC topology with high-performance operation under unbalanced conditions. For the improved topology, a conducting path is created for the harmonic currents to flow under unbalanced conditions. With a simple control strategy, the sinusoidal symmetrical AC grid current can be ensured and the DC link current/voltage ripples can be avoided at the same time. Furthermore, the added conducting path can also be a common mode path to restrict the high frequency current components within the converter, which can be applied to reduce the leakage current in the transformerless PV systems or eliminate the high frequency circulating current in multiple parallel converters. Different from existing hardware solutions, the improved topology does not increase the cost and size of the system since the added conducting path can be easily integrated to the power-stage printed circuit board. Effectiveness of the proposed approach is finally validated by simulation and experimental results.

II. PROBLEM ANALYSIS

Fig. 2(a) and (b) show the configurations of the LC-filtered VSC system under grid-connected mode and islanded mode. Generally, balanced grid current (or balanced load voltage) is expected to be provided by the VSC. However, under an unbalanced condition, controlling the VSC to inject balanced current to the grid (or balanced voltage to the load) will cause double-frequency power ripple due to the existence of the negative-sequence grid voltage (load current) components.

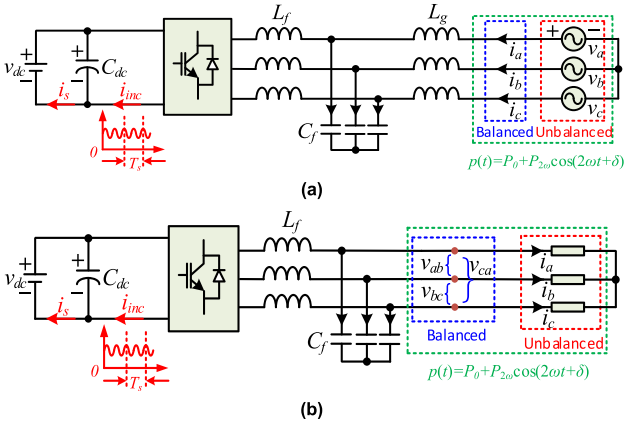

FIGURE 2. The conventional three-phase VSC under unbalanced three-phase conditions: (a) grid-connected mode, (b) islanded mode.

To illustrate it, take the grid-connected mode as an example, when the grid voltages (v_a, v_b and v_c) are unbalanced, the three-phase unbalanced grid voltage can be expressed as (1), while the grid currents (i_a, i_b and i_c) are balanced and sinusoidal which are given by (2).

$$\begin{cases} v_a = \sqrt{2}V_a \sin(\omega t + \alpha_1) \\ v_b = \sqrt{2}V_b \sin(\omega t + \alpha_2) \\ v_c = \sqrt{2}V_c \sin(\omega t + \alpha_3) \end{cases} \tag{1}$$

$$\begin{cases} i_a = \sqrt{2}I \sin(\omega t + \varphi) \\ i_b = \sqrt{2}I \sin(\omega t - 120^\circ + \varphi) \\ i_c = \sqrt{2}I \sin(\omega t + 120^\circ + \varphi) \end{cases} \tag{2}$$

where V_a, V_b and V_c are the root mean square (RMS) values of the grid voltages while α_1, α_2 and α_3 are the their initial phases. I is the amplitude of the three-phase balanced grid currents, and φ is the initial phase of the phase A grid current. ω is the fundamental angular frequency.

For simplicity, the power losses and the power in the filters are neglected. The AC side instantaneous output power $p_{ac}(t)$ of the three-phase VSC system can be given as

$$p_{ac}(t) = v_a i_a + v_b i_b + v_c i_c = P_0 + P_{2\omega}\cos(2\omega t + \delta) \tag{3}$$

where

$$\begin{aligned} P_0 = {} & V_a I \cos(\alpha_1 - \varphi) + V_b I \cos(\alpha_2 - \varphi + 120^\circ) \\ & + V_c I \cos(\alpha_3 - \varphi - 120^\circ) \end{aligned} \tag{4}$$

$$\begin{aligned} & P_{2\omega}\cos(2\omega t + \delta) \\ & = -(V_a I \cos(2\omega t + \alpha_1 + \varphi) \\ & \quad + V_b I \cos(2\omega t + \alpha_2 + \varphi - 120^\circ) \\ & \quad + V_c I \cos(2\omega t + \alpha_3 + \varphi + 120^\circ)) \end{aligned} \tag{5}$$

P_0 represents the average value of the active power while $P_{2\omega}$ and δ are respectively the amplitude and initial phase of the double-frequency pulsating power.

To better show the low-frequency component for the VSC input current i_{inc}, the high-frequency components (switching frequency harmonic components) are ignored, which are far

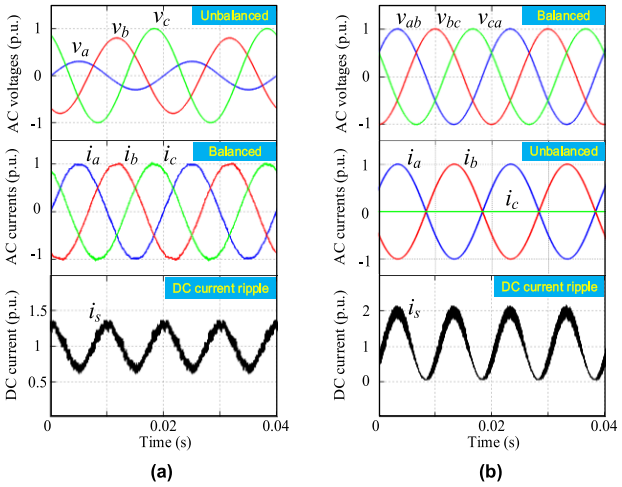

FIGURE 3. Waveforms of the three-phase VSC systems under unbalanced conditions: (a) grid-connected mode, and (b) islanded mode.

from double-frequency and thus does not affect the subsequent discussion. Therefore, i_{inc} can be derived as (6) considering the power balance between AC side and DC side.

$$i_{inc} \approx \frac{P_{ac}(t)}{v_{dc}} = \frac{P_0}{v_{dc}} + \frac{P_{2\omega}\cos(2\omega t + \delta)}{v_{dc}} \tag{6}$$

It can be observed from (6) that the double-frequency ripple will be generated in the DC current when the DC voltage is constant, which can also be explained by the simulation results in Fig. 3(a) while DC capacitance C_{dc} is small. This ripple current is detrimental to the DC sources and thus should be suppressed. However, due to the direct relation of the AC voltage unbalance and the power ripple, it is impossible to achieve the balanced output grid current and the constant output power simultaneously only using control strategies. Similar problem also exists in islanded mode, as seen from the simulation results shown in Fig. 3(b).

III. PROPOSED SOLUTION

In order to smooth the DC source voltage/current ripple while AC grid current (line-to-line voltage) is controlled to be sinusoidal and symmetrical under unbalanced three-phase voltage (load), an improved topology is proposed in Fig. 4. In this section, the improved topology will be illustrated from the following three parts: *A*. circuit configuration and operating principles, *B*. minimum DC voltage and current stress analysis, and *C*. other functions.

A. CIRCUIT CONFIGURATION AND OPERATING PRINCIPLES

Fig. 4 shows the improved three-phase VSC topology, where the common point of the three AC filter capacitors is connected to the DC negative bus. Without this modification, the double-frequency component flows mainly through the DC source as depicted by the black dashed line in Fig. 4, which significantly influences the source performance and AC-side grid current (or load voltage) quality. In comparison, the proposed solution provides an extra current flow path. As a result, with proper control, the double-frequency current component i_{path} can be restricted inside the VSC system as depicted by the red dashed line in Fig. 4, i.e. the DC source can be free of ripples, and at the same time, the AC output currents (or voltages) can be balanced and sinusoidal. Compared with the approach in [22], the improved topology will not increase the system size and cost, since the added path can be easily integrated into the power board.

To simplify the analysis, the power and voltage on LC-filters C_f and L_f (which are normally less than 5% p.u.) is neglected. As the double-frequency current is introduced into the LC filter capacitors, its corresponding characteristics will change accordingly. Before adding the path (i.e. conventional topology), the three AC capacitor voltages should satisfy equation (7), whose calculated results are shown in (8).

$$\begin{cases} v_{Cd1} - v_{Cd2} = v_a - v_b = \sqrt{2}V_{ab}\sin(\omega t + \theta_1) \\ v_{Cd2} - v_{Cd3} = v_b - v_c = \sqrt{2}V_{bc}\sin(\omega t + \theta_2) \\ v_{Cd1} + v_{Cd2} + v_{Cd3} = 0 \end{cases} \tag{7}$$

$$\begin{cases} v_{Cd1} = \dfrac{1}{3}(2\sqrt{2}\sin(\omega t + \theta_1)V_{ab} + \sqrt{2}\sin(\omega t + \theta_2)V_{bc}) \\ v_{Cd2} = \dfrac{1}{3}(-\sqrt{2}\sin(\omega t + \theta_1)V_{ab} + \sqrt{2}\sin(\omega t + \theta_2)V_{bc}) \\ v_{Cd3} = \dfrac{1}{3}(\sqrt{2}\sin(\omega t + \theta_1)V_{ab} - 2\sqrt{2}\sin(\omega t + \theta_2)V_{bc}) \end{cases} \tag{8}$$

where V_{ab} and V_{bc} are the RMS values of the AC side line-to-line voltages, and v_{Cd1}, v_{Cd2} and v_{Cd3} are the three capacitor voltages respectively.

On the other hand, after adding the path (i.e. improved topology), the AC capacitor voltages will contain the double-frequency component since the double-frequency ripple current of DC link flows into the AC capacitors. Apart from the double-frequency component, the AC capacitor voltages also contain a fixed DC voltage component because of the voltage difference between the phase-leg and DC negative bus. Therefore, the updated capacitor voltage expressions can then be given as

$$\begin{cases} v_{Cd1} = \dfrac{1}{3}(2\sqrt{2}\sin(\omega t + \theta_1)V_{ab} \\ \qquad +\sqrt{2}\sin(\omega t + \theta_2)V_{bc}) + v_{comp} \\ v_{Cd2} = \dfrac{1}{3}(-\sqrt{2}\sin(\omega t + \theta_1)V_{ab} \\ \qquad +\sqrt{2}\sin(\omega t + \theta_2)V_{bc}) + v_{comp} \\ v_{Cd3} = \dfrac{1}{3}(-\sqrt{2}\sin(\omega t + \theta_1)V_{ab} \\ \qquad -2\sqrt{2}\sin(\omega t + \theta_2)V_{bc}) + v_{comp} \end{cases} \tag{9}$$

$$v_{comp} = \frac{v_{dc}}{2} + B_{2\omega}\sin(2\omega t + \phi) \tag{10}$$

where v_{comp} is the common mode (CM) compensation voltage, which is injected into the three capacitors. $B_{2\omega}$ is the amplitude of the double-frequency component and ϕ is its phase difference with respect to the grid phase A voltage.

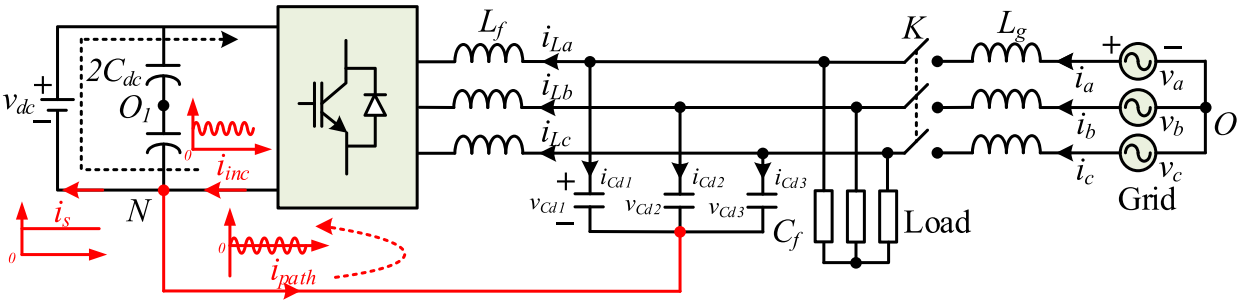

FIGURE 4. The improved three-phase VSC under unbalanced three-phase conditions.

By differentiating (9) and (10), the capacitor currents can be calculated as

$$\begin{cases} i_{Cd1} = \frac{1}{3}\omega C_f(2\sqrt{2}\cos(\omega t+\theta_1)V_{ab} \\ \quad +\sqrt{2}\cos(\omega t+\theta_2)V_{bc}) + i_{comp} \\ i_{Cd2} = \frac{1}{3}\omega C_f(-\sqrt{2}\cos(\omega t+\theta_1)V_{ab} \\ \quad +\sqrt{2}\cos(\omega t+\theta_2)V_{bc}) + i_{comp} \\ i_{Cd3} = \frac{1}{3}\omega C_f(-\sqrt{2}\cos(\omega t+\theta_1)V_{ab} \\ \quad -2\sqrt{2}\cos(\omega t+\theta_2)V_{bc}) + i_{comp} \end{cases} \tag{11}$$

$$i_{comp} = 2B_{2\omega}\omega C_f\cos(2\omega t+\phi) \tag{12}$$

where i_{Cd1}, i_{Cd2} and i_{Cd3} are the three capacitor currents respectively. C_f is the capacitance value of the three AC capacitors. i_{comp} is the CM compensation current, which is mainly introduced by the i_{path}.

The sum of the instantaneous power of the three filter capacitors P_{C_sum} will be

$$\begin{aligned} P_{C\_sum} &= v_{Cd1}\times i_{Cd1} + v_{Cd2}\times i_{Cd2} + v_{Cd3}\times i_{Cd3} \\ &= P_{C\_2\omega} + P_{C\_4\omega} \end{aligned} \tag{13}$$

where

$$\begin{aligned} P_{C\_2\omega} = \frac{1}{3}\omega C_f(&9B_{2\omega}v_{dc}\cos(2\omega t+\phi)+2V_{ab}^2\sin(2\omega t+2\theta_1) \\ &+2V_{bc}^2\sin(2\omega t+2\theta_2)+2V_{ab}V_{bc}\sin(2\omega t+\theta_1+\theta_2)) \end{aligned}$$

and

$$P_{C\_4\omega} = 3\omega C_f B_{2\omega}^2\sin(4\omega t+2\phi)$$

It can be clearly observed from (13) that a double-frequency ripple power $P_{C\_2\omega}$ exist in three capacitors. If this component equals to the ripple component of (3) (i.e. all the double-frequency pulsating power caused by three-phase unbalance is restricted to the added path), then the double-frequency ripple current flowing into the DC source can be avoided. However, this result cannot be realized only through circuit modification. Instead a proper control should be applied for the improved topology. Furthermore, it is worth noting that there is another fourth-order ripple power component $P_{C\_4\omega}$ introduced in (13), which results from the interaction between the double-frequency component in the capacitor voltages and currents. In this case, the fourth-order ripple power will be transferred into the DC link, which further leads to fourth-order current harmonic in DC source. Therefore, to solve this issue, a fourth-order component should be corresponding added to the CM voltage of capacitors v_{comp} as shown in (14).

$$v_{comp} = \frac{v_{dc}}{2} + B_{2\omega}\sin(2\omega t+\phi) + B_{4\omega}\sin(4\omega t+\phi_1) \tag{14}$$

where $B_{4\omega}$ is the amplitude of the fourth-order component and ϕ_1 is its phase difference with respect to the grid phase A voltage.

Thus, i_{comp} and the total instantaneous power in the three capacitors can be derived as

$$i_{comp} = 2B_{2\omega}\omega C_f\cos(2\omega t+\phi)+4B_{4\omega}\omega C_f\cos(4\omega t+\phi_1) \tag{15}$$

$$\begin{aligned} P_{C\_sum} &= v_{Cd1}\times i_{Cd1} + v_{Cd2}\times i_{Cd2} + v_{Cd3}\times i_{Cd3} \\ &= P_{C\_2\omega} + P_{C\_4\omega} + P_{C\_6\omega} + PC\_8\omega \end{aligned} \tag{16}$$

where

$$\begin{aligned} P_{C\_2\omega} &= \frac{1}{3}\omega C_f(9B_{2\omega}v_{dc}\cos(2\omega t+\phi)+2V_{ab}^2\sin(2\omega t+2\theta_1) \\ &\quad +2V_{bc}^2\sin(2\omega t+2\theta_2)+2V_{ab}V_{bc}\sin(2\omega t+\theta_1+\theta_2) \\ &\quad +9B_{2\omega}B_{4\omega}\sin(-2\omega t+\phi-\phi_1)) \\ P_{C\_4\omega} &= 3\omega C_f(B_{2\omega}^2\sin(4\omega t+2\phi) \\ &\quad +2B_{4\omega}v_{dc}\sin(4\omega t+\phi_1+\frac{\pi}{2})) \\ P_{C\_6\omega} &= 9\omega C_f B_{2\omega}B_{4\omega}\sin(6\omega t+\phi+\phi_1) \\ P_{C\_8\omega} &= 6\omega C_f B_{4\omega}^2\sin(8\omega t+2\phi_1) \end{aligned}$$

To eliminate the fourth-order ripple power from the system (i.e. $P_{C\_4\omega}=0$), the magnitude and phase of the fourth-order component in the capacitor CM voltage can be calculated as

$$\begin{cases} B_{4\omega} = \dfrac{B_{2\omega}^2}{2v_{dc}} \\ \phi_1 = 2\phi + \dfrac{\pi}{2} \end{cases} \tag{17}$$

However, it can be seen from (16) that the 6th and 8th ripple power are introduced into the system one after another, which results from the interaction between the 2nd and 4th terms in the capacitor voltages and currents. All in all, this implies

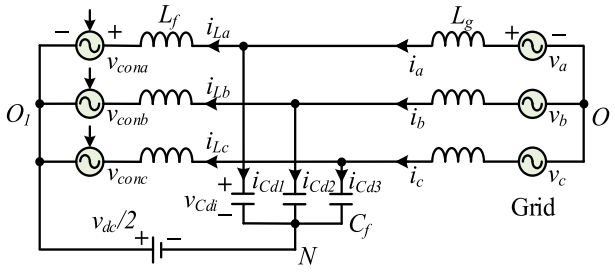

FIGURE 5. Equivalent circuit of the improved topology under grid-connected mode.

that there is always a residual pulsating power in the DC link because of power balance, and thus the complete elimination of the ripple power is not possible. Fortunately, the amplitude of fluctuating power is becoming smaller and smaller with the increase of the harmonic order, for example, the content of 8th pulsating power is generally below 1% of 2nd component from (16) and (17). Therefore, the CM compensation voltage, which is injected into the three capacitors, can be approximated as (14) for simplification in order to eliminate the main harmonic component in the DC source.

B. MINIMUM DC VOLTAGE AND CURRENT STRESS ANALYSIS

The DC voltage and current stress of power semiconductors are particularly of interest because they may directly determine the switching and conduction losses. In this section, those two features of the improved topology will be analyzed and discussed under single-phase voltage drop condition in grid-connected mode as an example.

In order to analyze the minimum requirement of DC link voltage and current stress in detail, the equivalent circuit of the improved topology is shown in Fig. 5, where the controlled voltage sources v_{cona}, v_{conb}, and v_{conc} are the output voltages of the phase-legs. According to the Kirchhoff's Current and Voltage Law, the phase-leg output voltages and converter input currents of the improved topology can be expressed:

$$\begin{cases} v_{cona} = v_{Cd1} - L\dfrac{di_{La}}{dt} - \dfrac{v_{dc}}{2} \\ v_{conb} = v_{Cd2} - L\dfrac{di_{Lb}}{dt} - \dfrac{v_{dc}}{2} \\ v_{conc} = v_{Cd3} - L\dfrac{di_{Lc}}{dt} - \dfrac{v_{dc}}{2} \end{cases} \tag{18}$$

$$\begin{cases} i_{La} = i_a - C_f\dfrac{dv_{Cd1}}{dt} \\ i_{Lb} = i_b - C_f\dfrac{dv_{Cd2}}{dt} \\ i_{Lc} = i_c - C_f\dfrac{dv_{Cd3}}{dt} \end{cases} \tag{19}$$

Therefore, to achieve the improved VSC normal operation, the DC bus voltage should be higher than the maximum peak value of three capacitor voltages on the premise of neglecting the inductor voltage. In this case, the three filter capacitor

TABLE 1. Parameters used for the simulation and experimental test.

	Description	Parameters	Value
General Parameters	Switching frequency	f_{sw}	10 kHz
	Fundamental frequency	f_n	50 Hz
	AC filter inductances	L_f	8 mH
	AC filter capacitances	C_f	30 μF
	DC link capacitance	C_{dc}	50 μF
	AC voltage (RMS)	v_a v_b v_c	110 V
	Power rating	P_0	1000 W
Grid-connected Mode	Unbalanced ratio of AC grid voltage	α_1	30%
	Phase A voltage	v_a	33 V
	Phase B voltage	v_b	88 V
	Phase C voltage	v_c	110 V
Islanded Mode	Unbalanced ratio of AC load current	α_2	100%
	Phase A load	R_A	30 Ω
	Phase B load	R_B	30 Ω
	Phase C load	R_C	$+\infty$

voltage waveforms of the improved topology obtained by combining equations (5), (9), (14), (16) and (17), using *General Parameters* from Table 1, are shown in Fig. 6(a) when phase A voltage dips to 0. It should be mentioned here that the three capacitor voltages not only contain fundamental component, but also include other components due to the CM voltage injection as expressed in (9) and (14). Then, the minimum DC voltage of improved topology is also shown in Fig. 6(a), which is equal to maximum peak value of the three capacitor voltages. Furthermore, it is noted from Fig. 6(a) that the minimum DC voltage only increases a little compared with that of the conventional topology. By defining the DC voltage index (*VI*) to be the ratio of the minimum DC voltage requirement of improved topology to that of the conventional topology as expressed in (20), a more generalized analysis of the minimum DC voltage requirement can be shown in Fig. 7(a), where it is clear that, the DC voltage index increases with the decrease of phase A voltage value and its maximum is only 1.12 p.u..

$$\begin{cases} VI = Max[\dfrac{V_{peaki}}{2\sqrt{2}V_g}] \quad (i = a, b, and\ c) \\ CI = Max[\dfrac{I_{peaki}}{2\sqrt{2}I_g}] \quad (i = a, b, and\ c) \end{cases} \tag{20}$$

where the V_{peaki} is the peak value of the capacitor voltage (v_{Cd1}, v_{Cd2}, v_{Cd3}). V_g is the phase voltage (v_a, v_b, v_c) RMS value under balanced grid condition. I_{peaki} is the peak value of the inductor current i_{Li}, while I_g is the grid current (i_a, i_b, i_c) RMS value.

On the other hand, due to the CM current injection, the VSC output current (i_{La}, i_{Lb} and i_{Lc}) will be affected, which should be discussed to obtain the highest current value for system design. From Fig. 5, it is obvious that the output

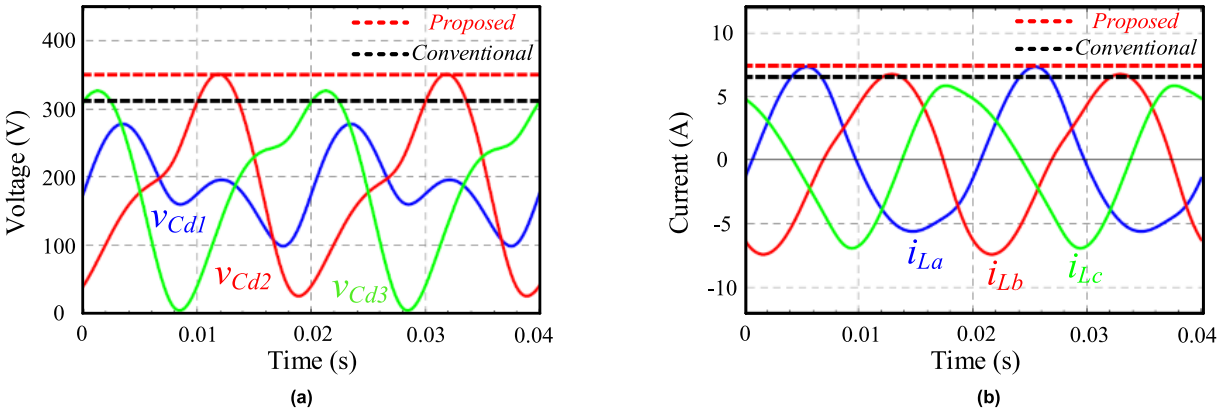

FIGURE 6. The three capacitor voltages and output currents of improved topology while phase A voltage dips to 0: (a) three capacitor voltages and minimum requirement of DC link voltage (b) VSC output currents and current stress.

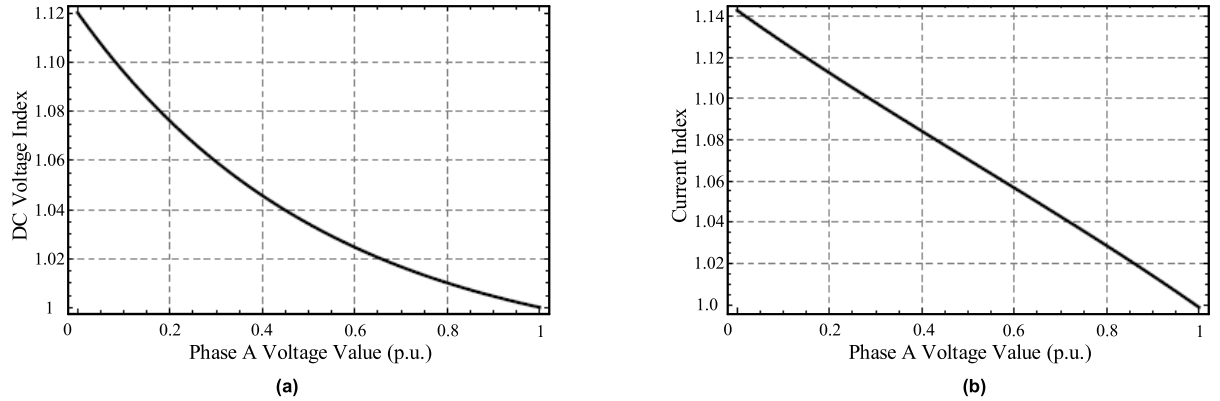

FIGURE 7. The DC voltage index and current index of improved topology with phase A voltage values.

currents are the difference between grid currents and filter capacitor currents as expressed in (19). Because the capacitor currents are much smaller compared with the grid currents, the highest output current value is just a little higher than the grid current as shown in Fig. 6(b). Similarly, by defining the current index (*CI*) to be the ratio of the highest VSC output current value to the balanced grid current value as expressed in (20), it can be seen from Fig. 7(b) that the current index increases as the phase voltage dips, and the highest current index is only 1.14 p.u. when phase A voltage dips to 0. Therefore, a little higher (within 15%) minimum requirement of DC voltage and current stress are suffered in order to eliminate the double-frequency ripple current/voltage of DC source for the improved topology under the condition of phase A voltage drop.

C. OTHER FUNCTIONS FOR HIGH-FREQUENCY CM CURRENT COMPONENT RESTRICTION

Interestingly, a very similar topology which connects to the DC midpoint O_1 rather than negative bus N (see Fig. 4) has been used to eliminate the leakage current in the transformerless PV system [23], [24]. Despite the similarity, that method cannot handle the double-frequency harmonic issue. Differently, the improved topology can not only solve the double-frequency harmonic issue but also eliminate the leakage current at the same time since the CM components can be restricted in the added path. Moreover, the high-frequency circulating current in multiple parallel converters is also high-frequency CM current component [25]. Therefore, the improved topology can also be extended to other applications such as elimination of the high-frequency circulating current in multiple parallel converters with the same principle. This section will illustrate the principle of high-frequency CM current components restriction by taking the leakage current elimination of the improved topology as example.

Fig. 8(a) shows the CM path of conventional topology in transformerless PV system, where Z_{PV} is the impedance of the parasitic capacitors and Z_E is the grounding impedance. It can be seen that leakage current circulation will exist between the stray capacitances of the PV grounded array and the system due to the loss of galvanic isolation, which leads to electromagnetic interference, safety issues, waveform distortion of the grid currents and increased power losses. In comparison, the CM equivalent circuit of improved topology is shown in Fig. 8(b), which has an added CM path compared with the conventional topology. Most of the CM current will

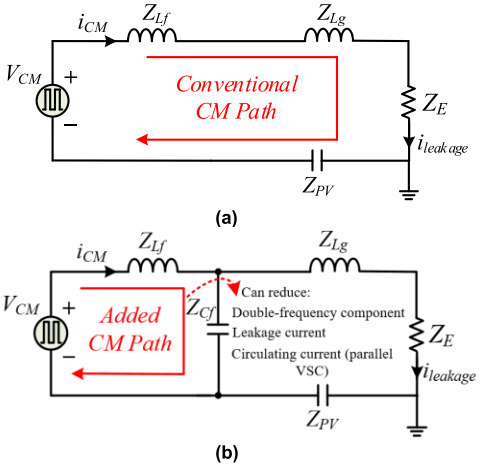

FIGURE 8. CM equivalent circuits: (a) conventional and (b) improved topology.

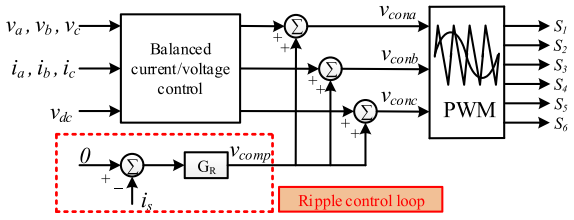

FIGURE 9. Control scheme of the improved topology.

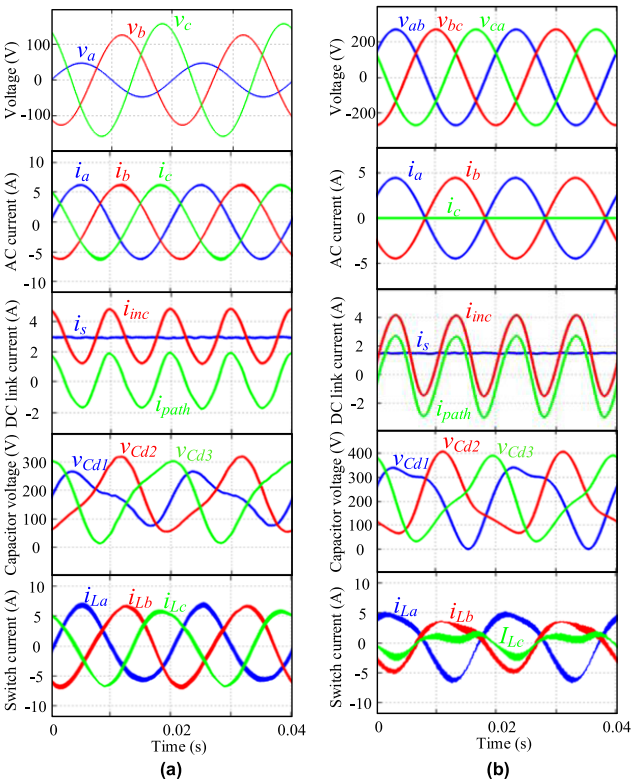

FIGURE 10. Simulation results of the improved VSC systems under unbalanced conditions: (a) grid-connected mode, and (b) islanded mode.

be introduced to the added CM path without control since the Z_{Cf} is much lower than the sum of Z_{Lg}, Z_E and Z_{PV} (C_{PV} is around 100 nF for a 1-kW PV system normally [26]) in the switch frequency. Therefore, the improved topology can be implemented in transformerless PV system to limit the ground leakage current without adding any components, which can also be extended to other applications for high-frequency CM current components restriction with the same principle and will hence not be explicitly described.

IV. CONTROL STRATEGY AND SIMULATION RESULTS

As mentioned previously, the high-frequency CM current components can be restricted in the added path only by the circuit characteristics and without extra control for the improved topology. Therefore, the control method for double-frequency harmonic current elimination of DC source are mainly discussed in this section. The control block of improved topology is shown in Fig. 9, which consists of two parts: balanced current/voltage control loop and ripple control loop. The main functionalities of the former are to regulate the output power by producing balanced sinusoidal current (or voltage), whose principle was well presented in the past and thus will not be elaborated in this paper.

In light of the ripple control loop, it also works for restricting the low-order ripple components in the added conducting path. According to the Kirchhoff's Current Law, this can be realized indirectly by controlling the ripples of the DC-source current to be zero. To implement it, the source current (i_s) is used as the feedback variable and the reference (i_{ref}) is set to zero in the control loop. Through the expression (14) of the CM voltage, the calculated current error should be integrated by a resonant controller shown as (21) in order to achieve zero tracking error at particular frequency under unbalanced conditions. Moreover, although the DC component also exists in the feedback signal (i_s), they have no effect on the resonator output because the resonator has a zero gain for DC signals. Therefore, the resonator controller output is added to the voltage reference produced by the balanced current/voltage control loop to realize the control objective. Certainly, the system can operate normally with the proposed control method under three-phase balanced condition, which is not affected by the ripple power control loop.

$$G_R(s) = \sum_{n=2,4} \frac{2k_n s}{s^2 + (n\omega)^2} \tag{21}$$

where n is the harmonic order, and k_n is the gain for the corresponding n component.

To illustrate the working principle of the proposed scheme, the system parameters can be found in Table 1, and simulation results of improved topology under the grid-connected and islanded modes are given in Fig. 10, where the figures from top to bottom are AC side voltages, AC side currents, DC link currents (ignoring switching frequency components), capacitor voltages and VSC output currents. It can be seen that VSC

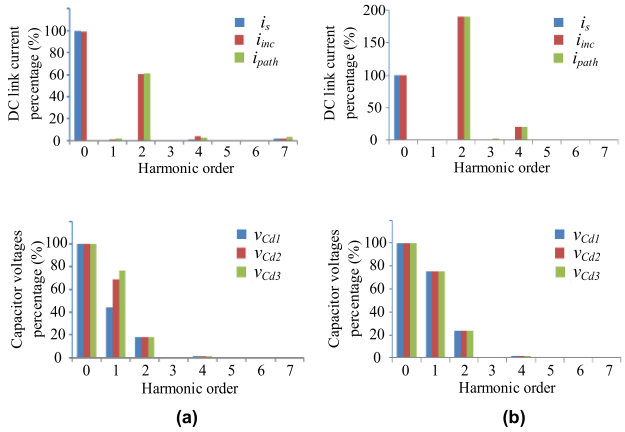

FIGURE 11. The FFT analysis of DC link currents and three capacitor voltages: (a) grid-connected mode, and (b) islanded mode.

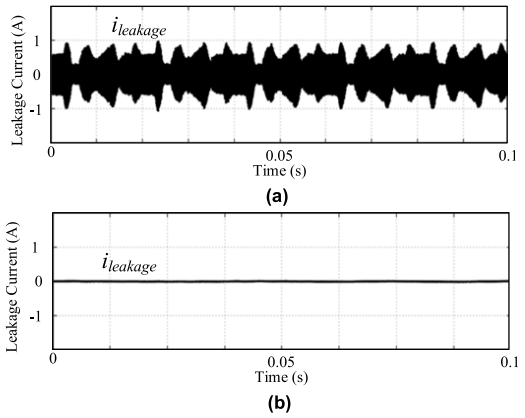

FIGURE 12. Simulation results in the transformerless PV system: (a) conventional topology (b) improved topology.

input current i_{inc} contains the same high double-frequency component as conventional topology under unbalanced conditions. However, the double-frequency component of DC source current i_s is eliminated since that is introduced into the added path for the improved topology, which can be proved by the FFT analysis of DC link current as shown in Fig. 11. Moreover, the corresponding spectrums of capacitor voltage are shown in Fig. 11, which are in full agreement with the operating principles as expressed in (9) and (14). To validate the effectiveness of the high-frequency CM current component restriction for the improved topology, Fig. 12 shows the simulation results in the transformerless PV system. For the conventional topology, the leakage current is almost 800mA as shown in Fig. 12(a), which may lead to harmonic current, safety issues and electromagnetic interference issues. In comparison, it can be seen from Fig. 12(b) that the leakage current of improved topology is very small, which is far below the standards DIN VDE V 0126-1-1 and IEC62109-2 limitation (300 mA) [27], [28].

Therefore, through above theoretical analysis and simulation results, the following are two points to consider in terms of the adoption of the proposed method:

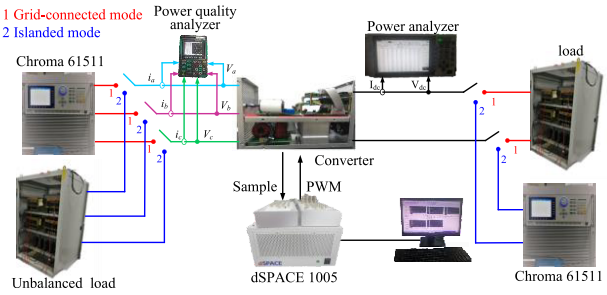

FIGURE 13. Experimental setup in the lab to validate the improved topology.

Remark 1: the double-frequency or other low-order harmonic currents on the DC source can be eliminated without affecting the basic control system, which are limited within the added conducting path through a simple ripple control loop.

Remark 2: the high-frequency components directly flows into the conducting path without control, thus the improved topology is a simple and effective scheme to eliminate the leakage current or the high-frequency circulating current in parallel converters.

V. EXPERIMENTAL RESULTS

To further verify the effectiveness of the improved topology, an experimental prototype was built in the lab as shown in Fig. 13, which was based on the same parameter values listed in Table 1 and can operate in both grid-connected mode and islanded mode. In the experiments, the AC grid and the DC source were emulated by a programmable AC/DC source Chroma 61511. Therefore, the DC link was built by the resistive load rather than ideal voltage source in the grid-connected mode (See Fig. 13) due to the limitation of the experimental conditions, which is different from the simulation and does not affect to validate the effectiveness of the improved topology. The dSPACE 1005 was used to implement the control algorithms. Besides, the voltage and current harmonics were measured by a HIOKI 3390 power analyzer, and the three-phase unbalanced ratio was measured through a KYORITSU KEW 6315 power quality analyzer.

To begin with, Fig. 14 shows the experimental results of the grid-connected mode operation. In this case, the waveforms of the unbalanced grid voltages (unbalanced ratio 30 %) are given in Fig. 14(a) and the experimental results of the conventional method and the proposed method are given in Fig. 14(b) and (c) respectively. When the grid currents are controlled to be balanced, obvious voltage ripple with a peak-to-peak value of 65 V is produced with the conventional method. In comparison, this value can be limited within 10 V with the proposed method. Moreover, in order to compare the traditional and the improved topology more clearly, Fig. 16(a) further compares the FFT analysis results of the DC voltage for these two methods, where the double-frequency ripple component can be greatly reduced from 6.57% to the 0.06% after using the proposed method, showing its effectiveness in grid-connected mode operation.

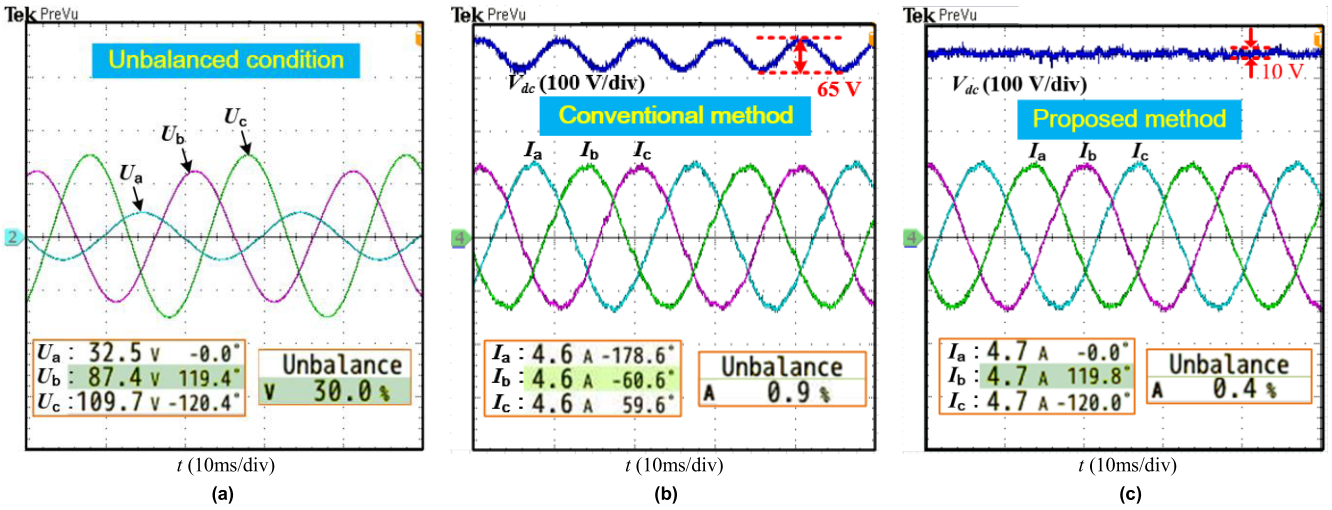

FIGURE 14. The experiment results of the conventional and improved three-phase VSC under unbalanced conditions in grid-connected mode.

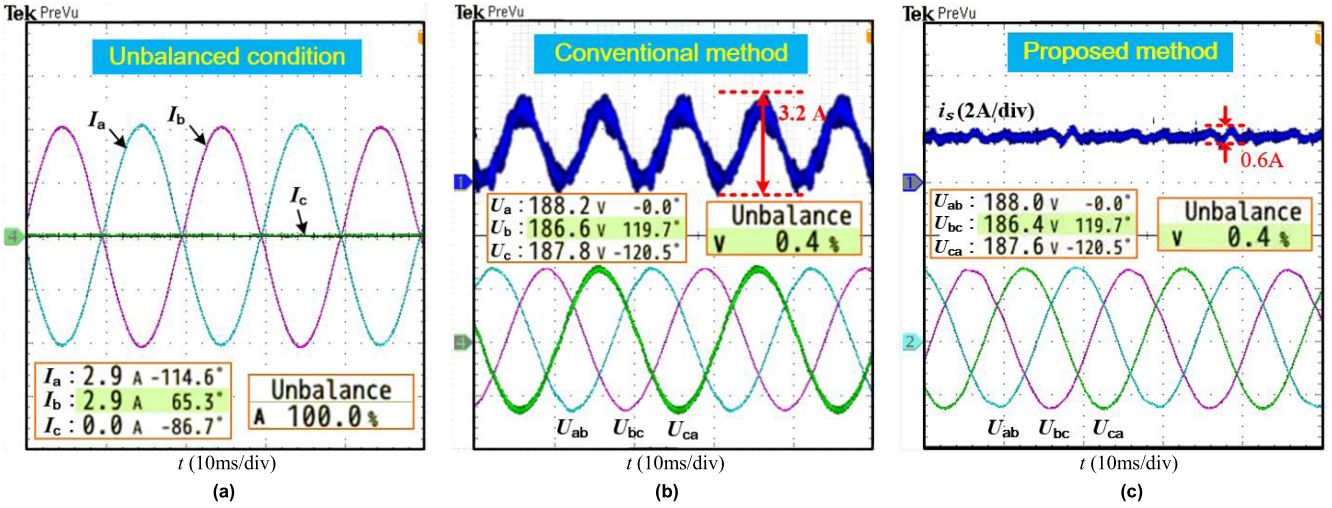

FIGURE 15. The experiment results of the conventional and improved three-phase VSC under unbalanced conditions in islanded mode.

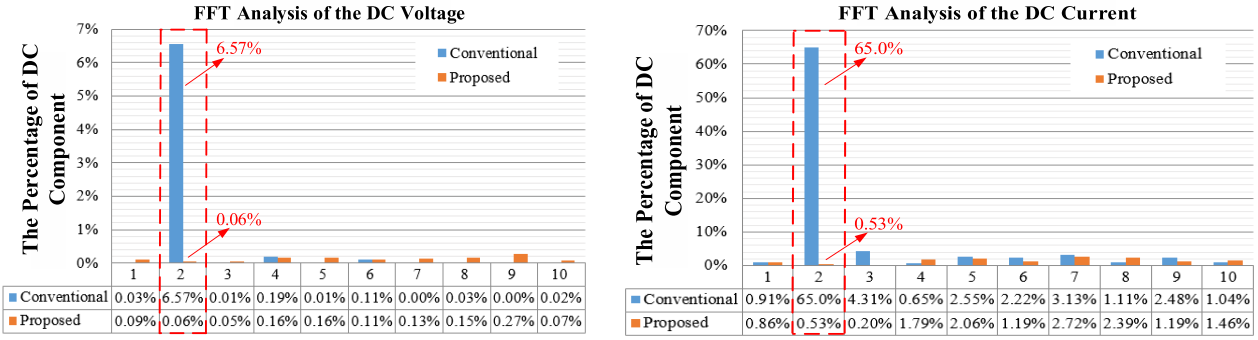

FIGURE 16. The FFT analysis of DC voltage in grid-connected mode and DC source current in islanded mode.

Next, Fig. 15 shows the results with unbalanced loads in islanded mode, where the output voltages are controlled to be balanced and the unbalanced ratio of the AC currents is 100% as shown in Fig. 15(a). It can be seen from Fig. 15(b) that the peak-to-peak value of the ripple current is 3.2 A for the conventional method, while it is only 0.6 A (see Fig. 15(c)) with the proposed method. This great improvement can also be observed from the FFT results in Fig. 16(b), where the

second-order component only accounts for 0.53% for the proposed method while it is 65% for the conventional method. Effectiveness of the improved topology under islanded mode can therefore be validated as well.

VI. CONCLUSION

In this paper, an improved three-phase VSC topology has been proposed for the grid-connected mode and islanded mode operation under unbalanced conditions. By introducing an extra conducting path into the system, the ripple current issue can be cost-effectively solved without increasing the size and complexity of the VSC system. With the proposed method, balanced current (or voltage) can be injected to the grid (or the load), and at the same time, the DC-source can be free from current and voltage ripples under unbalanced conditions. Although CM voltage is injected into the modulation to realize ripple power control loop, a little higher minimum requirement of DC link voltage and current stress are suffered compared with the conventional topology. Simulation and experimental results have been given to validate the effectiveness of the improved topology. It should be pointed out that application of the improved converter can also be extended to leakage current reduction and the high frequency circulating currents elimination in multiple parallel converters, which will be investigated in future work.

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