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A 62-90 GHz High Linearity and Low Noise CMOS Mixer Using Transformer-Coupling Cascode Topology

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ABSTRACT This paper presents a high linearity and low noise mixer for millimeter-wave applications in 65-nm CMOS process. A noise-reduction transformer with harmonic suppression is utilized and inserted between transconductance stage and switch stage to improve the linearity and noise figure (NF). Benefitted from the transformer-coupling cascode topology, the mixer can operate at a low supply voltage without sacrificing the linearity. In addition, this topology provides a great freedom for the choice of biases in transconductance stage and switch stage. Thus, linearity and noise performance can be further improved by optimizing the bias conditions of the two stages. According to experimental results, the proposed mixer exhibits a maximum conversion gain of 9.5 dB and a minimum single sideband NF of 9.2 dB with a local oscillator (LO) power of -3 dBm. The 3-dB bandwidth ranges from 62 to 90 GHz. The input 1-dB compression point ($P_{1\text{ dB}}$) is -3.8 dBm at 77 GHz. Due to the compact and fully symmetrical layout, the LO-to-RF isolation is better than 48 dB.

INDEX TERMS CMOS mixer, millimeter-wave applications, transformer-coupling topology, noise reduction, harmonic suppression.

I. INTRODUCTION

With the rapid development of wireless communication technology, millimeter-wave (mm-wave) frequencies have attained extensive attention. New products and services have been quickly emerged with huge market potential, such as multi-gigabit wireless personal area networks (WPANs) at 60 GHz, wireless fiber for the “Entire Last Mile” in E-band (71–75 GHz, 81–85 GHz, and 92–95 GHz), and anti-collision radars at 77 GHz [1]. For these applications, fabrication of mm-wave devices in CMOS processes remains attractive for the high integration and low cost [2], [3]. However, the poor linearity of devices in high frequency and inferior noise performance severely restrict the design of mm-wave circuits.

The mixer is an essential building block in transceivers. It is always required a sufficient linearity and a low NF to ensure the performance of the overall system. The Gilbert mixer has been widely used in CMOS circuits due to its high conversion

gain and low LO feed-through [4]. However, the conventional topology with three stacking transistors often suffers from poor linearity, which will deteriorate further when the supply voltage is reduced. Moreover, the noise performance may degrade significantly as operating frequency increases due to the parasitic capacitance between the transconductance stage (gm stage) and switch stage [5]. Improved Gilbert topologies have been proposed to enhance linearity or NF [6]–[9]. In [6] and [7], two RF mixers with third-order transconductance (g_{m3}) cancellation techniques are developed. However, they are not suitable for high-frequency applications, and also require a high supply voltage. The 31 GHz mixer presented in [8] applies multiple gate transistors (MGTR) to achieve an OIP3 of 21.4 dBm and a NF of 9.5 dB at the maximum gain. Nevertheless, the input third intercept point (IIP3) improvement is decreased when there has a large input signal. In [9], an active balun with common-source

and common-drain configurations employing common-mode noise and third-order intermodulation distortion cancellations is proposed for mm-wave CMOS mixer. An OIP3 of 12.4 dBm and a NF of 10.9 dB is achieved. However, the operation frequency and bandwidth are limited.

In this paper, a mm-wave mixer using transformer-coupling cascode topology (TCCT) is proposed. The noise-reduction transformer network with harmonic suppression is applied to improve the NF and linearity of the mixer. The dc path of the cascode configuration is also separated by the transformer to provide an independent bias for two stages. Therefore, the gm stage can be biased close to the 'gm3 zero-crossing point' without affecting the noise-optimization bias for the switch stage. Furthermore, the mixer features a wide bandwidth and can operate at a low supply voltage, which is suitable for multi-standard mm-wave radio applications.

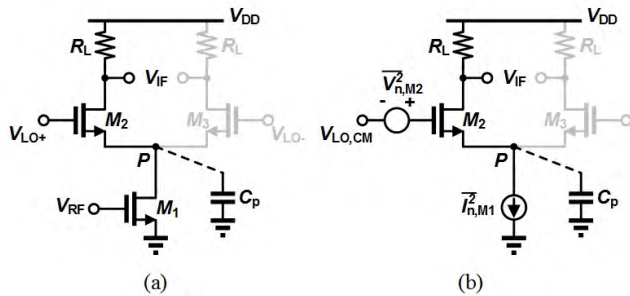


FIGURE 1. (a) Cascode topology and (b) noise sources in the single-balanced mixer at each half cycle.

II. CIRCUIT DESIGN AND ANALYSIS

A. IMPROVED NOISE FIGURE OF THE PROPOSED TOPOLOGY

To gain insight into the noise behavior of the proposed topology, a qualitative analysis for the conventional Gilbert mixer will be given first. Without loss of generality, consider the single-balanced mixer depicted in Fig. 1. In each half cycle of the LO, the circuit can be reduced to a cascode topology. By assuming abrupt LO transitions with a 50% duty cycle, the conversion gain in the presence of the Cp is expressed as [10].

$$A_{V,Cp} = \frac{2}{\pi} g_{m1} R_L \frac{g_{m2}}{\sqrt{C_p^2 \omega^2 + g_{m2}^2}} \quad (1)$$

where gmi denotes the transconductance of Mi, Cp is the parasitic capacitance at node P, and RL is the output load. The noise power at IF output is given by [10]

$$\overline{V_{n,IF}^2} = 2 \times \left[\frac{1}{2} \overline{I_{n,M1}^2} + \overline{V_{n,M2}^2} C_p^2 \omega^2 R_L^2 + 4kTR_L \right] \quad (2)$$

where In,M1 and Vn,M2 are the noise of transistors M1 and M2, k is the Boltzmann constant, and T is thermodynamic temperature. If (2) is divided by the square of (1), then the

input-referred noise voltage can be given as

$$\begin{aligned} \overline{V_{n,inCP}^2} &= \frac{(\overline{I_{n,M1}^2} + \overline{V_{n,M2}^2} C_p^2 \omega^2) R_L^2 + 8kTR_L}{\frac{4}{\pi^2} g_{m1}^2 R_L^2 \frac{g_{m2}^2}{C_p^2 \omega^2 + g_{m2}^2}} \\ &= \pi^2 \left(\frac{C_p^2 \omega^2}{g_{m2}^2} + 1 \right) kT \left(\frac{\gamma}{g_{m1}} + \frac{\gamma C_p^2 \omega^2}{g_{m2} g_{m1}^2} + \frac{2}{g_{m1} R_L} \right) \end{aligned} \quad (3)$$

Based on (1)-(3), it can be inferred that the input-referred noise is increased since the conversion gain decreases with effect of Cp. Besides, the term Vn,M2 Cp ω² (denoting the noise current injected by M2 into the IF output) in (2) is proportional to this capacitance. Therefore, at mm-wave frequencies, the effect of parasitic capacitances will become more serious, leading to a large RF current leakage and a significant degrade of noise performance.

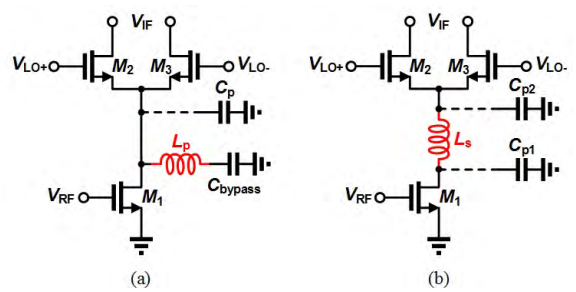


FIGURE 2. Schematic of the single-balanced mixer with (a) parallel and (b) series resonant inductor.

To overcome these drawbacks, a parallel [11] or a series [12] resonant inductor is designed and placed between the gm stage and switch stage, as shown in Fig. 2. Cp = Cp1 + Cp2 is the total parasitic capacitance. Lp and Ls are the inductors used to resonate the parasitic capacitances out. Both of the inductors are effective for reducing the noise of the cascode topology at mm-wave frequencies. Therefore, combing these two techniques and applying them to the design of mixer, the conversion gain and NF can be improved simultaneously. However, performing direct combination of these two inductors will occupy a large area. For this reason, a transformer is used to replace these two inductors. Fig. 3 (a) shows the transformer and its simplified equivalent model, which can be considered as a combination of series and parallel inductors. Fig. 3 (b) shows the schematic of the single-balanced mixer including the simplified equivalent model of the transformer. The noise contributed by Vn,M2 at the output port can be expressed as

$$V_{n,IF} = \frac{-R_L}{g_{m2}^{-1} + Z_P} V_{n2,M2} \quad (4)$$

where the impedance looking into node P (Zp) can be written as

$$Z_P(s) = \frac{s^3 C_{P1} (L_1 L_2 - M_{12}^2) + s L_2}{s^4 [C_{P1} C_{P2} (L_1 L_2 - M_{12}^2)] + s^2 (C_{P1} L_1 + C_{P2} L_2) + 1} \quad (5)$$

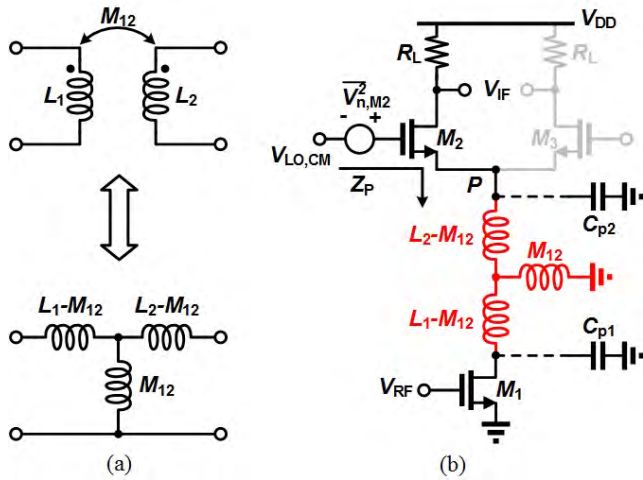


FIGURE 3. (a) Simplified equivalent model of the transformer and (b) single-balanced mixer including the transformer equivalent model.

Assuming drain-to-source resistance of the transistor M_1 is infinite. Note that if the denominator of (5) is approximately equal to zero, Z_P will tends to infinity so that the output noise in (4) is eliminated. Thus,

$$\omega^4 [C_{P1}C_{P2}(L_1L_2 - M_{12}^2)] - \omega^2(C_{P1}L_1 + C_{P2}L_2) + 1 = 0 \quad (6)$$

$$\omega^2 = \frac{(C_{P1}L_1 + C_{P2}L_2) \pm \sqrt{(C_{P1}L_1 - C_{P2}L_2)^2 + 4C_{P1}C_{P2}M_{12}^2}}{2C_{P1}C_{P2}(L_1L_2 - M_{12}^2)} \quad (7)$$

where ω is the frequency of interest for noise reduction. Since the device size of transistors and the operation frequency are determined, C_{P1} , C_{P2} and ω in (7) can be seen as constant. Therefore, the noise contribution of M_2 (also applies to M_3) can be minimized by properly tuning the design parameters L_1 and L_2 . Meanwhile, the conversion gain is changed by a factor β of (8), shown at the bottom of this page. It follows that

$$A_V = \frac{2}{\pi} g_{m1} R_D \beta \quad (9)$$

Note that (6) can be substituted in the denominator of (8) to produce and simplify

$$\beta = \frac{s^2 C_{P2}(L_1L_2 - M_{12}^2) + s g_{m2}(L_1L_2 - M_{12}^2) + L_1}{s^2 C_{P1}(L_1L_2 - M_{12}^2) + L_2} = \frac{C_{P2}(L_1L_2 - M_{12}^2) + \frac{1}{s} g_{m2}(L_1L_2 - M_{12}^2) + \frac{1}{s^2} L_1}{C_{P1}(L_1L_2 - M_{12}^2) + \frac{1}{s^2} L_2} \quad (10)$$

In our desired frequencies, the value of s is far greater than that of other terms and can be approximated as approaching

$$\beta = \frac{s^3 g_{m2} C_{P2}(L_1L_2 - M_{12}^2) + s^2 g_{m2}^2 (L_1L_2 - M_{12}^2) + s g_{m2} L_1}{s^4 C_{P1} C_{P2}(L_1L_2 - M_{12}^2) + s^2 (C_{P1} L_1 + C_{P2} L_2) + 1 + s^3 C_{P1} g_{m2} (L_1L_2 - M_{12}^2) + s g_{m2} L_2} \quad (8)$$

infinity. Thus, $C_{P2}(L_1L_2 - M_{12}^2)$ and $C_{P1}(L_1L_2 - M_{12}^2)$ dominate in the numerator and denominator respectively. Moreover, in most designs of Gilbert mixer, C_{P2} is not less than C_{P1} due to their transistor sizes, obtaining $\beta \approx 1$. Then, the conversion gain (9) with the noise-reduction transformer can be rewritten as

$$A_V = \frac{2}{\pi} g_{m1} R_D \quad (11)$$

and the input-referred noise voltage at the desired center frequency is thus given by

$$\overline{V_{n,in@fc}^2} = \frac{I_{n,M1}^2 R_D^2 + 8kTR_D}{\frac{4}{\pi^2} g_{m1}^2 R_D^2} = \pi^2 kT \left(\frac{\gamma}{g_{m1}} + \frac{2}{g_{m1}^2 R_D} \right) \quad (12)$$

Therefore, a compact transformer can be applied and inserted between two stages for noise and area reduction. The simulated NF_{min} of the proposed cascode with the transformer is 9.1 dB at 77 GHz, whereas the conventional cascode topology is 12 dB.

Fig. 4 compares the bias condition of the conventional cascode topology and the TCCT. Note that the transformer separates the dc path of the cascode configuration. If these two topologies work at the same supply voltage, each transistors in the TCCT can be assigned to a higher drain-to-source voltage than the conventional cascode topology, leading to a better linearity. This benefits from the reduction of a V_{DS} voltage in the TCCT. Thus, it also provides an approach of low-voltage designs in deep submicron processes. For a 65-nm CMOS process, using 1V supply voltage in a conventional Gilbert mixer will degrade the linearity because its multi-cascode structure leads the limited voltage headroom in gm stage. In this way, the mixer can operate at a low supply voltage without sacrificing the linearity.

B. LINEARIZATION METHOD AND MIXER DESIGN

In conventional Gilbert mixers, harmonics are generated mainly by nonlinearity of the gm stage [4]. Consider a common-source (CS) transistor biased in saturation region. Its small-signal output drain current can be expressed by using a Taylor series expansion as follows:

$$i_{ds} = g_m v_{gs} + g_{m2} v_{gs}^2 + g_{m3} v_{gs}^3 + \dots \quad (13)$$

where v_{gs} is the small-signal gate-to-source voltage, and $g_{m(n)}$ represents the n^{th} -order transconductance. The third-order coefficient g_{m3} performs an important role in the generation of the nonlinear harmonic. Then the IP3 can be expressed as:

$$IP3 = \sqrt{\frac{4}{3} \frac{g_m}{g_{m3}}} \quad (14)$$

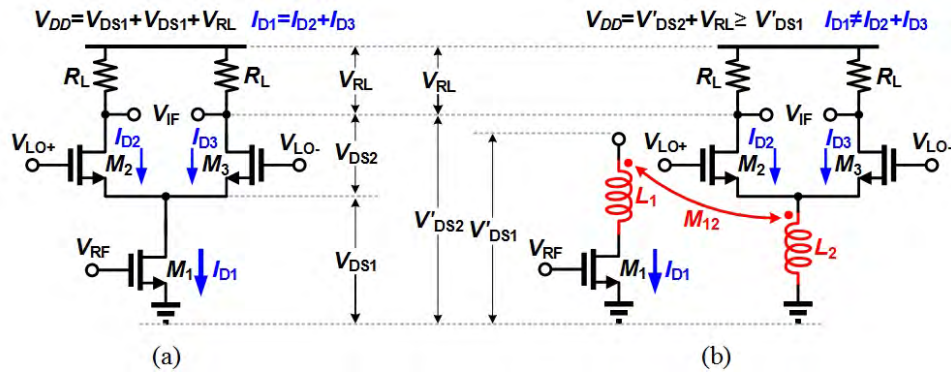


FIGURE 4. Bias condition of the single-balanced mixer using the (a) conventional cascode topology and the (b) TCCT.

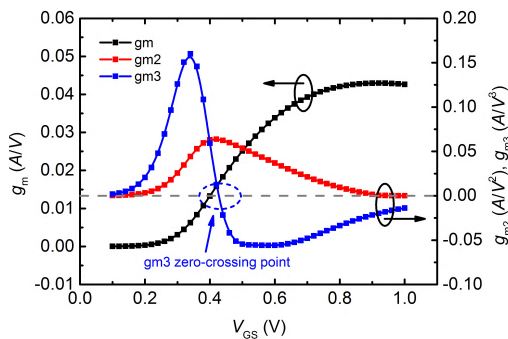


FIGURE 5. Expansion coefficients of g_m vs. V_{GS} at 1 V V_{DS} .

The IP3 of the device can be improved by reducing g_{m3} . Fig. 5 shows the expansion coefficients of g_m versus V_{GS} , which are calculated according to [13]. Note that there is a zero crossing point of g_{m3} . Since the TCCT provides an independent bias for two stages, the nonlinear effect of g_{m3} can be effectively alleviated if the g_m stage is consciously biased close to this point. In this work, the gate-to-source voltage of the g_m stage is set about 460 mV for avoiding a large g_{m3} . The switch stage is separately biased by a relatively small current source ($I_{D1} > I_{D2} + I_{D3}$) for reducing its noise contribution [5], as shown in Fig. 4. Besides, as the operation frequency increases to mm-wave frequencies, the utmost achievable linearity of the mixer is limited by the second-order interaction effect [7]. The generated second-order harmonics can couple back to the input of the g_m stage through the parasitic capacitor C_{gd} . Especially in this case, the second-order expansion coefficient g_{m2} reaches its peak when the transistors are biased around the zero-crossing point of g_{m3} . The second-order harmonics coupling to the positive and negative input sides of g_m stage are common-mode signals. But when they mix with the differential input fundamental signals, the IMD3 are generated and the linearity is deteriorated. Thus, an additional network with harmonic suppression is adopted. Fig. 6 shows a pair of series resonance tanks realized by open stubs at the primary input of the transformer. The resonance tanks resonate at the second

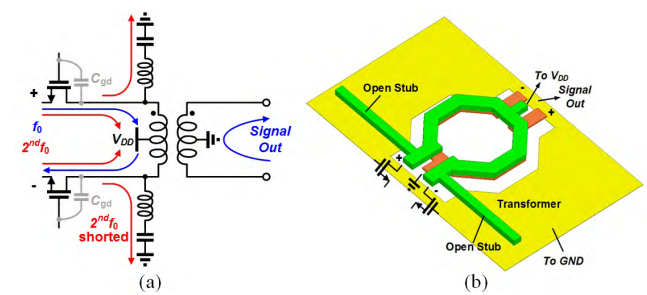


FIGURE 6. (a) Schematic and (b) proposed layout of the noise-reduction transformer with harmonic-suppression.

harmonic frequency, which causes the load impedance of the second harmonic frequency close to zero. As a result, the second harmonic components are shorted to the ground, instead of mixed with the fundamental signal. Fig. 7 shows the IIP3 comparison of the mixer with and without harmonic suppression network. The IIP3 is improved about 4.8 dBm from 5.8 to 10.6 dBm.

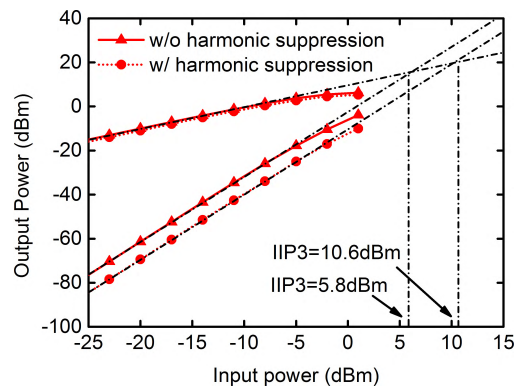


FIGURE 7. IIP3 comparison of the mixer with and without harmonic suppression.

Fig. 8 shows the simplified schematic of the proposed E-band mixer. The circuit is based on a double-balanced Gilbert structure. Transistors M_1 - M_2 ($36 \mu\text{m}/90 \text{ nm}$) are the

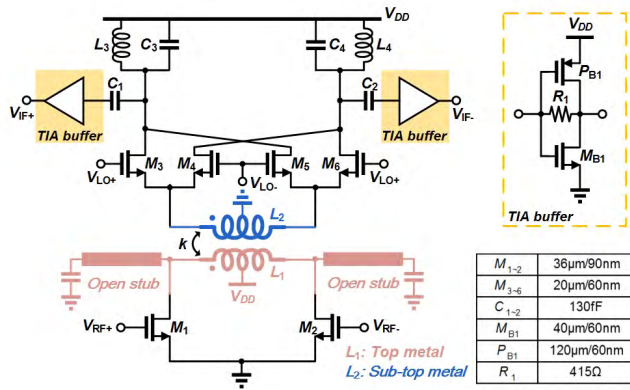


FIGURE 8. Simplified schematic of the proposed mixer.

gm stage for the RF input signal. The channel lengths are designed to be 90 nm for reducing the impedance transformation ratio between the 50-Ω source impedance and the large input impedance (mainly due to the imaginary part) looking into the gate of gm stage. Thus it is easy to implement a low loss in RF input balun with a broadband characteristics [14]. Large transistor size also mitigates the random mismatch and potential dc offset which helps to reduce the LO leakage power [15]. Transistors M_3 - M_6 (20 μ m/60 nm) are the switch stage driven by the local oscillator (LO) signals. The switching transistors are optimized to have a small overdrive voltage and thus allows a relatively low LO driving. A transimpedance amplifier (TIA) buffer stage is designed for practical applications. The 6-ports transformer network between gm stage and switch stage realizes noise reduction and harmonic suppression, while providing biases at the center tap. In such a transformer, the top two metals are used to improve the quality factor Q . A coupling coefficient k are optimized as 0.7 for a trade-off between bandwidth and gain [16]. The inductances of L_1 and L_2 are designed according to (7). To obtain a low loss, a regular octagonal shape is used in implementing the transformer. The resonance tank is realized by open stub. It needs to be carefully designed to ensure that there is no unnecessary coupling with the surrounding and negligible influence on the noise performance. Therefore, extensive electromagnetic (EM) simulations are required for the transformer network design. In this work, except the active devices, the entire layout is characterized by the EM simulator high frequency structure simulator (HFSS).

III. MEASUREMENT RESULTS

The proposed mixer is fabricated in a commercial 65-nm CMOS process. Fig. 9 shows a die microphotograph of the chip. The total chip size of the mixer is $0.62 \times 0.85 \text{ mm}^2$, including all testing pads and on-chip baluns. For the practical application, TIA output buffers are included in the design to enhance the drive capability. Operating at a 1-V supply voltage, the total dc power consumption is 15 mW, including IF buffers.

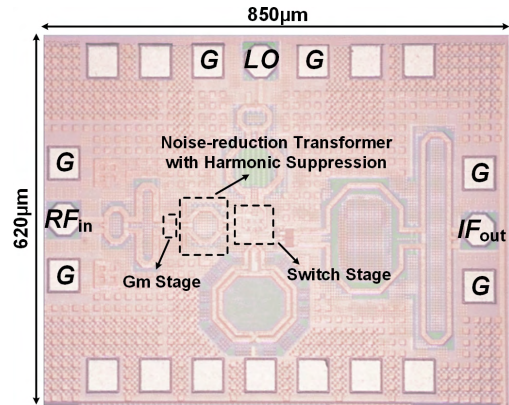


FIGURE 9. Die microphotograph of the proposed mixer.

The measurements are performed on a high-frequency probe station. The dc pads are directly wire-bonded to a printed circuit board (PCB) on standard FR-4 substrate. The signal pads are accessed through the GSG probes. The loss of the input cable and the probes are measured by a vector network analyzer (R&S ZVA67 & R&S ZVA-Z90E extension modules), and the values are manually entered into the spectrum analyzer (R&S FS67) to exclude their effect on the measurement.

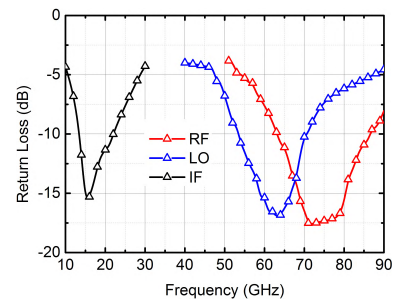


FIGURE 10. Measured return loss at the RF, LO and IF ports.

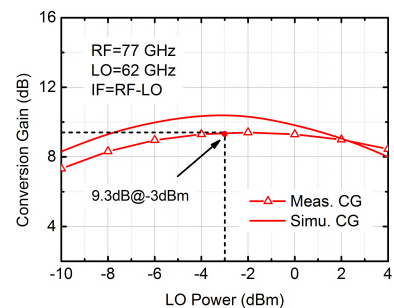


FIGURE 11. Simulated and measured conversion gain vs. the LO power at 77 GHz.

Fig. 10 shows the measured return loss at the RF, LO and IF ports. All of them are well matched within the operation frequencies. Fig. 11 shows the simulated and measured conversion gain versus the LO power with an RF input at 77 GHz and an LO frequency at 62 GHz. For low LO drive in

TABLE 1. Performance comparison of the state-of-the-art mixer.

Ref.	Tech.	Mixer Topology	Freq. (GHz)	Gain (dB)	NF (dB)	Input P _{1dB} (dBm)	LO power (dBm)	Isolation (dB)	Area (mm ²)	Power (mW)
[8]	45 nm SOI	MGTR	30.5-49	3.4	9.5	-4.2	3	37	0.8	21.2 @1.5V
[9]	65 nm	Double-Balanced	57-66	5.6	11	-7	0	35	0.35×0.41**	10 @1V
[17]	65 nm	Single-Balanced	77	6.8	21	-7	-5	-	0.79×0.59	3* @1.2V
[18]	90 nm	Source-Driven	53-70	5.9	16	-15.1	-6	37	0.55×0.55	3 @1.2V
This work	65 nm	TCCT	62-90	9.5	9.2	-3.8	-3	48	0.62 × 0.85	15 @1V

*: without buffer **: core area

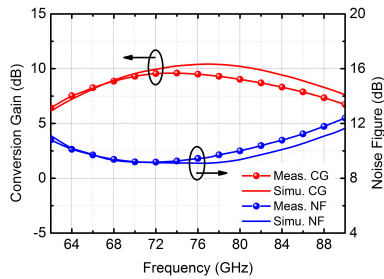


FIGURE 12. Simulated and measured conversion gain and NF vs. frequency.

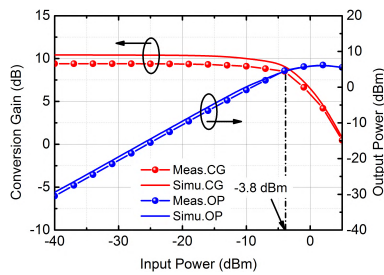


FIGURE 13. Simulated and measured input P_{1dB} and output power vs. input power at 77 GHz.

mm-wave applications, the LO power of -3 dBm is selected in this work for presenting measured data. Fig. 12 shows the simulated and measured conversion gain and NF, exhibiting a wide gain bandwidth from 62 to 90 GHz with a peak conversion gain of 9.5 dB and a minimal single sideband NF of 9.2 dB. It can be seen that the obtained measurements coincide well with the simulations. The large signal performance is showed in Fig. 13. When the working frequency is 77 GHz, the input P_{1dB} is -3.8 dBm, which is much better than the previous reported work. Due to the compact and fully symmetrical layout, the LO-RF isolation is better than 48 dB. Table 1 summarizes the performance of this mixer and compares it with other state-of-art works.

IV. CONCLUSION

A TCCT with harmonic suppression is presented, analyzed and applied to the design of mm-wave Gilbert mixer for the improvement of NF and linearity. Based on this topology, the proposed mixer can operate at a lower supply voltage without sacrificing the linearity. Moreover, the independent bias of two stages could further improve the NF and linearity

of the mixer. Compared with other works in CMOS process, the performance of this mixer is superior to the previously reported works.

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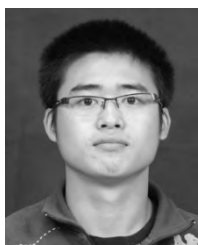
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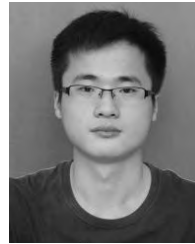


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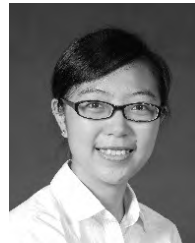
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