FPGA-Based Architecture for Medium Access Techniques in Broadband PLC

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ABSTRACT In this paper, two real-time architectures of medium access techniques useful for future generation of wireline and wireless communication systems are presented. One architecture is based on discrete cosine transform (DCT), while the second approach implements a filter-bank multi-carrier (FBMC) system. A comparative analysis, in terms of resource consumption, performance, and precision, is shown. The comparison considers a floating-point model, a fixed-point model, and experimental tests. These models make it possible to evaluate the effect of the fixed-point precision in the implementation and, in turn, to verify the correctness of the developed architecture. The simulation models and the experimental tests have been carried out in different practical environments in order to achieve a further analysis. The two proposed architectures have been implemented on a field-programmable gate array (FPGA) device. Furthermore, the architectures have been included as advanced peripherals in a system-on-chip, which also integrates a soft microprocessor to monitor the whole system and manage the data transfers. As a communication scenario, the proposed architectures have been particularized to operate in real time while meeting all timing requirements defined by a broadband power line communications standard. For that case, the system has achieved a desired transmission rate of 62.5 Ms/s at the converters, providing mean squared errors, at the output for an ideal channel, below $3 \cdot 10^{-5}$ for both the DCT and FBMC approaches, whereas each transmitter/receiver requires around 50% of the DSP cells available in the Xilinx XC6VLX240T FPGA, the most demanded resource in the device.

INDEX TERMS Field-programmable gate arrays, multi-carrier communication (MCM), filter-bank multi-carrier (FBMC) systems, broadband power-line communications, discrete cosine transform (DCT).

I. INTRODUCTION

Multicarrier Modulation (MCM), such as discrete multi-tone (DMT) and Orthogonal Frequency Division Multiplexing (OFDM), is currently the most adopted transmission scheme in both wired and wireless communication standards (e.g., [1]–[6]). When MCM is implemented by means of fast algorithms of the Discrete Fourier Transform (DFT) [7], it has several advantages such as low complexity, effectiveness against multipath, or frequency selective channels [8]. Nevertheless, DFT-based MCM is also questioned because of some weaknesses. One important drawback is the high sensitivity to synchronization errors [9], and particularly to Carrier Frequency Offset (CFO) coming either from differences between the oscillators at the transmitter and receiver or from the Doppler effect. The CFO involves two aspects: the reduction of the signal magnitude, since signals are not sampled at the expected time stamp; and the appearance of inter-carrier interference in the system, since the subcarriers are no longer orthogonal. Other weaknesses of DFT-based systems are the spectral/power inefficiency due to the guard intervals (the Cyclic Prefix CP that is often inserted), and the poor spectral containment of DFT-based subcarriers.

For the above reasons, new alternatives to OFDM have appeared during the last years, with the aim of improving the above OFDM drawbacks. In order to deal with the CFO problem, several authors have proposed the use of Discrete Trigonometric Transforms (DTT) for multicarrier modulation, mainly Type-II even and Type-IV even Discrete Cosine Transforms (DCT2e and DCT4e) [8], [10]–[12]. On the other hand, Filter-Bank Multicarrier (FBMC) modulation is a

promising technique for future wireline and wireless communication standards [13]–[15]. It avoids the use of redundant samples as the CP, and with FBMC systems, an increase in spectral efficiency and robustness to synchronization requirements can be achieved. In addition, FBMC allows more robustness in noisy environments, such as the power line channels [16]. For this reason, a type of FBMC is recommended in a physical layer of the IEEE 1901 Standard for broadband Power Line Communications (PLC) [4].

All these approaches imply a significant and complex computational load, which makes any feasible real-time architecture difficult. They often require high data rates and transfers, with high sampling frequencies and different parallel datapaths to be implemented. All these features imply that the design of an efficient architecture suitable for the implementation of novel medium-access multi-carrier techniques is a relevant topic nowadays. For that purpose, Field-Programmable Gate Array (FPGA) devices have become a feasible and suitable alternative for the implementation and first prototyping of algorithms in communication applications [17]–[19] requiring high clock frequencies, adaptability or flexibility, a certain degree of parallelism, and need for intermediate data storage. As a result, it is possible to find previous works where FPGAs are the key element in the proposal of architectures for the implementation of different multi-carrier modulations [6], [20]–[23]. In [24] a hardware architecture is proposed for 5G standard, dealing with an FBMC modulation. This work is extended in [25] with a detailed description of the pipelined architecture for the transmitter. A further step is proposed in [26], where FPGA coprocessor is merged together with GPPs (General-Purpose Processors), also for 5G. Furthermore, in this trend, it is also interesting to consider FPGA-based System-on-Chip (SoC) [27], where the die is often shared by a general-purpose processor and the configurable logic resources, merging the advantages of both sides.

With regard to the PLC standard, a transceiver based on OFDM and implemented on a Xilinx Spartan6 FPGA is described in [28], with data rates up to 107Mbps. In [29], a synchronization algorithm for OFDM is implemented on a FPGA for the same standard. A final example can be found in [30], where an OFDM physical layer for 3G-PLC is designed and implemented on a FPGA, together with an ARM processor in charge of higher-level algorithms.

The main contribution of this work is the proposal of an FPGA-based SoC architecture to deal with the real-time implementation of different MCM techniques, using broadband PLC as case study. The transmultiplexers for the different modulations considered can be inserted as advanced peripherals in the SoC architecture, achieving the required data rates and bandwidths. Two multi-carrier modulation schemes have been taken into account: one based on DCT4e and the other on FBMC. The SoC architecture has been evaluated, and, furthermore, a comparison between the two multi-carrier modulations has been carried out, in terms of resource consumption and fixed-point representation errors.

Compared to [23], which was focused on the single implementation of an FBMC approach, this work proposes and describes this novel SoC architecture, where peripherals for different modulation schemes can be integrated, which is a key aspect to achieve a flexible real-time system. Furthermore, the feasibility of the architecture has been verified by integrating, not only the FBMC approach in [23], but also a particular implementation for an approach based on DCT4e presented here. Finally, a final comparison between both, the FBMC and the DCT4e approaches, based on some preliminary experimental tests is shown. The rest of the manuscript is organized as follows: Section II describes the global SoC structure; Section III is dedicated to the architectures proposed for the implementation of the different medium-access techniques considered; Section IV shows some experimental results; and finally, conclusions are discussed in Section V.

II. GENERAL SYSTEM DESCRIPTION

The global SoC architecture is based on an FPGA device [31], where it is possible to integrate different multi-carrier transmitters and receivers, as can be observed in Fig. 1. A Microblaze soft microprocessor [32] is in charge of the management and control of the global system. It is worth noting that other processors with higher performance, such as ARM in Zynq architecture by Xilinx Inc., can easily replace Microblaze in the proposal, although the latter can cope with the current computational load.
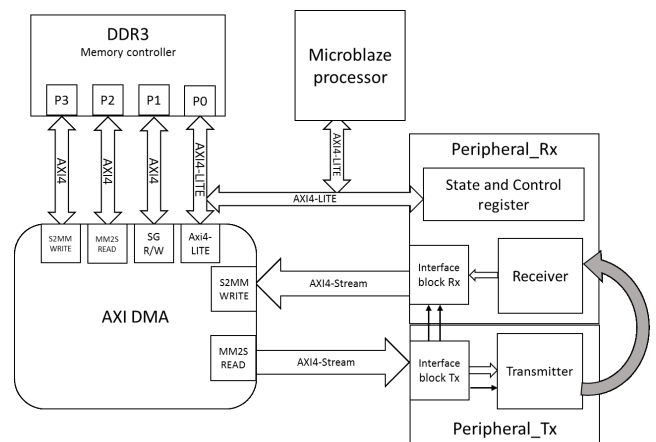

FIGURE 1. General block diagram of the proposed SoC architecture.

The architecture allows the flexible integration of any transmitter and/or receiver, corresponding to any medium-access technique (not only those described later), as an advanced peripheral (hardware accelerator). It is important to remark that these transmitters and/or receivers (peripherals) can be easily packaged and distributed as IP cores for its integration in any system based on AXI bus.

The data rate demanded by the communication standard is provided by a Direct Memory Access (DMA) controller, thus making it possible to transfer data from an external memory to the transmitter and from the receiver to an external memory [33]. The implemented MCM techniques provide a

solution with multiple input/output datapaths. For that reason, the DMA controller is used to generate suitable data rates for the transmitter and the receiver. The DMA is connected to an external DDR3 memory bank through a memory controller [34]. This releases the Microblaze processor from data-moving operations and allows it to perform only system management tasks. The DMA presents independent buses to communicate with the transmitter and the receiver.

With regard to the advanced peripherals, they should involve the communication interfaces with the corresponding DMA bus at the demanded rates. Furthermore, they include some control and status registers to be accessed and configured by Microblaze. All the buses involved in the architecture are based on several specifications of the AXI bus.

For clarity's sake, two medium-access techniques have been considered hereinafter as an example to show the feasibility and performance of the proposed SoC architecture. These techniques are based on the DCT4e and on an FBMC system. Nevertheless, it is worth noting that any other approach could be taken into account and integrated in the SoC architecture.

III. TYPE-IV EVEN DISCRETE CONSINE TRANSFORM MULTICARRIER MODULATION (DCT4e-MCM)

Several authors have proposed the use of DCT instead of DFT because the former offers benefits such as (1) excellent spectral compaction and energy concentration, which leads to less inter-carrier interference leakage to adjacent subcarriers; (2) more robustness against CFT; and (3) the use of only real arithmetic [8], [10]–[12].

FIGURE 2. Block diagram of the proposed DCT4e-MCM. Transmitter (left) and receiver (right).

Fig. 2 shows the block diagram to implement multicarrier modulation with DCT4e. At the transmitter (left side), data

are processed by an M-point inverse DCT4e, with M being the number of subchannels or subcarriers. At the receiver (right side), a DCT4e of the same size is performed. Note that the orthogonal definition of DCT4e is the same as that of its inverse counterpart [35]. Furthermore, when the DCT4e is used for multicarrier data transmission, the inter-block interference can be eliminated by adding a Symmetric Extension (SE) to each symbol, including a left prefix and a right suffix. We refer the reader to [10] for more information about the system configuration of DCT4e-MCM.

Focusing on Fig. 2, the input data $X_m[k]$ are modulated in a multicarrier scheme by means of the DCT4e [10]. Afterwards, an SE is added to the signal $p_m[n]$, thus obtaining $q_s[n]$. This signal is serialized to be transmitted through the channel. At the receiver, the signal $r[n]$ is deserialized to obtain $q'_s[n]$. The corresponding SE is removed and the resulting signal $p'_m[n]$ is inserted in the DCT4e module, obtaining the output signal $X'_m[k]$.

On both sides, transmitter and receiver, the DCT4e is defined by

$$p_m[n] = \sqrt{\frac{2}{M}} \cdot X_m[k] \cdot \cos\left[\frac{\pi}{M}\left(m + \frac{1}{2}\right)\left(n + \frac{M+1}{2}\right)\right],$$

(1)

where $p_m[n]$ is the output from the DCT4e, M is the number of points in the transform, and $X_m[k]$ is the corresponding input. The block can be divided into four stages:

- s1: Generate the sequence $Y_m[k]$ by multiplying the input signal $X_m[k]$ by a constant $e^{-jm\pi/2^M}$:

$$Y_m[k] = X_m[k] \cdot e^{-\frac{jm\pi}{2M}}$$

(2)

- s2: Obtain the signal $y_m[n]$ by applying a Fast Fourier Transform (FFT) on $Y_m[k]$ according to

$$y_m[n] = F\{Y_m[k]\}$$

(3)

where the operator $F\{\}$ performs an M-points FFT.

- s3: Rearrange the signal $y_m[n]$, obtaining the signal $z_m[n]$:

$$z_{2i+1}[n] = y_i[n]$$
$$z_{2i}[n] = conj\{y_{m-i}[n]\}$$

(4)

where $i = 0, \ldots, M/2 - 1$; $y_i[n]$ is the output from the FFT; and the operator $conj\{\}$ is the conjugate of the sample.

- s4: Generate the sequence $p_m[n]$ from the signal $z_m[n]$ by multiplying it by the constant $e^{-j\pi(2m+1)/4^M}$ according to

$$p_m[n] = 2 \cdot \frac{1}{\sqrt{2M}} \cdot Re\left\{z_m[n] \cdot e^{-\frac{j\pi(2m+1)}{4M}}\right\}$$

(5)

where $z_m[n]$ is the output from the rearrangement, $p_m[n]$ is the output from the DCT, and $Re\{\}$ is the real part.
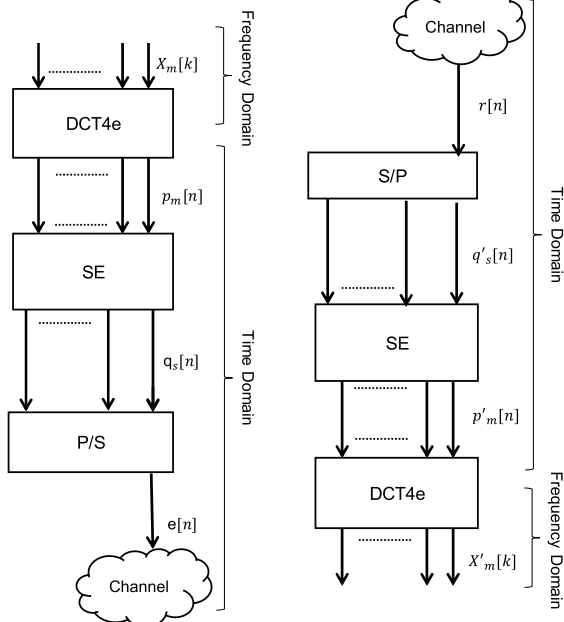
FIGURE 3. Block diagram of the architecture proposed for the DCT4e-MCM transmitter.
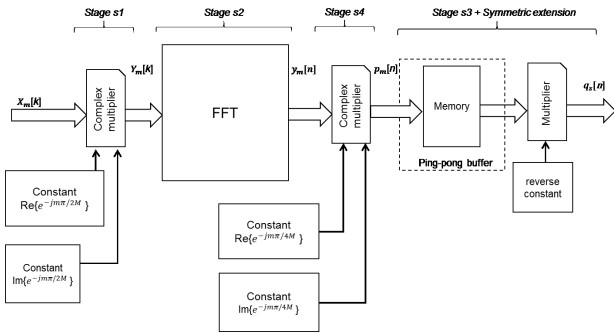

FIGURE 4. Block diagram of the architecture proposed for the DCT4e-MCM receiver.

A. DCT4e-MCM ARCHITECTURE

The DCT4e-MCM architecture is divided into two parts: the SE and the DCT4e. First, the SE replicates the beginning and end of the output array $p_m[n]$ to improve the transmission. This extension is carried out according to

$$q_s[n] = p_{\alpha-1-s}[n] \quad if \; 0 < s < \alpha$$

$$q_s[n] = p_{s-\alpha}[n] \quad if \; \alpha \le s < M + \alpha$$

$$q_s[n] = -p_{M-1-s+M+\alpha}[n] \quad if \; M+\alpha \le s < M+2\cdot\alpha \quad (6)$$

where $q_s[n]$ is the final signal to be serialized and transmitted, α is the length of the extension, and $s = 0, 1, \ldots, M + \alpha - 1$ and $m = 0, 1, \ldots, M - 1$.

As has already been mentioned before, the DCT4e has been divided into four stages (from s1 to s4), each one consuming their corresponding resources in function of the parallelism ratio. The parallelism ratio R_p is defined as the number of samples simultaneously processed by the architecture and is related to the number of parallel datapaths (lanes) existing in the proposal. In this way, a high R_p implies more resources but better throughput in the architecture, whereas a low R_p means less resources, reutilized over time, with lower throughput. These four stages have been assembled together with the SE module in order to obtain the architecture for the DCT4e-MCM transmitter, which can be observed in Fig. 3. Note that the stage s4 has been placed before s3, so this last one can use the same memory block as the SE. This transmitter architecture requires 49 multipliers for its implementation. Furthermore, since all the architecture has been pipelined, it presents a global latency of 1258 clock cycles.

On the other hand, it is possible to propose a similar architecture for the DCT4e-MCM receiver, considering the previous blocks in a reversed order, as is shown in Fig. 4. Note that in this case the stage s3 and the SE cannot share the same memory block. Here the architecture requires 48 multipliers and, due to the pipelined structure, presents a 1768-clock cycles latency. It is worth noting that the receiver requires one less multiplier, since the multiplier involved in the SE is merged together with the ones implemented in stage s1.
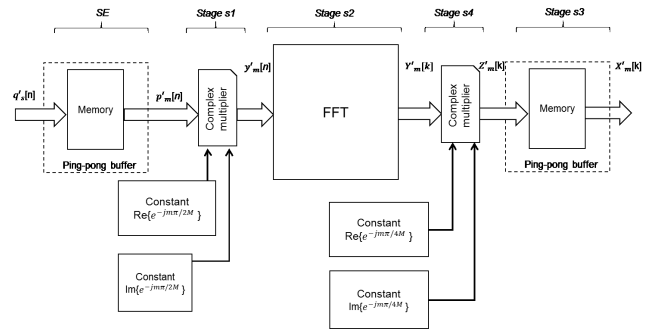
IV. FILTER-BANK MULTI-CARRIER (FBMC) APPROACH

The second MCM technique considered here, the FBMC approach, is based on a type of cosine-modulated filter bank. The proposed system and its implementation have been thoroughly studied in [16] and [23]. This technique also involves the same DCT4e module as in the DCT4e-MCM approach, together with a polyphase filtering bank that allows a better spectral separation between subcarriers than the OFDM solution. Another additional advantage of FBMC in general, and of this approach in particular, is that it does not require the inclusion of redundant samples, such as the SE.

The proposed FBMC transmitter can be observed in Fig. 5 (up). Following the scheme, each input signal $V_m[k]$ is multiplied by a constant θ_m. This constant ranges from -1 to $+1$, depending on the considered subcarrier m. This multiplication generates the signal $X_m[k]$, which is sent to the DCT4e module to obtain $p_m[n]$. The signals $p_m[n]$ go through a module that performs arithmetic computations, represented by matrices **I** and **J**. These matrices provide the signal $q_s[n]$ to be inserted in the polyphase filter bank. The resulting signals $t_s[n]$ are added in pairs to obtain the corresponding M subcarriers. Finally, the signal is serialized and sent through the communication channel.

On the other hand, at the receiver, the involved processing is described in Fig. 5 (down). The received signal $r[n]$ is deserialized and inserted in the filter bank. This bank is the same as the one in the FBMC transmitter. The obtained signals $q'_s[n]$ are processed by the matrices **I** and **J** to obtain $p'_m[n]$ and then inserted in the DCT4e module. Finally, this signal is multiplied by the constant θ_m to obtain the output signal $V'_m[k]$. We refer the reader to [16] and [23] for more information about the system model and a detailed architecture for the approach.

V. EXPERIMENTAL RESULTS

The proposed SoC architecture has been implemented in a Xilinx Virtex6 xc6vlx240t FPGA [36]. The resource consumption of the global system is presented in Table 1. Note that it consists of the Microblaze microprocessor, the external memory control, the DMA module, the synchronization
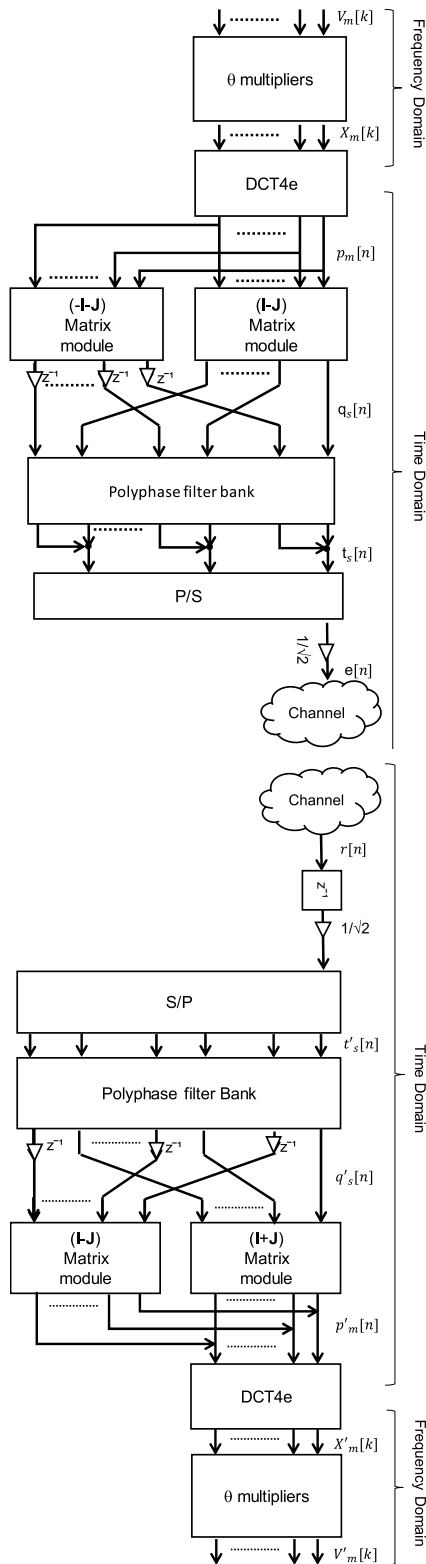
FIGURE 5. Block diagram of the proposed FBMC transmitter (up) and receiver (down).

TABLE 1. Resource consumption for DCT4e-MCM and FBMC in the global SoC architecture in a Xilinx xc6vlx240t FPGA.

	Flip Flops	*LUTs*	*BRAMs*	*DSP48E1*
Global system	12993	31659	107	93
Microblaze	1445 (11.12%)	3746 (11.83%)	19 (17.76%)	4 (4.30%)
AXI4	3658 (28.15%)	9230 (29.15%)	9 (8.41%)	0 (0.00%)
DDR3 Control	3123 (24.04%)	6506 (20.55%)	0 (0.00%)	0 (0.00%)
DMA module	1170 (9.00%)	2608 (8.24%)	2 (1.87%)	0 (0.00%)
Synchronization module	57 (0.44%)	131 (0.41%)	3 (2.80%)	0 (0.00%)
DAC Control	594 (4.57%)	1178 (3.72%)	3 (2.80%)	0 (0.00%)
ADC Control	144 (1.11%)	358 (1.13%)	0 (0.00%)	0 (0.00%)
Interface Block Tx	90 (0.69%)	181 (0.57%)	2 (1.87%)	0 (0.00%)
Transmitter DCT4e-MCM	1245 (9.58%)	3567 (11.27%)	33 (30.84%)	45 (48.39%)
Transmitter FBMC	1397 (9.58%)	3724 (11.27%)	45 (31.91%)	49 (47.11%)
Interface Block Rx	172 (1.32%)	393 (1.24%)	0 (0.00%)	0 (0.00%)
Receiver DCT4e-MCM	1060 (8.16%)	3197 (10.10%)	36 (33.64%)	44 (47.31%)
Receiver FBMC	1096 (8.16%)	3232 (10.10%)	58 (41.13%)	51 (49.03%)

consumption, a percentage with respect to the total architecture consumption is presented. Note that DCT4e-MCM and FBMC transmitters/receivers can be easily packaged and distributed as IP cores for their integration into any system based on AXI bus.

In order to obtain an experimental setup suitable for the validation of the proposed SoC architecture, the final design requires a synchronization module, as well as the corresponding analog–digital converters. Fig. 6 shows the final assembly, where a DAC (digital–analog converter) controller and an ADC (analog–digital converter) controller have been added in the transmitter and receiver datapaths, respectively, compared to that shown in Fig. 1. Furthermore, since a synchronization solution is out of the scope of this work, an ideal synchronization module has also been considered. Note that a real synchronization solution will affect the final performance in a certain degree, depending on the considered algorithm.

Fig. 7 shows the global experimental architecture for tests. Both converters, the ADC AD9467 [37] and the DAC FMC204 [38], have a 16-bit data width. This is a limitation that influences the fixed-point representation used for the implementation of the system. The converters have maximum sampling frequencies of 1 GHz for the DAC and 250 MHz for the ADC. In these tests, since we use the broadband PLC of IEEE 1901 as a study case [4], a transmission rate of 62.5 Msps has been considered, so these converters are able to transmit the corresponding signals. Furthermore, a suitable Analog Front-End (AFE) is necessary [3]. Nevertheless, the design of this AFE has not been included in this work and the following experimental results have been obtained in a PLC channel that is not connected to the grid.
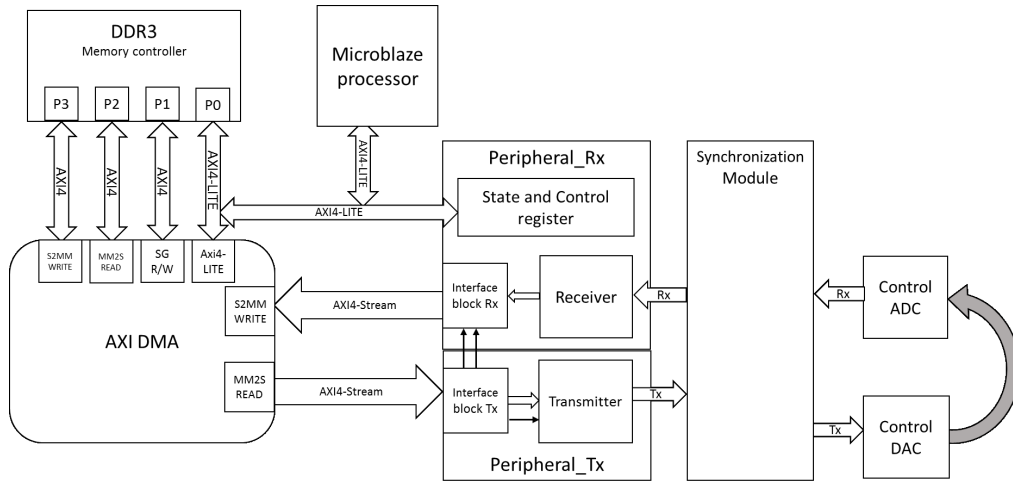
module, and the converter controllers. Table 1 shows the global resource consumption as well as the resource consumption required by each module. In addition to the resource

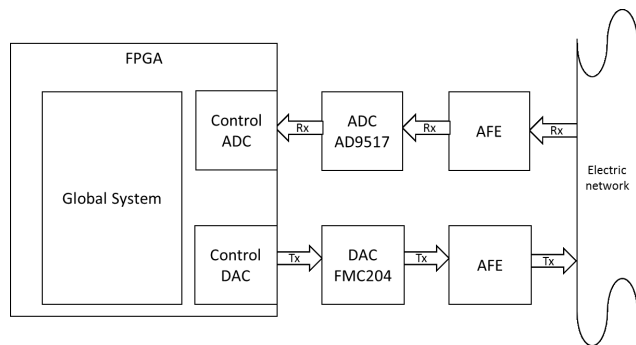**FIGURE 6.** Global SoC architecture developed for experimental tests.

FIGURE 7. Global experimental setup.

The Microblaze processor is in charge of generating the data to be transmitted. For that purpose, Pulse Amplitude Modulation (PAM) with 2, 4, 8, 16, and 32 levels has been implemented according to the PLC standard [4]. Thanks to the use of the PAM modulation, the Symbol Error Rate (SER) values for the ideal channel can be estimated. Also, the Signal-to-Noise Ratio (SNR), the Mean Square Error (MSE), the Peak Signal-to-Noise Ratio (PSNR), and the Maximum Error (ME) are calculated.

To obtain all these parameters, three types of tests have been carried out. Firstly, a floating-point simulation of the techniques is performed, which will be considered as a reference for further comparisons. Then, a fixed-point simulation describing the implemented architecture is used to verify the quality of the proposed fixed-point solution. Finally, the experimental tests are also included in the comparison to analyse the correspondence between simulations and real tests.

For the first real test case, an ideal channel has been considered, so the transmitter and the receiver are connected internally inside the FPGA (digital loopback). This ideal channel is used to verify the quality of the fixed-point representation defined for the global architecture. Fig. 8 shows the SNR for the DCT4e-MCM approach (left) as

TABLE 2. Performances obtained with the different proposals using an ideal channel.

		SNR	MSE	PSNR	ME
Experimental test	FBMC	45.35	$2.42 \cdot 10^{-5}$	50.04	0.0073
	DCT4e-MCM	45.44	$1.85 \cdot 10^{-5}$	50.13	0.0072
Fixed-point simulation	FBMC	43.64	$2.88 \cdot 10^{-5}$	48.33	0.0115
	DCT4e-MCM	43.83	$2.65 \cdot 10^{-5}$	48.54	0.0089
Floating-point simulation	FBMC	57.34	$1.57 \cdot 10^{-6}$	62.03	0.0080
	DCT4e-MCM	65.84	$3.13 \cdot 10^{-7}$	70.53	$7.99 \cdot 10^{-4}$

well as for the FBMC (right). To obtain these parameters, both simulations use the same input signal with a length of 40960 samples. This input signal is randomly generated in a range of [−1, 1]. The value provided for every subchannel m is the average of 80 packets, each with 512 samples. The final figures of merit are obtained as an average from all the subchannels m and are shown in Table 2.

As can be observed in Fig. 8, the lowest averaged SNR is obtained for the fixed-point model and the experimental tests due to the effect of the finite-precision representation. Additionally, the difference between the fixed-point model and the experimental tests comes from the fact that the FFT model used is a generic version and does not exactly characterize the internal operation of the implemented FFT module. Finally, the PAM modulation allows the SER values to be estimated for the ideal channel. In this case, all the results are null, since there is no symbol error within the ideal channel, and all the transmitted symbols have been correctly recovered.

In a second example scenario, an SMA cable has been considered for experimental tests, so the transmitter and receiver are connected outside the FPGA using the analog converters. This SMA cable can be considered as an almost ideal channel, so this test case is used to verify the quality of the global architecture, including the effect from the converters. Fig. 9 shows the averaged SNR per subchannel m for the DCT4e-MCM and FBMC approaches, respectively. Again, the input signal for simulations is the same as previously. Furthermore, the final global and averaged performance figures are listed in Table 3.
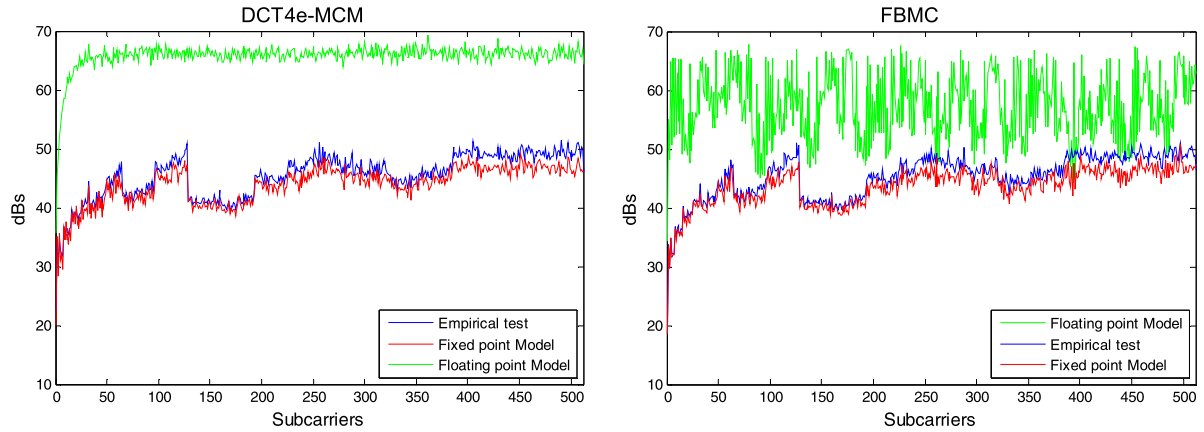
FIGURE 8. Averaged SNR per subchannel *m* for the DCT4e-MCM (left) and FBMC (right) approaches in the floating-point model, in the fixed-point one, and in the experimental tests with an ideal channel.
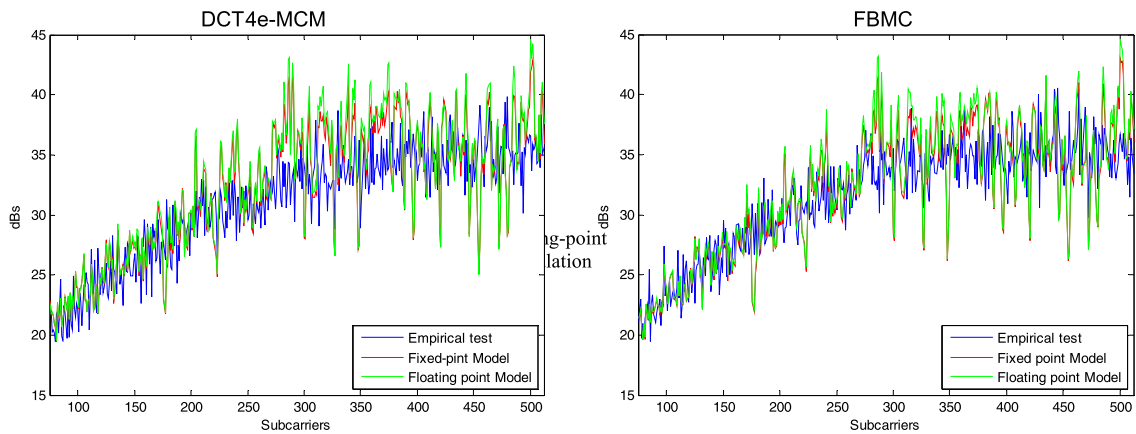

FIGURE 9. Averaged SNR per subchannel m for the DCT4e-MCM (left) and FBMC (right) approaches in the floating-point model, the fixed-point one, and the experimental tests with an SMA cable.

TABLE 3. Performances obtained with the different proposals using an SMA cable.

		SNR	MSE	PSNR	ME
Experimental test	FBMC	29.95	$5.00 \cdot 10^{-4}$	34.66	0.0581
	DCT4e-MCM	31.09	$5.00 \cdot 10^{-4}$	35.79	0.0475
Fixed-point simulation	FBMC	35.85	$3.32 \cdot 10^{-4}$	40.56	0.0351
	DCT4e-MCM	35.96	$3.28 \cdot 10^{-4}$	40.66	0.0331
Floating-point simulation	FBMC	37.13	$3.16 \cdot 10^{-4}$	41.84	0.0332
	DCT4e-MCM	37.51	$3.13 \cdot 10^{-4}$	42.21	0.0304

TABLE 4. SER values obtained when using an SMA cable.

	PAM	2	4	8	16	32
Experimental test	FBMC	0.00	0.00	0.0002	0.0170	0.1142
	DCT4e	0.00	0.00	0.0003	0.0186	0.1094
Fixed-point simulation	FBMC	0.00	0.00	$3.14 \cdot 10^{-4}$	0.0156	0.0792
	DCT4e	0.00	0.00	$7.32 \cdot 10^{-5}$	0.0132	0.0693
Floating-point simulation	FBMC	0.00	0.00	$2.28 \cdot 10^{-4}$	0.0149	0.0764
	DCT4e	0.00	0.00	$9.76 \cdot 10^{-5}$	0.0127	0.0667

In this case, a reduction of the performance can be observed. After analysing it, it can be concluded that it is due to the non-flat frequency response of the coupling transformer included in the DAC output path (transmitter output). In addition, this transformer shows a 3MHz lower cutoff frequency, so the subcarriers in this range have been discarded from the comparison for clarity's sake. With regard to Fig. 9, the differences between the floating-point model, the fixed-point one, and the experimental tests have been reduced, mainly due to the fact that the real behaviour of the analog components involved is more significant than the finite-precision error. In the same way, there are some differences between the fixed-point model and the experimental tests,

since the simulation uses an estimation of the transmission channel. In this case, different PAM modulations have also been applied to obtain the SER values. These results are shown in Table 4, where it is possible to observe that the rate is still null up to four modulation levels.

VI. CONCLUSIONS

An FPGA-based implementation of an SoC architecture for multi-carrier modulations in broadband power line communications has been presented. This architecture has been proposed for real-time performance, where it is possible to flexibly integrate different multi-carrier transmitters and receivers, corresponding to any medium-access technique, as an advanced peripheral (hardware accelerator). The design of any peripheral can be optimized for its integration as a

trade-off among real-time requirements involving the latency and throughput of the system, the effect of the fixed-point representation, and the resource consumption, by maximizing resource reutilization. A soft Microblaze microprocessor is in charge of the management and control of the whole system. Two multi-carrier medium access techniques have been analysed here and integrated in the global SoC architecture: a DCT4e-MCM approach and an FBMC one. Simulations and experimental results from an implementation based on a Xilinx XC6VLX240T FPGA have been particularized for the parameters recommended by the IEEE Standard 1901 for broadband PLC. They have successfully validated the proposal, achieving a transmission rate of 62.5Msps at the converters. The DCT4e-MCM and FBMC architectures provide mean squared errors below $3 \cdot 10^{-5}$ at the output for an ideal channel, whereas each transmitter/receiver requires around 50% of the DSP cells available in the FPGA, the most demanded resource in the device.

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