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A Design Approach to Maximize the Efficiency *vs.* Linearity Trade-Off in Fixed and Modulated Load GaN Power Amplifiers

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ABSTRACT This paper proposes a design method to minimize the phase distortion (AM/PM) in gallium nitride (GaN) power amplifiers (PAs) without significantly worsening other key features such as efficiency, amplitude distortion, and gain. The design strategy consists in the adoption of a smart two-stage architecture, in which the driver stage is devised to act as a sort of ''analogue AM/PM predistorter'' for the final one. Accounting for the actual trend in PA solutions, the proposed approach has been fine-tuned to implement a two-way class AB PA and a Doherty PA (DPA) for backhaul radio links. Both circuits, realized on the same 0.25-μm GaN technology and in monolithic form, have fully been characterized with continuous wave and modulated signals. At 7 GHz, the DPA shows 38 dBm of saturated output power and less than 3° of phase distortion with a power-added efficiency (PAE) higher than 41% in 6 dB of power back off. The class AB PA achieves almost the same level of saturated output power and maximum PAE, with an inevitable lower efficiency in back-off operation, whereas the registered AM/PM is lower than 1.5°. Moreover, when tested with modulated signals, at 32 dBm of average output power and without any digital predistortion, the DPA shows a spectral regrowth of around 36 dBc and a PAE of 40%, whereas the class AB PA achieves 40 dBc and 30%, respectively.

INDEX TERMS GaN class AB PA, DPA, linearity, AM/PM, efficiency.

I. INTRODUCTION

In the design of a power amplifier (PA), the efficiency versus linearity trade-off is a critical aspect. The former is usually maximized approaching the device saturation operating condition, whereas the latter is conversely improved moving towards back-off [1]. At the same time, in almost every communication system, both linearity and efficiency are extremely important features. Therefore, a lot of research effort has been devoting to find suitable PA design strategies to maximize such trade-off.

From a circuit perspective, and in particular for systems in which the involved signals show a large peak-to-average power ratio (PAPR), the Doherty power amplifier (DPA) architecture has been deeply investigated and successfully proposed as one of the most suitable solutions [2]–[5]. However, such architecture presents an inherent worst linearity as compared to class AB PA, especially in terms of phase distortion (AM/PM) [6]–[8], which dramatically affects the spectral regrowth and, moreover, results hard to be compensated by simple predistortion algorithms [9]. Indeed, even if the AM/AM of a DPA can be shaped to be similar to the one of a class AB by properly setting the device bias points and the input splitting ratio, its AM/PM will be always much worse than the one of the class AB PA [10].

From a technological point of view, Gallium Nitride (GaN) is undoubtedly the reference technology to implement high power amplifiers in nowadays systems [11], [12]. The distortion generation mechanisms for such devices have recently been clarified [10], [13], [14]. In particular, it was demonstrated that the nonlinear behavior of the device transconductance (g_m) is the main responsible of the amplitude distortion (AM/AM), whereas the nonlinear variation of the device input impedance (Z_{in}) is the main responsible of the AM/PM. Moreover, in [13] is highlighted that the AM/PM tends to have an opposite behaviour with respect to the AM/AM.

This paper presents a feasible two-stage architecture to implement GaN PAs with minimal phase distortion. A two-stage asymmetrical DPA architecture conceived to reduce the distortion was proposed also in [15]. In such a case, the linearity improvement was achieved by an adaptively

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control of the driver gate bias. However, to be implemented, it required an external circuitry (off-chip) and a feedback loop. Thus, the distortion minimization was obtained at the expenditure of the circuit complexity. In this paper, we propose a different approach. The idea is to exploit the driver stage as a sort of integrated analogue phase predistorter for the final one, i.e., equalizing the total AM/PM distortion and, in turn, decreasing the amplifier spectral regrowth. This means that the linearity improvement is obtained directly in the designed MMIC, without the need of any additional circuitry and feedback path, thus resulting in a more simple and compact amplifier. Moreover, the proposed architecture can be successfully applied to realize not only DPA but also standard class AB PA. In order to demonstrate the validity of the approach, the derived design guidelines are applied to implement a class AB PA and a DPA on the same 0.25 μm GaN technology available at Qorvo foundry. The MMICs are conceived for point-to-point RF link applications at 7 GHz, and their experimental characterization has shown promising results. Indeed, the DPA has shown 38 dBm of saturated output power and less than 3° of phase distortion, with a power added efficiency (PAE) higher than 41% in 6 dB of power back off. On the other hand, the class AB PA has shown the same saturated output power with even lower AM/PM (∼1.5°). The maximum value of PAE is around 60% for both circuits. Also, when tested with Quadrature Amplitude Modulated signals (QAM), both modules have shown relevant values of both spectral regrow and PAE. At 32 dBm of average output power, the DPA achieves 36 dBc and 40%, whereas the class AB PA reaches 40 dBc and 30%, respectively.

The paper is organized as follows: the background on distortion mechanisms in GaN active devices is reported in Section II. Derived design guidelines are proposed in Section III, whereas their implementation on actual MMICs is discussed in Section IV. The experimental results of both PAs are reported in Section V and the conclusions are finally drawn in Section VI.

II. BACKGROUND

Several research studies on distortion generation mechanisms in GaN devices have highlighted that the induced AM/PM at PA level is mainly related to the variation of the device input impedance [10], [13]. Starting from this result, the proposed design strategy aims to provide a feasible architectural solution to realize GaN-based PAs with minimal AM/PM.

To this purpose, let's refer to the simplified PA model reported in Fig. 1 [7], where the active device is simply represented through a voltage controlled current source ($g_m \cdot v_{gsi}$), an input resistance (R_g), and two equivalent capacitors, one at the input (C_{in}) and one at the output (C_{out}). The other parasitics elements of the device are embedded in the input and output matching networks, represented by the impedance $Z_S = R_S + jX_S$ and the admittance $Y_L = G_L + jB_L$, respectively.

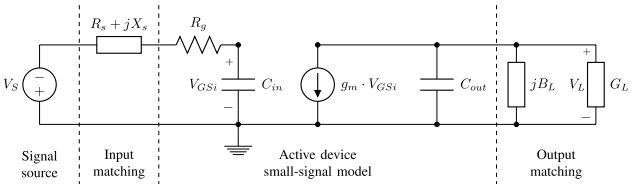


FIGURE 1. Simplified power amplifier model after Miller approximation.

It is to note that in this representation the device feedback capacitor (C_{gd}) has been embedded, by applying the Miller's approximation [16], in the input and output equivalent capacitors, resulting in:

$$\begin{aligned} C_{in} &= C_{gs} + C_{gd} \cdot (1 + g_m/G_L) \\ C_{out} &= C_{ds} + C_{gd} \cdot (1 + G_L/g_m) \end{aligned} \tag{1}$$

Notably, such equations have been derived considering $A_v = v_L/v_{GSi} = -g_m/G_L$ as voltage amplification. Moreover, since g_m/G_L is typically much higher than unity, and that both C_{ds} and C_{gd} show negligible nonlinearities with respect to the RF power level [13], the output capacitor can be neutralized all along the input power range by setting $B_L = -\omega C_{out}$ in the output matching network. Thus, the phase of the output voltage ($\angle v_L$) with respect to v_S, can be written as:

$$\begin{aligned} \angle v_L &= tan^{-1}\left(\frac{R_S + R_g}{X_S - \frac{1}{\omega C_{in}}}\right) \\ &= = tan^{-1}\left\{\frac{R_S + R_g}{X_S - \frac{1}{\omega\left(C_{gs}+C_{gd}+C_{gd}\cdot g_m/G_L\right)}}\right\} \end{aligned} \tag{2}$$

Even if this equation can appear oversimplified, it clearly reveals which are the main causes of the phase distortion in GaN-Based PAs. Indeed, since the latter is defined as the variation of the $\angle v_L$ versus the RF input signal, eqn. (2) suggests that the sources of AM/PM can be classified in two distinctive categories [17]:

- *Technological*, i.e., related to the variation of the device nonlinear parameters (essentially g_m, C_{gd}, C_{gs} and C_{ds}) as the RF input power varies.
- *Behavioural*, i.e., related to the possible variation of the output conductance, G_L, as for instance in a DPA.

III. PROPOSED DESIGN STRATEGY

From a circuital perspective, previous results bring to the following considerations:

- In fixed load PAs, such as class AB, the output loading condition is fixed ($G_L = G_{L,opt}$) along the whole RF input signal range. Thus the AM/PM distortion is mainly ascribed to the technological sources.
- In modulated load PAs, such as DPAs, where the output conductance (G_L) of the Carrier device is modulated from $G_{L,opt}/2$ to $G_{L,opt}$, also the behavioural source plays a relevant role, due to the presence of the term $C_{gd} \cdot g_m/G_L$ in (2).

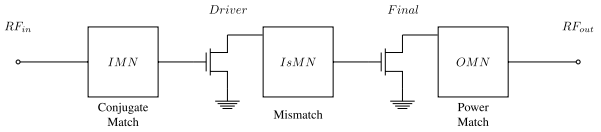


FIGURE 2. Two-stage PA with AM/PM compensation.

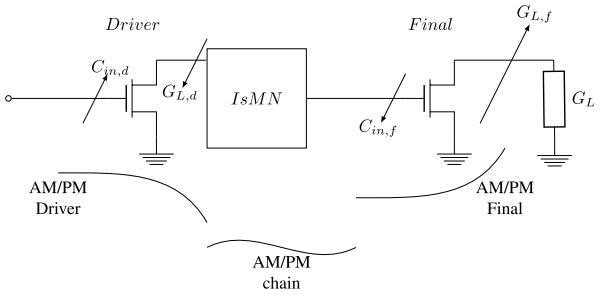


FIGURE 3. Two-stage Carrier and Peaking branches of a DPA with AM/PM compensation.

However, regardless of the PA principle of operation, i.e., based on either fixed or modulated output load, the adoption of a two-stage architecture can aid to realize a power amplifier with minimal phase distortion. In particular, the driver stage can be devised to act as a sort of " AM/PM compensator" for the final one. At the same time, accounting for the PA principle of operation, different expedients can be adopted to fine-tune the driver stage, in order to avoid significant drawbacks onto the other key features of the PA.

A. FIXED LOAD PAs

From a mathematical point of view, the sensitivity of function $tan^{-1}(\cdot)$ in (2) is maximal when the denominator of its argument is close to zero. Unfortunately, such situation arises when the input conjugate matching condition is fulfilled, thus, representing the worst case in terms of phase distortion. Indeed, since C_{in} varies with the applied input power whereas X_S is fixed, if the condition $X_S = 1/\omega C_{in}$ is verified even for one input power level (for instance realizing the small-signal conjugate matching condition), the induced AM/PM variation is maximized while the input power is changing. Therefore, the AM/PM of a fixed load PA could be mitigated by desensitizing the function $tan^{-1}(\cdot)$ through a suitable mismatch at the input section of the active device, i.e., assuring that the denominator of (2) remains different from zero inside the entire input power range, while showing a proper smooth behaviour. However, this solution can lead to unacceptable gain penalty in a single stage PA. On the contrary, by adopting a two-stage architecture, as schematically depicted in Fig. 2, a better trade-off between linearity and power added efficiency (PAE) can be realized. Notably, the AM/PM introduced by the final device can be minimized mismatching its input through the interstage matching network (IsMN), whereas the related gain reduction can be recovered thanks to the presence of the driver stage. Moreover, since the latter usually operates in almost linear condition, thus with a minimal variation of C_{in}, a conjugate matching condition at its input (i.e., through the IMN) can be still pursued. In conclusion, as compared to a single stage solution, the proposed approach leads to an overall chip, which adds to the expected higher gain and comparable PAE, a much lower AM/PM.

B. MODULATED LOAD PAs (DPA)

In such PAs, due to the presence of the term $C_{gd} \cdot g_m/G_L$ at the denominator of (2), the impact of the behavioural sources of distortion is dominant. Indeed, even if the active device was ideally devoid of non-linearities, (i.e., g_m, C_{gd}, C_{gs} and C_{ds} were constants), the resulting PA would be still characterized by a remarkable AM/PM [7], [13]. This is also the reason why DPAs usually show a higher phase distortion as compared to fixed load PAs [10]. Unfortunately, another drawback of the DPA is the lower gain typically registered with respect to comparable class AB PAs [2]. Therefore, the adoption of the previous solution, i.e., a mismatch through the IsMN as shown in Fig.2, could result in an unacceptable overall gain penalty, as for instance experienced in [17]. Nevertheless, also for a DPA, a two-stage architecture can be successfully implemented to mitigate the AM/PM of the overall chip. In this case, the driver stage can be tailored to introduce almost the same AM/PM of the final one, but with opposite slope, thus achieving, at chip level, an almost flat AM/PM behaviour, as graphically represented in Fig. 3. Therefore, as compared to the solution in Fig.2, the gain penalty due to the lossy IsMN is overcome, while achieving a further AM/PM mitigation with a proper design of the driver stage. In fact, in the "Doherty region", while $G_{L,f}$ increases for both Carrier and Peaking devices due to the active load modulation, the input capacitance of the final stage $C_{in,f}$ decreases according to (1), leading to an AM/PM with positive slope [13]. This causes a reduction of the conductance seen by the driver ($G_{L,d}$) and, thus, a consequent increase of the driver's input capacitance ($C_{in,d}$), that produces an AM/PM with opposite slope [13]. Therefore, for a two-stage DPA architecture, the IsMN should be as simple as possible and, more important, without any impedance inverting behaviour. Of course, the structure in Fig. 3 has to be adopted to realize both the Carrier and Peaking branches of the DPA.

IV. DESIGNS

Previous design guidelines have been adopted to implement a class AB PA and a DPA, whose preliminary simulations and measurements have been reported in [18] and [19] and in [20] and [21], respectively. Both circuit are based on the same technology, a commercial 0.25 μm gate length GaN-on-SiC process. Moreover, in order to make a fair comparison between the two solutions, the same carrier frequency $f_c = 7$ GHz and saturated output power level $P_{out} = 38\,dBm$ have been targeted for back-haul applications [22].

The class AB PA was obtained parallelizing two identical chains of Fig. 2. On the contrary, the DPA was realized

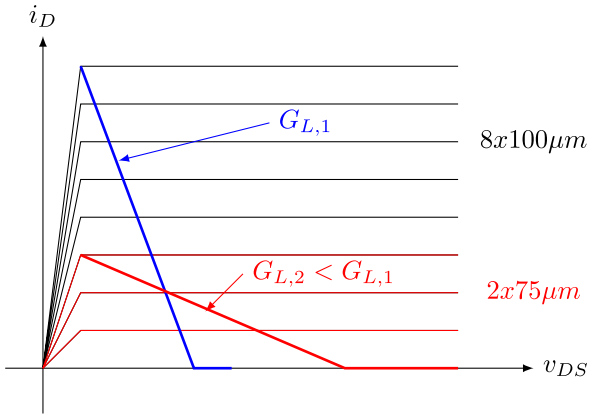


FIGURE 4. Simplified representation of the optimum load-line for a big (blue) and a small (red) device for the driver stage.

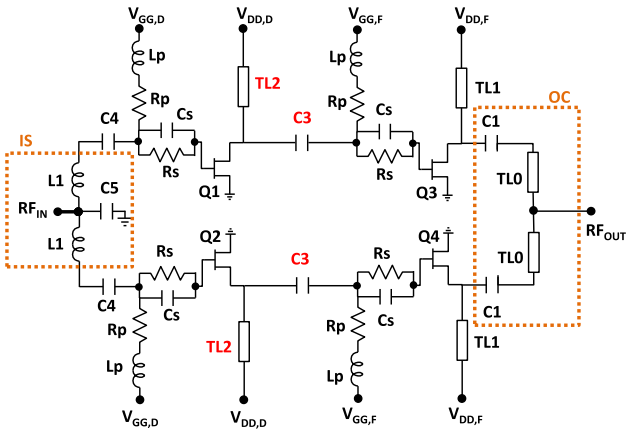


FIGURE 5. Electrical scheme of the class AB PA.

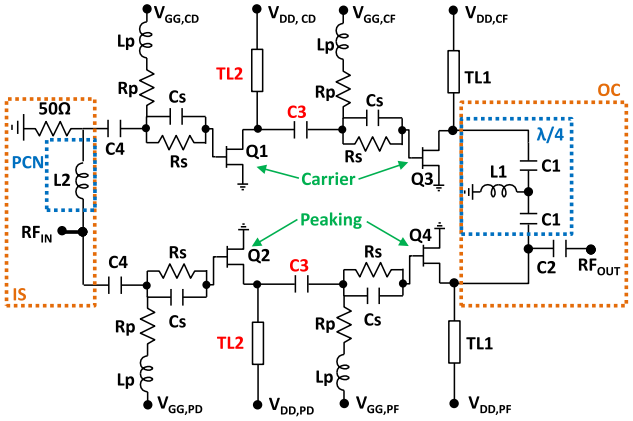


FIGURE 6. Electrical scheme of the DPA.

adopting the scheme shown in Fig. 3 to implement both Carrier and Peaking branches, whereas the output combiner was modified to properly implement the λ/4 transformer to pursue the load modulation [2].

In order to achieve the required output power level, two $8 \times 100\,\mu$m active devices were adopted in the final stage of both MMICs. The drain bias voltage (V_{DD}) was fixed to 28 V. Under this condition, each $8 \times 100\,\mu$m device provides a maximum output power of roughly 35 dBm, with an optimum output resistance of about 105 Ω. For the design of the driver stage, a suitable device was selected. In particular, it was observed that in both architectures, a power level of about 0.6 W (27.7dBm) was required to correctly drive the final stage into saturation. Such power level could be reached with a smaller device, about 150μm of active periphery, having an optimum output load of about 500Ω. However, since the input impedance of the final stage is much lower than such value, an interstage matching network (IsMN) with an extremely high impedance transformation ratio (i.e., from about 10Ω to 500Ω) would be required, resulting in a narrower band behaviour and larger occupied area. Thus, to avoid such drawbacks, the same $8 \times 100\mu$m device was adopted in the driver stage of both PAs, whereas their drain bias voltage was reduced from 28 V to 10 V to keep the efficiency as high as possible. By reducing the drain bias voltage at about one third without changing the output load G_L, would lead to a power reduction of about one tenth, thus from 35 dBm to 24.7 dBm. Consequently, to achieve the power requirement of 0.6 W at the input of the final stage, the output conductance seen by the driver device has to be increased. Therefore, besides allowing the realization of more compact and with larger bandwidth MMICs, the fact to have a bigger device in the driver stage also simplifies the implementation of the " AM/PM analogue predistorter" concept. Indeed, as schematically depicted in Fig. 4, a larger device with reduced drain bias voltage results in a higher optimum conductance G_L (blue load-line in the figure), which further minimize the sensitivity of (2). On the other hand, since the achievable efficiency for a given device can be roughly estimated as $\eta = \eta_{ideal} \cdot [1 - (V_k/V_{DD})]$, where η_{ideal} is the text-book efficiency for a given PA class (e.g., 50% for a class A PA) and V_k is the knee voltage of the device, this choice can introduce some efficiency degradation if the V_k of the adopted technology is too high [23]. However, being the efficiency of a two stage PA given by $\eta_{2stage} = \eta_F/\{1 + [\eta_F/(\eta_D \cdot G_F)]\}$, where η_F and G_F are the efficiency and gain of the final stage, respectively, and η_D is the driver efficiency, the impact of the higher V_k/V_{DD} value onto the overall PA efficiency can be assumed to be marginal. In particular, in the MMICs reported in the following, the maximum difference between the PAE of the last stage alone and the one of the overall two stage amplifier is about four percentage points.

The electrical schemes of both class AB PA and DPA are depicted in Fig. 5 and Fig. 6, respectively.

From a topological point of view, the two architectures differ for the input splitter (IS) and output combiner (OC), highlighted in orange boxes in Fig. 5 and Fig. 6. For the class AB PA, both IS and OC are simple in-phase structures. The former is realized through the series inductors $L1$ and the shunt capacitor $C5$, whereas the latter is simply composed by the dc-blocks $C1$ and the transmission lines $TL0$.

Conversely, in the DPA, in order to realize the active load modulation, the OC includes an impedance inverting network, the λ/4 enclosed in the blue box in Fig. 6, that is

composed by $C1$-$L1$-$C1$ T-network. Similarly, the IS comprises a phase compensation network (PNC, blue box) realized through a simple inductor ($L2$) in this case. It is needed to recover the phase shift introduced by the OC network [2].

In the class AB PA, the final devices (Q_3 and Q_4), were biased at $V_{DD,F} = 28\,\text{V}$ and $V_{GG,F} = -2.65\,\text{V}$, deep class AB. Their unconditional stability was assured in band through the series $Rs//Cs$ (150 Ω // 2pF) block, and out of band through the parallel $Rp - Lp$ (75 Ω-1.4 nH) path towards the gate bias. Their output matching networks were designed to attain, at the intrinsic plane of each device, a fundamental impedance of roughly 105 Ω. This condition has been obtained by resonating the output capacitance through the biasing stub $TL1$, and properly tuning both the dc-block $C1$ and the lines $TL0$ (see Fig. 5). As previously state, for the driver stage the same gate periphery ($8 \times 100\mu$m) was adopted for either Q1 and Q2, but biased at lower drain voltage $V_{DD,D} = 10\,\text{V}$ and $V_{GG,D} = -2.15\,\text{V}$. Their unconditional stability was achieved with similar structure $Rs//Cs$ and $Rp-Lp$. The interstage matching network was optimized following the approach described in the previous section, i.e., by exploiting the mismatch through the biasing stub $TL2$ and the capacitance C_3 (which acts as dc-decoupling also). Finally, the input section of the PA was designed fulfilling the conjugate matching condition at its input. As first step, a network composed by $C4$-$L1$-$2C5$ (16 pF-1.5 nH-2x10pF) was optimized to match each device to 100 Ω. Then, the two branches were combined through a T-junction, thus resulting in the 50 Ω input matching.

Referring to Fig. 6, in the final stage of the DPA, the Carrier device (Q_3) was biased in class AB ($V_{DD,CF} = 28\,\text{V}$ and $V_{GG,CF} = -2.65\,\text{V}$), whereas the Peaking one (Q_4) in class C ($V_{DD,PF} = 28\,\text{V}$ $V_{GG,PF} = -3\,\text{V}$). In the driver stage, the $8 \times 100\mu$m device in the Carrier branch (Q_1) was biased with $V_{DD,CD} = 10\,\text{V}$ and $V_{GG,CD} = -2.15\,\text{V}$, whereas the one in the Peaking branch with $V_{DD,PD} = 10\,\text{V}$ and $V_{GG,PD} = -3.65\,\text{V}$. The same stabilization network was adopted. For the interstage network, the biasing stub $TL2$ and the capacitor $C3$ were optimised with the aim to exploit the AM/PM reduction mechanism previously described. In this case, the length of TL_2 was properly optimized to avoid impedance inverting behaviour, thus actualizing the phase distortion compensating mechanism. At the input, an uneven splitting was synthesised through the block C4-L2-C4. Since the input port (RF_{in}) is placed in front of the Peaking branch, such network also acts as phase compensator.

The effectiveness of proposed design approaches can be evaluated looking at Fig. 7, where the simulated AM/PM behaviours of both PAs as functions of the output power back-off (e.g., 0 dB means maximum output power) are reported. The upper plot shows the AM/PM behaviours for the class AB PA when the gate terminal of the device in the final stage is conjugately matched and when it is mismatched of about 1 dB. As can be noted, in the latter case the AM/PM is reduced from 11° to just 2°. The lower plot deals with the DPA design. In particular, it compares the AM/PM

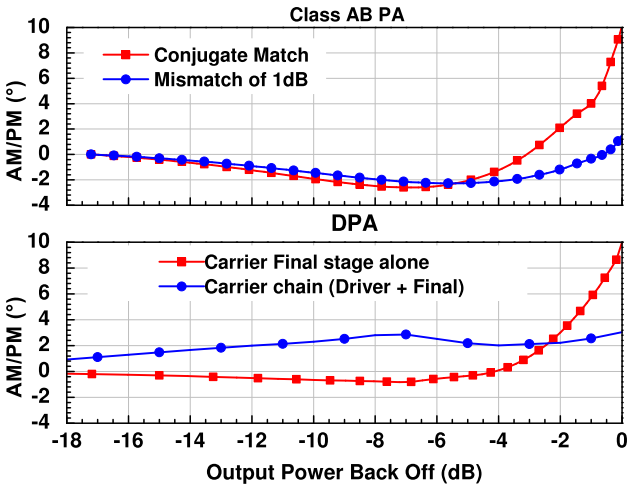


FIGURE 7. Comparison between the AM/PM of the final stage alone and the overall chain for the class AB PA (upper) and for the DPA (lower).

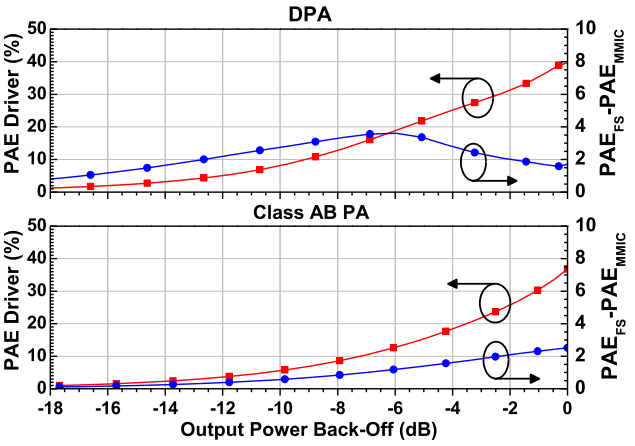


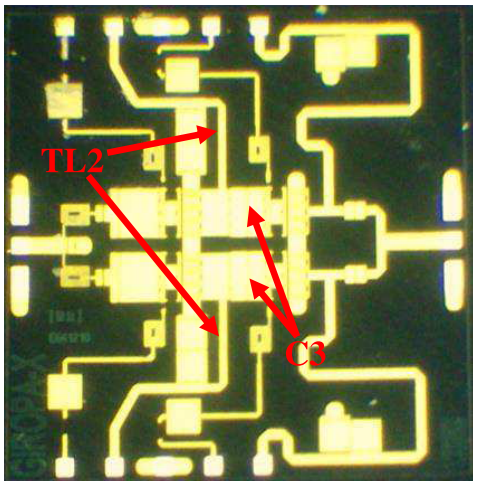
FIGURE 8. PAE of the driver stage and difference between the PAE of the final stage (PAE_{FS}) and of the overall MMIC (PAE_{MMIC}) as functions of the output back-off.

behaviours of the final stage alone with the one achieved by the overall active chain. Specifically, the latter shows a trend similar to the one graphically pointed out in Fig. 3. It barely increases until the output load of the final stage $G_{L,f}$ is constant, whereas, when it starts to be modulated, i.e., around 6 dB of output back-off, the trend reverses, since the AM/PM of the driver begins to have an opposite slope as compared to the one of the final stage. This behaviour clearly put into evidence the beneficial effect of the driver stage as an analogue predistorter. Numerically, in this case, the AM/PM is reduced from 10° to just 3°.

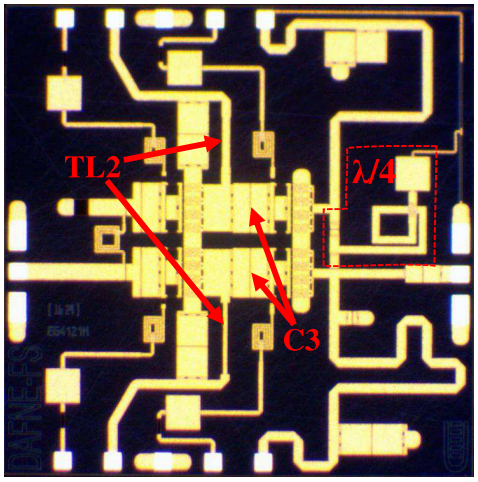
Finally, in order to provide an estimation about the impact of the driver stage onto the overall MMIC efficiency, Fig. 8 shows the simulated PAE of such stage in both architectures as functions of the output back-off at centre frequency. In the formula $PAE = (P_{out,D} - P_{in,D})/P_{DC,D}$, the RF output power ($P_{out,D}$) is evaluated at the input of the stabilized devices in the final stage, thus including the IsMN losses, whereas the RF input power ($P_{in,D}$) and the DC consumption

TABLE 1. Amplifiers' bias conditions.

Amplifier	Final Stage	Driver Stage
PA	$V_{DD,F} = 28\,V$ $V_{GG,F} = -2.65\,V$	$V_{DD,D} = 10\,V$ $V_{GG,D} = -2.25\,V$
DPA	$V_{DD,CF} = 28\,V$ $V_{GG,CF} = -2.65\,V$ $V_{DD,PF} = 28\,V$ $V_{GG,PF} = -3\,V$	$V_{DD,CD} = 10\,V$ $V_{GG,CD} = -2.15\,V$ $V_{DD,PD} = 10\,V$ $V_{GG,PD} = -3.65\,V$

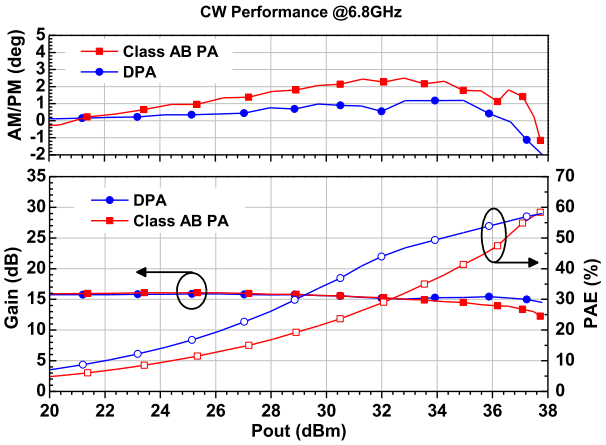


(a)



(b)

FIGURE 9. Photo of the realized MMICs: (a) class AB PA; (b) DPA.



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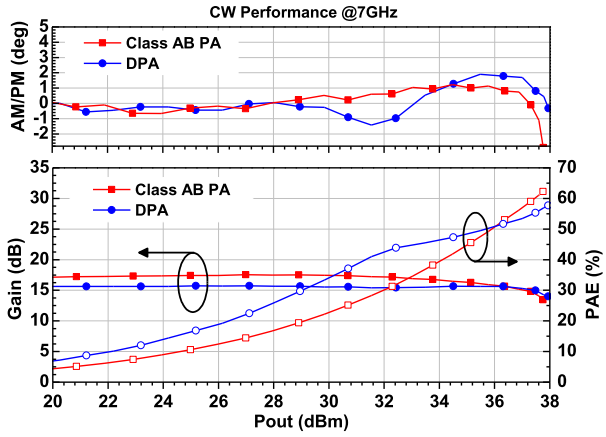

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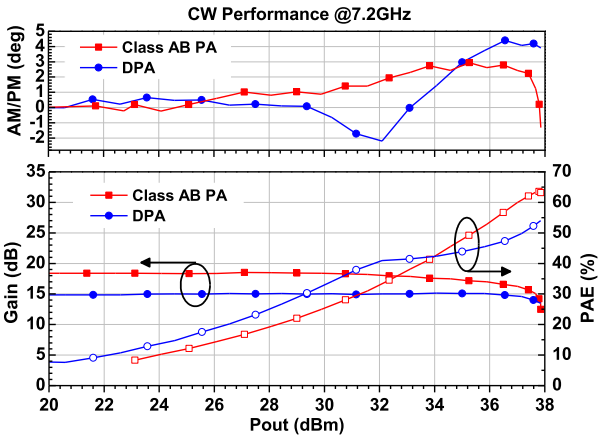

(c)

FIGURE 10. Comparison between CW measurements of both amplifiers at: (a) 6.8 GHz, (b) 7.0 GHz, and (c) 7.2 GHz.

($P_{DC,D}$) correspond to the input power of the overall MMIC (i.e., $P_{in,D} = P_{in,MMIC}$) and the DC power absorbed by the driver devices themselves. The registered value at saturation is around 40 % in the DPA and 38 % in the class AB PA, respectively. In the same figure is also reported the difference between the PAE of the final stage alone (PAE_{FS}) and the one of the overall MMIC (PAE_{MMIC}). In particular, the former was calculated considering $P_{in,FS} = P_{out,D}$ as input power and $P_{out,FS} = P_{out,MMIC}$ as output power, whereas the DC power ($P_{DC,FS}$) is only the one consumed by the two devices in the final stage. Therefore, the presence of the driver stage causes a maximum PAE reduction of about four and three percentage points in the DPA and class AB PA, respectively. On the other hand, as compared to an hypothetical amplifier composed by the final stage only, the benefit is twofold in

TABLE 2. Comparison with other GaN MMIC PAs.

REF	*Frequency*	*Gain*	P_{MAX}	*OBO*	*PAE@*P_{MAX}	*PAE@OBO*	Max. AM/AM	Max. AM/PM
[17]	7 GHz	7 dB	40 dBm	6 dB	46%	33%	1.8 dB	13 deg
[24]	5.8–8.8 GHz	10 dB	36 dBm	9 dB	30%	31%	3 dB	n.d.
[25]	6.35–7.35 GHz	11 dB	37.5 dBm	7 dB	46%	37%	2 dB	n.d.
[26]	6.7–7.8 GHz	12 dB	36 dBm	9 dB	45%	30%	3 dB	25 deg
[27]	7 GHz	10 dB	37 dBm	7 dB	49%	47%	3 dB	10 deg
Class AB	7 GHz	16 dB	38 dBm	6 dB	60%	41%	2 dB	1.5 deg
DPA	7 GHz	15 dB	38 dBm	6 dB	58%	30%	1 dB	3 deg

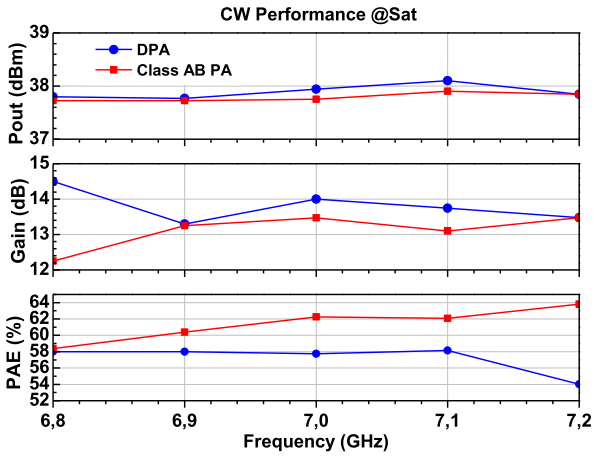

FIGURE 11. Measured CW performance of both PAs at saturation (a) and at 6 dB back-off (b), as function of frequency.

both architectures. The AM/PM is reduced of about 80% and the gain is significantly increased.

V. EXPERIMENTS

The realized MMICs, whose photos are reported in Fig.9, both $3 \times 3mm^2$, were measured with either continuous wave (CW) and modulated signals in the targeted bandwidth, i.e., from 6.8 GHz to 7.2 GHz.

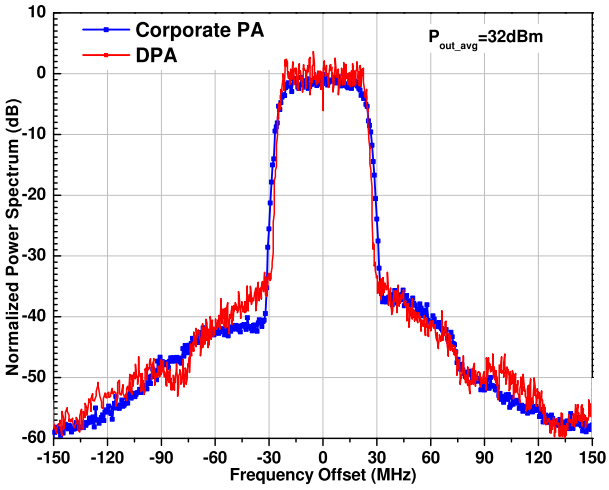

FIGURE 12. Measured output spectra of both PAs.

The nominal bias conditions are summarised in the following Table 1.

The CW measured performances of both MMICs, in terms of Gain, PAE and AM/PM, as functions of output power and for the lower (6.8 GHz), center (7 GHz), and higher (7.2 GHz) frequency, are shown in Fig. 10. Red lines plus square refer to the DPA whereas blue ones plus circle are used for the class AB PA.

Both chips achieve a saturated output power of about 38 dBm, whereas the PAE peak is always higher than 60% and 55% for the class AB PA and the DPA, respectively. Such PAE trend is, instead, opposite at 6 dB back-off, where the PAE of the DPA is always higher than 41%, whereas for the other is around 30%. Saturated output power and efficiency peaks show some marginal differences over frequency that can be ascribe to the intrinsic narrower response of the DPA architecture.

About the AM/PM behaviors, both amplifiers show a minimal variation from small-signal up to compression for every tested frequency point. For instance at 7 GHz, the DPA shown less than 3°, whereas the class AB PA just 1.5°. Such results are well in agreement with the expectations, demonstrating the beneficial effects of the proposed design strategies.

Fig. 11 shows the CW performances as functions of frequency at both saturation and at 6 dB back-off. In the former case, the output power is close to 38 dBm for both MMICs, whereas, as already discussed, some differences are visible on gain and PAE at the edges of the band. At 6 dB back-off, the DPA shown a PAE of 41 %, while the class AB PA operates with a PAE of 30 % only, thus resulting in a reduced average efficiency when operated with modulated signal. In order to check the effects of the reduced AM/PM and the different principle of operation of the two MMICs, both were measured at 7 GHz with a 256 QAM modulated signals, having 60 MHz video bandwidth and 7 dB of Peak-to-Average power ratio. The resulting spectra are shown in Fig. 12, measured for a 32 dBm of average output power and without any digital predistortion applied. As can be noted, the spectral regrowth is always lower than 36 dBc, whereas the registered average PAE is around 40% for the DPA and 30% for the class AB PA.

A comparison between the performance of the presented amplifiers with recently published GaN MMICs, mainly DPAs, is carried out in Table 2. Considering the realizations at similar center frequency, both class AB PA and DPA show performance at the top edge of the current state-of-the-art in terms of efficiency and output power, whereas assuring significant lower phase and amplitude distortions.

VI. CONCLUSION

A design method to minimize the AM/PM in GaN PAs has been presented. The proposed two-stage architecture has been applied to realize a class AB PA and a DPA in the same 0.25 μm GaN MMIC technology for backhaul applications. Experimental results have confirmed the validity, and, at the same time, the versatility of the proposed approach. Indeed, an almost null phase distortion has been registered in both PA configurations without leading to a relevant deterioration of other features. At 7 GHz the DPA shows 38 dBm of saturated output power and less than 3° of phase distortion, with a PAE higher than 41% in 6 dB of power back off. The class AB PA achieves almost the same level of saturated output power and maximum PAE value, with an inevitable lower efficiency in back off operation. When tested with QAM modulated signals, at 32 dBm of average output power and without any predistortion, the DPA shows a spectral regrowth of around 36 dBc and a PAE of 40%, whereas the class AB PA achieves 40 dBc and 30%, respectively.

REFERENCES

[1] P. M. Lavrador, T. R. Cunha, P. M. Cabral, and J. C. Pedro, "The linearity-efficiency compromise," *IEEE Microw. Mag.*, vol. 11, no. 5, pp. 44–58, Aug. 2010.
[2] V. Camarchia, M. Pirola, R. Quaglia, S. Jee, Y. Cho, and B. Kim, "The Doherty power amplifier: Review of recent solutions and trends," *IEEE Trans. Microw. Theory Techn.*, vol. 63, no. 2, pp. 559–571, Feb. 2015.
[3] A. Grebennikov and S. Bulja, "High-efficiency Doherty power amplifiers: Historical aspect and modern trends," *Proc. IEEE*, vol. 100, no. 12, pp. 3190–3219, Dec. 2012.
[4] R. Giofrè, L. Piazzon, P. Colantonio, and F. Giannini, "Being seventy-five still young: The doherty power amplifier," *Microw. J.*, vol. 55, no. 4, pp. 72–88, 2012.
[5] B. Kim, J. Kim, I. Kim, and J. Cha, "The Doherty power amplifier," *IEEE Microw. Mag.*, vol. 7, no. 5, pp. 42–50, Oct. 2006.
[6] L. C. Nunes, P. M. Cabral, and J. C. Pedro, "AM/PM distortion in GaN Doherty power amplifiers," in *IEEE MTT-S Int. Microw. Symp. Dig.*, Jun. 2014, pp. 1–4.
[7] L. Piazzon *et al.*, "Effect of load modulation on phase distortion in Doherty power amplifiers," *IEEE Microw. Wireless Compon. Lett.*, vol. 24, no. 7, pp. 505–507, Jul. 2014.
[8] C. F. Campbell, K. Tran, M.-Y. Kao, and S. Nayak, "A K-band 5W Doherty amplifier MMIC utilizing 0.15 μm GaN on SiC HEMT technology," in *Proc. IEEE Compound Semiconductor Integr. Circuit Symp. (CSICS)*, Oct. 2012, pp. 1–4.
[9] H. Sarbishaei, D. Y.-T. Wu, and S. Boumaiza, "Linearity of GaN HEMT RF power amplifiers—A circuit perspective," in *IEEE MTT-S Int. Microw. Symp. Dig.*, Jun. 2012, pp. 1–3.
[10] R. Quaglia *et al.*, "Experimental investigation of bias current and load modulation effects in phase distortion of GaN HEMTs," *Electron. Lett.*, vol. 50, no. 10, pp. 773–775, 2014.
[11] A. Ghavidel, F. Tamjid, A. Fathy, and A. Kheirdoost, "GaN widening possibilties for PAs: Wide-band GaN power amplifiers utilize the technology's special properties," *IEEE Microw. Mag.*, vol. 18, no. 4, pp. 46–55, Jun. 2017.
[12] P. Colantonio, F. Giannini, and R. Giofrè, and L. Piazzon, "Evaluation of GaN technology in power amplifier design," *Microw. Opt. Technol. Lett.*, vol. 51, no. 1, pp. 42–44, 2009. [Online]. Available: http://dx.doi.org/10.1002/mop.23958
[13] L. Cotimos Nunes, P. M. Cabral, and J. C. Pedro, "AM/AM and AM/PM distortion generation mechanisms in Si LDMOS and GaN HEMT based RF power amplifiers," *IEEE Trans. Microw. Theory Techn.*, vol. 62, no. 4, pp. 799–809, Apr. 2014.
[14] T. Rahkonen, S. Hietakangas, and J. Aikio, "AM-PM distortion caused by transistor's signal-dependent input impedance," in *Proc. 20th Eur. Conf. Circuit Theory Design (ECCTD)*, Aug. 2011, pp. 833–836.
[15] Y.-S. Lee, M.-W. Lee, S.-H. Kam, and Y.-H. Jeong, "Highly linear and efficient asymmetrical Doherty power amplifiers with adaptively bias-controlled predistortion drivers," in *IEEE MTT-S Int. Microw. Symp. Dig.*, Jun. 2009, pp. 1393–1396.
[16] A. S. Sedra and K. C. Smith, *Microelectronic Circuits*, 5th ed. Oxford, U.K.: Oxford Univ. Press, 2004.
[17] V. Camarchia *et al.*, "A design strategy for AM/PM compensation in GaN Doherty power amplifiers," *IEEE Access*, vol. 5, pp. 22244–22251, 2017.
[18] R. Giofrè, P. Colantonio, and F. Giannini, "High efficiency and low distortion GaN MMIC power amplifier for 7 Ghz applications," in *Proc. 21st Int. Conf. Microw., Radar Wireless Commun. (MIKON)*, May 2016, pp. 1–4.
[19] R. Giofrè, P. Colantonio, and F. Giannini, "A design approach for two stages GaN MMIC PAs with high efficiency and excellent linearity," *IEEE Microw. Wireless Compon. Lett.*, vol. 26, no. 1, pp. 46–48, Jan. 2016.
[20] R. Giofrè, P. Colantonio, and F. Giannini, "A design approach to mitigate the phase distortion in GaN MMIC Doherty power amplifiers," in *Proc. 11th Eur. Microw. Integr. Circuits Conf. (EuMIC)*, Oct. 2016, pp. 133–136.
[21] R. Giofrè and P. Colantonio, "A high efficiency and low distortion 6 W GaN MMIC Doherty amplifier for 7 GHz radio links," *IEEE Microw. Wireless Compon. Lett.*, vol. 27, no. 1, pp. 70–72, Jan. 2017.
[22] V. Camarchia, R. Quaglia, and M. Pirola, *Electronics for Microwave Backhaul* (Artech House Microwave Library). Norwood, MA, USA: Artech House, 2016. [Online]. Available: https://books.google.it/books?id=RG6uDgAAQBAJ
[23] P. Colantonio, F. Giannini, and E. Limiti, *Power Amplifier Fundamentals*. Hoboken, NJ, USA: Wiley, 2009, pp. 1–47.
[24] D. Gustafsson, J. C. Cahuana, D. Kuylenstierna, I. Angelov, and C. Fager, "A GaN MMIC modified Doherty PA with large bandwidth and reconfigurable efficiency," *IEEE Trans. Microw. Theory Techn.*, vol. 62, no. 12, pp. 3006–3016, Dec. 2014.
[25] L. Piazzon, P. Colantonio, F. Giannini, and R. Giofrè, "15% bandwidth 7 GHz GaN-MMIC Doherty amplifier with enhanced auxiliary chain," *Microw. Opt. Technol. Lett.*, vol. 56, no. 2, pp. 502–504, 2014.
[26] D. Gustafsson, J. C. Cahuana, D. Kuylenstierna, I. Angelov, and N. Rorsman, "A wideband and compact GaN MMIC Doherty amplifier for microwave link applications," *IEEE Trans. Microw. Theory Techn.*, vol. 61, no. 2, pp. 922–930, Feb. 2013.
[27] V. Camarchia, J. Fang, J. J. Moreno Rubio, M. Pirola, and R. Quaglia, "7 GHz MMIC GaN Doherty power amplifier with 47% efficiency at 7 dB output back-off," *IEEE Microw. Wireless Compon. Lett.*, vol. 23, no. 1, pp. 34–36, Jan. 2013.

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