

# An Algorithm for Automatically Calculating Component Current Ratings in Switched-Capacitor DC-DC Converters

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**ABSTRACT** Switched capacitor (SC) dc–dc converters, which have traditionally been used for on-chip power supplies, are now being considered for medium to high-power applications. This paper presents a method for automatically synthesizing SC converters as well as deriving the expressions for their charge-multipliers. Charge multipliers can be used to calculate important design characteristics such as converter output voltage regulation, efficiency, and component current ratings, which can then be used to appraise different topologies. However, whilst a full appraisal of converters also requires component voltage ratings, this work is the first step in developing an automatic software tool that will employ a search-based algorithm to generate optimum SC topologies for a given application. The method is based on the proposition that all SC converters can be synthesized from a so-called “basic cell”. The automatic derivation and solution of the charge transfer equations for a traditional Fibonacci SC converter is presented as an example of the proposed method, which is validated against existing analytic equations as well as a detailed Spice simulation. The automatic calculation of the charge-multipliers for two other well-known SC converters is also demonstrated, including a new, arbitrarily generated circuit, which again is validated against detailed spice simulations.

**INDEX TERMS** Switched capacitor circuits, dc-dc power converters, circuit analysis computing, circuit topology.

## I. INTRODUCTION

Thanks to their inductor-less structure, switched capacitor (SC), DC-DC converters are an ideal topology for on-chip applications and have been widely implemented in integrated circuits, for example power management in advanced chip-microprocessors [1]. However, SC DC-DC converters suffer from high impulse currents during charge transfers between the capacitors. This means that they have to operate at high switching frequencies or use large capacitors in order to keep converter transistor and capacitor conduction losses and peak current stress to a minimum [2]. This has mostly limited the use of SC DC-DC converters to low-power applications.

An alternative approach is to operate SC converters in resonant mode, which eliminates impulse currents. Resonant operation can be achieved by adding small inductors to the structure of the SC circuit [3], [4], noting that this inductor plays no part in the step up/down process of the converter. Resonant SC converters also benefit from soft-switching operation which enables the converter to

operate at high switching frequency, and results in lower capacitor energy-storage requirements and in general, a lower equivalent output resistance [5].

Resonant operation mode has made it possible to extend the use of SC DC-DC converters to medium and high-power applications. Therefore, they have been recently considered for HVDC transmission, automotive and PV industries [6]–[9]. In these applications, the essential requirement is for a compact DC-DC converter with a high voltage-conversion ratio, for example voltage step-up from wind-turbine to transmission voltages, battery to traction drive and solar panel to the electric grid respectively.

The design of converters for these new medium/high power applications consists of optimising a number of conflicting criteria, for example requirements for high efficiency, minimising converter size/weight, the number of power electronic switches, component voltage/current stress and insulation requirements; in addition, easing manufacturing costs through a modular design. Therefore, investigations must be carried out to assess different SC DC-DC circuit

topologies – existing and newly devised - against these criteria.

SC converters achieve voltage or current conversion by the dynamic re-configuration of several common SC cells. This is usually carried out between two phases which correspond to the charging and discharging of the cell capacitor respectively. The number of new topologies that could be synthesised to achieve the same voltage-conversion ratio depends on the magnitude of the voltage-conversion ratio itself. Therefore, in terms of carrying out investigations of circuits for applications with high voltage-step up ratios, such as HVDC, there will be many different topologies that for a given step-up ratio (a) exist and/or (b) need to be appraised. Consequently, it is desirable to develop a method that can automatically (a) synthesise and (b) appraise, SC circuit variants for a particular voltage-conversion ratio. This would include generating the topologies and comparing their performance in terms of the criteria mentioned previously.

#### A. AUTO-SYNTHESIS OF SC DC-DC CONVERTERS

Auto-synthesis of a circuit from individual switches and capacitors, which does not include design rules, would lead to a large number of impractical circuits – for example capacitors short-circuited through switches. Such an approach would correspond to a randomly generated netlist. Another method would be to consider the automation of existing synthesis techniques; unfortunately, there is no general and systematic approach to synthesise SC DC-DC circuits at the moment. Most of the existing SC DC-DC topologies have been devised in a manual, ad-hoc manner with many being a variation of the well-known Cockcroft-Walton and Marx generator [2]. The Cockcroft-Walton circuit is constructed from uncontrolled switches and is fed from an AC source, and therefore is classified as an AC-DC circuit and termed a voltage multiplier. For DC-DC capability, these circuit must be implemented using at least semi-controlled switches. In [10] an attempt was made to formulate topology generation and analysis for these types of AC-DC voltage multiplier circuits. However, an algorithm to automate topology generation was not presented in the paper. Further work in [11], which was based on the method in [10], proposed a technique for the automatic generation of AC-DC voltage multipliers, with auto-appraisal being based on Artificial Intelligence (AI) decisions. Extending this method to SC DC-DC converters becomes intractable due to the presence of controlled switches.

In [12] a cell-based approach is proposed to synthesise SC DC-DC circuits. Here a number of so-called switching cells, each consisting of a well-formed circuit including a capacitor and a number of switches, are connected together to form a converter. Cell-based methods inherently include design rules into the auto-synthesis. However the method in [12] is restricted to a so-called cascade connection of cells, which means a large number of potential SC topologies cannot be generated. Furthermore, [12] has not proposed a method for auto-synthesis or appraisal.

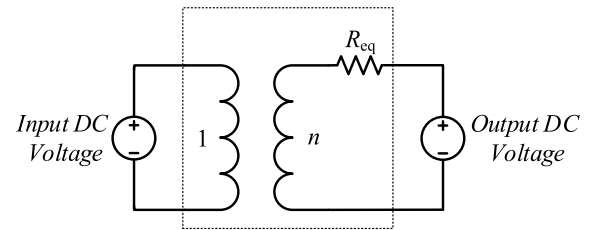


FIGURE 1. SC converter steady-state average model.

#### B. AUTOMATIC CIRCUIT APPRAISAL OF SC DC-DC CONVERTERS

One of the key performance indicators to evaluate and compare different SC converters is output equivalent resistance, which is a topic of on-going research in this area. Circuit averaging of SC DC-DC converters results in a model that consists of an ideal DC transformer with a circuit topology dependent turns-ratio  $n$ , followed by an output equivalent resistance  $R_{eq}$ , as shown in Fig. 1 [2]. The equivalent resistance  $R_{eq}$  is the key parameter for SC converters as it fully determines its steady-state performance such as efficiency and load regulation. Load regulation is important because in general there is no mechanism for adjusting the output voltage of an SC converter.

Different approaches have been adopted to calculate SC circuit output equivalent resistance [13]–[16], some of which have been automated. In addition, some methods give analytic expressions [13]–[15], where others give numerical solutions [16]. In [16] state-space equations for the SC circuit are derived. These are then solved numerically in the time domain to calculate output voltage and current, from which the output equivalent resistance is obtained. Whilst this method gives auto-appraisal, it suffers from long computation run-times and needs an initial netlist description of the circuit. It also requires the generation of the basic loop matrices for the circuit to obtain the state-space equations [17], for each charge/discharge phase. The algorithm for this method is therefore very complex and difficult to implement in software. In addition, the results are numeric, which for example give no insight into how circuit performance depends on the value of the voltage-conversion ratio.

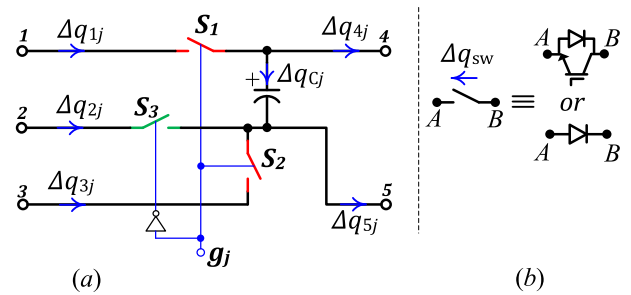
Purely analytic methods of appraisal are based on deriving an expression for output impedance from conduction losses. In [13], component conduction losses are calculated based on their average current and analytical expressions for output equivalent resistance are derived for both conventional hard-switched and resonant SC converters. This method is completely general with no restriction on so-called fast or slow switching limits (FSL, SSL), which are related to the converter switching frequency and have been defined in [14]. However, auto-appraisal is not described in this paper. In [14] itself, a systematic analysis method is developed which provides expressions for output equivalent resistance, but is restricted to the two modes of operation: FSL and SSL. Again, there is no description of how the method could be automated. However, the main feature of this method is

the introduction of so-called charge-multipliers, which is a powerful concept that can be used not only to obtain output equivalent resistance but also the peak, average or RMS current ratings of components. Charge-multipliers, which were first introduced in [15], are governed by the circuit topology and are therefore derived using fundamental network theory methods [18]. A charge-multiplier is the ratio of the charge that passes through a component during either the charging/discharging phase, to the charge that is delivered at the converter output over the full switching period. Whilst the automatic calculation of charge-multipliers was not presented in [14], the technique described would require a complex algorithm to construct the fundamental network matrices in order to automate the process. In addition, the method requires the automatic generation of the circuit netlist.

The main disadvantage of previous work on auto-synthesis and auto-appraisal of SC circuits, as described above, is their complexity. This has meant that until now there has been no method to both synthesise and appraise SC DC–DC converters automatically. This paper addresses this problem by proposing that all SC converters can be synthesised from a so-called “basic cell”, which is then used as the basis of a method for the automatic generation of SC topologies and their appraisal. This new method uses charge-multipliers to calculate figure-of-merit attributes such as converter output impedance and component current ratings, which can be used for auto-appraisal. However, for a complete appraisal of an SC topology, the component voltage ratings are also required. The automatic calculation of voltage ratings is not provided in this paper; nonetheless the proposed method can readily be extended to include them, as will be shown in a future paper. The ultimate aim of this work is to use the auto-synthesis and appraisal method in a search algorithm to automatically generate optimum SC topologies for a given application. This paper is therefore the first step toward this objective, describing a method that allows cell-based auto-synthesis and the automatic calculation of charge-multipliers. Component current ratings are used here as an example of a figure-of-merit that can be used as part of the appraisal process.

The paper first describes how a circuit can be synthesised from the basic cell using a simple cell-connection matrix. A unique method of analysis for SC converters is then presented that uses cell-based, discrete state-equations to describe the operation of the converter. These equations are then solved recursively using a simple algorithm to derive charge-multipliers, which allows the current ratings of the converter components to be obtained in terms of converter output current and cell number.

The so-called Fibonacci SC converter is used as an example of how the cell connection matrix is derived and how the proposed algorithm can be used to derive expressions for the converter charge-multipliers. These expressions are validated against existing equations that have been presented in [14]. The algorithm is further validated against the results from an automatic implementation of the algorithm using MATLAB code, which numerically calculates charge-multipliers and



**FIGURE 2.** (a) The basic Switched Capacitor cell, (b) convention used for the direction of charge-transfer through a switch.

compares them against detailed circuit simulations using Micro-Cap Spice software. The numerical validation is then repeated for a number of other traditional SC converters. Finally, the method is applied to a new arbitrary SC topology, which was randomly generated using the cell connection matrix. The generation of this new topology demonstrates how easily the method can provide auto-synthesis. The charge-multipliers are computed for this arbitrary topology using the developed MATLAB code and results are again validated against a detailed Spice simulation.

## II. THE BASIC SWITCHED CAPACITOR CELL

The proposed basic Switched Capacitor cell, which is based on the Addition cell introduced in [19], is shown in Fig. 2(a). Note that the cell is capable of bi-directional power flow depending on the implementation of the switches as transistors and/or diodes – see Fig. 2(b). The convention for the direction of charge transfer through a switch,  $\Delta q_{sw}$ , has been chosen as shown in Fig. 2(b). Charge flow for the capacitor follows the passive sign convention.

The analysis described here is for voltage step-up operation of the basic cell from its left-hand terminals 1-3 to those on the right, 4 and 5 as shown in Fig. 2. The terminals 1-3 are then defined as inputs and 4 and 5 as outputs. However, it should be noted that the results of the analysis also apply to step-down operation, where the definition of inputs and outputs is simply exchanged. In this paper, up-stream cells are defined as those cells connecting to the *input* of another cell and down-stream as connecting to its *outputs*.

The basic cell shown in Fig. 2 is denoted as the  $j^{\text{th}}$  cell of a total of  $N$  cells, which are inter-connected to form an overall converter. The cell consists of three ideal switches, where the red switch pair ( $S_1, S_2$ ) are fed from a 50% duty cycle gate logic signal  $g_j$  and the green switch  $S_3$  is fed from its logical inverse  $\bar{g}_j$ . For voltage step-up operation, the cell capacitor is charged from a single, up-stream cell when the red switch pair ( $S_1, S_2$ ) are on and  $S_3$  is off, which corresponds to the switch gate-signal  $g_j = 1$ . Likewise, the cell capacitor is discharged into down-stream cell(s) and/or the output terminal of the converter when the switch states are inverted,  $g_j = 0$ . A cell is therefore characterised as having two distinct switching phases, which correspond to the charging and discharging of the cell capacitor. The sum of the duration of these two phases is the total switching period, which is denoted  $T_s$ .

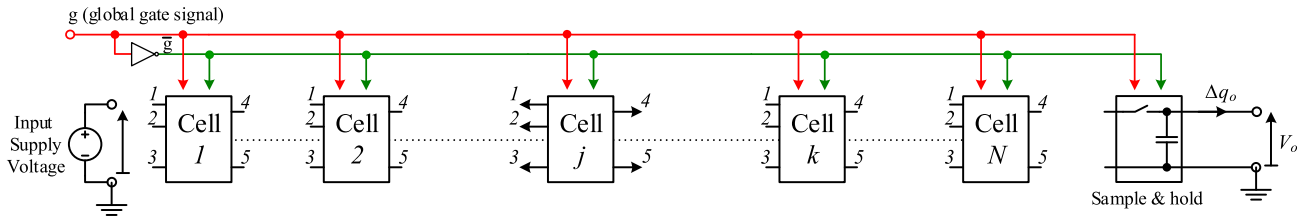


FIGURE 3. General cell arrangement for an SC converter.

### III. DERIVATION OF CHARGE TRANSFER EQUATIONS FOR A GENERAL SC CONVERTER

The arrangement of a general  $N$  cell converter is shown in Fig. 3, where each cell is assigned a cell number  $j = 1 \rightarrow N$ . The figure also introduces the converter DC input voltage source  $V_{in}$ , which has its lower terminal defined as ground. The output of one of the cells, which is usually the  $N^{th}$  cell, is used to provide the output voltage of the converter, which is defined as  $V_o$ , with respect to ground. Note for step-up operation, then  $V_o > V_{in}$ . The output  $V_o$  is captured using a so-called Sample and Hold, switch/capacitor circuit as shown in Fig. 3, which is controlled by the global gate-signal  $g$  or its inverse.

It is proposed that the inter-connection of cells for a particular converter can be defined using a cell connection matrix  $c$ ,

$$c = \begin{pmatrix} c_{11} & c_{12} & \dots & c_{1N} \\ c_{21} & c_{22} & \dots & c_{2N} \\ c_{31} & c_{32} & \dots & c_{3N} \end{pmatrix} \quad (1)$$

Where each element  $c_{ij}$  represents the cell number to which the  $i^{th}$  input of the  $j^{th}$  cell is connected. Each element in the cell connection matrix is an integer between 0 and  $N - 1$ . The proposed cell connection matrix for defining SC converter circuits is a powerful technique that can be used to synthesise new circuits. Whilst a new converter could hypothetically be devised by simply filling the matrix with random integers, this would be a very inefficient method of automatically synthesising undiscovered circuits. This is because there may be many circuits that are generated where traditional design rules are violated, such as the creation of redundant cells. Redundant cells are those that do not contribute to voltage step-up/down of the converter. The proposed method therefore implements the following design rule:

#### SYNTHESIS RULE 1

Input terminals 1 and 2 can only connect to terminal 4 of a single up-stream cell or the input DC voltage  $V_{in}$ , whereas terminal 3, can only connect to terminal 5 of a single up-stream cell or ground.

This rule ensures that for step-up operation the voltage increases monotonically from cell-to-cell. This minimises the number of redundant cell connections. It also means that, for example in Fig. 3, the  $j^{th}$  cell will connect to the  $k^{th}$  cell. Following on from this rule: a zero entry in the cell connection matrix  $c$  is defined as the connection of inputs 1 and/or 2 to the supply voltage  $V_{in}$ , and input 3 to ground.

In order to determine charge-multipliers for a circuit, the charge transfer through a cell must be determined in terms of the converter output charge transfer  $\Delta q_o$  shown in Fig. 3. The net charge transferred out of the  $j^{th}$  cell outputs  $\Delta q_{4j}$  and  $\Delta q_{5j}$ , shown in Fig. 3, can be found as the summation of the charge transfer into the inputs of higher potential cells, for example cell  $k$  which is shown in the same figure.

As previously mentioned, the basic cell has a charging and discharging state, and the active state is determined by the logical gate control signal  $g_j$ , which can have a value of 0 or 1. The net amount of transferred charge from the outputs of the  $j^{th}$  cell during the  $g_j$  state, which are denoted by  $q_{4j}[g_j]$  and  $q_{5j}[g_j]$  in Fig. 3, are then given by the discrete state equations,

$$\Delta q_{4j}[g_j] = \sum_{\substack{c_{xy}=j \\ x=1,2 \\ y=(j+1) \rightarrow N}} \Delta q_{xy}[g_y] \quad (2)$$

$$\Delta q_{5j}[g_j] = \sum_{\substack{c_{3y}=j \\ y=(j+1) \rightarrow N}} \Delta q_{3y}[g_y] \quad (3)$$

The relationship between the input and output charge transfer state equations for the  $j^{th}$  cell can be obtained by noting from [14] that in the steady-state, the cell-capacitor charge transfer over a switching period  $T_s$  is zero, or  $\Delta q_{Cj}[g_j] = -\Delta q_{Cj}[\bar{g}_j]$ . By inspection of the basic cell circuit it is then found that the net amount of charge transferred to the cell capacitor during state  $g_j$ , denoted by  $\Delta q_{Cj}[g_j]$  is hence given by,

$$\Delta q_{Cj}[g_j] = -\bar{g}_j \cdot \Delta q_{4j}[g_j] + g_j \cdot \Delta q_{4j}[\bar{g}_j] \quad (4)$$

Circuit analysis is then used to find the cell charge transfers at the input terminals,  $\Delta q_{1j}[g_j]$ ,  $\Delta q_{2j}[g_j]$  and  $\Delta q_{3j}[g_j]$  shown in Fig. 3, in terms of the charge transfers at the cell output terminals, and after using (4) to eliminate  $\Delta q_{Cj}[g_j]$  from these equations, it is found that the cell input charges are,

$$\begin{aligned} \Delta q_{1j}[g_j] &= g_j (\Delta q_{4j}[g_j] + \Delta q_{4j}[\bar{g}_j]) \\ \Delta q_{2j}[g_j] &= \bar{g}_j (\Delta q_{5j}[g_j] + \Delta q_{4j}[g_j]) \\ \Delta q_{3j}[g_j] &= g_j (\Delta q_{5j}[g_j] - \Delta q_{4j}[\bar{g}_j]) \end{aligned} \quad (5)$$

The analysis of a particular converter, which has a topology defined by (1), then proceeds by solving equations (2)-(5) in an iterative manner starting with the  $N^{th}$  cell, which has

output charge transfer  $\Delta q_o$  and working back to cell 1. In this way state-equations are obtained for each cell in terms of the converter output charge  $\Delta q_o$ .

Finally, the total charge transfer through each component over a switching period  $T_s$  can be obtained as follows: starting with the switches, charge is only transferred through a switch when it is closed, and from Fig. 2 it can be seen that this occurs when,

- $g_j = 1$  for  $S_1$  and  $S_2$
- $g_j = 0$  for  $S_3$

In addition, since  $S_1$ ,  $S_2$  and  $S_3$  are connected to terminals 1,3 and 2 of the basic cell respectively, the charge transfer for each switch is then,

$$\begin{aligned} \Delta q_{SW1j} [1] &= -\Delta q_{1j} [1] \\ \Delta q_{SW2j} [1] &= -\Delta q_{3j} [1] \\ \Delta q_{SW3j} [0] &= \Delta q_{2j} [0] \end{aligned} \quad (6)$$

Since the charge transfer through a switch is zero when it is open, then the total charge transfer during the complete switching period  $T_s$ , denoted by  $\Delta q_{SW1j}$ ,  $\Delta q_{SW2j}$  and  $\Delta q_{SW3j}$  will be,

$$\begin{aligned} \Delta q_{SW1j} &= \Delta q_{SW1j} [1] = -\Delta q_{1j} [1] \\ \Delta q_{SW2j} &= \Delta q_{SW2j} [1] = -\Delta q_{3j} [1] \\ \Delta q_{SW3j} &= \Delta q_{SW3j} [0] = \Delta q_{2j} [0] \end{aligned} \quad (7)$$

Note that a positive or negative value for  $\Delta q_{SW1j}$ ,  $\Delta q_{SW2j}$  and  $\Delta q_{SW3j}$  in (6) indicates whether the switch can be implemented using a diode or a transistor. For unidirectional converters, based on the convention for the direction of charge flow through the switch shown in Fig. 2(b), if the value is positive the switch must be implemented as a transistor, otherwise a diode can be used. For bidirectional converters,  $\Delta q_o$  takes on both positive and negative values and therefore all switches must be implemented using transistors with anti-parallel diodes.

The charge transfer into a cell-capacitor is equal and opposite during both the charging and discharging phases, therefore the value of charge transferred to/from the capacitor over period  $T_s$ , denoted  $\Delta q_{Cj}$  is given by,

$$\Delta q_{Cj} = \Delta q_{Cj} [1] = -\Delta q_{Cj} [0] \quad (8)$$

which represents the capacitor ripple current. The charge-multipliers for the circuit can then be obtained by simply normalising equations (6) or (8) by  $\Delta q_o$ . In this way, the output equivalent resistance of the converter can be obtained from these charge multipliers as described in [14]. The switch and capacitor average currents are calculated by dividing (6) or (8) by  $T_s$ . In addition, if the shape of the current waveform is known, then an expression for the ratios of RMS:average or peak:average can be obtained in order to calculate the component RMS or peak currents. In general, the waveform shapes consist of either a decaying exponential for a hard-switched converter or half-sinusoid for a resonant circuit as described for example in [13].

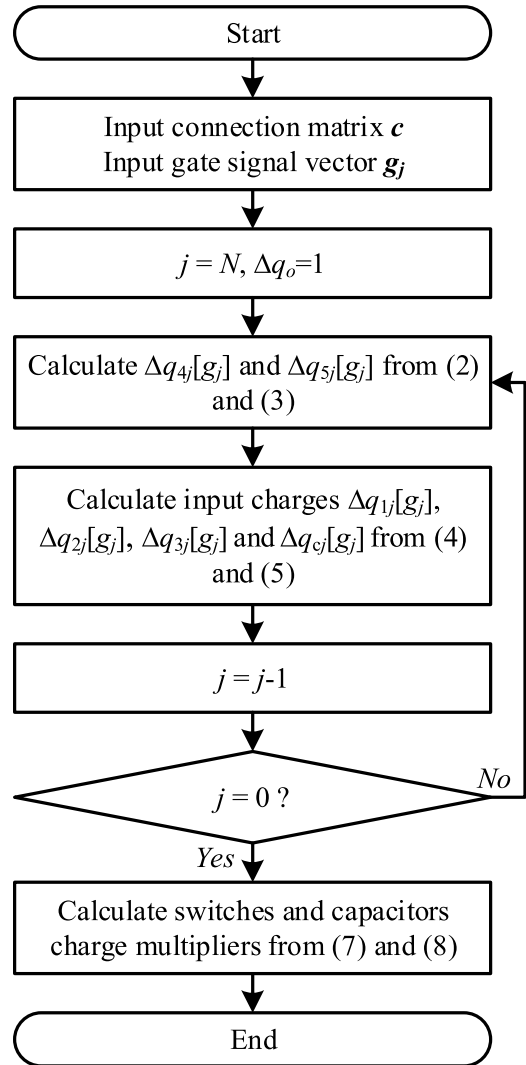


FIGURE 4. Flowchart for the calculation of charge-multipliers.

An algorithm to calculate charge multipliers for auto-appraisal of SC DC-DC converters, which is based on the above analysis, is summarised by the flowchart shown in Fig. 4. The algorithm is very simple and can be implemented using a suitable software programming language such as MATLAB.

In order to use this algorithm for a particular circuit, the circuit topology needs to be pre-defined using the  $3 \times N$  connection matrix  $c$  and a Boolean vector of length  $N$  and denoted by  $g_c$ , which specifies whether a cell gate-signal is connected to the global gate-signal  $g$  or its complement  $\bar{g}$ . This matrix and vector are the only inputs required to the algorithm and the generation of these two inputs corresponds to circuit synthesis. Circuit synthesis is carried out for either:

- *Existing circuits*: the circuit topology needs to be represented in terms of basic cells. The cell connection matrix can then be generated manually by an inspection of the relative interconnection of the cells. All of the popular SC converters can be represented using the basic cell.

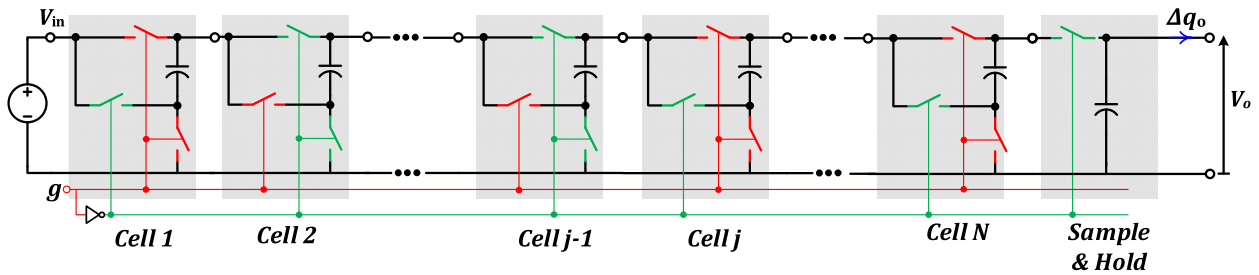


FIGURE 5. The Fibonacci SC converter.

- *New circuits*: in particular this corresponds to auto-synthesis using a computer algorithm. One method would be to fill the connection matrix with random integers, whilst following *Synthesis Rule 1*. In addition, random Boolean values can be entered into the gate-signal vector  $\mathbf{g}_c$ .

Alternatively combining this method with auto-appraisal using an optimisation algorithm, would allow certain cost functions to be minimised. For example, the minimisation of capacitor energy storage requirements and hence converter size. This technique is being investigated further and will be presented in a future paper.

#### IV. EXAMPLE – USING THE PROPOSED METHOD TO DETERMINE AND VALIDATE CHARGE-MULTIPLIERS FOR A FIBONACCI CIRCUIT

In this section the well-known Fibonacci SC circuit is used to demonstrate how the proposed method can be used to derive the charge multipliers for the circuit. First it is shown how the connection matrix  $\mathbf{c}$  and gate-signal vector  $\mathbf{g}_c$  are derived. These are then used as inputs to the algorithm shown in Fig. 4. As a first-step in the validation of the proposed method, the algorithm is used to derive analytic expressions for charge multipliers, where it is found that the results are identical to those obtained previously by circuit inspection as presented in [2]. Secondly the algorithm was coded in MATLAB to automatically derive numerical values for the charge multipliers and additional validation of the method is provided by comparison with a detailed Spice simulation.

##### A. ANALYTICAL DERIVATION OF CHARGE-MULTIPLIERS FOR THE FIBONACCI CIRCUIT USING THE PROPOSED ALGORITHM

The voltage-conversion ratio for an  $N$  cell Fibonacci converter [15] is given by the Fibonacci Number,

$$\frac{V_o}{V_{in}} = F_{N+2} \quad (9)$$

The Fibonacci circuit can be implemented from the basic cell and is shown in Fig. 5, where it can be seen that the Fibonacci converter consists of a cascade connection of the basic cell. From this figure, input terminals 1 and 2 of cell  $j$  connect to the previous cell  $j - 1$  so that  $c_{1j} = c_{2j} = j - 1$ . In addition,

terminal 3 connects to ground so that  $c_{3j} = 0$ . The complete connection matrix  $\mathbf{c}$  is then given by,

$$\mathbf{c} = \begin{pmatrix} 0 & 1 & 2 & \dots & N - 1 \\ 0 & 1 & 2 & \dots & N - 1 \\ 0 & 0 & 0 & \dots & 0 \end{pmatrix} \quad (10)$$

For example, column 3 in the above connection matrix represents the 3<sup>rd</sup> cell of the converter and shows that input terminals 1 and 2 – represented by row 1 and 2 – connect to output terminal 4 of the previous cell 2 – see *Synthesis Rule 1*. In addition, the gate control signal  $g$  and its inverse feed every alternate pair of cells respectively, so that  $g_j = \bar{g}_{j-1}$ . The converter output voltage  $V_o$  is taken from terminal 4 of the  $N^{\text{th}}$  cell using a sample-and-hold circuit. Terminal 5 is unconnected for all cells so that the charge transfers at the cell inputs will be purely a function of the terminal 4 charge  $\Delta q_{4j} [g_j]$ , hence following the algorithm and starting with the  $N^{\text{th}}$  cell,

$$\Delta q_{4N} [g_N] = \bar{g}_N \Delta q_o \quad (11)$$

and then from (5) the  $N^{\text{th}}$  cell input charge transfers are,

$$\begin{aligned} \Delta q_{1N} [g_N] &= g_N \Delta q_o \\ \Delta q_{2N} [g_N] &= \bar{g}_N \Delta q_o \\ \Delta q_{3N} [g_N] &= -g_N \Delta q_o \end{aligned} \quad (12)$$

This then continues with the  $N - 1^{\text{th}}$  cell, then the  $N - 2^{\text{th}}$  cell and so on, such that in general for the  $j^{\text{th}}$  cell it is found that,

$$\begin{aligned} \Delta q_{1j} [g_j] &= g_j (\Delta q_{1(j+1)} [\bar{g}_j] + \Delta q_{1(j+2)} [g_j]) \\ \Delta q_{2j} [g_j] &= \bar{g}_j \Delta q_{1(j+1)} [\bar{g}_j] \\ \Delta q_{3j} [g_j] &= -g_j \Delta q_{1(j+1)} [g_j] \end{aligned} \quad (13)$$

where it is observed from the first equation of (13) that the transferred charge through the converter cells follows a descending Fibonacci series. The transferred charge through the individual switches and capacitor of each cell can then be found from (7), (8), (12) and (13),

$$\begin{aligned} \Delta q_{SW1j} &= F_{N-j+2} \cdot \Delta q_o \\ \Delta q_{SW3j} = \Delta q_{Cj} = -\Delta q_{SW2j} &= F_{N-j+1} \cdot \Delta q_o \end{aligned} \quad (14)$$

Note that dividing (14) through by  $\Delta q_o$  gives the charge-multipliers for the circuit components, which can then be used

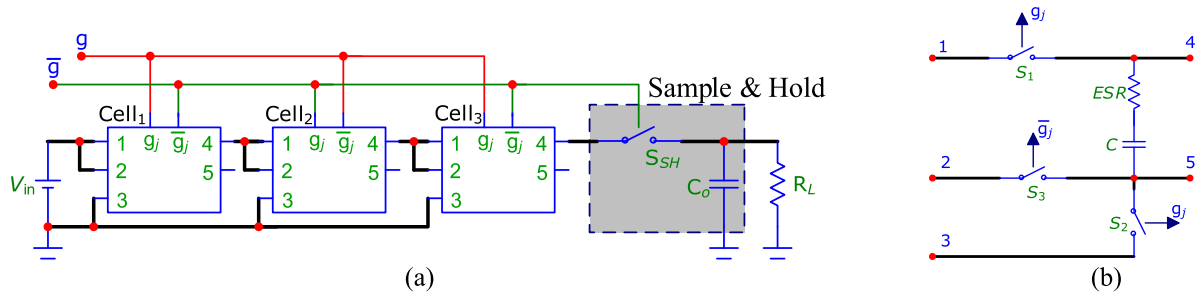


FIGURE 6. (a) Micro-Cap Spice circuit schematic for the 3-cell Fibonacci SC converter (b) Cell sub-circuit schematic used in Micro-Cap simulation.

TABLE 1. Connection matrix and gate signals for traditional topologies and an arbitrary SC converter.

Topology	Connection matrix	Cell gate signal $g_c$
	$c$	
Fibonacci	$\begin{pmatrix} 0 & 1 & 2 \\ 0 & 1 & 2 \\ 0 & 0 & 0 \end{pmatrix}$	$g_j = \overline{g_{j-1}}$ [1, 0, 1]
Series-Parallel	$\begin{pmatrix} 0 & 0 & 0 & 0 \\ 0 & 1 & 2 & 3 \\ 0 & 0 & 0 & 0 \end{pmatrix}$	$g_j = g_{j-1}$ [1, 1, 1, 1]
MMSCC	$\begin{pmatrix} 0 & 1 & 2 & 3 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \end{pmatrix}$	$g_j = \overline{g_{j-1}}$ [1, 0, 1, 0]
Arbitrary Topology	$\begin{pmatrix} 0 & 0 & 1 & 3 \\ 0 & 1 & 1 & 2 \\ 0 & 0 & 1 & 2 \end{pmatrix}$	[1, 1, 0, 1]

Note: it is assumed that  $1 = g, 0 = \overline{g}$

for example to evaluate the converter output resistance from the circuit parasitics [14]. These expressions are identical to those derived using inspection as detailed in [2], which therefore validates the proposed method. Finally, dividing (14) through by  $T_s$  gives the average currents for the components in terms of the converter output current  $\Delta q_o/T_s$ , which can be used as a figure-of-merit if required for limited circuit appraisal against alternative topologies. As previously mentioned a full appraisal would also need to include voltage ratings, and the derivation of voltage ratings.

**B. NUMERICAL COMPUTATION OF CHARGE-MULTIPLIERS AND SIMULATIONS RESULTS FOR THE FIBONACCI CIRCUIT**

To automate the calculation of numerical values of charge-multipliers and provide further validation of the method, the algorithm shown in Fig. 4, was coded in MATLAB, for a 3 cell Fibonacci circuit,  $N = 3$ . The corresponding connection matrix array from (10) and gate-signal vector that are input to the algorithm are shown in Table 1. The charge multipliers calculated by analysis and by the MATLAB algorithm for the switches and capacitors of the  $j^{th}$  cell, are shown in columns three and four of Table 2 respectively. In this table, the switch and capacitor charge-multipliers are denoted by

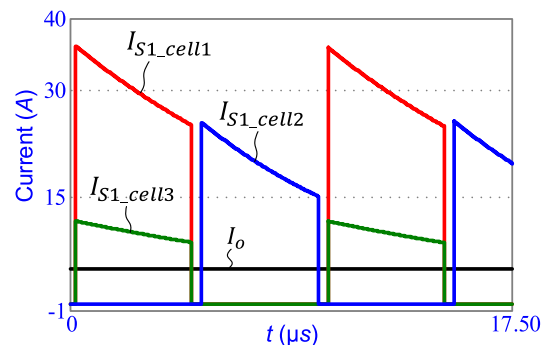


FIGURE 7. Simulation results for current waveform for switch S1 of cells 1-3 in a 3-cell Fibonacci SC converter.

$a_{Swi,j}$  and  $a_{C,j}$  respectively,  $i$  being the number of the switch within a cell – see Fig. 2.

A detailed simulation of a 3 cell, hard-switched, Fibonacci circuit was carried out in Micro-Cap Spice in order to further verify the MATLAB results. This simulation included switch on-state resistances of 20 mΩ, output and cell capacitance were 200 μF with an ESR of 10 mΩ and the switching frequency of the converter was set to 100 kHz with 500 ns dead-time between the 2 switching phases. The input DC voltage was 100 V and the load a 100 Ω resistor. These values represent typical parameters for a 3-kW residential PV SC converter application. The Micro-Cap schematic for the 3 cell Fibonacci circuit is shown in Fig. 6(a) and the sub-circuit schematic for each cell is shown in Fig. 6(b), where the 3 input terminals 1-3 and the two output terminals 4, 5 correspond to the basic cell of Fig. 2.

The current waveforms calculated using the Spice simulation for switch  $S_1$  of cells 1-3, denoted  $I_{S1,cell1}$ ,  $I_{S1,cell2}$  and  $I_{S1,cell3}$  are shown as an example in Fig. 7. The waveforms have the classic exponential decay that is a characteristic of hard-switched SC converters. A numerical integration of these current waveforms over switching period  $T_s$  for the switches and capacitors, as well as the converter output current, was carried out in order to calculate the charge-multipliers from the Spice simulation. These results are shown in column 5 of Table 2, where it can be seen there is very close agreement with the results from the MATLAB algorithm, with errors being less than 1.5%.

TABLE 2. Analysis, MATLAB and simulation results for charge-multipliers for different SC topologies with conversion ratio 5.

Charge-Multiplier				
Topology		Analytic result from solving state equations	MATLAB computation result	Micro-Cap Spice calculated result
Fibonacci	$a_{SW1,j}$	$F_{N-j+2}$	[3, 2, 1]	[ 2.974, 1.984, 0.991]
	$-a_{SW2,j}, a_{SW3,j}, a_{c,j}$	$F_{N-j+1}$	[ 2, 1, 1]	[1.983, 0.989, 0.991]
Series-Parallel	$a_{SW1,j}, -a_{SW2,j}, a_{SW3,j}, a_{c,j}$	1	[1, 1, 1, 1]	[0.992, 0.992, 0.992, 0.991]
MMSCC	$a_{SW1,j}, -a_{SW2,j}, a_{SW3,j}, a_{c,j}$	1	[ 1, 1, 1, 1]	[1.005, 1.005, 1.005, 1.004]
Arbitrary Topology	$a_{SW1,j}$	Not available	[3, 1,1, 1]	[3.038, 1.011, 1.015, 1.013]
	$-a_{SW2,j}$		[2, 2, 1, 1]	[2.025, 2.024, 1.015, 1.013]
	$a_{SW3,j}$		[1, 1, 1, 1]	[1.010, 1.010, 1.013, 1.010]
	$a_{c,j}$		[2, 1, 1, 1]	[2.025, 1.010, 1.015, 1.010]

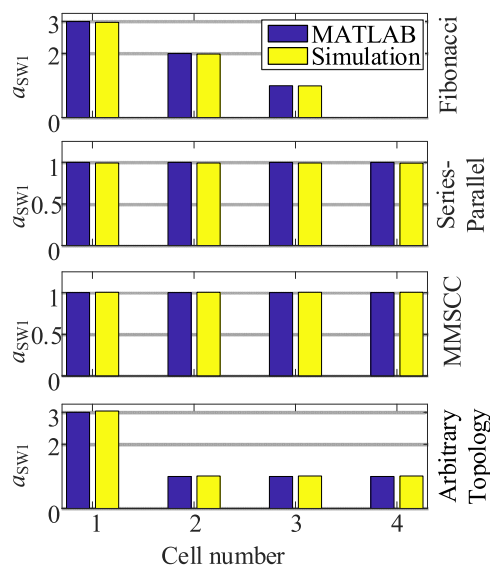


FIGURE 8. MATLAB and simulation results for switch  $S_1$  charge multiplier of each cell for the Fibonacci, Series-Parallel, MMSCC and the Arbitrary topology.

Since the fundamental principle for obtaining charge multipliers is based on applying KCL equations to the basic-cell in the steady-state, the values of the charge-multipliers are independent of transistor dead-time and values of SC capacitance and switch/capacitor resistance. This was confirmed by re-running the simulations, with these parameters changed by an order of magnitude. It was found that the values of the charge-multipliers remained the same.

To aid comparison of the MATLAB and Spice simulation results, bar charts showing the calculated charge multipliers

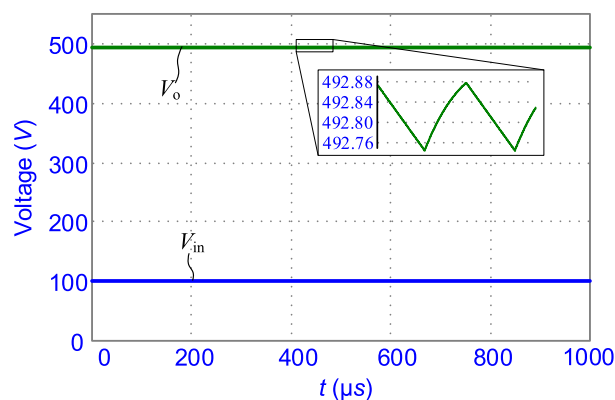


FIGURE 9. Simulation results for input and output voltage of 3 cell Fibonacci circuit.

are shown in the top graph of Fig. 8. The small errors between the MATLAB and Spice results are due to the finite time-step used in the Spice simulation.

The analytic expressions for the charge multipliers, which were derived from the state-equations above (14), are also included in Table 2 for comparison. It can be seen that there is excellent agreement between the three methods – analytic, MATLAB, and Spice.

An example that demonstrates the usefulness of charge multipliers is the calculation of the converter output voltage regulation. To verify the result, the value calculated from the Spice simulation was first obtained from the converter output voltage waveform shown in Fig. 9.

From (9), the step-up ratio for a 3-cell Fibonacci converter is equal to 5, giving a nominal output voltage of 500 V. Under load, the output equivalent resistance of the converter results



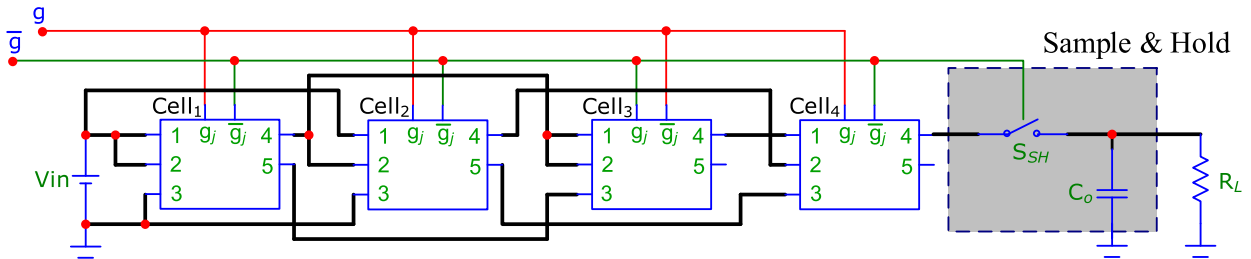


FIGURE 10. Micro-Cap Simulation schematic for arbitrary generated topology based on the connection matrix and gate signals given in Table 1.

in the voltage being slightly below this as can be seen from the zoomed in portion of Fig. 9, where  $V_o = 492.8 V$ . The theoretical value of output resistance was then calculated from the charge multipliers using the technique described in [13]. This gives a value of  $1.38\Omega$  using the MATLAB calculated from the values of charge multipliers shown in Table 2. With the  $100 \Omega$  load used in the simulation this gives a predicted output voltage of  $493.2 V$ , which compares very well with the Spice result. Unlike the calculation of charge-multipliers themselves, the output equivalent resistance is dependent on transistor dead-time and this explains the small difference in the calculation of voltage drop from the MATLAB simulation and the Spice simulation.

V. ANALYSIS OF SERIES-PARALLEL AND MMSCC SC CONVERTERS

The MATLAB algorithm was used to calculate the switch and capacitor charge-multiplier equations for two more, well-known SC circuits namely the Series-Parallel and Multi-level Modular SC Converter (MMSCC) [20]. The number of cells for these converters was chosen to give the same voltage-conversion ratio as the Fibonacci converter  $F_5 = 5$ . Table 1 gives the cell connection matrix and gate-signal vectors for these converters. The results from the MATLAB algorithm are again shown in Table 2, along with the charge-multiplier values calculated from Micro-Cap Spice for validation. Once more, it can be seen there is very good agreement between the MATLAB and Spice results with errors of no greater than 1.5%; these results are also shown by the two middle graphs in Fig. 8. The Spice simulation was also carried out for the resonant variant of these two converters and this again showed very good agreement with the MATLAB results.

VI. SYNTHESIS AND ANALYSIS OF A NEW SC TOPOLOGY

Finally, a completely random SC circuit topology was devised, which has the circuit topology shown in Fig. 10. The circuit was synthesised by simply filling the cell-connection matrix with arbitrary integers, whilst satisfying the design rule that was specified in section III. Since the circuit was generated randomly, it does not have any particularly attractive features, which is to be expected. However, it does demonstrate the simplicity of generating new topologies using the proposed cell-connection matrix.

The connection matrix and gate-signal vector for this new circuit along with the calculation of its charge-multipliers are shown in Table 1 and Table 2/ Fig. 8 respectively. Note that an analytic expression for the charge-multipliers for this circuit is intractable as it lacks a structure that can be defined as a mathematical sequence.

VII. A QUALITATIVE, LIMITED APPRAISAL OF THE CIRCUITS

The charge-multipliers shown in Table 2 also represent the average component currents, normalised to the converter output current. Since the voltage-conversion ratio is the same for all the converters then so are their output currents. It is therefore possible to make a limited, qualitative appraisal of all four circuits presented in Table 2 based on current ratings:

- The components of the input cell of the Fibonacci and Arbitrary converter have high average currents when compared to the Series-Parallel and MMSCC circuits.
- The cells of the Series-parallel and MMSCC converters components have equal current ratings, offering the potential for a modular design.
- The switches and capacitor of the Arbitrary converter all have different current ratings within the same cell and from cell-to-cell. This would be problematic for manufacture since each cell would have to be constructed from different components.

Since these results are based on the calculation of charge multipliers, a similar, limited appraisal could also be carried out based on for example voltage regulation or efficiency. However, in order to carry out a direct comparison of converter performance further converter attributes need to be included such as converter size, which for example is influenced by capacitor energy storage requirements. This metric is encapsulated by the total VA rating of the converter components, which would require the calculation of the voltage ratings of individual devices. This is the objective of the next stage of this research, which then gives the possibility of auto-optimisation of SC converter circuits.

VIII. CONCLUSION

This paper has presented a method for defining SC topologies by proposing a basic cell topology along with a method for defining their inter-connection through a simple connection matrix. By applying a single design constraint on the inter-connection of the cells, this then allows for the auto-

synthesis of SC converters, at the same time eliminating most of the redundant topologies that would arise through placing purely random entries into the matrix.

The charge-multipliers for the SC converters are then obtained by solving the discrete state equations for the converter. This process can be implemented automatically using a simple recursive algorithm, which provides the charge-multipliers numerically. The charge multipliers can then be used to obtain the converter output resistance and component average, peak and RMS currents. The converter output resistance, efficiency and current ratings can then be used to give a limited comparison of the performance of different topologies; a technique termed auto-appraisal. A full comparison would need to include for example converter size, which requires the calculation of component voltage ratings, for which the proposed method is also applicable.

The proposed algorithm was described using the well-known Fibonacci converter as an example, and the results were validated against existing analytic equations as well as a detailed Spice simulation. The algorithm was then implemented in MATLAB script to demonstrate how the charge-multipliers for two other well-known converters – the Series-Parallel and MMSCC circuits could be calculated automatically. Finally, an arbitrary SC converter was devised using the proposed connection matrix method, and its charge-multipliers also calculated using the algorithm. Again, these results were confirmed using detailed Spice simulations.

The method of analysis described in this paper can be used to automatically synthesise and appraise different SC converter topologies in order to search for an optimum circuit for a given application. Whilst this paper has shown how the method can be used to obtain charge multipliers for the calculation of converter component current ratings, a future paper will include component voltage ratings. This then allows the VA rating of a converter to be established, so that a direct comparison of different circuits can be made.

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