A V-Band Doherty Power Amplifier Based on Voltage Combination and Balance Compensation Marchand Balun

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ABSTRACT This paper presents a V-band Doherty power amplifier (PA) which is implemented in a standard 65-nm CMOS technology. The voltage combination technique is used to realize the millimeter-wave Doherty PA without the λ/4 transmission lines. A Marchand balun with balance compensation is designed to combine the output power with reduced power loss. Moreover, a nonlinear driver is used to drive the peaking amplifier to enhance the output power and the turn-on speed of it. The power-added efficiency (PAE) of this PA at the 6-dB power back-off point is 8.7% and the peak PAE reaches 16.8%. The small signal power gain is 18 dB, and the maximum output power is 14.9 dBm. The core circuit only costs 0.195 mm^2 chip area as no λ/4 transmission lines.

INDEX TERMS CMOS, Doherty power amplifiers, millimeter-wave, Marchand balun, voltage combination.

I. INTRODUCTION

The requirement of the high-speed communication greatly increases with the multimedia information explosion. Millimeter-wave (mm-wave) frequency band is attractive for realizing gigabit-per-second (Gbps) communication because of the broad absolute bandwidth [1]–[3]. Standards in this band, such as IEEE 802.11.ad, provide the option of OFDM mode to enhance the communication speed. However, this gives the signal a high peak-to-average ratio (PAPR), which requires PAs to have a high PAE at the power back-off region. The Doherty PA [4] is one of the competitive techniques. Since no extra control circuit is needed, the Doherty PA is not limited by the bandwidth of the control circuit compared with the other techniques, such as dynamic biasing, envelope tracking, and transistor reconfiguration. However, impedance-transforming network, which is usually implemented by λ/4 transmission lines, is indispensable in the conventional Doherty PAs. The λ/4 transmission lines usually consume large area and work only in a narrow bandwidth [5]. Moreover, the Class-C mode peaking amplifiers in mm-wave frequency region suffer from low power gain and have a low efficiency when it starts to turn on [6].

The voltage combination technique is able to realize active load modulation without impedance transformer network [7]–[11]. However, the λ/4 transmission lines are also needed to realize a zero impedance for the peaking amplifier [7], [8]. A 60GHz Doherty PA free of the λ/4 transmission lines is presented in this paper. A Marchand balun with balance and phase compensation is used to realize the output voltage combination. In order to improve the performance of the peaking amplifier, a nonlinear driver is used to make the peaking amplifier obtain a higher output power and power gain. At the same time, the nonlinear driver enables the peaking amplifier to have a steeper turn-on performance. The V-band Doherty PA is realized in a standard 65nm CMOS technology. The peak PAE reaches 16.8%, while it is 8.7% at the 6-dB power back-off point. Since no λ/4 transmission lines are needed, the core area only costs 0.195 mm^2.

Section II gives a detailed analysis of the active load modulation method in the mm-wave frequency region and the implementation based on a Marchand balun. Section III presents a V-band Doherty PA based on the proposed method. The measurement result is given in Section IV. Finally, the paper is concluded in Section V.
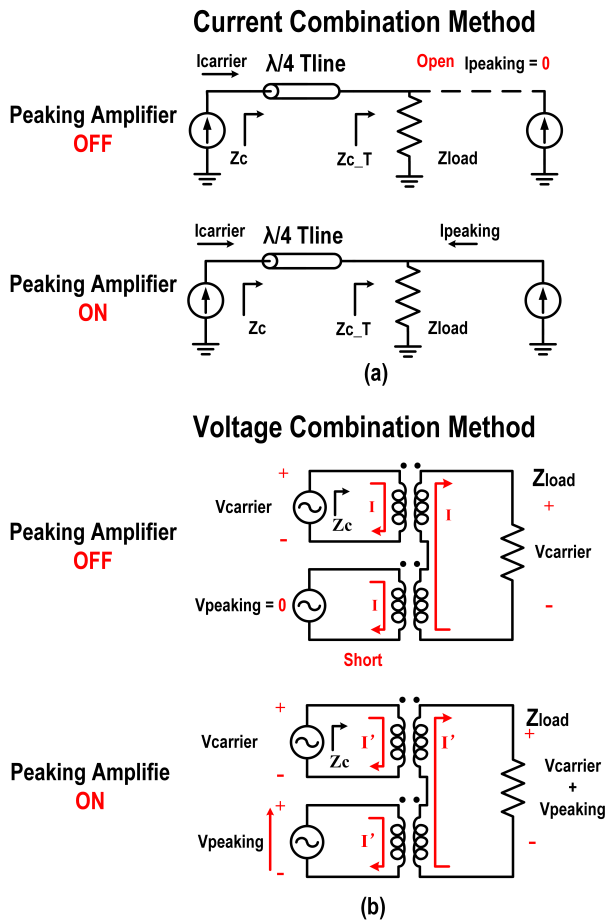
Current Combination Method

FIGURE 1. The operation principles of active load modulation. (a) The current combination technique. (b) The voltage combination technique.

II. ACTIVE LOAD MODULATION IN MM-WAVE FREQUENCY

A. CURRENT COMBINATION ACTIVE LOAD MODULATION IN THE MM-WAVE FREQUENCY REGION

The conventional Doherty PA consists of two amplifiers (carrier amplifier and peaking amplifier) and the impedance transforming network. Fig. 1(a) shows the simplified current source models of the current combination active load modulation. When the input power is lower than the turn-on threshold power, the peaking amplifier is turned off, and its output impedance is infinity. The load impedance of the carrier amplifier (Z_c) is constant according to (1)

$$Z_c = \frac{Z_0^2}{Z_{c\_T}} = \frac{Z_0^2}{Z_{Load}} \qquad (1)$$

After the peaking amplifier is turned on, the current of the peaking amplifier is delivered to the load, and then the load impedance of carrier branch (Z_{c_T}) increases. As a result, Z_c decreases as given in (2). A smaller load impedance Z_c enables the carrier amplifier to push out more output current with the maximum efficiency. The impedance variation of the load impedance in current combination Doherty PA is shown
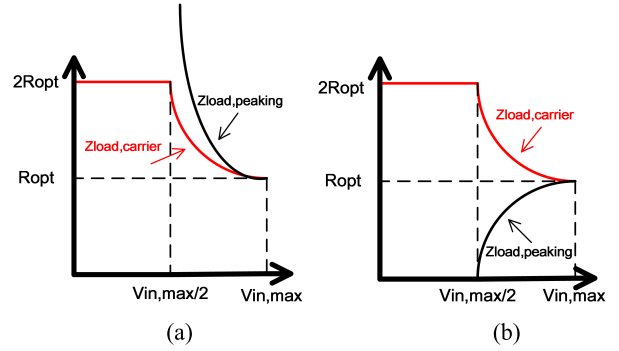

FIGURE 2. Load impedance variation of (a) the current combination technique and (b) the voltage combination technique.

in the Fig. 2 (a).

$$\left.\begin{array}{l} Z_c = \dfrac{Z_0^2}{Z_{c\_T}} \\[2ex] Z_{c\_T} = Z_{Load}\left(1 + \dfrac{I_{Peaking}}{I_{Carrier}}\right) \end{array}\right\}$$

$$\Rightarrow Z_c \downarrow = \frac{Z_0^2}{Z_{Load}}\left(1 - \frac{I_{Carrier}}{\uparrow I_{Peaking} + I_{Carrier}}\right) \qquad (2)$$
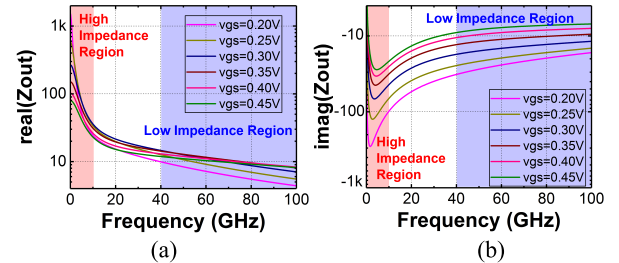

FIGURE 3. The (a) real part and (b) imaginary part of a transistor's output impedance.

The current combination method faces an enormous challenge in the mm-wave frequency region. The output impedance of the peaking amplifier cannot be treated as an open circuit in the back-off region. On the contrary, it is more like a short circuit as the impedance is very small when the frequency reaches the mm-wave frequency region. Fig. 3 shows the output impedance versus frequency of a transistor with 144 um width at the different bias voltages. The magnitude of the impedances' real parts and imaginary parts are very high when the frequency is lower than 3 GHz, which can be treated as an open terminal. However, their values' magnitudes fall rapidly versus frequency and are close to a short terminal in the mm-wave frequency region. This phenomenon is even worse when the bias condition is close to Class-C mode. The low output impedance of the peaking amplifier makes the current of carrier amplifier flow into the peaking amplifier when the peaking amplifier is off, which decreases the efficiency or even makes the active load modulation work wrongly. The impedance variation versus frequency can be explained by a simplified model [12] as
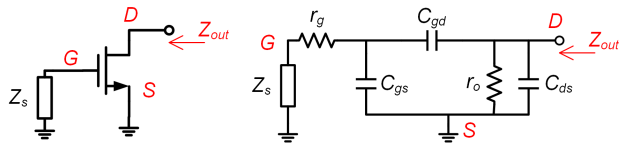
FIGURE 4. The equivalent model of a transistor in the cut-off region.

shown in Fig. 4. Since the transistor is biased at Class-C mode and working in the cut-off region, the output impedance is mainly determined by the parasitic components. The output impedance can be expressed as

$$Z_{out} = 1/(1/(\frac{Z_s + r_g}{1 + j\omega C_{gs}(Z_s + r_g)} + \frac{1}{j\omega C_{gd}}) + j\omega C_{ds} + \frac{1}{r_o})$$
$$\approx \frac{1/r_o}{1/r_o^2 + \omega^2 C^2} - j\frac{\omega C}{1/r_o^2 + \omega^2 C^2} \quad (3)$$

where C represents

$$C = \frac{C_{gd}C_{gs}}{C_{gd} + C_{gs}} + C_{ds} \quad (4)$$

It can be seen that both of the real and imaginary parts are close to zero when the ω increases, which agrees with the simulation result in the Fig. 3.

B. VOLTAGE COMBINATION ACTIVE LOAD MODULATION IN THE MM-WAVE FREQUENCY REGION

Voltage combination technique is another technique to realize the active load modulation [7], [8], [13]. The simplified model is shown in Fig. 1(b). In the lower power condition, the peaking amplifier is turned off. The voltage and output impedance of it is close to zero with no energy consumed. At the same time, the carrier amplifier delivers voltage to the load through the transformer. The load impedance of the carrier amplifier is constant and equal to load impedance (Z_{load}) as given in (5).

$$Z_c = \frac{V_{carrier}}{I} = Z_{Load} \quad (5)$$

When the carrier amplifier reaches the maximum PAE point, the peaking amplifier is turned on. The two amplifiers add the output voltage to the load through the voltage series combination transformer. With the output voltage of the peaking amplifier increasing, the load impedance of the carrier amplifier decreases according to (6).

$$\left.\begin{array}{l} Z_C = \dfrac{V_{Carrier}}{I'} \\ I' = \dfrac{V_{Carrier} + V_{Peaking}}{Z_{Load}} \end{array}\right\} \Rightarrow Z_c \downarrow = \dfrac{V_{Carrier}Z_{Load}}{V_{Carrier} + V_{Peaking} \uparrow} \quad (6)$$

The carrier amplifier can deliver more current with the maximum efficiency. The variation of the load impedance in voltage combination Doherty PA is shown in Fig. 2 (b). No $\lambda/4$ transmission line is employed to realize the active load modulation. However, $\lambda/4$ transmission lines are still essential in the real voltage combination Doherty PA in the
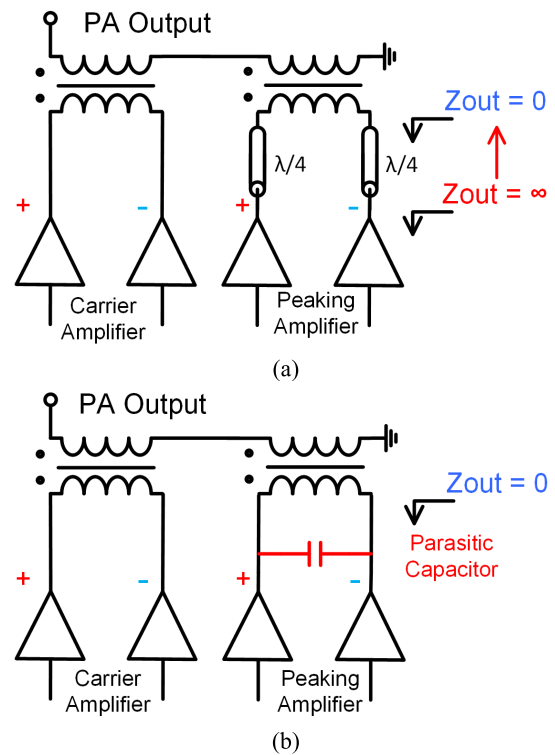

FIGURE 5. The voltage combination Doherty PA in (a) the low-frequency region and (b) the high-frequency region.

low-frequency region. As stated before, the peaking amplifier should show a zero output impedance. The $\lambda/4$ transmission lines transfer the high output impedance of the peaking amplifier to zero [7], [8] as shown in Fig. 5(a). In the mm-wave frequency region, the $\lambda/4$ transmission lines can be avoided, as the output impedance is approximately zero as shown in Fig. 3. The voltage combination Doherty PA can be simplified to the schematic in the Fig. 5(b) in the mm-wave frequency region. The output terminals of the carrier amplifier and the peaking amplifier can be combined directly.

C. VOLTAGE COMBINATION MARCHAND BALUN WITH BALANCE COMPENSATION

The voltage combination is usually implemented by the transformers [14] in the PA design. The transformers can be employed as baluns at the same time [15], [16]. The operation principle of the transformers is the magnetic field coupling as shown in Fig. 6(a). For the transformer balun, the main problem is the imbalance of the differential terminals [17], [18]. The impedance difference of the terminals increases the loss of the balun and even makes the load impedance far from the optimized impedance (R_{opt}) for best output power or PAE performance. The main reason for the imbalance is the addition capacitive parasitic components [18]. The parasitic current (I_c) flows from the input coil to the output coil through the parasitic capacitor is contrary to the original output current (I_{out}) as shown in the Fig. 6(a), which
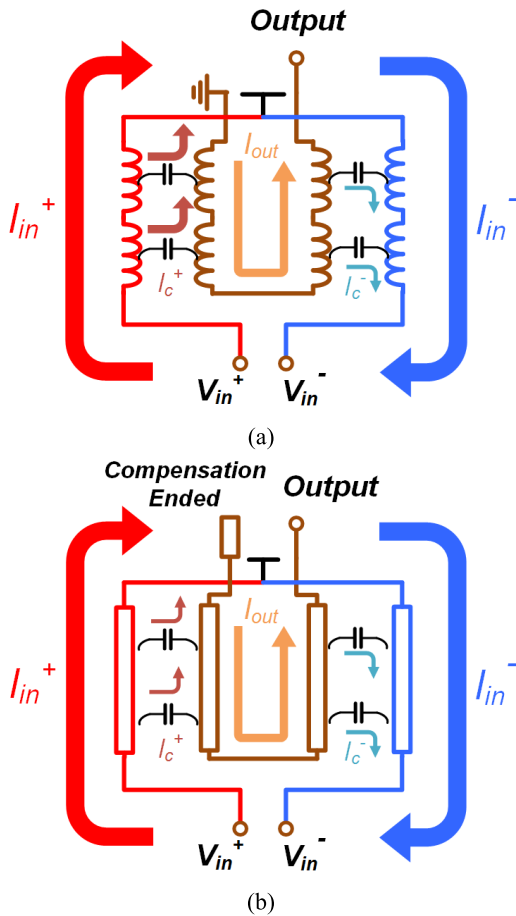
(a)

(b)

FIGURE 6. (a) The transformer balun and (b) the Marchand balun with the balance compensation.

increases the power loss.

$$P_{out} = (I_{out} - I_c^+ - I_c^-)R_{Load} \qquad (7)$$

The load impedance from each terminal can be expressed as

$$\begin{cases} Z_{Load}^+ = \dfrac{V_{in}^+}{I_{in}^+ + I_c^+} \\ Z_{Load}^- = \dfrac{V_{in}^-}{I_{in}^- + I_c^-} \end{cases} \qquad (8)$$

The Ic from the positive terminal (I_c^+) is higher than that from the negative terminal (I_c^-), and the currents have different phases, which generates the imbalance.

$$I_c^+ \neq I_c^- \Rightarrow Z_{Load}^+ \neq Z_{Load}^- \qquad (9)$$

The reason for this phenomenon is that the output coil is connected to the ground directly and the I_c^+ flow to the ground through a low impedance path. On the contrary, the I_c^- is much smaller and has a different phase, since the output terminal is connected to a fixed load.

An offset transformer balun is used in [18] to decrease the parasitic capacitors. However, the offset also reduces the power coupling. A balance compensation Marchand balun is

proposed as shown in Fig. 6(b). The main idea is to reduce I_c^+ to the same value as I_c^-, which makes impedance equal. The Marchand balun enables the usage of the open-ended transmission line instead of the grounded inductors. The open terminal of the Marchand balun cuts off the direct current path to the ground. Then the I_c^+ can be reduced. An additional open-ended transmission line is added to the open terminal to tune the magnitude and phase of the I_c^+ to make it equal to the I_c^-. Then the Z_{Load}^+ and Z_{Load}^- are balanced. Because of the decrease of I_c, the power loss is also reduced.

III. V-BAND DOHERTY PA CIRCUIT DESIGN
A. CIRCUIT OVERVIEW
A V-band Doherty PA is designed in the 65 nm bulk CMOS technology. Fig. 7 shows the schematic of the proposed PA. Voltage combination method is used to realize the Doherty operation, and a voltage series combination Marchand balun with balance compensation is adopted. Each amplifier core uses the stacked transistors to enhance the voltage supply and then increase the output power [19]. To increase the stability and power gain, neutralization technique is used [20]. The carrier PA is working in the Class-AB mode. The peaking amplifier is driven by a Class-C mode nonlinear driver to obtain a faster current growing and a better power gain. The driver before the carrier amplifier is used to balance the gain and phase of the two paths. To obtain a wide-band matching, the transformers are inserted between the stages as the matching networks. The input power divider is also based on the Marchand balun.

B. BALANCE COMPENSATED MARCHAND BALUN
The output voltage series combination Marchand balun is shown in Fig. 8 (a). The 3-D view is shown in Fig. 8(b). The output network consists two series Marchand balun. The balun for peaking amplifier is ended with a balanced compensation open transmission line as described in Section II. A phase compensation line is inserted between the baluns for carrier and peaking amplifier to make the voltages combined in an accurate phase. The layout of the two baluns is set in the orthogonal direction to minimize the coupling between the coils [21], [22], which avoids the imbalance and power loss generated by the unwanted coupling. The output terminal is connected to a G-S-G pad. The Marchand balun transfers the load impedance to the optimized load impedances without any other matching networks.

C. POWER AMPLIFIER AND NONLINEAR PEAKING AMPLIFIER DRIVER
The peaking amplifier is usually implemented by a fixed Class-C mode PA. However, the fixed Class-C mode amplifiers deliver lower output power as the red line in Fig. 9(a) [23]. This is more serious in the mm-wave region. Both of the output power and power gain drop rapidly when the bias voltage decreases as shown in Fig.9 (b). The power gain is usually less than 5 dB, which is unusable in reality.
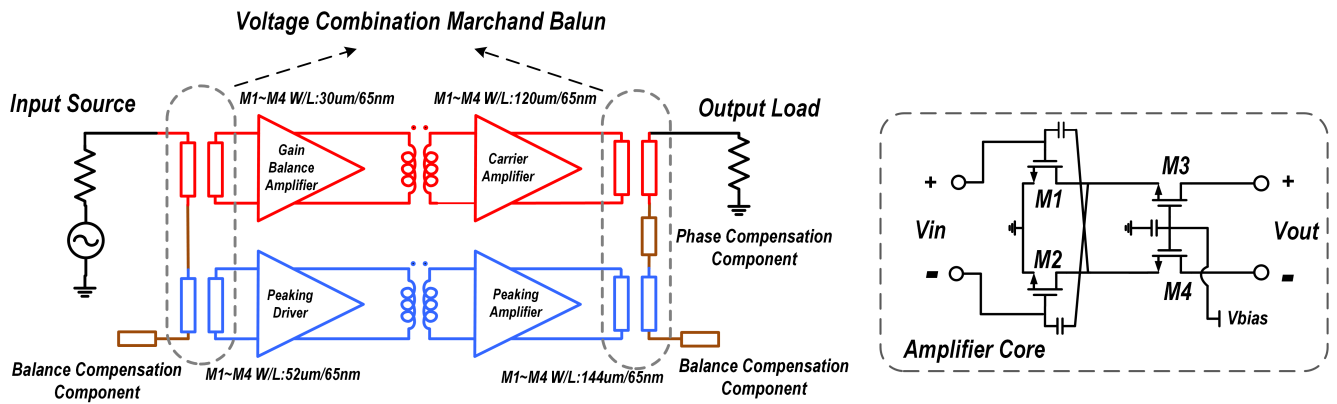
FIGURE 7. Schematic of the proposed V-band Doherty PA using the voltage combination Marchand balun.
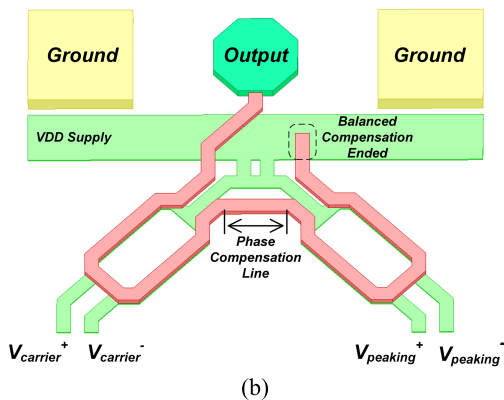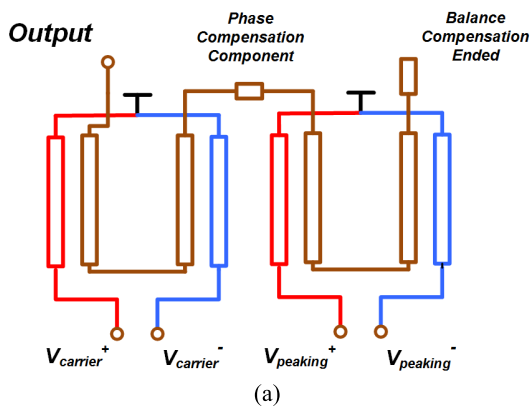

FIGURE 8. The (a) output voltage series combination Marchand balun and the (b) 3-D view.

FIGURE 9. The (a) normalized output voltage of amplifiers and the (b) power gain of PA with different bias voltage.

FIGURE 10. The nonlinear driven peaking amplier.

The efficiency is also very low when the peaking amplifier starts to turn on. On the other hand, the cut-off performance deteriorates if the bias voltage increases. Therefore, a nonlinear power gain of the peaking amplifier is needed as the green line in the Fig. 9(a). Adaptive bias technology [24]–[27] is a common solution for the problem. However, this requires the adaptive bias circuit's bandwidth larger than that of the envelope signal, which is difficult to achieve for the high-speed systems with the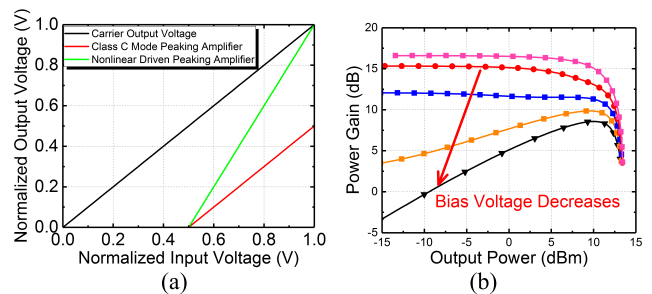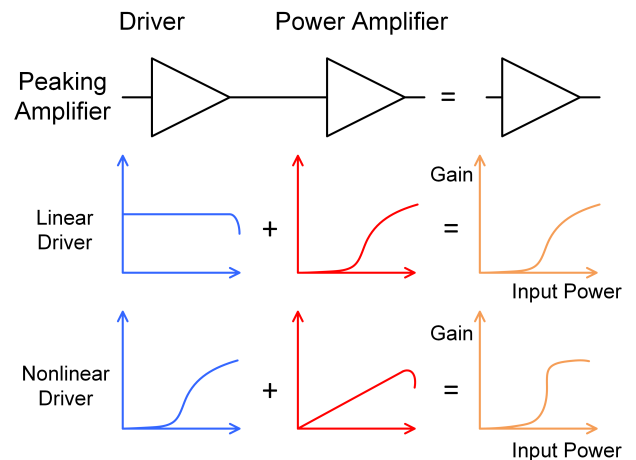 multi-Gbps transmission rate. An uneven power splitting method is proposed in [7] taking advantage of the nonlinearity of the transistors' parasites capacitors in 180 nm CMOS technology. However, it cannot be implemented in the 65nm CMOS technology, since the nonlinearity is reduced with the reduced transistor size.

A nonlinear driver with gain expansion can be placed before the peaking amplifier to make it have a steeper turn-on performance [6]. In this design, a Class-C mode driver is used with a light Class-C peaking PA. The nonlinearity of the

TABLE 1. Comparison of state-of-art mm-wave PA.

| Reference	[9]	[26]	[27]	[28]	[29]	[30]	[31]	**This work**
Technology	40nm CMOS	65nm CMOS	65nm CMOS	28nm UTBB FD-SOI	40nm CMOS	28nm CMOS	130nm SiGe	**65nm CMOS**
Type	Doherty	Doherty	Doherty	Reconfigurable	Class AB	Doherty	Doherty	**Doherty**
Freq (GHz)	72	57-64	60	60	70.3-85.5	32	39	**60**
Supply (V)	1.5	1.8	1.8	1.0	0.9	1.0	1.5	**2.0**
P_{sat} (dBm)	21	11.8	16	18.8	20.9	19.8	17	**14.9**
Peak PAE (%)	13.6	19	14	21	22.3	21	21.4	**16.3**
6dB Back-off PAE (%)	7	8[#]	8	11[*]	7	13[*]	12.6	**8.7**
Gain (dB)	20	16	12.8	15.4	14-16	22	16.6	**18**
Area (mm²)	0.19	0.43	0.52	0.162	0.462	0.59	1.76	**0.195**

*estimated from the plot   # drain efficiency
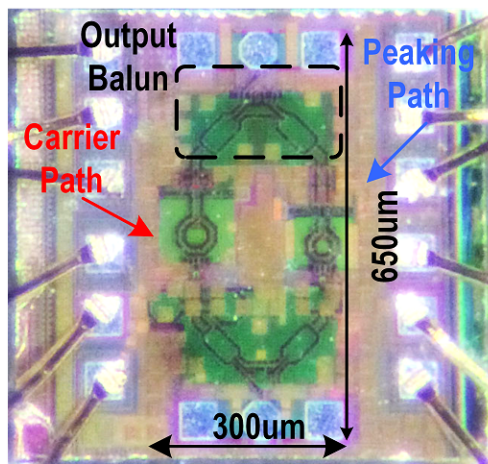
FIGURE 11. The die photo of the proposed V-band Doherty PA.
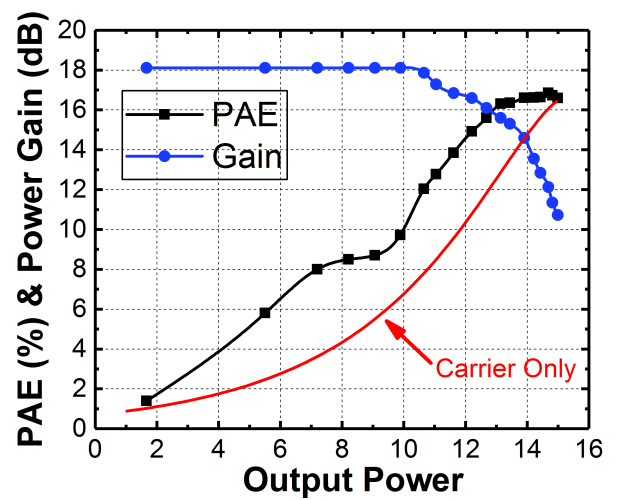
FIGURE 13. The large signal performance versus output power.
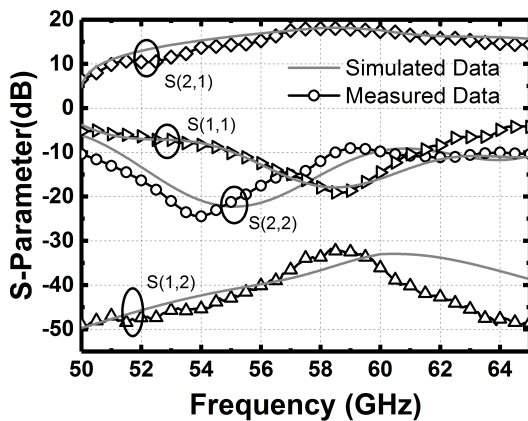
FIGURE 12. The simulated and measured S-parameters.
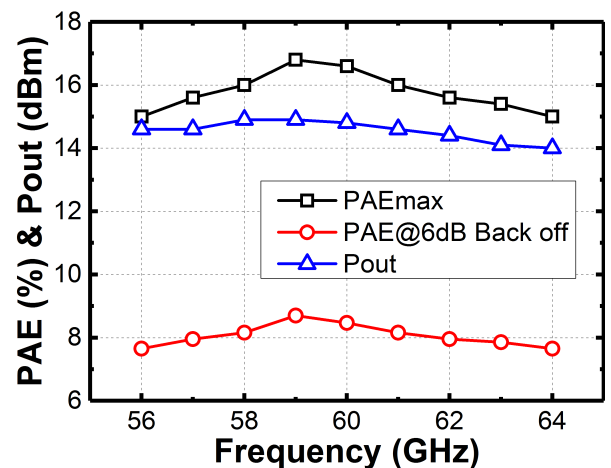
FIGURE 14. The large signal performance versus frequency.

driver enables the peaking PA having a higher bias point with a better performance as shown in Fig. 10. With a higher bias point, the peaking PA can deliver more power and get a higher power gain.

The carrier PA is biased at the Class-AB mode. The driver of the carrier PA is designed to balance the power gain and phase of two paths [5].

IV. MEASUREMENT RESULT

The Doherty PA is fabricated using a standard 65nm bulk CMOS process. The die photo is shown in Fig. 11. With no $\lambda/4$ transmission lines, the core region of the power amplifier

is only 0.195 mm^2 including the input and output RF pads. Fig. 12 shows the measured small signal S-parameter. The maximum S21 is 18 dB and the 3 dB bandwidth is 5.2 GHz. Fig. 13 shows the large signal performance versus output power. The maximum output power is 14.9 dBm and the peak PAE is 16.8% at 59 GHz. The PAE reaches 8.7% at the 6 dB power back-off point. The red line shows the simulated PAE of carrier PA only. It can be seen that the proposed PA shows a better PAE performance in the power back off region. Fig. 14 shows the large signal performance versus the frequency. Table 1 summarizes the comparison with the state-of-art silicon-based mm-wave power amplifiers.

V. CONCLUSION

A V-band Doherty PA is implemented using the voltage combination method. A voltage series combination Marchand balun with balance compensation is used to improve the performance. To improve the performance of the peaking amplifier, a nonlinear Class-C mode driver is adopted to enhance the current growing. The PAE reaches 8.7% at the 6 dB power back-off point [28]–[31].

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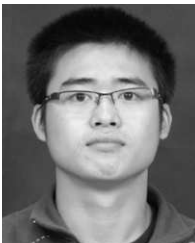
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