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A Simplified Modulation Strategy of Nine-Switch Inverter to Cut Off Half of Switching Modes

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ABSTRACT Nine-switch inverters were designed by sharing three-switches to realize dual-outputs, which are normally realized by two three phase inverters with 12 power semiconductors. Therefore, its modulation strategy is very complex and hard to implement. For this reason, a simplified modulations strategy for the nine-switch inverter is proposed. Based on the switched system model, m-modes controllability of the nine-switch inverter is first proposed to design a simplified space vector pulse width modulation (SVPWM) strategy. Compared with the conventional SVPWM strategies, the newly proposed switching scheme cannot only reduce half of the operating modes but also reduce the switching frequencies. It is significant since it can simplify the control, increase power efficiency and reduce economy cost. Finally, a prototype is designed to verify the proposed modulation strategy.

INDEX TERMS Controllability, nine-switch inverter, switched linear system, SVPWM.

I. INTRODUCTION

By sharing three switches of two three-phase inverters, a nine-switch inverter was presented with reduced number of semiconductors. It is a promising converter that has been studied in many engineering applications, such as the multiple-generator drivetrain [1], motor drive system [2]–[4], grid-connected power sources [5], [6], uninterrupted power supply (UPS) [7] and hybrid power filters [8]. Modulation strategies of the nine-switch inverter is complicate, in order to achieve superior performance of the inverter, modulation strategies, such as the sinusoidal pulse width modulation (SPWM) [9]–[11] and the space vector pulse width modulation (SVWPM) [12]–[16], also have been studied in numerous research papers. Due to the inherent features of nine-switch inverter topology, its control and modulations strategies presented in aforementioned papers are very complicated, which will result in high switching frequencies and switching losses. In order to solve this problem, a novel modulation for simplifying the modulation is eagerly required.

It is considered that the switching frequencies of the power semiconductors can be reduced if less operating modes are involved in the switching sequence. Therefore, the purpose of this paper is to design a novel SVPWM strategy by minimize the number of the operating modes and semiconductors switching of the inverter used in the SVPWM strategy from the aspect of controllability theory.

Though it is of great significance both in applications and in theory, researching on controllability issues of power converters is scanty. One of the main reason is that power converters are inherent strong nonlinearity, it is difficult to study its controllability issues systematically without an accurate mathematical model [17]. Hence, a novel modeling theory is used to model the power converters as a hybrid system, namely, switched linear system model [18], thereafter, controllability of the power converters based on hybrid systems model are studied, such as the controllability and reachability of the boost converter, the periodic controllability and, output controllability of DC/DC converters [19], [20], and the controllability of three-phase inverter [21]. However, the controllability of the nine-switch inverter has not been concerned. More importantly, the switching sequence of the system is not a primary concern in aforementioned papers.

In order to achieve a better performance of the SVPWM strategies of the nine-switch inverter, this paper investigates

the state controllability and m-modes controllability of the nine-switch inverter based on the switched system model, consequently, develop a new design methodology for designing new switching sequences for power converters.

The rest of the paper is organized as follows. Section II describes how to model the nine-switch inverter as a hybrid system, namely switched linear system. In section III, the controllability feature of the proposed hybrid system model of nine-switch inverter is studied. Main results of this paper is presented in section IV, in where a novel SVPWM scheme is proposed to control the nine-switch inverter. In section V, a prototype is designed to verify the proposed modulation strategy. Finally, Section VI draws the conclusions.

II. A SWITCHED LINEAR SYSTEM MODEL

In terms of modeling methods of hybrid system theory, a power converter can be described by the following differential equations:

$$\begin{cases} \dot{x}(t) = A_{\sigma(t)}x(t) + B_{\sigma(t)}u(t) \\ y(t) = C_{\sigma(t)}x(t) \\ \sigma(t) = \varphi(t, u(t), x(t)/y(t)) \end{cases} \tag{1}$$

where $x(t) \in R^n$ is the state vector, $u(t) \in R^p$ is the input vector, $y(t) \in R^q$ is the measured output, $\sigma(t)$ is the switching signal which is decided by the specific control algorithm, and $\sigma(t) \in \{1, 2, \cdots k\}$, where k is the total number of operating modes of the converter.

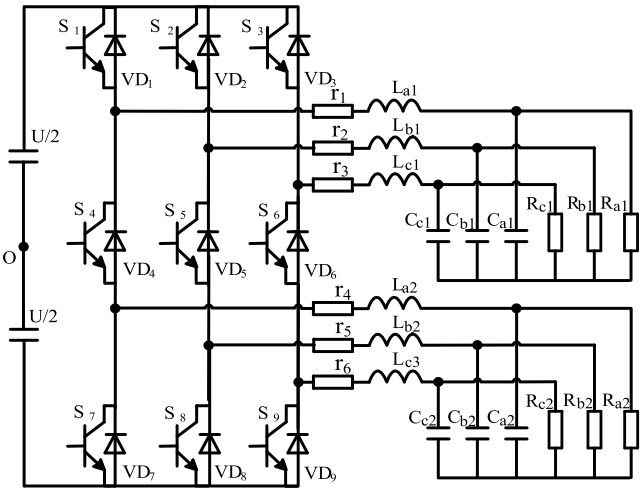


FIGURE 1. Circuit of the dual output nine-switch inverter.

The circuit diagram of the dual output nine-switch inverter is shown in Fig. 1. Therein, the nine-switch inverter can be divided into two parts, namely, the upper part consisting of S_1, S_2, S_3, S_4, S_5, S_6, and the lower one consisting of S_4, S_5, S_6, S_7, S_8, S_9, particularly, the switches S_4, S_5 and S_6 are shared with the upper and the lower inverters.

The conventional SVPWM scheme consists of 14 vectors (also named 14 modes) as shown in Table 1. Denote the state variables of the nine-switch inverter

TABLE 1. Operating modes, switching state and vectors of SVPWM.

mode	S1	S2	S3	S4	S5	S6	S7	S8	S9	vector
①	1	0	0	0	1	1	1	1	1	a100
②	1	1	0	0	0	1	1	1	1	a110
③	0	1	0	1	0	1	1	1	1	a010
④	0	1	1	1	0	0	1	1	1	a011
⑤	0	0	1	1	1	0	1	1	1	a001
⑥	1	0	1	0	1	0	1	1	1	a101
⑦	1	1	1	1	0	0	0	1	1	b100
⑧	1	1	1	1	1	0	0	0	1	b110
⑨	1	1	1	0	1	0	1	0	1	b010
⑩	1	1	1	0	1	1	1	0	0	b011
⑪	1	1	1	0	0	1	1	1	0	b001
⑫	1	1	1	1	0	1	0	1	0	b101
⑬	1	1	1	0	0	0	1	1	1	111
⑭	0	0	0	1	1	1	0	0	0	000

*: "1" means the power semiconductor turns on; "0" means the power semiconductor turns off.

as $x = \{x_1\ x_2\}^T$, where $x_1 = \{i_{au}, i_{bu}, i_{cu}, u_{au}, u_{bu}, u_{cu}\}^T$ *and* $x_2 = \{i_{ab}, i_{bb}, i_{cb}, u_{ab}, u_{bb}, u_{cb}\}^T$, therein, i_{au}, i_{bu}, i_{cu}, u_{au}, u_{bu}, u_{cu} are the currents through the inductances L_{a1}, L_{b1}, L_{c1} and the capacitor voltages on C_{a1}, C_{b1}, C_{c1} of the upper inverter, i_{ab}, i_{bb}, i_{cb}, u_{ab}, u_{bb}, u_{cb} are the inductor currents and capacitor voltages of the lower inverter,. For convenience, assuming the capacitance value of C_{a1}, C_{b1} and C_{c1} equal C_U, C_{a2}, C_{b2}, and C_{c2} equal C_L; the inductance value of L_{a1}, L_{b1}, and L_{c1} equal L_U, L_{a2}, L_{b2} and L_{c2} equal L_L; the resistance value of R_{a1}, R_{b1}, and R_{c1} equal R_U, R_{a2}, R_{b2} and R_{c2} equal R_L; the resistance value of the wire equivalent impedance r_1, r_2, r_3, r_4, r_5 and r_6 equal r. Hence, the switched linear system model with the aforementioned 14 operating modes (14 vectors shows in Table 1) can be described by equation (1), where $k = 14$, *and*

$$A_1 = \cdots = A_{14} = \begin{bmatrix} A_{11} & 0 \\ 0 & A_{22} \end{bmatrix} \tag{2}$$

$$\begin{bmatrix} B_1 & B_2 & \cdots & B_{14} \end{bmatrix} = \begin{bmatrix} B_{11} & 0 \\ 0 & B_{12} \end{bmatrix} \tag{3}$$

$$C_1 = \cdots = C_8 = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 & 1 \\ 0 & 0 & 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 1 & 0 & 0 \end{bmatrix} \tag{4}$$

and

$$A_{11} = \begin{bmatrix} -\frac{r}{L_U} & 0 & 0 & -\frac{1}{L_U} & 0 & 0 \\ 0 & -\frac{r}{L_U} & 0 & 0 & -\frac{1}{L_U} & 0 \\ 0 & 0 & -\frac{r}{L_U} & 0 & 0 & -\frac{1}{L_U} \\ \frac{1}{C_U} & 0 & 0 & -\frac{1}{R_U C_U} & 0 & 0 \\ 0 & \frac{1}{C_U} & 0 & 0 & -\frac{1}{R_U C_U} & 0 \\ 0 & 0 & \frac{1}{C_U} & 0 & 0 & -\frac{1}{R_U C_U} \end{bmatrix} \tag{5a}$$

$$A_{22}=\begin{bmatrix} -\frac{r}{L_L} & 0 & 0 & -\frac{1}{L_L} & 0 & 0 \\ 0 & -\frac{r}{L_L} & 0 & 0 & -\frac{1}{L_L} & 0 \\ 0 & 0 & -\frac{r}{L_L} & 0 & 0 & -\frac{1}{L_L} \\ \frac{1}{C_L} & 0 & 0 & -\frac{1}{R_L C_L} & 0 & 0 \\ 0 & \frac{1}{C_L} & 0 & 0 & -\frac{1}{R_L C_L} & 0 \\ 0 & 0 & \frac{1}{C_L} & 0 & 0 & -\frac{1}{R_L C_L} \end{bmatrix} \tag{5b}$$

$$B_{11}=\begin{bmatrix} \frac{1}{2L_U} & \frac{1}{2L_U} & -\frac{1}{2L_U} & -\frac{1}{2L_U} & -\frac{1}{2L_U} & \frac{1}{2L_U} & \frac{1}{2L_U} & -\frac{1}{2L_U} \\ -\frac{1}{2L_U} & \frac{1}{2L_U} & \frac{1}{2L_U} & \frac{1}{2L_U} & -\frac{1}{2L_U} & -\frac{1}{2L_U} & \frac{1}{2L_U} & -\frac{1}{2L_U} \\ -\frac{1}{2L_U} & -\frac{1}{2L_U} & -\frac{1}{2L_U} & \frac{1}{2L_U} & \frac{1}{2L_U} & \frac{1}{2L_U} & \frac{1}{2L_U} & -\frac{1}{2L_U} \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \end{bmatrix} \tag{6a}$$

$$B_{22}=\begin{bmatrix} \frac{1}{2L_L} & \frac{1}{2L_L} & -\frac{1}{2L_L} & -\frac{1}{2L_L} & -\frac{1}{2L_L} & \frac{1}{2L_L} & \frac{1}{2L_L} & -\frac{1}{2L_L} \\ -\frac{1}{2L_L} & \frac{1}{2L_L} & \frac{1}{2L_L} & \frac{1}{2L_L} & -\frac{1}{2L_L} & -\frac{1}{2L_L} & \frac{1}{2L_L} & -\frac{1}{2L_L} \\ -\frac{1}{2L_L} & -\frac{1}{2L_L} & -\frac{1}{2L_L} & \frac{1}{2L_L} & \frac{1}{2L_L} & \frac{1}{2L_L} & \frac{1}{2L_L} & -\frac{1}{2L_L} \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \end{bmatrix} \tag{6b}$$

III. CONTROLLABILITY OF NINE SWITCH INVERTERS

The nine-switch inverter shows in Fig. 1 has many redundant operating modes due to numerous switching states (switch on or switch off) of the nine power semiconductors. Apparently, not all the operating modes are required to generate the desired output, it is decided by different control algorithms, for instance, the normal SPWM algorithm uses 12 operating modes to generate desired sinusoidal waveforms while 14 operating modes are normally adopted in the SVPWM technique, therefore, it is of great significance to study the problem of how many operating modes are required indeed to generate any desired output voltage, i.e. how many operating modes are required indeed to make the system be state controllable. In order to study this problem, we give the definition of m-modes controllable as follows.

Definition 3.1: A power converter is m-modes controllable, if and only if its controllable set or nested subspace is the full space, i.e., $w_n = R^n$, while only m operating modes are adopted in the switched linear system model.

If the nine-switch is *m-modes controllable*, it means that the inverter can generate any desired output voltage using only $m(m \leq 14)$ operating modes to modulate the inverter. It also means that the inverter will not be state controllable (can not generate specific desired output voltage or current) if only $p(p < m)$ operating modes are used in the modulation. Therefore, the key point of the problem is to find out which $m(p < m \leq 14)$ operating modes are necessary to make the switched linear system model be completely state controllable.

The m-modes controllability of the nine switch inverter can be investigated as following.

Given a coefficient matrix $A \in R^{n\times n}$ and a linear subspace $w \in R^{n\times n}$, denote

$$\langle A|w\rangle = \sum_{i=1}^{n} A^{i-1} w \tag{7}$$

where $\langle A|w\rangle$ is a minimum A-invariant subspace that contains coefficient matrix A.

In terms of the feature of minimum invariant subspace, the rank of controllability set of the nine-switch inverter can be described as $w_1 = \langle A_1|B_1\rangle + \langle A_2|B_2\rangle + \cdots + \langle A_{14}|B_{14}\rangle$, let $A = A_1 = A_2 = \cdots = A_{14}$, then we have

$$\begin{aligned} w_1 &= \langle A|B_1\rangle + \langle A|B_2\rangle + \cdots + \langle A|B_{14}\rangle \\ &= span\{B_1, \cdots, B_{14}, AB_1, \cdots, AB_{14}, A^2B_1, \cdots, \\ &\quad A^2B_{14}, \cdots A^nB_1, \cdots, A^nB_{14}\} \end{aligned} \tag{8}$$

Then, the nested subspace sequence is obtained as

$$w_2 = \langle A|w_1\rangle, \quad w_3 = \langle A|w_2\rangle \cdots, \ w_{14} = \langle A|w_{13}\rangle \tag{9}$$

Plug matrices (2), (3), (5), (6) in equations (7), (8) and (9), it is not difficult to notice that the rank of the matrix w_1 is $\dim(w_1) = 12$, consequently,

$$\dim(w_2) = \dim(w_3) \cdots = \dim(w_{13}) = 12 \tag{10}$$

which means $w_n = R^{12}$, i.e. the nested subspace is the full space. The nine-switch inverter has only twelve state variables, therefore, in terms of controllability criterion, the nine-switch inverter is completely state controllable Then, restudy the nested subspace sequences, it is noticed that

$$\begin{aligned} w_1 = span\{&B_2, B_4, B_6, B_7, B_9, B_{11}, AB_2, AB_4, AB_6, \\ &AB_7, AB_9, AB_{11}\} \end{aligned} \tag{11}$$

or

$$\begin{aligned} w_1 = span\{&B_1, B_3, B_5, B_8, B_{10}, B_{12}, AB_1, AB_3, AB_4, \\ &AB_8, AB_{10}, AB_{12}\} \end{aligned} \tag{12}$$

It shows in equation (11) and equation (12) that the linear independent vectors of the system are only related to operating modes ②, ④, ⑥, ⑦, ⑨ and ⑪; or related to operating modes ①, ③, ⑤, ⑧, ⑩, and ⑫. Obviously, only 6 operating modes are required to make the nested subspace be full space, i.e., the system is m-modes controllable where $m = 6$, namely, 6-modes controllable. It implies that the nine-switch inverter can generate any desired outputs using only 6 operating modes rather than 14 operating modes.

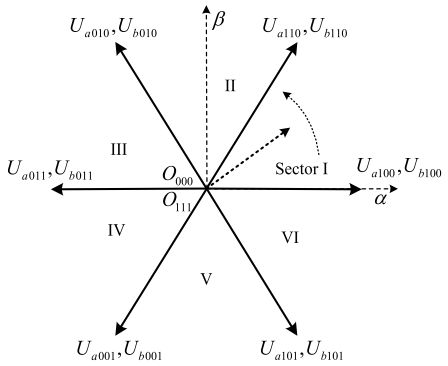


FIGURE 2. Operating modes and space vectors used in conventional SVPWM algorithm of a nine-switch inverter.

TABLE 2. Conventional switching sequence used in SVPWM algorithm.

sector	switching sequence	number of switching
sector I	⑭-①-②-⑬-②-①-⑭-⑦-⑧-⑬-⑧-⑦-⑭	12
sector II	⑭-③-②-⑬-②-③-⑭-⑨-⑧-⑬-⑧-⑨-⑭	12
sector III	⑭-③-④-⑬-④-③-⑭-⑨-⑩-⑬-⑩-⑨-⑭	12
sector IV	⑭-⑤-④-⑬-④-⑤-⑭-⑪-⑩-⑬-⑩-⑪-⑭	12
sector V	⑭-⑤-⑥-⑬-⑥-⑤-⑭-⑪-⑫-⑬-⑫-⑪-⑭	12
sector VI	⑭-①-⑥-⑬-⑥-①-⑭-⑦-⑫-⑬-⑫-⑦-⑭	12
Total		72

TABLE 3. Switching sequence with lower switching frequency.

Sector	Switching sequence	Number of switching
sector I	⑭-②-①-②-⑭-⑦-⑧-⑦-⑭	8
sector II	⑭-②-③-②-⑭-⑨-⑧-⑨-⑭	8
sector III	⑭-④-③-④-⑭-⑨-⑩-⑨-⑭	8
sector IV	⑭-④-⑤-④-⑭-⑪-⑩-⑪-⑭	8
sector V	⑭-⑥-⑤-⑥-⑭-⑪-⑫-⑪-⑭	8
sector VI	⑭-⑥-①-⑥-⑭-⑦-⑫-⑦-⑭	8
Total		48

IV. THE PROPOSED SVPWM

A. CONVENTIONAL SVPWM ALGORITHM

For the conventional SVPWM algorithm, the 14 operating modes used in the algorithm are shown in Fig. 2, therein, each arrow indicate two operating mode.

Table 2 shows the commonly used SVPWM strategy for the nine-switch inverter. Therein, the corresponding modes ①, ②, $\cdots$ ⑭ are described in Table 1.

It shows that the operating modes must change 12 times in every carrier wave period, it will result in high switching frequencies of the power semiconductors. Therefore, SVPWM strategy with reduced number of semiconductor switching was proposed, such as switching scheme presented in Table 3. It shows that the switching scheme uses fourteen operating modes and still changes 8 times in every carrier wave period.

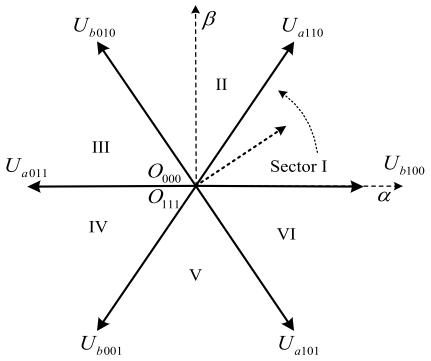


FIGURE 3. Diagrams of space vectors with corresponding operating modes ②, ④, ⑥, ⑦, ⑨, ⑪. (upper inverter U_{a110}, U_{a101}, U_{a011} lower inverter U_{b100}, U_{b010}, U_{b001}).

TABLE 4. Proposed switching sequence with operating modes ②, ④, ⑥, ⑦, ⑨, ⑪ (switching sequence in the odd cycle).

upper inverter	lower inverter	switching sequence	number of switching
sector I	sector IV	⑥-⑨-⑭-②-⑪	4
sector II	sector V	②-⑪-⑭-④-⑦	4
sector III	sector VI	②-⑪-⑭-④-⑦	4
sector IV	sector I	④-⑦-⑭-⑥-⑨	4
sector V	sector II	④-⑦-⑭-⑥-⑨	4
sector VI	sector III	⑥-⑨-⑭-②-⑪	4
Total			24

TABLE 5. Proposed switching sequence with operating modes ②, ④, ⑥, ⑦, ⑨, ⑪ (switching sequence in the even cycle).

upper inverter	lower inverter	Switching sequence	Number of switching
sector I	sector IV	⑪-②-⑭-⑨-⑥	4
sector II	sector V	⑦-④-⑭-⑪-②	4
sector III	sector VI	⑦-④-⑭-⑪-②	4
sector IV	sector I	⑨-⑥-⑭-⑫-④	4
sector V	sector II	⑨-⑥-⑭-⑫-④	4
sector VI	sector III	⑪-②-⑭-⑨-⑥	4
Total			24

B. THE NOVEL SVPWM ALGORITHM

In terms of the definition 3.1 equation (11) and equation (12) the switch linear system model of nine-switch inverter is completely state controllable with only 6 operating modes, namely operating modes ②, ④, ⑥, ⑦, ⑨ and ⑪, or operating modes ①, ③, ⑤, ⑧, ⑩ and ⑫. Therefore, new switching sequences, with only 6 operating modes, can be constructed to achieve a lower switching frequencies of the power semiconductors. As it is shown in Fig.3, a rotating vector is formed with 6 operating modes, namely, ②, ④, ⑥, ⑦, ⑨ and ⑪.

The novel SVPWM algorithm (switching sequences) are presented in Table 4, Table 5, therein, only 6 non-zero vectors are used. Apparently, a lower switching frequencies of the

TABLE 6. Proposed switching sequence with operating modes ①, ③, ⑤, ⑧, ⑩, ⑫ (switching sequence in the odd cycle).

upper inverter	lower inverter	Switching sequence	Number of switching
sector IV	sector I	⑫-③-⑭-⑧-⑤	4
sector V	sector II	⑧-⑤-⑭-⑩-①	4
sector VI	sector III	⑧-⑤-⑭-⑩-①	4
sector I	sector IV	⑩-①-⑭-⑫-③	4
sector II	sector V	⑩-①-⑭-⑫-③	4
sector III	sector VI	⑫-③-⑭-⑧-⑤	4
Total			24

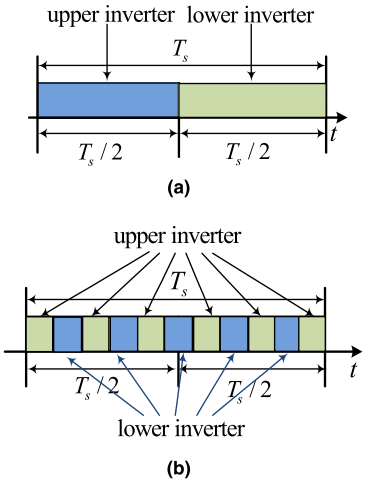


FIGURE 4. Alternative control of nine-switch inverter. (a) conventional control. (b) alternative control.

power semiconductors can be achieved since the operating modes only change four times in every carrier wave period.

In order to further reduce the switching frequencies of the power semiconductors, the switching sequences in odd carrier cycle and even carrier cycle are constructed respectively, i.e. the counter-clockwise switching sequences adopted in odd cycle and clockwise switching sequences adopted in even cycle respectively. For instance, consider the first row in Table 6 and Table 5, the switching sequence is set as ②-⑪-⑭-④-⑦ in the odd carrier cycle, meanwhile, a different switching sequence is constructed as ⑦-④-⑭-⑪-② in the even carrier cycle. Apparently, by using the counter-clockwise sequences and clockwise switching sequences, the number of power semiconductors switching will be reduced by half and two-thirds respectively compared with the switching sequences show in table 3 and Table 2.

In addition, alternative control effect was adopted by the novel SPWM strategy as shows in Fig.4. It shows in Fig.4 (a) that the operating modes of each inverter (upper inverter, lower inverter) will not work in half period. While in Fig.4 (b), the operating modes of upper inverter and lower inverter will work alternatively, this will fast the response time, also reduce the total harmonic distortion.

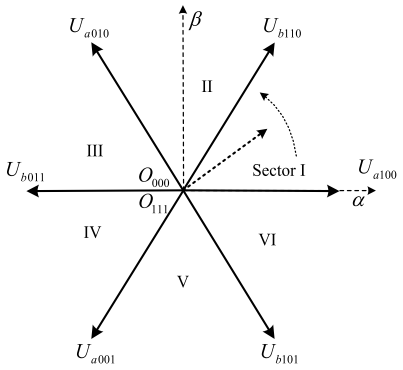


FIGURE 5. Space vector diagrams with operating modes ①, ③, ⑤, ⑧, ⑩, ⑫. (upper inverter U_{b110}, U_{b101}, U_{b011} lower inverter U_{a100}, U_{a010}, U_{a001}).

TABLE 7. Proposed switching sequence with operating modes ①, ③, ⑤, ⑧, ⑩, ⑫ (switching sequence in the even cycle)

upper inverter	lower inverter	Switching sequence	Number of switching
sector IV	sector I	⑤-⑧-⑭-③-⑫	4
sector V	sector II	①-⑩-⑭-⑤-⑧	4
sector VI	sector III	①-⑩-⑭-⑤-⑧	4
sector I	sector IV	③-⑫-⑭-⑥-⑩	4
sector II	sector V	③-⑫-⑭-⑥-⑩	4
sector III	sector VI	⑤-⑧-⑭-③-⑫	4
Total			24

TABLE 8. Circuit parameters of the nine-switch inverter.

R (Ω)	L (mH)	C (μF)	frequency(kHz) carrier wave	frequency upper (Hz)	frequency lower (Hz)
0.5	1.0	25.0	10.0	50.0	25.0

In terms of the aforementioned analysis results, the operating modes ①, ③, ⑤, ⑧, ⑩ and ⑫ also can be used to modulate the system. The corresponding space vectors of the operating modes shows in Fig.5.

The switching sequences are shown in Table 6 and Table 7, which clearly shows that the number of semiconductors switching is also reduced by two-thirds compared to normal SVPWM, hence, verified the feasibility of the proposed method for constructing the simplified switching sequence.

V. EXPERIMENTS

Experiments are conducted and the experiment results of the proposed SVPWM strategy using operating modes ②, ④, ⑥, ⑦, ⑨ and ⑪ are given in this section. The experimental set-up is depicted in Fig. 6.

Therein the control IC is TMS320F28335, driver IC is the HCPL 332J and the MOSFET model is SPW47N60S5, and the circuit parameters of the nine-switch inverter are shown in Table 8.

The line voltage and phase voltage for the upper inverter of the nine switch inverter are depicted in Fig. 7 and Fig. 8,

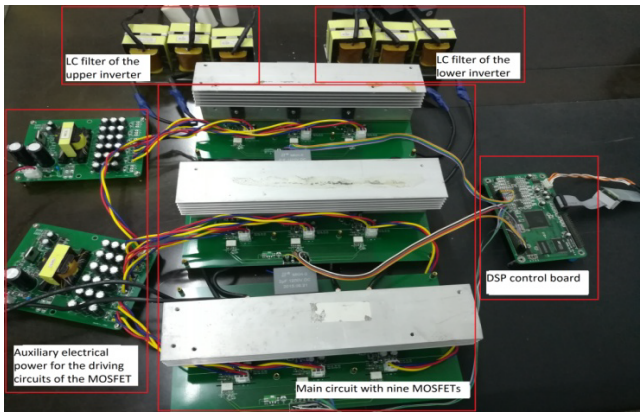


FIGURE 6. Experimental set-up.

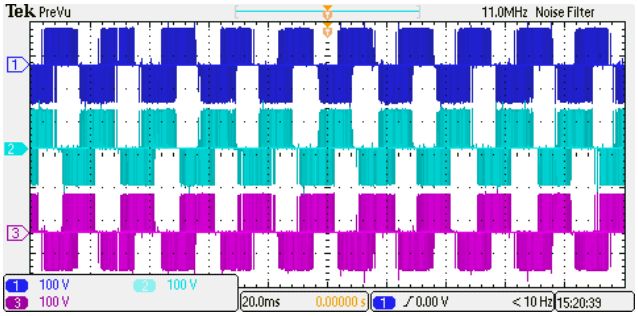


FIGURE 7. Output voltage of the dual output nine-switch inverter (line voltage, upper inverter, without LC filter).

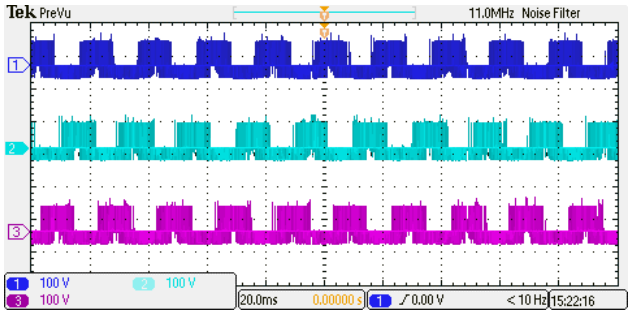


FIGURE 8. Output voltage of the dual output nine-switch inverter (phase voltage, upper inverter, without LC filter).

while Fig. 9 depicts the phase voltage for both upper inverter and lower inverter of the nine switch inverter with the LC filters.

For the designed 10kHz carrier frequency, the number of switching and switching frequencies of each power semiconductor for nine-switch inverter using different SVPWM strategies (Table 2, Table 3 and proposed modulation strategy shows in Table 4 $\sim$ Table 8) in a fundamental period ($T = 0.02$s) are calculated as shows in Table 9.

As is seen in Table 9, number of switching is considerably reduced using proposed SVPWMs (Table 4, Table 5 and Table 6, Table 7).

It is shown in Fig. 10 (b) that the efficiency of the system is improved, meanwhile, as shows in Fig. 10 (a), the total

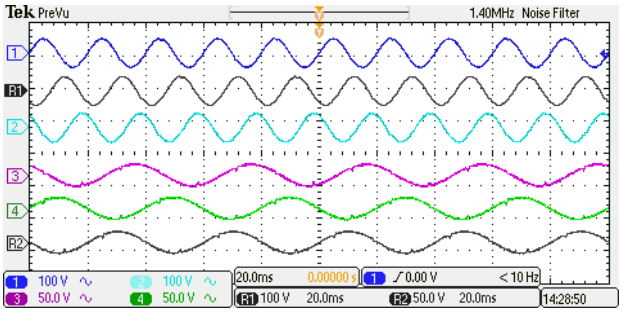
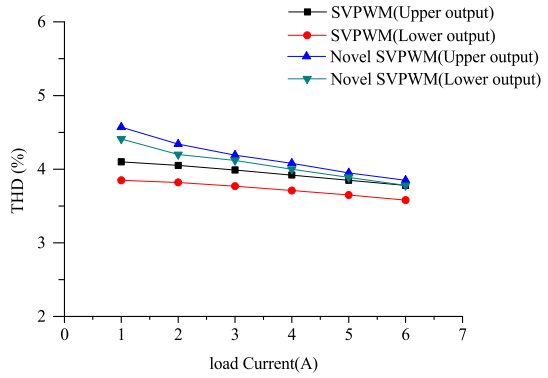


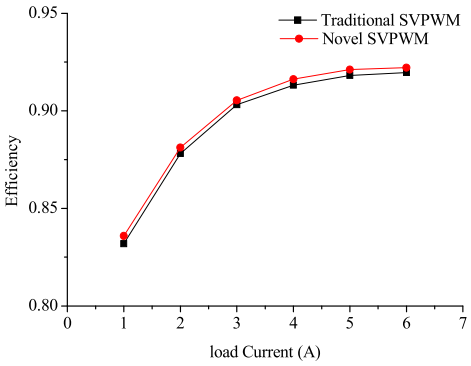
FIGURE 9. Output voltage of the dual output nine-switch inverter ((phase voltage, upper inverter 50Hz, lower inverter 25Hz).

TABLE 9. Number of semiconductor switching.

	SVPWM (Table II)	SVPWM (Table III)	Proposed SVPWMs
Number of switching	200	133	67
Switching frequencies	10kHz	6.67kHz	3.33kHz



(a)



(b)

FIGURE 10. THD and the efficiency of the conventional SVPWM and the proposed SVM. (a) Total harmonic distortion. (b) Efficiency.

harmonic distortion (THD) is increased due to the lower switching frequencies of the power semiconductors which is reduced by two-thirds compared to the normal SVPWM strategy. Generally, the experiment results proved that three-phase output voltage can be generated by the proposed

simplified pulse width modulation algorithm with only half number of the operating modes and one third of the switching frequencies of the power semiconductors (using the same carrier frequency for both conventional and proposed simplified SVPWM strategy). Apparent, experiment results correspond to the theoretical analysis, therefore verified the correctness of the m-modes controllability theory and feasibility of the proposed simplified pulse width modulation strategy.

VI. CONCLUSIONS

A novel concept, named *m-modes controllable*, has been proposed in this paper based on the switched linear system theory. As a consequence, the *m-modes controllable* of the dual output nine-switch inverter has been investigated. Theoretical analysis shows that only half number of the operating modes are required to keep the dual output nine-switch inverter being state controllable, namely, 6-modes controllable. Accordingly, a novel SVPWM strategy was designed with the specific six operating modes. It is proved by the theoretical analysis and experiments that, the switching frequencies of the power semiconductors is as low as 3.3kHz (with a carrier frequency of 10kHz) when the proposed simplified SVPWM algorithm was used, while the lowest switching frequencies is 6.67kHz for existing normal SVPWM algorithms. It is forwarded that the concept and design methodology proposed in this paper is also applicable to other power converters to construct novel modulation strategies with better performance.

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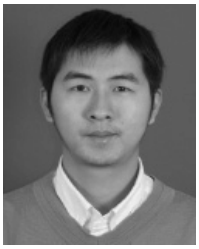

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