A Novel Fault Diagnostic Approach for DC-DC Converters Based on CSA-DBN

QUAN SUN[1], YOUREN WANG[1], AND YUANYUAN JIANG[1,2]

[1]College of Automation Engineering, Nanjing University of Aeronautics and Astronautics, Nanjing 211106, China
[2]College of Electrical and Information Engineering, Anhui University of Science and Technology, Huainan 232001, China

Corresponding author: Youren Wang (wangyrac@nuaa.edu.cn)

ABSTRACT Effective fault diagnosis for mission-critical and safety-critical systems has been an essential and mandatory technique to reduce failure rate and prevent unscheduled shutdown. In this paper, to realize fault diagnosis for a closed-loop single-ended primary inductance converter, a novel optimization deep belief network (DBN) is presented. First, wavelet packet decomposition is adopted to extract the energy values from the voltage signals of four circuit nodes, as the fault feature vectors. Then, a four-layer DBN architecture including input and output layers is developed. Meanwhile, the number of neurons in the two hidden layers is selected by the crow search algorithm (CSA) with training samples. Not only the hard faults such as open-circuit faults and short-circuit faults but also the soft faults such as the component degradation of power MOSFET, inductor, diode, and capacitor are considered in this study. Finally, these fault modes are isolated by CSA-DBN. Compared with the back-propagation neural network and support vector machine fault diagnosis methods, both simulation and experimental results show that the proposed method has a higher classification accuracy that proves its effectiveness and superiority to the other methods.

INDEX TERMS Crow search algorithm, dc-dc power converter, deep belief network, fault diagnosis, feature extraction, wavelet packets.

I. INTRODUCTION

DC-DC converters have been witnessing remarkable progress in various fields such as aerospace, photovoltaic/wind power generation, smart grid and electric vehicles [1], [2]. With the increase in switching frequency and power level of the power electronic converters (PECs), power electronic systems such as DC-DC converters are becoming more complex and prone to performance degradation. Critical failures can occur when they are exposed to harsh operating and environmental conditions such as high temperature, over current, over voltage, mechanical vibration, electromagnetic stress and radiation. Additionally, redundancy strategies are sometimes not applicable or cost effective on faulty PECs due to the constraints on their volume and fault tolerance. Therefore, effective fault diagnosis techniques have emerged as an essential advanced technology to prevent DC-DC converters from malfunctioning in many mission-critical and safety-critical systems, which can improve the reliability and availability of the system and reduce the downtime and maintenance cost [3].

In general, fault modes in power electronic circuits are mainly classified into two categories: namely, structural faults (hard faults) and parametric faults (soft faults). Two types of hard faults are generally observed: short circuit fault (SCF) and open circuit fault (OCF). A hard fault could cause a distinct and catastrophic effect such as a sudden voltage drop or current rise in the power electronic system, while a soft fault such as parameter drift may cause a gradual decrease in system performance as a result of components wearing out or aging [4]. However, research shows that a soft fault not be fixed in time could evolve into a hard fault. In other words, more attention should be paid to both hard and soft faults of PECs, as they have become an issue in research regarding prognostics and health management (PHM). According to a questionnaire on the reliability of power electronics based on over 200 products from 80 companies, the power

semiconductor devices and capacitors are the two major components that are responsible for more than 50% of the breakdowns in PECs [5], [6], as shown in Fig. 1.
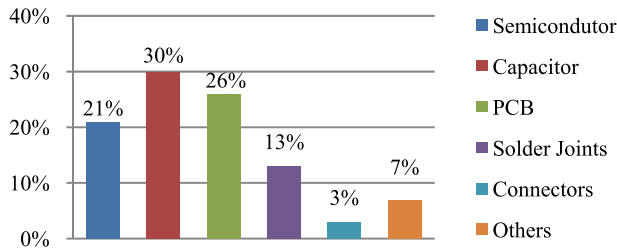
FIGURE 1. Failure distribution and ranking of power electronic converters.

Harada *et al.* [7] perceived that the equivalent series resistance (ESR) of the electrolytic capacitor increases as the capacitor deteriorates, and the ESR can be estimated utilizing the knowledge that ripple varies proportionally to the increase in ESR for the forward-type converters and Buck-Boost converters. Amaral and Cardoso [8] proposed an on-line fault detection strategy for electrolytic capacitors based on the relationship between input current and output voltage ripple. Yao *et al.* [9] deduced the ESR and capacitance computational formulas from analyzing the capacitor voltage ripple and designed a measurement system based on DSP without additional current sensor. This method has an advantage that only two voltage values of the output capacitor at different moments need to be sampled within a switching cycle, and the ESR and capacitance variation can be monitored at different working conditions. Sun *et al.* [10] presented a parameter estimation method based on particle swarm optimization algorithm to complete multi-component (including inductor, capacitor and power MOSFET) soft fault diagnosis. Wang *et al.* [11] proposed an OCF diagnosis method for power MOSFETs of brushless DC motor (BLDCM) by detecting line voltage differences during the PWM_ON and PWM_OFF time. An accelerated test system under power cycling was developed to trigger the failure mechanism in regards to die-attach damage, due to mismatch on the coefficient of thermal expansion of the different elements in the component's packaged structure. The variation of the drain-to-source on-resistance was identified as the failure precursor of the power MOSFET, which was dependent on junction temperature [12], [13]. A hybrid method based on two sub-systems was proposed in [14] to diagnose both the OCF and SCF for non-isolated DC-DC converters.

Most of these diagnostic techniques can be classified as model-based [11], [14] and data-driven approaches [15], [16]. The model-based approaches have to take into account the physical processes and interactions between components in the system; however, accurate mathematical representations in some occasions could be difficult to obtain. Data-driven approaches could be used to directly analyze the measured signals and obtain fault features, thereby implementing fault detection and classification using intelligent algorithms. Currently, intelligent pattern recognition algorithms can provide

effective fault detection and diagnosis capability. Neural networks are commonly used to solve classification or regression problems, which can be applied to power electronics fault detection and diagnosis as well [15]. Dhumale and Lokhande [16] proposed an ANN fault diagnostic strategy combined with Park's vector transform and discrete wavelet transform (DWT) to identify both single and multiple open switch faults when the voltage source inverters operate under variable load conditions. However, these intelligent methods such as the back propagation neural network (BPNN) and the support vector machine (SVM) are named as shallow learning networks, which cannot complete the sophisticated functions representing. Thus, when the fault features are complicated and have higher dimensions, the BPNN and SVM may have weak ability to classify these fault modes.

Fortunately, the concept of deep belief network (DBN) put forward by Hinton *et al.* [17] in 2006 was a new area of machine learning research, which overcame the limitations of shallow network methods. Due to multi-layer structure of the DBN, it can provide more extensive modeling capacity to form a specific feature vector which is more suitable for classification. DBN has already been applied successfully in many fields, such as information retrieval [18], nature language processing [19] and data classification [20]. However, the DBN model is vulnerable to the change in the number of network layers and the size of hidden units, and the performance is not stable. Coates *et al.* [21] conducted extensive experiments to demonstrate that the number of hidden nodes in the model may be more important than the factors of learning algorithm or the depth of the model. Therefore, in this paper, we propose a novel fault diagnostic method for the single-ended primary-inductor converter (SEPIC) based on the crow search algorithm and deep belief network (CSA-DBN). The CSA is used to optimize the number of hidden nodes in DBN, which is proposed by Askarzadeh [22] in 2016 and presents better performance, avoiding critical flaws such as the premature convergence to sub-optimal solutions and the limited exploration exploitation balance in the search strategy. Both the hard faults and soft faults diagnosis for the power converter are analyzed and conducted. Simulation and experiment results show that the proposed method provides higher accuracy in comparison with the BPNN and SVM methods.

II. FAULT DIAGNOSIS BASED ON DEEP BELIEF NETWORK
A. DEEP BELIEF NETWORK (DBN)
The deep belief network (DBN) is a probabilistic generative model that consists of multiple stacked Restricted Boltzmann Machines (RBMs). That means RBMs are the fundamental blocks of DBN. An individual RBM contains a layer of visible neurons and a layer of hidden neurons. The neurons within each layer are connected only between the visible layer and the hidden layer; in other words, there are no visible-visible or hidden-hidden connections in the same layer. The schematic architecture of an RBM with n visible units
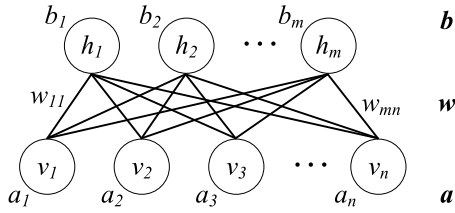
FIGURE 2. An RBM with n visible neurons and m hidden neuron.

$\mathbf{v} = (v_1, v_2, \ldots, v_n)$ and m hidden units $\mathbf{h} = (h_1, h_2, \ldots, h_m)$ is shown in Fig. 2, where $\mathbf{v}$ and $\mathbf{h}$ both take binary stochastic values $\mathbf{v} \in \{0, 1\}^n$, $\mathbf{h} \in \{0, 1\}^m$.

For the RBM model, the energy function of the joint configuration $(\mathbf{v}, \mathbf{h})$ is given by:

$$E(\mathbf{v}, \mathbf{h}) = -\mathbf{a}^T \mathbf{v} - \mathbf{b}^T \mathbf{h} - \mathbf{v}^T \mathbf{w} \mathbf{h}$$
$$= -\sum_{i=1}^{n} a_i v_i - \sum_{j=1}^{m} b_j h_j - \sum_{i=1}^{n} \sum_{j=1}^{m} v_i w_{ij} h_j \quad (1)$$

where v_i and h_j represent the states of the ith neuron in the visible layer and j^{th} neuron in the hidden layer, respectively; a_i and b_j represent the bias of v_i and h_j, respectively; w_{ij} is the symmetric interaction term of the connection weight between v_i and h_j. The probability distribution of every possible pair of a visible and a hidden vector can be obtained through the energy function:

$$p(\mathbf{v}, \mathbf{h}) = \frac{1}{Z} \exp(-E(\mathbf{v}, \mathbf{h})) \quad (2)$$

where Z is a normalization constant or partition function, as expressed in (3), which can be calculated by summing over all possible pairs of visible and hidden vectors.

$$Z = \sum_{\mathbf{v}} \sum_{\mathbf{h}} \exp(-E(\mathbf{v}, \mathbf{h})) \quad (3)$$

Additionally, the margin distribution that RBM assigns to a visible vector of the network is given by the following equation:

$$p(\mathbf{v}) = \sum_{h} p(\mathbf{v}, \mathbf{h}) = \frac{1}{Z} \sum_{h} \exp(-E(\mathbf{v}, \mathbf{h})) \quad (4)$$

Because there are no connections in the same layer, the conditional probability distribution of visible neurons $\mathbf{v}$ and hidden neurons $\mathbf{h}$ can be expressed as:

$$p(h_j = 1|\mathbf{v}) = \sigma\left(b_j + \sum_{i=1}^{n} w_{ij} v_i\right) \quad (5)$$

$$p(v_i = 1|\mathbf{h}) = \sigma\left(a_i + \sum_{j=1}^{m} w_{ij} h_j\right) \quad (6)$$

where $\sigma(x)$ is the logistic sigmoid function.

$$\sigma(x) = \frac{1}{1 + e^{-x}} \quad (7)$$

It is noteworthy that the probability of a training vector can be increased by adjusting the weights and biases to lower

the energy of that vector, whereas the probability can be decreased by adjusting them to increase the energy. Therefore, the model parameters of the RBM can be estimated with stochastic maximum log-likelihood. The derivative of the log-likelihood with respect to the model parameters w_{ij}, v_i and h_j can be derived from (4) and given as follows:

$$\frac{\partial \log p(\mathbf{v})}{\partial w_{ij}} = p(h_j = 1|\mathbf{v})v_i - \sum_{v} p(\mathbf{v})p(h_j = 1|\mathbf{v})v_i$$
$$= \langle v_i h_j \rangle_{data} - \langle v_i h_j \rangle_{model} \quad (8)$$

$$\frac{\partial \log p(\mathbf{v})}{\partial a_i} = v_i - \sum_{\mathbf{v}} p(\mathbf{v})v_i = \langle v_i \rangle_{data} - \langle v_i \rangle_{model} \quad (9)$$

$$\frac{\partial \log p(\mathbf{v})}{\partial b_j} = p(h_j = 1|\mathbf{v}) - \sum_{\mathbf{v}} p(\mathbf{v})p(h_j = 1|\mathbf{v})$$
$$= \langle h_j \rangle_{data} - \langle h_j \rangle_{model} \quad (10)$$

Here, $\langle \cdot \rangle_{\text{data}}$ and $\langle \cdot \rangle_{\text{model}}$ denote the expectation with respect to the data distribution and the model, respectively. However, the expectation under the model distribution is intractable to be calculated due to the partition function Z. To address this concern, a training method called contrastive divergence (CD) was proposed by Hinton *et al.* [17]. For RBM training, the CD learning with one-step (CD-1) of Gibbs sampling has been shown to work extremely well. First, the training data are given to the visible units v_i, and the hidden states h_j are obtained by (5). Then the obtained hidden states are used to produce the reconstruction of visible states using (6). Thus, based on (8-10), the update rule of the model parameters are presented as follows:

$$\Delta w_{ij} = \alpha(\langle v_i h_j \rangle_{data} - \langle v_i h_j \rangle_{recon}) \quad (11)$$
$$\Delta a_i = \alpha(\langle v_i \rangle_{data} - \langle v_i \rangle_{recon}) \quad (12)$$
$$\Delta b_j = \alpha(\langle h_j \rangle_{data} - \langle h_j \rangle_{recon}) \quad (13)$$

where $\alpha \in (0, 1)$ is a learning rate and refers to the expectation over the reconstructed data.
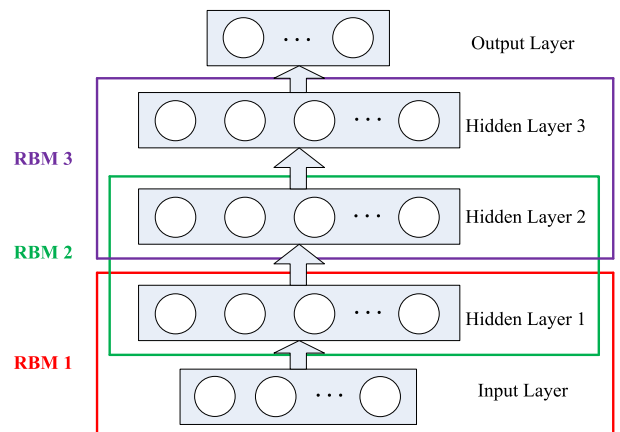

FIGURE 3. Multilayered architecture for the deep belief network.

As mentioned above, the DBN is constructed by several RBMs. For example, Fig. 3 shows that three RBMs are

stacked to construct a DBN. The first and second layers (input layer and hidden layer 1) are the visible and hidden layers of RBM 1, respectively. It is important to note that the first layer is often considered to be a data input layer of the DBN. The second layer (hidden layer 1) and the third layer (hidden layer 2) form the visible and hidden layers of RBM 2, separately. Also, the third and fourth layers (hidden layer 2 and 3) form the visible and hidden layers of RBM 3.

The overall learning process of the DBN classifier model mainly contains two steps. In step (1), each successive layer is trained in an unsupervised greedy layer-wise fashion as the RBMs learn by the CD-1 algorithm, which means the DBN learning process is performed by the successive learning of each individual RBM. When the training of the first RBM (RBM 1) is complete, the process continues for RBM 2 and RBM 3. In step (2), which is performed after layer-by-layer pre-training of the DBN, all the parameters (weights and biases) of the pre-trained model can be fine-tuned by a supervised back-propagation algorithm. The parameters of the DBN model are updated in order to obtain an optimal classifier and improve the accuracy.

B. OPTIMIZATION OF THE DBN USING THE CROW SEARCH ALGORITHM (CSA)

Although the DBN has been successfully applied in fields such as speech recognition, image processing and classification, the performance of the DBN model is greatly related to its architecture. Coates *et al.* [21] noted that the number of hidden neurons in the DBN model may be more important than the other factors of the learning algorithm or the depth of the model. Additionally, few literatures could provide an effective strategy on how to choose the number of hidden layers. Therefore, in this paper, a DBN with two hidden layers is developed for the fault diagnosis of power converters.

The crow search algorithm (CSA) is a recently proposed evolutionary computation technique based on the behavior in flocks of crows [22]. Compared with other evolutionary algorithms, CSA presents superior performance in that it has a greater global searching capability and faster convergence in the search strategy. Crows are considered to be one of the most intelligent animals in the world; thus, their behavior can provide interesting heuristics. One of the intelligent behaviors of the crows is that they can hide their excess food in specific hiding places and recall the hiding location when necessary. On the other hand, crows can be greedy in that they follow other crows to their hiding places and steal their food once the owner leaves. As a result, crows would take extra precautions in order to prevent their food from being pilfered. The CSA tries to mimic this intelligent behavior to provide an efficient methodology to solve optimization problems. Therefore, CSA is adopted in this work to determine the optimal number of hidden layers in the DBN.

It is assumed that in a flock of N crows in the CSA, the position of crow i at iteration k is given by x_i^k. The hiding place for the food is memorized by crow i. The crow moves in the search place and tries to find the best food source,

which is defined as m_i^k. There are two probable scenarios in the searching approach of the CSA. The first one is that the owner crow j of the food source does not know that it has been followed by thief crow i; therefore, the thief crow reaches the hiding place of the owner crow. The updating process of the crow thief's position is given by:

$$x_i^{k+1} = x_i^k + r_i \times fl_i^k \times (m_j^k - x_i^k) \qquad (14)$$

where r_i is a random number between 0 and 1, fl is a parameter that controls the flight length.

The other probable scenario is that the owner crow j knows that it is followed by the thief crow i; thus, the owner crow will deceive crow i by going to another position within the search space. The position of crow i is updated by a random position. These two cases in the CSA can be summarized by the following expression:

$$x_i^{k+1} = \begin{cases} x_i^k + r_i \times fl_i^k \times (m_j^k - x_i^k), & r_j \geq \text{AP} \\ \text{a random position}, & \text{otherwise} \end{cases} \qquad (15)$$

where the parameter AP is named as the awareness probability in range [0, 1]. Unlike other search algorithms, there are two specific parameters in CSA: flight length (*fl*) and awareness probability (AP). The parameter *fl* determines the step size of the movement towards the hiding place of interest. When *fl* is between 0 and 1, the new position of a crow will be between its current position and the position of the hiding place of interest. If the value of *fl* is larger 1, the crow can visit beyond the hiding place of interest. The parameter AP provides a balance between diversification and intensification. Small values of AP increase intensification and large values increase diversification.

The required steps of CSA are presented in the flow chart in Fig. 4. The first step is the initialization of the CSA, including *fl*, AP, flock size and stopping criteria. The next step is to randomly initialize the crow positions and evaluate them by computing the fitness function. The positions are uniformly distributed in the search space. After that, the new positions are generated according to (15). All the new positions are evaluated in the objective function, and the memory is updated. Finally, the stopping criteria are verified in order to terminate or continue with the iterative process.

An overview of the fault diagnostic method for the SEPIC converter is schematically represented in Fig. 5, and the general procedure for SEPIC fault diagnosis using the CSA-DBN is illustrated as follows:

Step 1: Define the normal operating condition and fault modes (including hard faults and soft faults) of the SEPIC circuit;

Step 2: Collect voltage signals and extract the fault feature vector for hard and soft faults based on wavelet packet energy (WPE) of the entire samples;

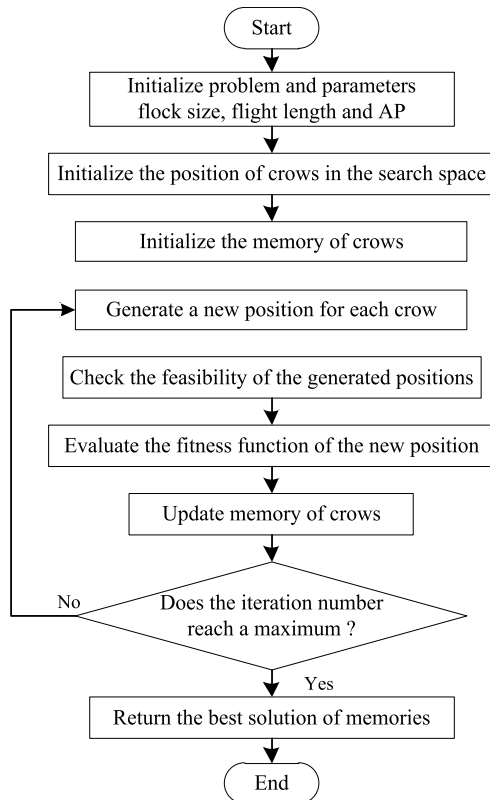Step 3: Divide the fault samples into training samples and testing samples, and initial the architecture of the DBN;

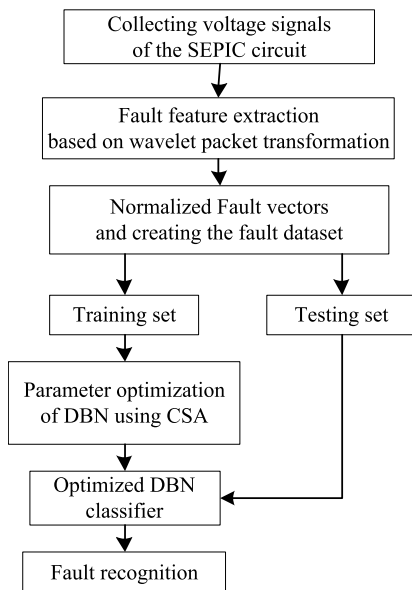**FIGURE 4.** The flow chart of the CSA algorithm.

FIGURE 5. Framework of the proposed fault diagnostic approach based on CSA-DBN.

Step 4: Use the CSA to optimize the DBN classifier, and determine the neurons number in the first and second hidden layers on the training samples;

Step 5: Classify the testing samples of hard and soft fault modes using the CSA-DBN;

Step 6: Calculate the classification accuracy and give the fault diagnosis results;

It is worth noting that the fault diagnostic rate is generally viewed as the optimization objective; however, in this paper, the misclassification error is defined as the fitness function in the CSA-DBN, which turns this issue to solving a minimum optimization problem.

III. FAILURE ANALYSIS AND FEATURE EXTRACTION OF THE SEPIC

The single-ended primary-inductor converter (SEPIC) is a kind of DC-DC converter that enables a DC voltage to be efficiently converted to either a lower or higher voltage. SEPIC converters are especially useful for PV maximum power tracking purposes, in which the objective is to draw the maximum possible power from solar panels at all times, regardless of the load. In this paper, a closed-loop SEPIC is considered using the controller UC3843, as shown in Fig. 6, which converts an input voltage of 28V DC to an output voltage of 12V DC with a switching frequency of 20 kHz. Additionally, the circuit parameters of the SEPIC converter under the normal condition are shown in Table 1. It is worthwhile to note that the symbols VD and VT represent the diode and the power MOSFET in Fig. 6, respectively.
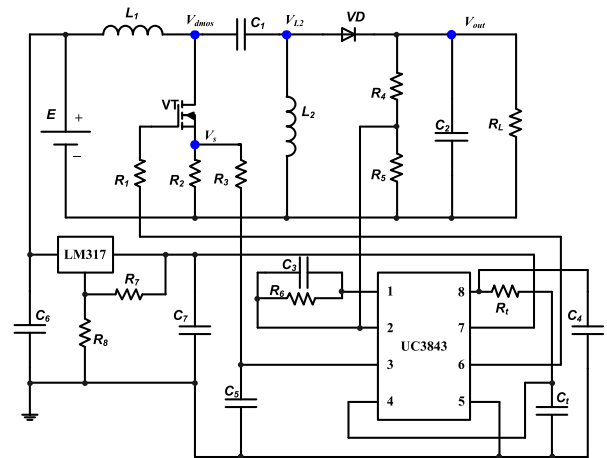

FIGURE 6. Schematic diagram of the closed-loop SEPIC converter.

A. FAILURE ANALYSIS AND EQUIVALENT MODEL OF KEY COMPONENTS

In practical industrial applications, environmental stress and operating stress such as high temperature, mechanical vibration, over voltage or switching impulse during regular operations may cause components aging which could affect power converters characteristics like output voltage ripple, switching loss, conduction loss, etc. Therefore, analysis of these electronic components failure is an essential part for the PECs fault diagnosis. In this section, the potential failure mode and failure mechanism of common electronic devices are briefly illustrated in Table 2. Similarly, the most vulnerable components such as electrolytic capacitor, schottky barrier

TABLE 1. The parameters of the SEPIC under the normal condition.

Symbol	Description	Value
E	Input voltage	28V
f	Switching frequency	20kHz
L_1	Inductance of inductor 1	470μH
L_2	Inductance of inductor 2	470μH
R_{dson}	On-resistance of power MOSFET (VT)	80mΩ
R_D	On-resistance of diode (VD)	50mΩ
C_1	Capacitance of capacitor 1	470μF
ESR_1	ESR of capacitor 1	80mΩ
C_2	Capacitance of capacitor 2	2200μF
ESR_2	ESR of capacitor 2	300mΩ
R_L	Load resistance	15Ω
V_{out}	Output voltage	12V

TABLE 2. Potential Failure mode and failure mechanism of electronic devices in power converters.

Element	Failure Mode	Failure mechanism
Resistor	Open Circuit	Leads fracture
Capacitor	Electrical parameter drift (ESR increase, C decrease)	Aging of Electrolyte Electrolyte vaporization
	Short Circuit	Dielectric Breakdown
	Open circuit	Terminals disconnected
Inductor	Open circuit	Coil wire crack
	Drop in Inductance	Insulation damaged
Schottky Barrier Diode	Parameter drift	Defects in material
	Short circuit	Contact Migration
	Open circuit	Excessive current thermal fatigue
	change of on-state resistance	Die attach fatigue wire-bond lift off
Power MOSFET	Gate Oxide Short	Time Dependent Dielectric breakdown
	Gate Oxide Breakdown	Electrical overstress Electronic Static Discharge
	Change of Leakage Current	Hot Carrier

diode and power MOSFET, are described in this subsections. Additionally, the equivalent models of these key components are also established.

1) ELECTROLYTIC CAPACITOR
Electrolytic capacitors have become one of the most critical components in power converters and have been widely used for filtering, coupling, bypass and many other applications. Unfortunately, they are also responsible for a large amount of breakdowns in power electronics systems [1]. It is known that the common failure modes are open circuit, short circuit, capacitance (C) decreases and equivalent series resistance (ESR) increases [7]–[10]. The former two types are hard faults while the last two are soft faults.

During the operation time, when electrolytic capacitors are submitted to current spikes and voltage surges, fault modes like dielectric breakdown and leads crack are very likely to occur, which eventually leads to OCF and SCF. The main aging mechanism of degradation failure is electrolyte vaporization which influenced by temperature, ripple current, over-voltage, etc. Meanwhile, the reduction of the electrolyte enables the electrolyte resistivity to increase and the contact area between the electrolyte and dielectric to reduce. This causes a decrease in capacitance and an increase of the ESR. Thus, ESR and C are often used as fault characteristic parameters (FCP) for the electrolytic capacitor. It's suggested that the lifetime of an electrolytic capacitor has ended when its ESR value increases by 280-300% of its initial value or the capacitance C decreases by 20% below its pristine condition value at room temperature [8], [9]. The simplified equivalent circuit of an electrolytic capacitor consists of an ideal resistance in series with an ideal capacitor.

2) SCHOTTKY BARRIER DIODE
Compared to pn diodes, schottky barrier diodes (SBD) are built using a metal-semiconductor contact with a lower forward voltage drop and a much shorter switching time, therefore, they are commonly used in switching power supplies, voltage clamping, reverse current and discharge protection applications. However, they may be exposed to excessive current, thermal fatigue, these external forces may result in OCF and SCF [23]. On the other hand, many research proved that the performance degradation of diode mainly reflects in the increase of both reverse leakage current IR and the series on-resistance R_D. Consequently, the equivalent model of SBD is represented by series combination of an ideal switch and an on-resistance R_D which is used as the FCP of SBD.

3) POWER MOSFET
Power MOSFET is a power semiconductor switch used for the conversion of electrical energy. In the reality, the devices are often subjected to thermal stress and electrical overstress which may cause them to deteriorate. The failure mechanisms for a MOSFET can be divided into two groups: chip-related failures and packaging-related failures. The reasons for chip-related failures are electrical overstress (EOS), electrostatic discharge (ESD), latch-up, etc. The packaging-related failures are mainly related to the dissimilarity between the coefficients of thermal expansion (CTE) of chip and the package which lead to the contact migration, wire lift-off, die solder degradation. Therefore, the structure of a power MOSFET can be characterized as a series of an ideal switch and the drain to source on-resistance R_{dson} in the field of fault diagnosis [12], [13].

B. FAULT MODES OF THE SEPIC
Generally, the power converter circuit consists of the main circuit (in the upper portion of Fig. 6) and the control circuit (in the lower part of Fig. 6). Because the main circuit operates

at a high switching frequency and high voltage, the performance degradation of the components in the main circuit is faster than those in the control circuit. In other words, the main circuit is more likely to suffer a failure. Therefore, several faults (including hard faults and soft faults) occur in the main circuit of the SEPIC and are considered in this study.

TABLE 3. The fault modes of hard faults for the SEPIC converter.

Fault code	Fault mode	Fault code	Fault mode
HF1	Normal	HF7	C_2 SCF
HF2	VT OCF	HF8	L_1 OCF
HF3	VD OCF	HF9	L_2 OCF
HF4	VD SCF	HF10	R_2 OCF
HF5	C_1 OCF	HF11	R_2 SCF
HF6	C_2 OCF		

1) HARD FAULT MODES OF THE SEPIC

The two main hard fault types in power converter systems are open-circuit (OC) and short-circuit (SC) faults. Many efforts have been made to diagnose the OC and SC faults of power semiconductor switching devices in PECs. Common causes of OC switch faults include wire bond lift-off and the cracking of solder layers. Nevertheless, other component faults such as inductor, capacitor and diode faults may also affect the performance of power converters. Diode failure may cause current waveform distortion because current can flow in both directions in the circuit branch when a diode SC fault occurs; current will stop flowing if an OC fault occurs. When the inductor operates under high temperature conditions, the coil wire and/or the insulation will be damaged, which may lead to an OC fault. Electrolytic capacitor failures are mainly caused by dry soldering and terminals disconnected during the manufacturing process, which can eventually lead to an OC fault. Dielectric breakdown under temperature cycling, ripple current and over-voltage can lead to an SC fault. An OC fault in the filter capacitor of power converters could increase current harmonics in addition to normal ripple across the capacitor terminals. As shown in Table 3, eleven kinds of hard fault modes are considered in our work, including the normal condition HF1.

2) SOFT FAULT MODES OF THE SEPIC

The performance of the SEPIC converter will gradually decrease as a result of components wearing out or aging like parameter drift. When the capacitors suffer degradation, both the value of capacitance and ESR will change simultaneously, following the relationship between the two parameters. Ten kinds of soft fault modes in the SEPIC circuit are considered in this work, including the capacitors C_1 and C_2, the power MOSFET and SBD, as shown in Table 4. It should be noted that, take soft fault of power MOSFET as example, when the R_{dson} is increased by 20~50%, it means that $1.2R_{dson0} \leq R_{dson} < 1.5R_{dson0}$, where R_{dson0} represents the initial value of on-resistance of power MOSFET. Parameter

TABLE 4. The fault modes of soft faults for the SEPIC converter.

Fault code	Fault mode
SF1	Normal
SF2	C_1 decreased by 20%~50% and ESR_1 increased by 25~100%, respectively
SF3	C_1 decreased by 50%~80% and ESR_1 increased by 100~300%, respectively
SF4	C_2 decreased by 20%~50% and ESR_2 increased by 25~100%, respectively
SF5	C_2 decreased by 50%~80% and ESR_2 increased by 100~300%, respectively
SF6	R_{dson} increased by 20~50%
SF7	R_{dson} increased by 50~80%
SF8	L_1 decreased by 20-50%
SF9	L_2 decreased by 20-50%
SF10	R_D increased by 30-60%

changing descriptions of other fault modes are in the same way as above mentioned.

C. FAULT FEATURE EXTRACTION OF THE SEPIC

To conduct fault detection and classification, four node voltage signals (V_{dmos}, V_s, V_{L2}, V_{out} as shown in Fig. 6) in steady-state conditions are chosen for analysis and used for feature extraction. In this study, fault features are obtained by wavelet packet transform and statistical analysis.

The wavelet packet transform (WPT) is a generalization of discrete wavelet transform (DWT) and hence of multi-resolution analysis [24]. It can decompose a signal into several levels of wavelet packet (WP) nodes forming a WP tree structure, in which each level represents one frequency resolution. The wavelet packet function can be defined as follows:

$$W_{j,k}^n(t) = 2^{j/2} W^n(2^j t - k) \tag{16}$$

where j is the scaling parameter and k is the translation parameter. The symbol n represents an oscillation parameter. The wavelet packet coefficients at each node (j, n) can be calculated using the inner product between signal $f(t)$ and each wavelet packet function as shown in the following equation:

$$C_j^n(k) = \langle f(t), W_{j,k}^n(t) \rangle \tag{17}$$

Each node of the WP tree is indexed with the pair of integers (j, n) with $n = 0, 1, \cdots, 2^j - 1$. A vector of WP coefficients C_j^n corresponds to each node (j, n). Thus, the energy E_j^n of a packet W_j^n is given by:

$$E_j^n = \sum_k [C_j^n(k)]^2 \tag{18}$$

To normalize the energy of a packet W_j^n, the energy E_n is divided by the total energy of the signal as shown in (19):

$$NE_j^n = \frac{E_j^n}{E_{total}} = \frac{E_j^n}{\sum_{n=1}^{2^j} E_j^n} \times 100\% \tag{19}$$

Therefore, all the relative energies of each frequency band in level j are acquired to construct the vector as shown in the following expression:

$$T = [NE_j^1, NE_j^2, \cdots, NE_j^n] \tag{20}$$

IV. CSA-DBN BASED FAULT DIAGNOSIS FOR SEPIC

To verify the effectiveness of the proposed fault diagnostic approach for the SEPIC, both simulation and experiment tests are developed. All the proposed methods are implemented with MATLAB R2016a and executed on a computer with an Intel Core i7-6700 CPU @ 3.40 GHz/16 GB RAM.

TABLE 5. The cases of training dataset and testing dataset.

| Case	Training dataset (%)	Testing dataset (%)
Case 1	80	20
Case 2	60	40
Case 3	50	50

A. SIMULATION RESULTS AND ANALYSIS

The simulation circuits of the SEPIC are modeled by the software Synopsys/Saber 2012. Due to manufacturing variability, the pristine parameter of each component varies from device to device. Therefore, the simulation of the SEPIC circuit is conducted by the Monte Carlo analysis method with tolerances of the components set as 5%. Each fault type as shown in the Table 3 and 4 has 100 samples. Moreover, the value changed in the range of the degradation components (as shown in Table 4) is uniformly distributed. In this work, each node voltage signal is decomposed into a three-layer wavelet coefficient to get the wavelet packet energy spectrum. A fault feature vector is constructed by the wavelet packet energy spectrum of the four node voltage (V_{dmos}, V_{L2}, V_s and V_{out}). Therefore, the dimension of each fault feature vector is 32. Additionally, in order to analyze the performance of the CSA-DBN, the samples are divided into three cases, as shown in Table 5.

The other two common methods based on BPNN and support vector machine (SVM) are also discussed for comparison. For the BPNN classifier, we employ a type of three-layer architecture: one input layer, one hidden layer and one output layer. The sigmoid transfer function is used and the number of units in the hidden layer is determined by several trials, which is in the range of 10 through 30. It is found that the classification results based on BPNN perform better when the number of units in the hidden layer is 18. Similarly, in SVM training, RBF kernel function is applied to train the SVM model and the two main model parameters, namely, the penalty factor and the radius of the kernel function, are 0.35 and 0.70, respectively. For the hard fault diagnosis, the input layer and the output layer of the DBN are constructed with 32 and 11 neurons, respectively, in terms of the dimensions of fault feature vectors and fault modes. For the soft fault diagnosis, the output layer is consisted of 10 neurons. The
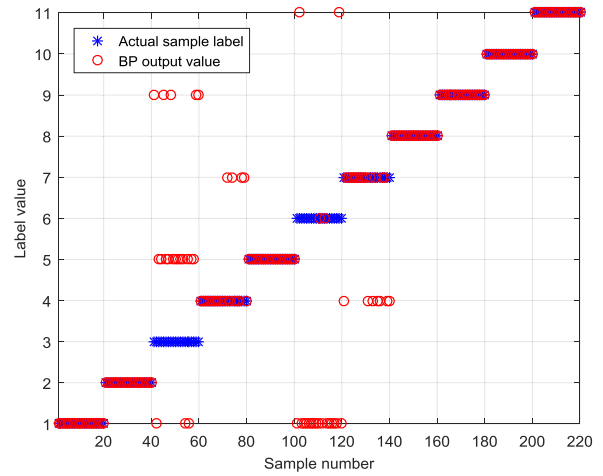
FIGURE 7. The hard fault diagnosis results based on BPNN.
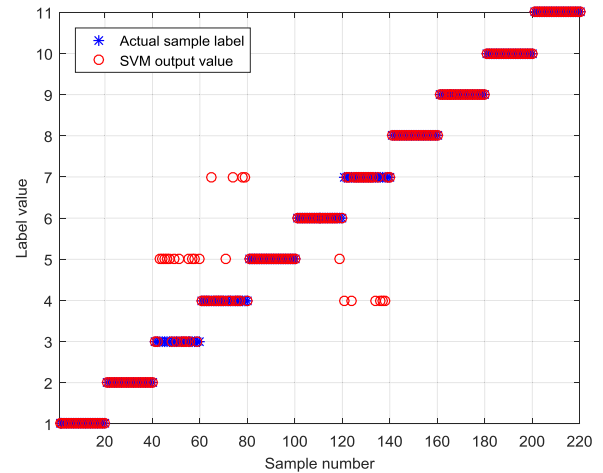
FIGURE 8. The hard fault diagnosis results based on BPNN.

pre-training of each RBM in the DBN is completed by 500 iterations. The parameters such as flock size, awareness probability, flight length and maximum iterations of CSA are 50, 0.1, 2 and 500, respectively.

1) HARD FAULT DIAGNOSIS RESULTS

The diagnostic results of case 1 based on BPNN is as shown in Fig. 7, and the average classification accuracy rate is 77.73%. Fig. 7 shows that the fault type HF3, HF4, HF6 and HF7 cannot be correctly identified; the entire test samples of HF3 and HF6 have been classified to the wrong labels. Meanwhile, the classification results for case 1 based on SVM is shown in Fig. 8. The average diagnostic rate of the test samples is 89.55%, while the classification results for fault types HF3, HF4 and HF7 are 45%, 75% and 70%, respectively. In this case, the SVM classifier is better than the BPNN.

The hidden layers of DBN are optimized by the CSA algorithm combined with the training samples. As shown in Fig. 9, in case 1, the hard fault classification accuracy changes with
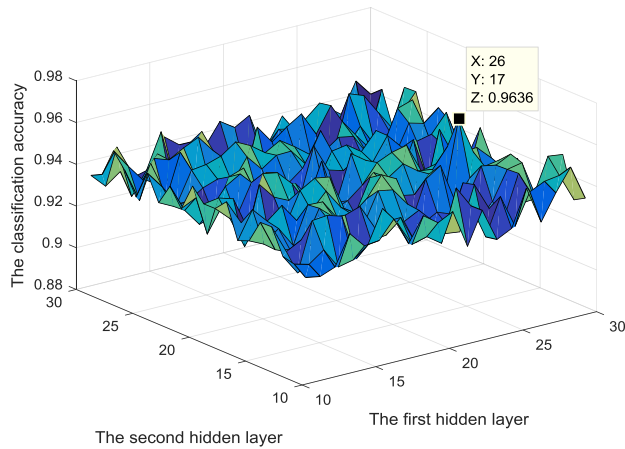
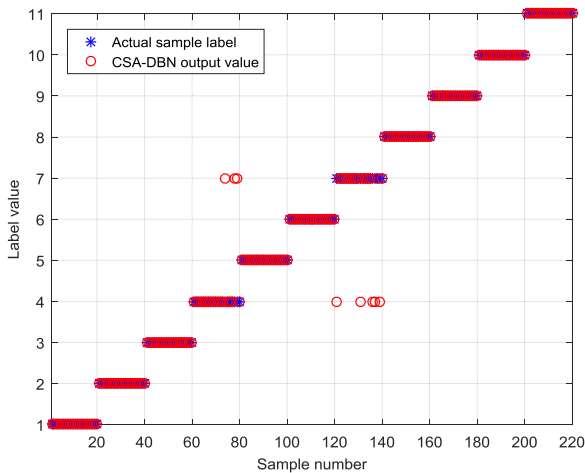**FIGURE 9.** The hard fault classification results with different numbers of units in the two hidden layers.

FIGURE 10. The hard fault classification results based on CSA-DBN.

TABLE 6. The classification accuracy and computation time for hard faults in the three cases.

Methods	Case1		Case2		Case3	
	Accuracy	t_c/s	Accuracy	t_c/s	Accuracy	t_c/s
BPNN	77.73%	6.03	72.73%	4.75	72.73%	3.84
SVM	89.55%	3.48	89.09%	2.69	80.55%	2.16
CSA-DBN	96.36%	32.6	95.68%	27.36	92.55%	25.83

TABLE 7. The classification results for each hard fault mode under case1.

Methods	Classification Accuracy of Each Hard Fault Code					
	HF1	HF2	HF3	HF4	HF5	HF6
BPNN	100%	100%	0%	90%	100%	0%
SVM	100%	100%	45%	75%	100%	95%
CSA-DBN	100%	100%	100%	85%	100%	100%
	HF7	HF8	HF9	HF10	HF11	
BPNN	65%	100%	100%	100%	100%	
SVM	70%	100%	100%	100%	100%	
CSA-DBN	75%	100%	100%	100%	100%	

TABLE 8. The classification accuracy and computation time for the soft faults in the three cases.

Methods	Case1		Case2		Case3	
	Accuracy	t_c/s	Accuracy	t_c/s	Accuracy	t_c/s
BPNN	74.5%	5.48	68.5%	3.82	62%	3.09
SVM	84%	3.39	80.5%	2.57	78%	2.28
CSA-DBN	92.5%	28.49	88.5%	22.81	86%	21.13

the numbers of units in the two hidden layers, which are both in the range of 11 through 30. Thus, the numbers of units in the first and second hidden layers determined by CSA are set to 26 and 17, respectively. It takes 32.6 seconds to seek the optimal architecture of DBN by CSA and complete the hard faults diagnosis, whose classification accuracy reaches the maximum value 96.36% (in case 1), that means there are only eight testing samples that cannot be classified correctly, as shown in Fig. 10. Additionally, it can be concluded that the hard fault diagnosis results based on the CSA-DBN are much better than BPNN and SVM.

The classification results and computation time for the three cases based on BPNN, SVM and CSA-DBN are recorded in Table 6. The computation time of CSA-DBN is greater than the other two methods because it needs some time to obtain the optimal neuron numbers of the two hidden layers. However, it is clearly revealed that the CSA-DBN performs better than the BPNN and SVM methods for the three cases. The classification results for each fault type are demonstrated in Table 7.

2) SOFT FAULT DIAGNOSIS RESULTS

The soft fault classification results and computation time tc for the three cases based on BPNN, SVM and CSA-DBN are as shown in Table 8. We can see that the diagnosis rate of soft faults based on the CSA-DBN performed better than the other two methods BPNN and SVM, although the CSA-DBN takes more computation time. The soft fault diagnosis rate is related to the number of training samples in that the diagnosis accuracy increases with the number of training samples. In addition, there are more samples need to be processed during the training period, as a result of the computation time in Case3 is less than in Case1 when using the same classification method

Under the condition of case 1, the DBN gets the best performance, whose architecture optimized by CSA is 32-23-19-10, as shown in Fig. 11. The classification rate based on the CSA-DBN is 92.5%, and the results are shown in Fig. 12. It can be seen that several samples of SF2 and SF3 cannot be classified correctly, which may be because some parameters of the degradation components have little difference between SF2 and SF3. This could in turn lead to similar feature vectors when the capacitance C_1 decreased by 50% and the ESR_1 increased by 100% or so. This phenomenon occurs in SF4 and SF5 as well. The classification results for each soft fault code are shown in Table 9.

TABLE 9. The classification results for each soft fault mode under case 1.

| Methods	Classification Accuracy of Each Soft Fault Code				
	SF1	SF2	SF3	SF4	SF5
BPNN	90%	60%	50%	70%	70%
SVM	100%	70%	80%	75%	70%
CSA-DBN	100%	80%	90%	80%	85%
	SF6	SF7	SF8	SF9	SF10
BPNN	80%	70%	80%	85%	90%
SVM	90%	80%	85%	90%	100%
CSA-DBN	95%	100%	95%	100%	100%
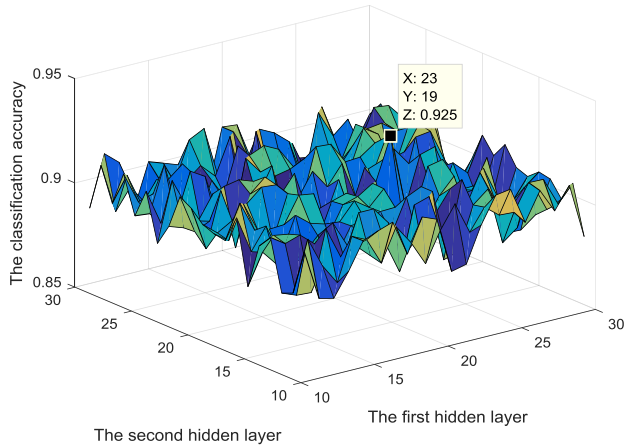
FIGURE 11. The soft fault classification results with different numbers of units in the two hidden layers.
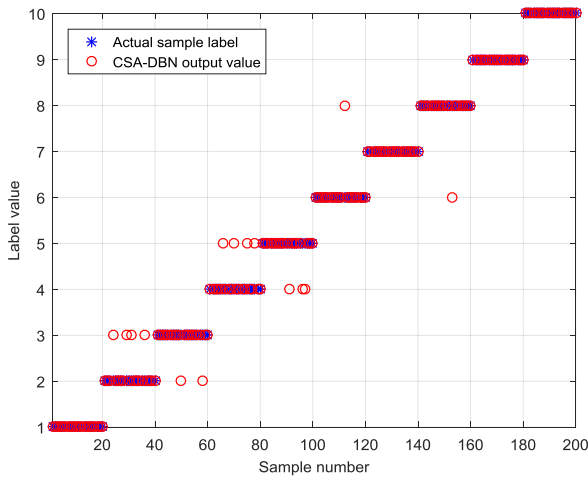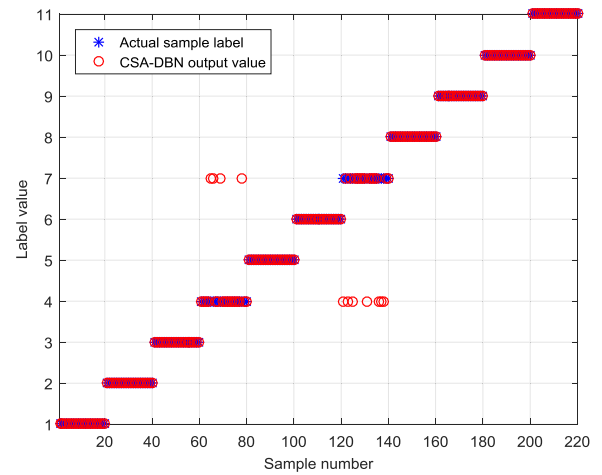

FIGURE 12. The soft fault classification results based on CSA-DBN.

B. EXPERIMENT RESULTS AND ANALYSIS

To validate the effectiveness and feasibility of the proposed method, an experimental study has been conducted on a closed-loop SEPIC circuit with a 28V DC input and a resistive load 15.2Ω. The test rig is shown in Fig. 13, and it is composed of a DC power supply, a 4-channel data acquisition system, the SEPIC converter and a laptop. For the convenience of hard and soft faults study, the main circuit board is separated
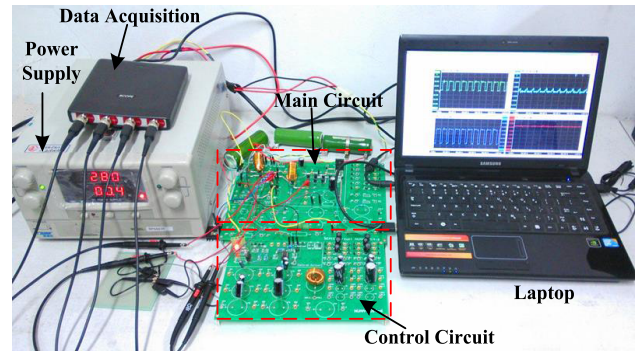
FIGURE 13. The experimental setup of fault diagnosis rig for the SEPIC circuit.

**FIGURE 14.** The hard fault classification results based on CSA-DBN.

from the control circuit of the SEPIC converter. The parameters of the inductors, resistors and capacitors are measured by Agilent 4263 LCR meter. The OCF of the SEPIC is simulated by disconnecting the component from the main circuit, while the SCF is simulated by connecting the terminals of the components. For soft fault simulation, the components such as inductors, capacitors, power MOSFETs in the main circuit are replaced by other components with different inductance, capacitance, *ESR* and R_{dson} values. In addition, in order to obtain considerable samples under variable fault modes, the input voltage varies in the range of 26.6V to 29.4V.

1) HARD FAULT DIAGNOSIS RESULTS

The diagnosis rate of hard faults based on the CSA-DBN is 95%, as shown in Fig. 14; the number of training samples and test samples for each fault type is 80 and 20, respectively. The classification result is 72.73% and 87.27% based on BPNN and SVM, respectively. Table 10 shows the classification accuracy for each fault code based on the BPNN, SVM and CSA-DBN methods. In the experiments, the optimal architecture of the DBN determined by CSA is 32-24-18-10. That is, 24 hidden neurons in the first hidden layer and 18 hidden neurons in the second layer is the best option. According to

TABLE 10. The classification results for each hard fault mode under case1.

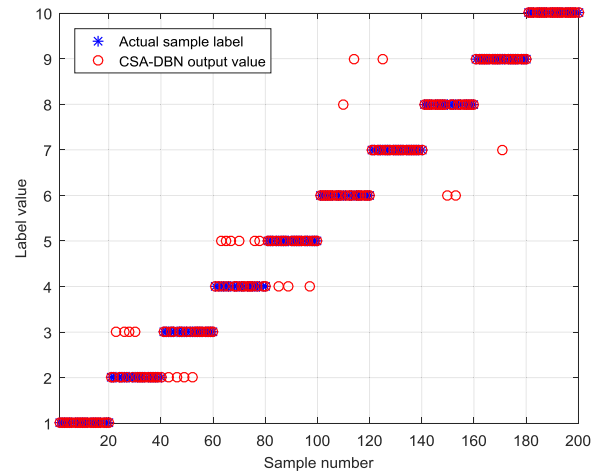| Methods	Classification Accuracy of Each Hard Fault Code					
	HF1	HF2	HF3	HF4	HF5	HF6
BPNN	100%	90%	10%	75%	90%	10%
SVM	100%	90%	45%	70%	100%	100%
CSA-DBN	100%	100%	100%	80%	100%	100%
	HF7	HF8	HF9	HF10	HF11	
BPNN	45%	100%	90%	90%	100%	
SVM	65%	100%	90%	100%	100%	
CSA-DBN	65%	100%	100%	100%	100%	
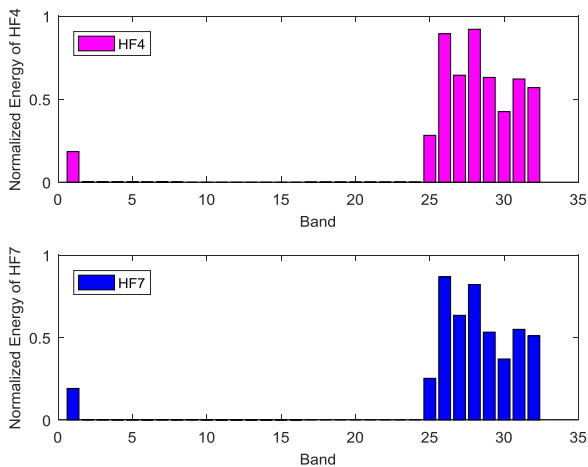
FIGURE 15. The fault feature vector for the fault type HF4 and HF7.

Fig. 14 and Table 10, the fault type HF4 and HF7 cannot be separated from each other. When the fault mode HF4 occurs, the node voltage signal V_{L2} is the same as V_{out}. The values of V_{L2} and V_{out} signals are very small which approximate to zero. Meanwhile, it is known that the value of voltage signal V_{out} equals to zero if fault mode H7 happens. Therefore, these two scenarios are similar with each other, leading to some samples of them have similar fault feature vectors (as shown in Fig. 15). The diagnosis results are consistent with the simulation tests mentioned above, which confirm that the classification accuracy of the proposed method is higher than the other methods.

2) SOFT FAULT DIAGNOSIS RESULTS

Fig. 16 shows the soft fault diagnosis results based on the proposed CSA-DBN approach. The classification accuracy based on CSA-DBN is 88.5%, while the other methods based on BPNN and SVM have an accuracy of 68.5% and 78%, respectively. The diagnosis rate for each soft fault type is demonstrated in Table 11, which indicates that the BPNN performs the worst, and the proposed method has a higher accuracy under the condition of case 1. In the experiment, the optimal architecture of the DBN for soft fault diagnosis is 32-20-18-10, which means it contains 20 hidden neurons in the first hidden layer and 18 hidden neurons in the second

FIGURE 16. The soft fault classification results based on CSA-DBN.

TABLE 11. The classification results for each soft fault mode under case 1.

Methods	Classification Accuracy of Each Soft Fault Code				
	SF1	SF2	SF3	SF4	SF5
BPNN	75%	45%	55%	55%	60%
SVM	85%	60%	65%	60%	75%
CSA-DBN	100%	80%	80%	70%	85%
	SF6	SF7	SF8	SF9	SF10
BPNN	80%	70%	75%	80%	90%
SVM	90%	80%	85%	85%	95%
CSA-DBN	90%	95%	90%	95%	100%
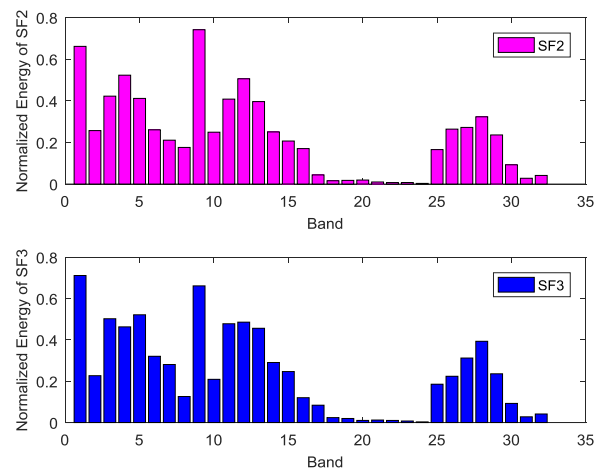
FIGURE 17. The fault feature vector for the fault type SF2 and SF3.

hidden layer determined by the CSA. Table 11 demonstrates that the classification accuracies of SF2, SF3, SF4 and SF5 are lower than other fault codes. The misclassification occurs between SF2 and SF3 mainly because the parameters of degradation capacitor C_1 changed slightly near the boundary value, which further leads to similar fault feature vectors in SF2 and SF3, as illustrated in Fig. 17. This reason can also be used to explain the misclassification between SF4 and SF5.

V. CONCLUSIONS

To realize fault diagnosis for DC-DC power converters, an optimization deep learning based diagnostic approach for both hard faults and softs fault of a SEPIC has been presented in this paper. Four node voltage signals are chosen for fault feature extraction based on wavelet packet transform. A four-layer DBN classifier is constructed for the SEPIC fault diagnosis. The numbers of neurons in the two hidden layers are determined by the crow search algorithm. Due to the initialized parameters of multiple layers acquired in the pre-training process, DBN has better performance than conventional neural networks with random values. Several simulations and experiments have been conducted in order to evaluate the applicability of the proposed technique. The results demonstrate that the proposed optimization DBN approach has a higher accuracy than other intelligent (BPNN and SVM) fault diagnosis methods which validates the effectiveness and accuracy of the proposed method. This is mainly because of the capability of the DBN to learn the highly nonlinear relationship between the inputs and the diverse fault codes of the SEPIC. It is known that useful sensing points choosing for fault feature extraction is related to the topology of the converters. Nevertheless, the output and feedback signals of the converters are often used as the indicators to reflect their health state. Future studies will focus on improving the calculation efficiency of the proposed method. The DBN will be further investigated for prognostics and remaining useful life prediction applications.

REFERENCES

[1] X. Ding, J. Poon, I. Čelanović, and A. D. Domínguez-García, "Fault detection and isolation filters for three-phase AC-DC power electronics systems," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 60, no. 4, pp. 1038–1051, Apr. 2013.

[2] A. Chakraborty, "Advancements in power electronics and drives in interface with growing renewable energy resources," *Renew. Sustain. Energ. Rev.*, vol. 15, no. 4, pp. 1816–1827, May 2011.

[3] M. S. Nasrin, F. H. Khan, and M. K. Alam, "Quantifying device degradation in live power converters using SSTDR assisted impedance matrix," *IEEE Trans. Power Electron.*, vol. 29, no. 6, pp. 3116–3131, Jun. 2014.

[4] Y. Wu, Y. Wang, Y. Jiang, and Q. Sun, "Multiple parametric faults diagnosis for power electronic circuits based on hybrid bond graph and genetic algorithm," *Measurement*, vol. 92, pp. 365–381, Oct. 2016.

[5] S. Y. Yang, D. W. Xiang, A. Bryant, P. Mawby, R. Li, and P. Tavner, "Condition monitoring for device reliability in power electronic converters: A review," *IEEE Trans. Power Electron.*, vol. 22, no. 11, pp. 2734–2752, Nov. 2011.

[6] S. Y. Yang, A. Bryant, P. Mawby, R. Li, and P. Tavner, "An industry-based survey of reliability in power electronic converters," *IEEE Trans. Ind. Appl.*, vol. 24, no. 3, pp. 1441–1451, May 2011.

[7] K. Harada, A. Katsuki, and M. Fujiwara, "Use of ESR for deterioration diagnosis of electrolytic capacitor," *IEEE Trans. Power Electron.*, vol. 8, no. 4, pp. 355–361, Oct. 1993.

[8] A. M. R. Amaral and A. J. M. Cardoso, "On-line fault detection of aluminium electrolytic capacitors, in step-down DC-DC converters, using input current and output voltage ripple," *IET Power Electron.*, vol. 5, no. 3, pp. 315–322, Mar. 2012.

[9] K. Yao, W. Tang, W. Hu, and J. Lyu, "A current-sensorless online ESR and C identification method for output capacitor of buck converter," *IEEE Trans. Power Electron.*, vol. 30, no. 12, pp. 6993–7005, Dec. 2015.

[10] Q. Sun, Y. R. Wang, Y. Y. Jiang, and Y. Wu, "On-line component-level soft fault diagnostics for power converters," in *Proc. Prognostics Syst. Health Manage. Conf.*, 2016, pp. 1–5.

[11] Q. Wang, Y. Wang, Z. Zhang, and Z. Song, "A diagnosis method for inverter open-circuit faults of brushless DC motor driver systems," *Chin. Soc. Elect. Eng.*, vol. 33, no. 24, pp. 114–120, Aug. 2013.

[12] S. Dusmez and B. Akin, "An accelerated thermal aging platform to monitor fault precursor on-state resistance," in *Proc. IEEE Int. Electr. Mach. Drives Conf.*, May 2015, pp. 1352–1358.

[13] J. R. Celaya, A. Saxena, C. S. Kulkarni, S. Saha, and K. Goebel, "Prognostics approach for power MOSFET under thermal-stress aging," in *Proc. Annu. Proc. Rel. Maintainability Symp.*, Jan. 2012, pp. 1–6.

[14] M. Shahbazi, E. Jamshidpour, P. Poure, S. Saadate, and M. R. Zolghadri, "Open- and short-circuit switch fault diagnosis for nonisolated DC–DC converters using field programmable gate array," *IEEE Trans. Ind. Electron.*, vol. 60, no. 9, pp. 4136–4146, Sep. 2013.

[15] A. Oukaour *et al.*, "Ageing defect detection on IGBT power modules by artificial training methods based on pattern recognition," *Microelectron. Reliab.*, vol. 51, no. 2, pp. 386–391, Feb. 2011.

[16] R. B. Dhumale and S. D. Lokhande, "Neural network fault diagnosis of voltage source inverter under variable load conditions at different frequencies," *Measurement*, vol. 91, pp. 565–575, Sep. 2016.

[17] G. E. Hinton, S. Osindero, and Y. W. Teh, "A fast learning algorithm for deep belief nets," *Neural Comput.*, vol. 18, no. 7, pp. 1527–1554, Jul. 2016.

[18] A. Mohamed, G. E. Dahl, and G. Hinton, "Acoustic modeling using deep belief networks," *IEEE/ACM Trans. Audio, Speech, Language Process.*, vol. 20, no. 1, pp. 14–22, Jan. 2012.

[19] R. Sarikaya, G. E. Hinton, and A. Deoras, "Application of deep belief networks for natural language understanding," *IEEE/ACM Trans. Audio, Speech, Language Process.*, vol. 22, no. 4, pp. 778–784, Apr. 2014.

[20] Y. Liu, S. Zhou, and Q. Chen, "Discriminative deep belief networks for visual data classification," *Pattern Recognit.*, vol. 44, nos. 10–11, pp. 2287–2296, Oct. 2011.

[21] A. Coates, H. Lee, and A. Y. Ng, "An analysis of single-layer networks in unsupervised feature learning," *J. Mach. Learn. Res.*, vol. 15, pp. 215–223, Jan. 2011.

[22] A. Askarzadeh, "A novel metaheuristic method for solving constrained engineering optimization problems: Crow search algorithm," *Comput. Struct.*, vol. 169, pp. 1–12, Jun. 2016.

[23] R. Wu, F. Blaabjerg, H. Wang, and M. Liserre, "Overview of catastrophic failures of freewheeling diodes in power electronic circuits," *Microelectron. Rel.*, vol. 53, no. 9, pp. 1788–1792, Sep. 2013.

[24] M. Gan, C. Wang, and C. Zhu, "Construction of hierarchical diagnosis network based on deep learning and its application in the fault pattern recognition of rolling element bearings," *Mech. Syst. Signal Process.*, vols. 72–73, pp. 92–104, May 2016.

QUAN SUN received the B.Sc. and M.Sc. degrees from the Nanjing Institute of Technology, University of Shanghai for Science and Technology, China, in 2009 and 2012, respectively. He is currently pursuing the Ph.D. degree with the Department of Automation, Nanjing University of Aeronautics and Astronautics, China. His main research interest is power electronic circuit fault diagnosis and prognosis.

YOUREN WANG was born in Changzhou, China, in 1963. He is currently a Professor and a Ph.D. Supervisor with the College of Automation Engineering, Nanjing University of Aeronautics and Astronautics, Nanjing, China. His research interests include analog and digital circuits design, test, fault tolerance, and prognosis, intelligent information on process, and evolvable hardware design.
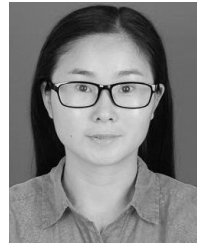
YUANYUAN JIANG was born Huainan, China, in 1982. She is currently pursuing the Ph.D. degree with the Nanjing University of Aeronautics and Astronautics, Nanjing, China. She is currently an Associate Professor with the College of Electrical Engineering, Anhui University of Science and Technology, China. Her research interests include analog circuits test and measurement, electronic prognosis, and health management.

• • •