IEEE Access
Multidisciplinary : Rapid Review : Open Access Journal

Received November 15, 2017, accepted December 12, 2017, date of publication December 15, 2017,
date of current version March 9, 2018.

Digital Object Identifier 10.1109/ACCESS.2017.2784318

Embedded Real-Time Simulation Platform for Power Distribution Systems

MIGUEL E. HERNANDEZ[1], (Student Member, IEEE),
GUSTAVO A. RAMOS[1], (Senior Member, IEEE), MIN LWIN[2], (Member, IEEE),
PIYAPATH SIRATARNSOPHON[2], (Student Member, IEEE),
AND SURYA SANTOSO[2], (Fellow, IEEE)
[1]Department of Electrical and Electronic Engineering, Universidad de los Andes, Bogota 111711, Colombia
[2]Department of Electrical and Computer Engineering, The University of Texas at Austin, Austin, TX 78712, USA

Corresponding author: Miguel E. Hernandez (me.hernandez47@uniandes.edu.co)

The work of M. E. Hernandez and G. A. Ramos was supported by the Colombian Department of Science, Technology, and Innovation (Colciencias) and the Universidad de los Andes. The work of M. Lwin, P. Siratarnsophon, and S. Santoso was supported in part by The University of Texas at Austin.

ABSTRACT The inclusion of distributed renewable energy sources, new goals of efficiency and reliability, and the technological advancement of the power grid has led to a significant increase in the complexity of distribution systems. Although multiple devices can be controlled to achieve these objectives during smart grid operation, many proposed algorithms are based on ideal scenarios where the complex distribution system is assumed to be fully observable or measurable. As this condition obstructs many advanced applications, it is necessary to implement novel alternatives that provide support and validation in the field. In this paper, we show that embedded simulation is capable of providing accurate results of the system real-time condition. The designed platform exploits the technological development of mobile devices, a specific purpose solver, and concurrent processing to embed the power systems simulation into small, flexible, and affordable devices. Simulation results demonstrate the accuracy and timeliness of the proposed real-time simulation based on the IEEE 37 bus test feeder emulation and other large-scale scenarios such as the IEEE 8500 node test feeder. We anticipate that this simulation approach will be useful for applications covering advanced protection relaying, volt–var control, topological reconfiguration, distributed generation management, storage control, and cyber security assessment among others.

INDEX TERMS Power distribution, power system analysis computing, power system simulation, real time systems, smart grids.

I. INTRODUCTION

Evolving the power system to a smart grid will unlock unimaginable capabilities to respond to environmental impacts, energy efficiency goals, and better-living conditions to our societies. Nevertheless, the upgrade requires significantly more intelligent devices integrated into the existing power systems. In this context, the importance of distributed intelligence and analysis to deal with current automation challenges [1] have highlighted the importance of developing embedded platforms that can perform dynamic validations in real-time on the field. For evolving distribution systems, it is expected that many control dynamics will be coexisting with the traditional electrical dynamic of the grid [2]. Since most of the aggregated complexity is related to the interaction of automatic devices, dynamic simulations are the main alternative to achieve a comprehensive analysis of future distribution systems.

Validation of devices and strategic operations and impact to system operations before deployment is becoming more important and challenging. Moreover, different validation techniques are also associated with the selection of allocation and size, setting adjustment, and user training among other applications [3]. These processes are usually addressed in three categories of validation platforms, where the validation type is usually selected based on economical, precision, and realism factors [4]–[6].

A pilot implementation is usually recognized as a highly reliable source of validation. In this scenario, utilities use small segments of their grids to test the real implementation of the approach under consideration. Results of this validation

2169-3536 © 2017 IEEE. Translations and content mining are permitted for academic research only.
Personal use is also permitted, but republication/redistribution requires IEEE permission.
See http://www.ieee.org/publications_standards/publications/rights/index.html for more information.

are highly realistic, as the real electrical conditions have been included to validate a novel strategy or device. However, there are significant restrictions in cost and security concerns, since novel field equipment or algorithms are subject to unsuspected conditions that could cause physical damage to human health and electrical infrastructure. Even with adequate precautions and investment, this alternative usually requires the longest time of implementation (e.g. months or years).

This research focuses on the other two remaining alternatives to obtain safe and reliable validations for smart grids. The testbed approach is widely applied to perform modeling and validation by means of a scaled representation of the power system. There are plenty of testbed developments reported on applications that cover the research and design for microgrids, distributed generation, renewable sources, electrical transportation, and advanced automation, among many others. Some developments focus on the use of software implementations and basic electrical interfaces to reproduce the expected complex operation of the system. For instance, these platforms are capable of interacting with field communications protocols in order to involve external controllers and meters [7]–[9].

Other testbeds are based on real power equipment and control hardware to represent certain portions of a large system. The mixed deployment of power equipment and computational platforms leads to a validation environment with realistic electrical conditions under emulated complex scenarios [10]–[15]. Since the real equipment is involved, non-electrical variables can also be validated with this approach. In this way, other sources of uncertainty, such as temperature and noise, could be controlled in the laboratory environment. Nevertheless, real power equipment implies significant restrictions on flexibility and cost, so the last category has been conceived to obtain the highest combination of flexibility and realism.

On the other hand, powerful computational platforms can be employed as dedicated simulation devices to enhance the test bed's flexibility. In this approach, the validation core relies on a central platform – or cluster – with advanced signal processing capabilities to reproduce the electrical signals provided by continuous computational simulations. The number of validation developments based on powerful computation has been increasing as a result of the potential capability in many research topics of power systems. Some research centers have successfully deployed this method [16]–[19], and powerful power systems laboratories are obtaining a growing role as the next generation of validation for smart grids. The increasing development of powerful computational platforms increases the potential application of studies with large distribution systems, where the solution process has challenging scales. In this context, contributions to modeling approaches in this area are usually focused on restrictions imposed by the computational efficiency and flexibility for specific purpose analysis.

Little is, however, known about successful approaches to utilize the full potential of the computational capabilities of low-cost microprocessors for large-scale simulations at real-time. This paper shows an approach to achieve real-time simulations based on the technological development of embedded microprocessors, a specific purpose solver, and concurrent processing to embed the power systems simulation into small, flexible and low-cost devices. In this way, the proposed simulator provides an innovative and efficient approach for calculating power flow in embedded simulation environments, and advanced applications based on field simulation. The proposed embedded real-time simulator was conceived as a field device based on a conceptual design to guarantee the correctness of the outputs and their timeliness. However, this device is not intended to obtain evidence to validate externally tested devices. Instead of supporting hardware-in-the-loop (HIL) operation, the proposed platform aims to be a precise real-time simulation alternative for applications where the local availability of the entire electrical model can be exploited to improve the operation.

In connection with the growing complexity of the distribution systems, field controllers are also challenged to evolve to support wider scenarios in multiple applications. This phenomenon has been observed on multiple initiatives such as setting-less protection, comprehensive volt-var control, grid-edge compensation, active management of electric vehicle chargers, tied-connected smart converter, and energy storage, among others. In this way, researchers have considered control alternatives covering local and remote solutions in both centralized and decentralized schemes. In this context, the implementation of the approach proposed in this paper brings the opportunity to include embedded simulators to support controllers on, at least, two scenarios. First, voltage and current magnitudes simulated for the whole model that can be integrated into the control logic to achieve system-awareness and enhance its capabilities (real-time simulation). And second, multi-scenario simulations that can be used as a validation tool to verify the effectiveness of control actions or the accuracy of local measurements (faster than real-time simulation). The implementation results documented in the following sections show that this approach is not only capable of supplying real-time simulation on low-cost hardware architecture, but also has a competitive performance to be applied as a simulator alternative for on-field or laboratory applications. Finally, it is important to highlight that this approach is based on the quasi-steady state time-sequential simulation as a resource that mimics the real performance of multiple control dynamics in complex systems; however, the modular task designation shows outstanding solution times that can be exploited on other simulation modes in the future.

First, the real-time framework used for this research is contextualized on Section II. Then, section III will describe a novel approach for embedded real-time simulators where architecture and implementation details are discussed. Section IV will finally focus on the experimental results and analysis based on the critical features of real-time platforms.

II. REAL-TIME SIMULATION

The time-sequential simulation has been successfully employed by real-time simulators as a tool to support the design, analysis, and validation processes in power systems [20]. Since there has been a considerable amount of previous academic research in this field, this section presents relevant concepts and developments to contextualize the main challenges and objectives of this research.

A. DEFINITIONS AND CLASSIFICATIONS

It is possible to find a wide variety of definitions for Real-Time (RT), as a result of the rich diversity of applications in different fields and the evolution of computational implementations. Unlike other computational topics, this concept has significant differences in certain contexts; therefore, it is convenient to include a proper definition for the proposed simulation platform.

Among other definitions, the general approach of Laplante and Ovaska [21] has a wide acceptance within the literature related to this topic. Laplante and Ovaska [21] discuss two practical concepts that are useful to define real-time systems in many applications. The first one involves the concept of a failed system as a system that cannot satisfy one or more predefined requirements.

Definition 1: ‘A real-time system is a computer system that must satisfy bounded response-time constraints or risk severe consequences, including failure’ [21, pp. 5].

Definition 2: ‘A real-time system is one whose logical correctness is based on both the correctness of the outputs and their timeliness’ [21, pp. 5].

This research is developed in the context of the last definition, where the system’s outputs are numerical results of distribution systems simulations. In terms of timeliness, the proposed platform is required to provide a low variance on computational times, while the correctness of the outputs are related to the numerical precision of calculated voltages and currents. The simulation process is continuously updated with measurements of electrical interfaces, so the obtained results can react to dynamic changes on the real power system. In this context, these systems are frequently classified as reactive, where programming tasks respond to a series of interactions from the outside. It is common to find these applications for real-time simulation within computational platforms known as *embedded*. These devices are composed of at least a central processing unit and a set of peripherals dedicated to providing interfaces with the outside.

It is well known that any embedded platform will present an average time to respond to scheduled tasks. This time, which can be denoted as t_R, results from a set of values that are between an upper limit $(t_R + \epsilon_U)$ and a lower limit $(t_R - \epsilon_L)$. In all cases, ϵ_U and ϵ_L are positive with the expectation of having near-zero values $(\epsilon_U, \epsilon_L \rightarrow 0^+)$. The existence of these values is the combined effect of the *latency* and propagation delays in hardware and software components. These phenomena cause variable response times (*jitter*) within the defined ranges. A proper implementation of real-time simulators must be designed to comply with latency and jitter restrictions that provide determinism and high accuracy in execution time.

B. APPLICATIONS IN POWER SYSTEMS

The technological evolution of the distribution system has been a topic of concern for many types of research in Smart Grid modeling. As computational simulation is a common tool in this process, some authors have identified the major characteristics of power systems simulators to solve current and planned needs. In this perspective, main characteristics could be summarized on model’s flexibility, data management and accuracy, interoperability with other validation platforms, and advanced integration of automation algorithms [3], [22]–[24].

These and other principles have been used in numerous studies with the real-time simulation approach [25]. This section summarizes a series of real-time applications that highlight for diverse design aspects. This review covers novel computational architectures, theoretical modeling approaches or embedded implementations. All these platforms report various alternatives to provide deterministic responses with high accuracy and timeliness; as a consequence, their revision provides important guideline for defining the architecture of the proposed platform.

Abbes *et al.* [26] present the design of a simulation platform focused on a supervisory control scheme for a system with photoelectric and wind generation backed by energy storage. The platform employs controllable power supplies, controllable loads, and dSPACE DS1104 hardware platforms with the Newton-Raphson method for the continuous solution of differential equations. This mathematical modeling is obtained from the model representation in Matlab/Simulink, where the hardware platform is capable of a maximum sampling frequency of 100 kHz. The authors state that the time resolution (10 ms) allows a correct modeling of the control dynamics for each sub-system, with an appropriate accuracy to reproduce the voltage and current signals related to the control loops, although it is not capable of simulating the actions and signals related to the system’s converters. This proposal includes an operational mode that allows 30 min of simulation in 30 s of computational execution; this feature is commonly recognized as faster than real-time simulation.

Champagne *et al.* [27] present a simulation platform to validate the operation of a control system designed for a power inverter based on IGBT semiconductors. The test case model was implemented in Matlab/Simulink, and the equivalent formulation in C language was generated and transferred to the Hypersim computational platform. The simulation does not include power signals and runs with a continuous simulation of control signals with a 50 µs time step. The authors highlight the importance of validation of real-time signals compared to *off-line* simulations for the same test system. Most of the reported differences are direct consequences of the time conditions of each model’s component. The RT simulator records the responses of a simulated electrical machine as well as the control actions of the real driver under test; however, the driver calculates the control signals on a basis of 250 ns, while the *off-line* simulator calculates its control actions on the basis of 1 µs time-step.

Craciun *et al.* [28] show a hardware in the loop simulation to study the interaction of non-linear loads with conventional protection schemes in low-power systems. The model is implemented using Matlab/Simulink on RT-LAB HIL platform with a 30 µs time-step. This implementation makes a significant effort to compensate the undesirable effects of delays and other quality problems in the current signal generation. However, the application of the additional control loop is highly dependent on this particular architecture. The power emulation is adjusted through a power amplifier and a transformer with 8 kVA nominal power, reaching the possibility to simulate currents of up to 1.5 kA in a 2 kHz frequency range.

Dinavahi [29] shows an alternative for transmission systems simulation with the capability to reproduce electromagnetic transient phenomena based on FPGA programming. This platform solves the model with 11.2 µs time-step. The simulator's architecture includes a highly detailed segmentation of the mathematical model using the parallel capability of FPGA devices. The results of this implementation show that the segmentation is flexible and efficient for transmission simulations. Nevertheless, the model definition for power electronic devices represents a big challenge and it is a significant obstacle for large-scale simulations. It is important to highlight the use of calculations based on floating point decimal numbers to increase the accuracy in some parts of the model. For the other parts, in which the accuracy is not a critical issue, the calculation can be converted and performed in the fixed-point format in those stages where the data accumulation is required.

Dinavahi *et al.* [30] present an RT platform for experimental verification to evaluate the performance of a driver applied to a 5 kV D-STATCOM. The most significant contribution in this proposal consists of an automatic adjustment of the switching signals of the control device and the time resolution of the electric model. The authors propose a methodology for timeliness correction that allows the platform to synchronize the control actions with the system's solution status when the switching signals are executed.

Larose *et al.* [31] show one of the first developments for RT simulation based on computational clusters. The article includes the platform description and an application with 55 µs time-step, where 4 processing units were involved. The authors present the conceptual aspects of the architecture design which was adopted by the commercial simulator HYPERSIM in 2003. One of the most significant components consists of the synchronization scheme used between the various components of parallel processing. In this implementation, each unit receives a stimulus to broadcast the completion of a time-step in the remaining units. Therefore, each unit is able to adjust its own idle time to reach synchrony. An alternative to address this issue consists of the variable time-step simulation [32]. In this way, it is possible to make adjustments and obtain different levels of synchronism by means of the adjustment of the time-step as a response to the system's complexity in different moments of execution.

Monga *et al.* [33] show a simulation platform with a general approach to obtain RT synchronism. In this implementation, the analysis focused on dynamic models for vehicles; however, the methodology is useful for large power systems simulators. The main concept of this approach consists essentially of delegating some computational functions to FPGA devices while other aspects of simulation are delegated to a high-performance processor. In this scheme, it is necessary that the FPGA devices are intercommunicated to perform the calculation processes. The article reports a 64-bit bus with a frequency of 200 MHz.

Vlad *et al.* [34] present a review of temporal performance aspects for an RT platform emulating a wind power generation system with their corresponding power converter. Based on this paper, it is possible to conclude that the effectiveness of the power electronics model is highly related to the timeliness of the platform. The small signal modeling of power converters usually demands high computational power and the undesirable jitter condition produces significant errors on the emulated signals. In this context, other modeling strategies are required for large distribution systems in the presence of power electronic devices.

Finally, other proposals such as [35] and [36] are designed based on simplifications and reductions to specific models for each application. The reported comparison of solution methods for floating-point calculations on FPGA devices is a powerful resource to validate the performance of other emulators [35]. These architectures have satisfactory performance based on low-cost devices; however, the scalability and flexibility for implementing other models can be challenging.

Other papers such as [37] and [38] provide detailed reviews regarding common architectures, devices, and capabilities in this field. The reading of these and other compendiums points to an inevitable conclusion: the use of real-time simulations is diverse and growing on multiple laboratory-implemented validation scenarios. This paper aims to present an alternative with technical and financial feasibility to perform continuous validations regardless of the locations or applications of interest. The usage of this platform on long-term simulations for large distribution systems has been conceived as part of a set of tools documented in [39]–[41].

III. EMBEDDED REAL-TIME SIMULATOR

The proposed platform has been designed with four main modules to achieve the optimal usage of hardware and software resources on embedded devices. Solver, scheduler, network, and application tasks are then proposed as a set of subroutines that can be implemented on two main application scenarios (Fig. 1).

In first place, the embedded platforms can be used as an autonomous simulator device (Right side on Fig. 1). In this case, the user is able to perform real-time simulations on

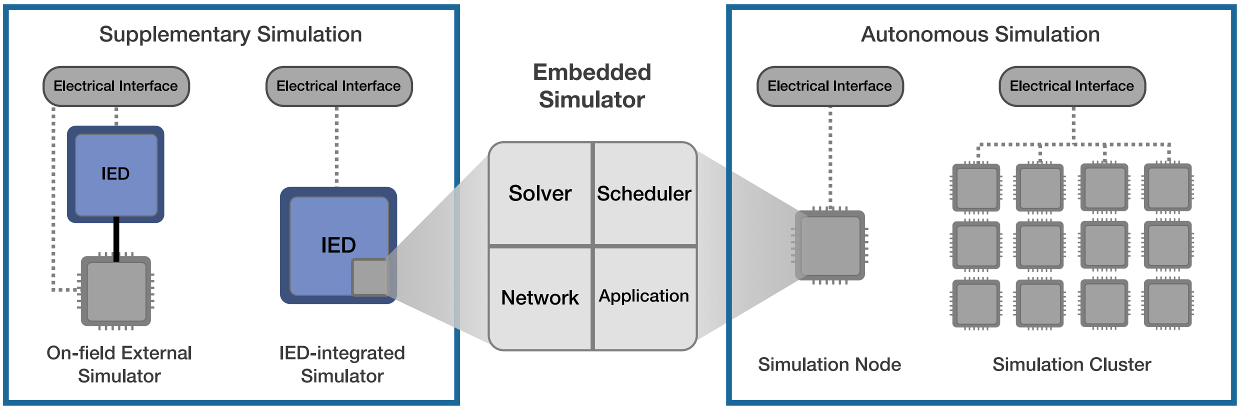

FIGURE 1. Illustration of application scenarios for embedded simulators.

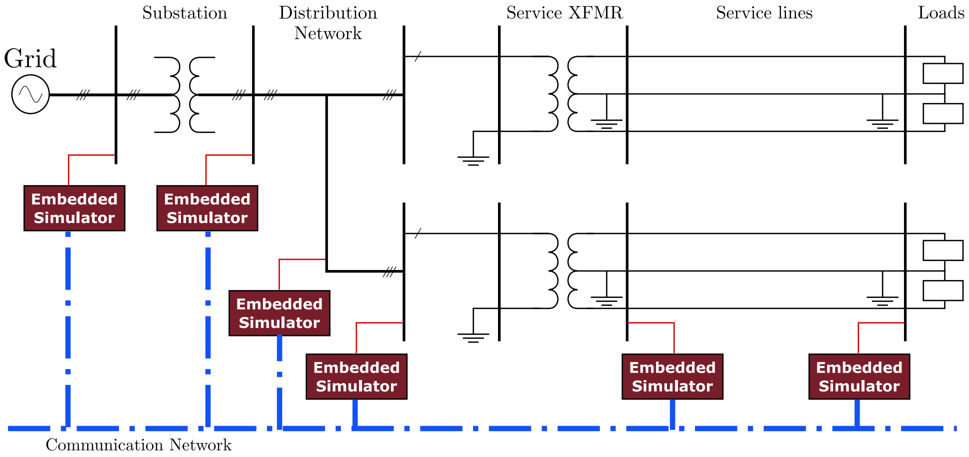

FIGURE 2. Candidate locations for the embedded simulator.

each simulation node with the low latency required to emulate the continuous measurement of electrical signals on real networks. This operation mode is usually applied in the design stage to enhance the realism of validation for new algorithms or devices. For instance, the simulation can be configured to reproduce the network operation with multiple transitions to fault conditions and an experimental algorithm for fault location, isolation, and service restoration can be included as an application task on the platform. Researchers and designers would be able to validate the experimental algorithm and use the platform as part of the process of incremental prototyping. As can be seen on section III-C, a single computational node is capable of calculating the power flow solution of the IEEE 8500 node test case with average solution times of $37\mu s$. Therefore, the platform is also capable of performing faster than real-time simulations on validations that are not dependent on real-time interactions. Both, real-time and faster than real-time simulations, can be scaled to a computational cluster for concurrent or cooperative simulation. The proposed computational approach that uses microprocessors instead of full-scale processors enables low-cost scalability and an alternative range of applications to support field controllers (Further detail regarding the design can be found on following subsections).

In this matter, the second application scenario is the use of the proposed platform as a supplementary source of information for other intelligent electronic devices (IEDs). As can be seen on the left side of Fig. 1, the embedded approach can be integrated with IEDs as an internal or external component. Certainly, the software implementation can be applied to the existing microprocessor units on field devices. However, the computational complexity of the large-scale power flow solution should be considered on devices with high priority tasks. For example, the approach can be deployed on a certain control unit of a voltage regulating device due to its available computational capacity, but it would be an excess of computational effort for certain protection devices in which the microprocessor is performing near to its maximum capability. In these scenarios with critical task priority or low computational power, the embedded simulator can be integrated as an external device (microprocessor).

The hardware and software design allows the platform to be installed at laboratories or field locations, such as substations, power poles or end users (see Fig. 2). In this context, multiple grid agents would be able to obtain a beneficial implementation of the proposed approach. The following list includes a starting point with some applications that can be considered, however, there is a broad spectrum of solutions that can be developed based on this concept.

- Researchers and manufacturers with requirements for low-cost real-time validation of new devices or strategies intended to be deployed on large-scale systems.
- Researchers and manufacturers with an interest in proposing control units supported by on-field real-time simulation to increase its adaptability, performance, or minimizing the number of settings.
- Distribution system and distributed generation operators with requirements for real-time autonomous confirmation or enhancement of existent field-controllers on scenarios of growing complexity. Essentially, additional algorithms can be implemented in the embedded platform and the digital input and outputs on field-controllers can be programmed to integrate their results. Among others, the following controllers are known to be highly responsive to the grid modernization, and, therefore, potential applications of this approach.
  - Protection devices.
  - Grid-tied inverters.
  - Power electronics devices for system-wide power conditioning.
  - Voltage regulating devices.
  - Electric vehicle charging stations.
- Users with requirements for a large number of concurrent simulations on optimization applications.
- Users with requirements for statistical analysis based on extensive simulation of scenarios.
- Users with requirements for on-field simulation for decentralized operation support.

Each embedded simulator device is equipped with the real-time capability to acquire electrical samples of one electrical bus, obtain an external estimation of unknown variables, perform a local simulation of the power grid model, and apply the simulation results for specific application processes. When more than one embedded simulator is connected to form a real-time simulation cluster, multiple electrical measurements are used to improve the external state estimation and obtain enhanced real-time simulations in each device. The simulation cluster is achieved by means of the TCP/IP connection of independent devices.

The embedded devices used in this simulator take advantage of the technological development of mobile platforms. Currently, the mobile market has low-cost units with high computational performance and low power consumption. The success of these devices is not only due to the overwhelming demand, but the precise design of Systems on a Chip (SoC) that can be exploited for other technical purposes. In this research, it is proposed that the real-time simulation approach is used in combination with distributed strategies to consolidate an alternative multi-purpose validation platform.

Furthermore, the specific design of embedded devices has not been oriented to satisfy the real-time simulation requirements. One of the most significant restrictions is the use of non-real-time operating systems and the corresponding absence of precise task schedulers. These schedulers are a fundamental component of real-time simulators because they allow the platform to satisfy a computation time constraint even with several simultaneous tasks. For this reason, this development includes software and hardware approaches to overcome the concurrent performance of the electrical measurement, power flow calculation, and off-line simulator interface. The following section describes the implemented architecture and the employed methodology.

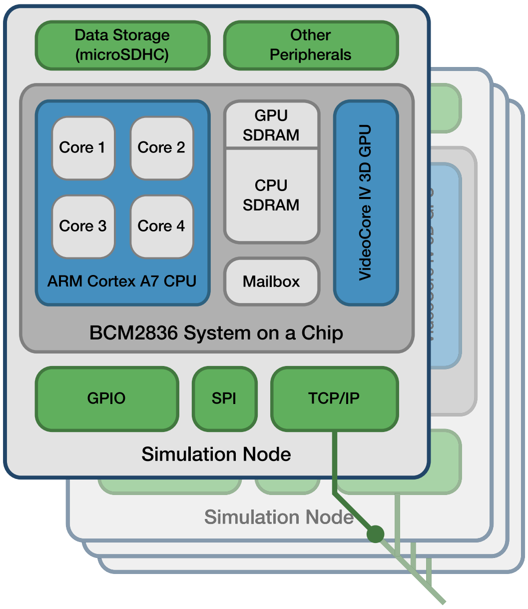

FIGURE 3. Hardware architecture of a simulation node.

A. ARCHITECTURE

Figure 3 shows the hardware architecture of a simulation node. As can be seen, each device is composed of a SoC and a set of peripherals for data exchange and electrical interface. The SoC is composed of a central processor unit (CPU), random access memory (SDRAM), and a graphics processor unit (GPU). The implementation of this platform was developed on the Raspberry Pi 2 Model B (RBP2) that uses the SoC BCM2836. Traditionally, SoCs are developed in a close connection with embedded device manufacturers, where hardware and software details are not available to the public. However, the RBP has been widely applied to custom applications in consequence of being one of the first SoC with open access to the developer community. The computational performance is characterized by a 900 MHz quad-core ARM Cortex-A7 CPU, 1 GB of SDRAM and the VideoCore IV 3D GPU.

The proposed software implementation requires a hardware platform including multi-core CPUs, GPUs, the capability to run with a customized Linux kernel, and data peripherals integrated with low latency buses. Essentially, the approach described in this section can be implemented on multiple computational architectures, such as personal computers, high-performance computing clusters, dedicated servers or embedded devices. However, this paper focuses on the embedded devices based on SoCs, which brings unique benefits in front of new applications for power system simulation.

In comparison with personal computers, the technological evolution of embedded and mobile devices has focused on a range of applications in which size, cost, power consumption, and peripherals are miniaturized. As this technological trend provides a holistic implementation of fundamental computation units on SOCs (i.e. CPUs, RAMs, and GPUs), the development can be mainly focused on the application layer. The development of real-time simulators based on high-performance computational platforms requires a significant effort on the hardware design and consequent software adjustments, while embedded real-time simulators can be developed with a modular approach focused on the software side. In this way, the use of embedded devices brings opportunities for alternative applications, and, at the same time, it facilitates its adaptability and scalability with minimum focus on the hardware design.

Some considerations of cost and performance could be useful to contextualize a software-hardware architecture intended to achieve real-time simulations using SoCs. As the applications for high-performance hardware architectures and embedded devices are substantially different, this analysis should not be considered as a direct comparison of platforms but as a summary of features to contextualize. Among multiple platforms (Opal-RT, RTDS, Typhoon, dSPACE) the ePHASORSIM tool developed by Opal-RT can be used as a reference point because of the theoretical similitude between the quasi-steady-state simulation reported in this document and the phase domain solution performed by the ePHASORSIM tool. In terms of performance, the ePHASORSIM tool is reported to achieve typical time steps in the range between 1 ms and 10 ms with a capability of 10.000 nodes per CPU core [42]. The results obtained from the implementation of the embedded platform shows that the power flow solution of a system with 8500 nodes requires an average computational time of 37 μs in one computational node. It is necessary to consider that certain dynamics could require multiple power flow iterative solutions to obtain the final results for a time-step in the circuit. However, the embedded platform exhibits the computational capability to solve large-scale systems with potentially higher time resolution.

In terms of cost, there is a plethora of considerations highly dependent on the application scenarios, including peripherals, processor units, synchronism mechanism, etc. However, a useful context between high-performance simulators and embedded simulators can be established by means of a cost comparison of their processing units. Currently, OpalRT provides a set of four high-performance platforms for real-time simulation in which the ePHASORSIM tool is supported [43]. These platforms use Intel Xeon processor units in the E3 and E5 versions. At the time of this publication, the Intel Xeon E3 has a price range between $200 (USD) and $638 (USD), while the Intel Xeon E5 has a price range between $225 (USD) and $2790 (USD). On the other hand, the BCM2836 and its ARM Cortex-A7 CPU can be found on the RBP2 by $35 (USD). This difference in the price range of processor units is a significant factor for new applications with low-cost on hardware deployment and increased scalability opportunities.

The conceptual model of this simulator involves particular tasks for the sampling, solution and estimation processes. As can be seen in Fig. 4, the platform requires information about the system status (i.e. current topology, mode of operation, etc.) and local electrical measurements to obtain a real-time simulation synchronized with the current system operation. In this way, the simulation is able to consider the change of operational behaviors, such as the dynamic demand or other electrical changes upstream to the simulated area.

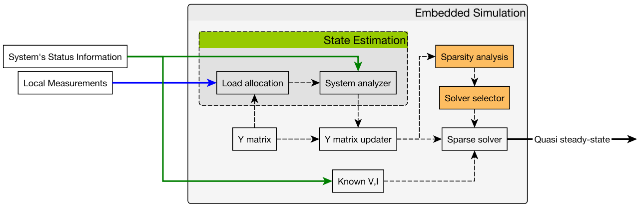

FIGURE 4. Fundamental components for embedded simulation.

The system information is used by the state estimation module to obtain updated factors of system demand (boxed in green in Fig. 4). This module is based on a load allocation algorithm that provides load multiplying factors for every system load, reflecting the locally measured voltage and current conditions. This information is used by the system analyzer to determine the required changes in the system model. Finally, the admittance matrix Y is updated with new estimations for the updated allocation and the solution process can be achieved. For the proposed platform, an external off-line simulator was employed as a system estimator synchronized with the real-time operation.

The remaining modules in Fig. 4 show the solution process. The solver algorithm is selected in accordance with the sparsity condition of the admittance matrix. These subprocesses (shown in orange in Fig. 4) are performed only as a consequence of new system models in the platform. Sparse matrices are solved with a specialized solution kernel described in Section III-C. The resulting quasi-steady-state solution provides valuable information for the additional applications that can be embedded in this platform.

B. IMPLEMENTATION AND EXPERIMENTAL SETUP

An experimental setup was designed to validate that a reference system (external RT simulation) was properly

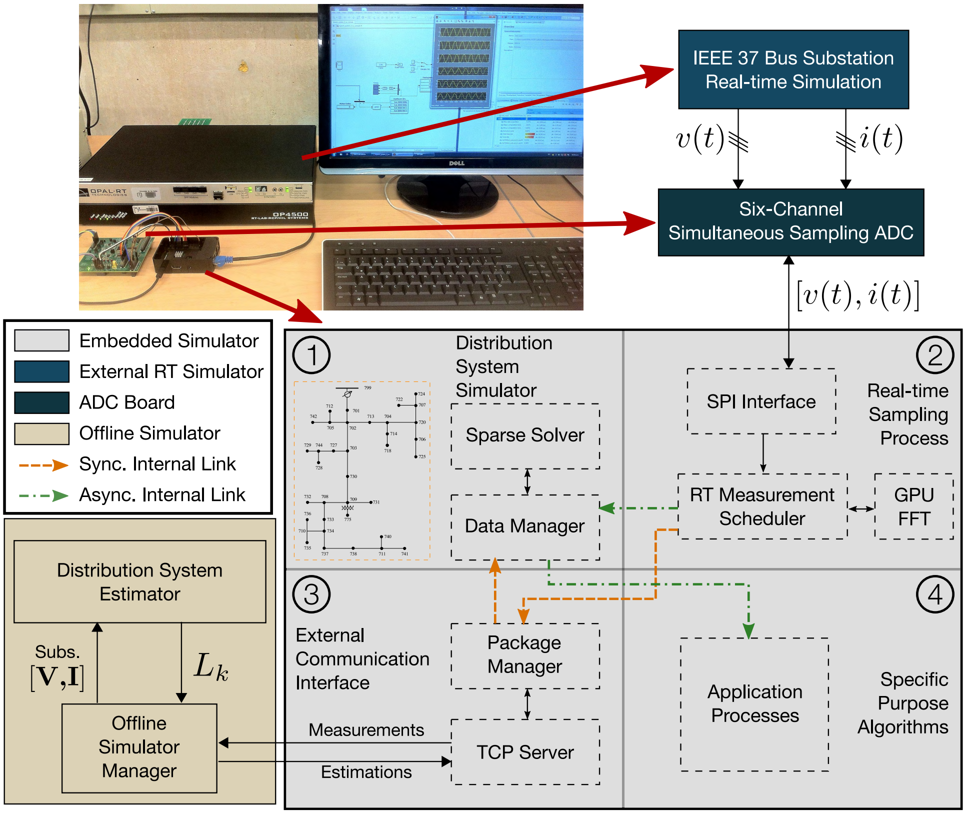

FIGURE 5. Block diagram of software/hardware implementation of the embedded simulator.

simulated on the implementation of the proposed approach (embedded simulator). The embedded simulator is intended for measuring three-phase electrical variables and making use of distribution system estimation to obtain the consequent adjustment of the internal model. This dynamic update of the embedded model is used to obtain the real-time simulation results. As the reference results can be compared with the embedded simulator implementation, the experimental setup validates and demonstrates the simulation correctness and timeliness.

The experimental setup, given in Fig. 5, starts with an external real-time simulator that provides analog voltage and current signals of the emulated substation. This module can be replaced with actual terminals of potential and current transformers upon field implementation. In this way, the experimental setup reflects the practical constraint of measurement availability on the field. Next, the analog-to-digital converter (ADC) module is employed to measure and communicate the electrical variables. One of the significant features of this component is the capability to simultaneously sample multiple channels. This characteristic allows the platform to obtain an accurate calculation of complex power and other phasor measurements. For this purpose, the ADS8556 manufactured by Texas Instruments was selected as a simultaneous high-speed multi-channel signal acquisition device. Local measurements are provided by the ADC board to the serial peripheral interface bus (SPI) attached to the embedded simulator.

Making use of the quad-core capability of the embedded device, a concurrent approach of programming was implemented. The high-performance computing alternative known as the message passing interface (MPI) is a system widely used among researchers and industrial developers in many parallel computing architectures. In particular, this platform employs the MPI approach to obtain an optimised layout of internal processes and their corresponding messages. As can be seen in Fig. 5, the internal functionality of the embedded device (depicted by Fig. 4) was divided into four processes. First, the distribution system simulator (process one) receives an asynchronous communication of local measurements as well as a synchronous update of systems estimation to obtain the power flow solution. These results are available as an asynchronous message that can be employed by application tasks managed by the fourth process/core. At the same time, the real-time sampling process is executed to receive the SPI communication from the ADC board and the fast Fourier Transform (FFT) of the sampling window. The use of the FFT algorithm embedded on the GPU obtains a fast calculation of the signal amplitude to be synchronously sent to the external communication interface process. Finally, this process is aimed to have a synchronized communication by TCP protocol over the Ethernet interface. In this way, external off-line simulators can be connected to the embedded device.

The real-time functionality was achieved by means of the custom compilation of the Linux kernel for the RBP2. As the standard Linux kernel is designed to support a variety of concurrent applications without a deterministic time scheduling, the real-time kernel requires a deep customization to comply with the platform's time constraints. In this case, the Ingo Molnar's real-time preemption patch and the Thomas Gleixner's generic clock event layer were employed to obtain an accurate scheduling of each computational task. After obtaining the custom Linux kernel, the C code implementation described by Fig. 5 is compiled and continuously executed in the embedded device. Optimisations of task priority and memory management were applied to reduce some minor changes at execution time (described on section IV-B).

C. SPARSE SOLUTION

Power distribution system simulation is performed as a sequential calculation of power flow solutions obtained from the system admittance matrix for 60 Hz. Continuous solutions with load variations reflect the dynamic of steady-states in the distribution system. This quasi-steady-state simulation provides a set of solutions that can be managed in the CPU scheduler for deterministic simulation times. Tasks related to the sparse solution and data management are referred as process one inside the embedded simulator blocks in Fig. 5.

The admittance matrix is stored in the embedded device by means of the matrix market exchange format. This approach allows the simulator to obtain a flexible update of the system model in a scalable manner for field implementation with multiple embedded devices. In a broader perspective, the data file management for system models on embedded simulators takes substantial relevance as a result of the complexity and dynamic of the network topology. This aspect should be considered in terms of compression, precision, and portability.

Another significant factor is related to the power flow solution method. The embedded simulator uses the direct solution approach optimised for sparse matrices of electrical circuits. In this field, the KLU solver is a well-recognized set of algorithms for solving the sparse linear system of equations [44], [45]. For instance, Fig. 6 shows the sparsity pattern for admittance matrix of the IEEE 37 bus test feeder. This matrix is shaped by 117 rows and columns, where a total number of 13689 elements can be stored. However, only 1031 are nonzero elements in this system model (7.5% of the total capacity).

The KLU solver was implemented based on C code provided by Tim Davis with slight adaptations for real-time operation on the embedded platform. Each power flow solution is obtained as a result of the sparse solution of the linear system $I = YV$, where I is a known vector of currents, Y is the known admittance matrix and V is the unknown vector of electrical node voltages. The KLU factorization method is aimed to optimise the number of floating-point operations and the memory usage for sparse matrices that are typical for electrical circuit models. As both characteristics are highly useful for the restricted computational features of embedded devices, the KLU solver is a desirable method for multiple systems models.

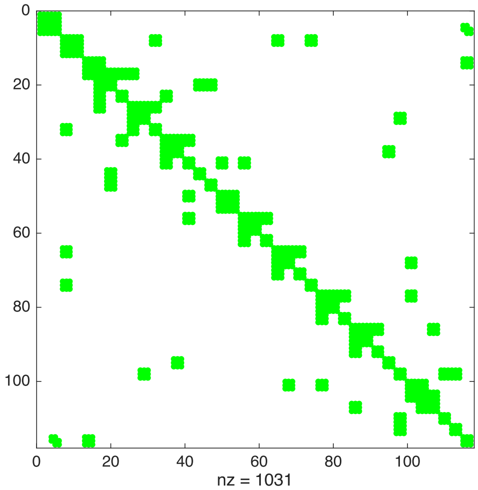

FIGURE 6. **Sparsity pattern for the IEEE 37 bus test feeder. Green dots represent nonzero values in the admittance matrix.**

As the solver computational performance has to be tested, Table 1 reports the results obtained from the embedded solutions for multiple distribution systems [46], [47]. The test consists of the computational timing of 1000 sequential solutions of the power flow for each distribution system, where the average time per power flow solution was recorded in μs. Admittance matrices were obtained from the OpenDSS model for each test feeder, and the number of nonzero elements for each case is reported in the second column in Table 1. These results show an outstanding performance of the dedicated solution process, with times as low as 37.4 ms for the most complex feeder. This characteristic provides an excellent opportunity for distributed calculation of large-scale distribution systems on this platform.

TABLE 1. **Solution time for selected test cases.**

Test case	nz	Average time [μs]
IEEE 13 bus	267	136.3
IEEE 34 bus	1092	544.0
IEEE 37 bus	1031	508.9
IEEE 123 bus	1982	1049.3
IEEE 8500 nodes	46299	37413.0
EPRI ckt 5	13917	9956.6
EPRI ckt 7	17196	11309.5
EPRI ckt 24	33672	24805.8

The correspondence between computational solution time and the number of nonzero elements can be seen in Fig. 7. This relation can be approximated by fitting a curve of the form $y = 4.369 \times 10^{-06}x^2 + 0.6026x - 36.79$. It can be concluded that the computation time is almost a linear factor of the number of nonzero elements in the admittance matrix.

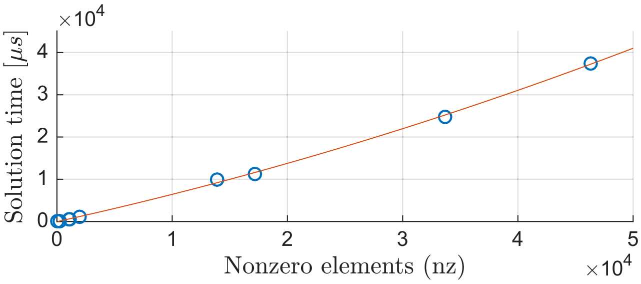

FIGURE 7. Power flow solution time vs. number of nonzero elements in the admittance matrix.

In this way, larger models can be distributed among multiple embedded devices, and the subsystem assignment can be determined by the size and time requirements according to with the previous expression.

IV. EXPERIMENTAL RESULTS

The platform prototype was tested in a laboratory setup to reproduce the condition of connection in the field with a remote state estimation. This test was focused on the measurement of factors that illustrate the correct real-time performance of the prototype. In this context, the relevant topics include the computational latency, accuracy on electrical measurements and effectiveness of embedded power flow solution.

A. TEST CASE

The selected distribution system was the IEEE 37 bus test feeder. This feeder was modeled by means of the OpenDSS simulator in which the admittance matrix could be extracted for the embedded solution. In order to perform an exploratory test, all the customer loads were considered as constant impedance. This assumption produces slight differences with the IEEE report for the power flow solution, but avoids the need for additional iterations of direct solutions to solve the non-linear behavior of constant power loads. However, the current development is also compatible with the future algorithmic implementation of solutions for these non-linear cases.

An external real-time platform is used to emulate the substation's electrical variables. These electrical signals are represented by six low-voltage channels that reproduce the voltage and current waveform continuously available at the substation. An OPAL-RT OP4500 was selected and configured to reproduce the voltage and current on different load conditions of the test feeder. As shown in Fig. 5, the substation emulation was connected to the ADC board which was responsible for simultaneously sampling three-phase voltage and current by demand.

B. REAL-TIME SCHEDULING

The strategy to measure the timeliness of the real-time schedule was driven by the sampling task. As this critical process is intended to obtain periodic samples of the electrical waveform, it is possible to validate the accomplishment of the required sample time by using the sampled signal and latency measurements.

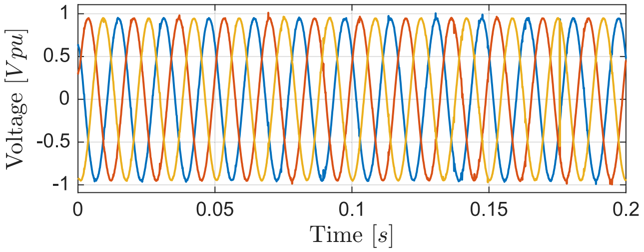

FIGURE 8. Sampled voltage waveforms obtained on the embedded simulator.

The sampling rate was calculated to obtain 2048 samples in a standard measurement window of 12 cycles at 60 Hz (200 ms). The measured electrical signals, given in Fig. 8, were post-processed to analyze the timing accuracy by means of the comparison between the frequency spectrum of the ideal sinusoidal signals and the sampled data. In this way, a significant difference between sampling intervals would be represented by significant differences between the reference and sampled spectrum. The fast Fourier transform (FFT) of the sampled signals shows that the frequency domain spectrum matches the emulated system condition (ideal signal) within the 95% confidence interval. In conclusion, the frequency domain analysis shows that the samples were taken at evenly spaced time intervals.

Additionally, latency measurements were taken for the sampling process. The success of the real-time implementation on the platform should show a high determinism of the sample time, even while other tasks are simultaneously computed. Fig. 9 shows the latency for 1000 sample windows of 200 ms. As can be seen, the average latency exhibits values around 0.8 μs. This time represents a convenient value of 0.8% of the sample time. However, maximum latency represents the 18.4% of the sample time and further adjustments to the kernel are required to avoid this undesired conditions.

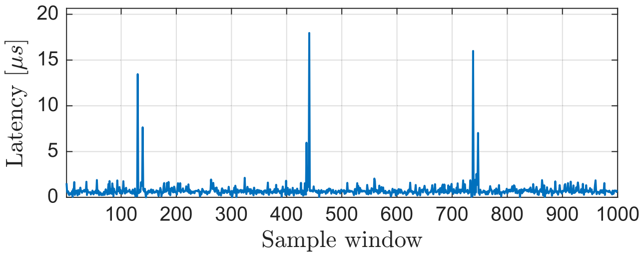

FIGURE 9. Measured latency for 1000 sampling windows of 200 ms.

As shown in Fig. 10, the histogram of measured latency depicts the achieved determinism on the embedded simulator. A high concentration of frequency in a small amount of latency values is mandatory for the real-time operation. Based on the histogram, an empirical probability of 0.7% is observed for latencies greater than 2.5 μs. As it is not possible to obtain this kind of concentration on the traditional operative system used by SoCs, these results show

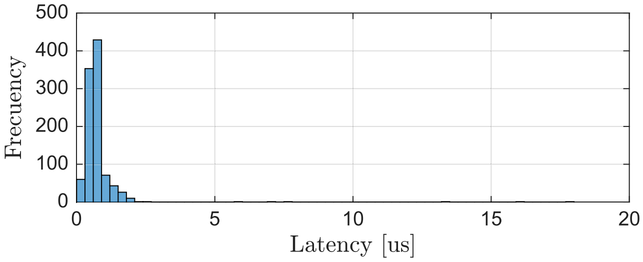

FIGURE 10. Histogram of the measured latency at the sampling process.

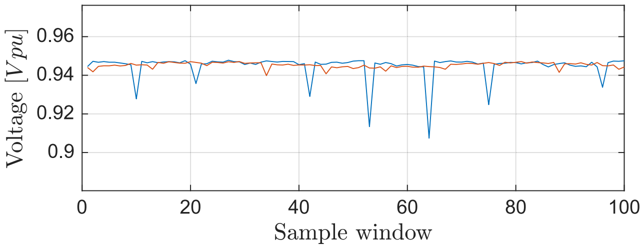

FIGURE 11. Calculated amplitude of the sampled signals for phase A. Real-time optimized in red and base kernel in blue.

that the implemented architecture achieves the aimed time constraints.

In addition to the latency measurement, results of the amplitude spectrum reflect the deterministic condition at the sampling process. If all the 2048 samples have the same sample time in the window of 200 ms, the amplitude spectrum obtained by the FFT will have an accurate representation in the frequency domain. As the sampling frequency and the number of samples were selected to obtain bin center frequencies separated by 5 Hz, it is expected that the 60 Hz amplitude can be obtained without interpolation. Therefore, the 60 Hz value on the amplitude spectrum calculated from multiple time windows obtained from a constant sinusoidal electrical waveform must lack any interpolation variance.

This phenomenon was employed to verify the scheduler accuracy and precision. Fig. 11 shows the amplitude corresponding to 60 Hz calculated by the internal FFT over 100 sample windows of a constant amplitude sinusoidal signal. Results without proper real-time optimisation, as shown in blue in Fig. 11, exhibit wrong amplitude values for certain sample windows. These low voltage amplitude peaks are located at random time instants, as a result of the remaining tasks in the embedded device and a poor performance of the real-time scheduler. Although the amplitude error is an effect of the latency variance, results in Fig. 11 shows a maximum difference of 4% with respect to the actual signal amplitude. On the other hand, the red line in Fig. 11 depicts a maximum amplitude error of 0.6% as a result of the optimised execution on the embedded platform.

C. EMBEDDED SOLUTION

The embedded simulation was tested by means of the continuous solution of the IEEE 37 bus test feeder power flow.

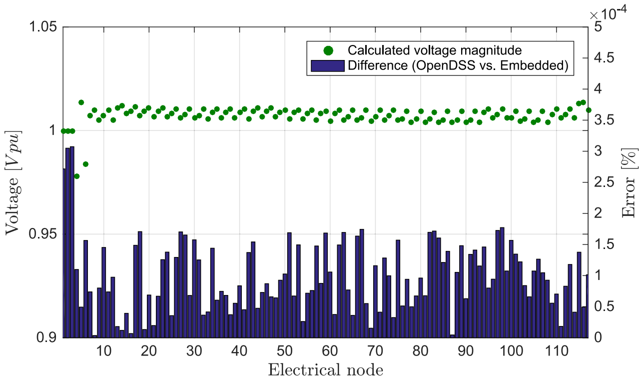

FIGURE 12. Power flow results for the 117 electrical nodes of the test case. Scatter plot in green with voltage magnitudes. Blue bars with percentage of error between OpenDSS and embedded results.

Each solution is a consequence of updated system conditions, where the external estimator provides the updated load factors that reflect the locally sampled condition. In this section, the peak load condition was used to compare the embedded results with the reference solution of the power flow. In this context, the embedded real-time calculation of nodal voltages was compared directly with the power flow solution obtained in an offline simulation with OpenDSS. This reference simulation was applied to the test case model, with the load models simplified to constant impedance values.

The results, given in Fig. 12, show the voltage condition and precision for the 117 electrical nodes of the test case model. In this representation, the scatter plot associated with the left vertical axis illustrates the calculated voltage magnitude, while the bars associated with the right axis show the difference with respect to the OpenDSS reference solution. It is important to highlight that the node order does not reflect the geographic distance to the substation, and it is only related with the random order defined by the admittance matrix construction. As can be seen, the voltage magnitudes are consistent with the expected low voltage drop profile of the IEEE 37 bus system, with values slightly over 1 Vpu for most of the electrical nodes, and the evident unbalance between phases (adjacent triplets in the electrical node list).

As illustrated by the right axis on Fig. 12, there is little difference between embedded solutions and OpenDSS reference results. The total mean squared error (MSE) for the 117 voltage magnitudes is equal to 1.3410×10^{-12}, while the corresponding mean absolute error (MAE) is equal to 1.0055×10^{-6}. Essentially, these favorable results show that the embedded solution provides a reliable calculation in comparison with offline tools.

A detailed inspection of the individual differences in Fig. 12 shows higher magnitudes for the first three electrical nodes. Although these differences are small in magnitude (less than $3 \times 10^{-4}\%$), those values reflect the effect of calculations on actual values instead of per unit values. The first three magnitude values correspond to the grid equivalent at the primary of the substation transformer. These electrical

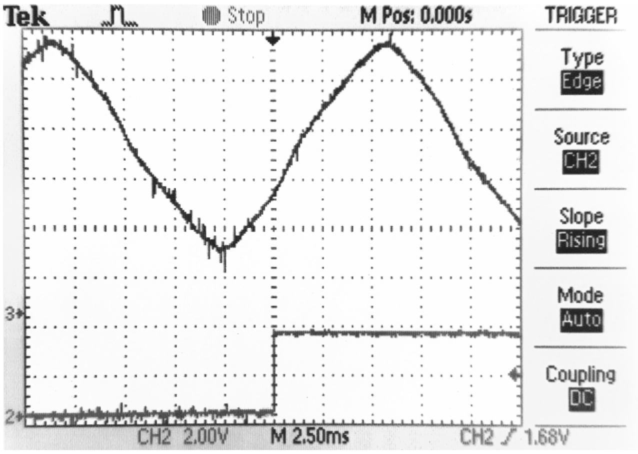

FIGURE 13. **Waveforms captured demonstrating implementation of the embedded real-time simulator for an advanced protection application.**

nodes, rated to 230 kV, are susceptible to higher precision errors than the remaining magnitudes calculated at 4.8 kV; however, the calculation on per unit base is not the most convenient alternative for distribution systems and equipment.

D. APPLICATION TO ADVANCED PROTECTION RELAYING

In this section, an application of the proposed embedded real-time simulator for advanced protective relaying is described. The application is for a protective relaying framework termed Model-Based Distributed Intelligence (MBDI), presented in [48] and [49], which integrates the output of embedded simulators within the relay to supervise distance relay decisions in real-time. The objective of the MBDI relaying framework is to supervise and secure the operation of remote backup protection elements. A brief overview of the MBDI algorithm and its integration with the proposed embedded real-time simulator follows below. The MBDI algorithm is first initiated when the apparent impedance of the relay enters distance elements zones 2 or 3. In parallel with the conventional time-delay setting, the potential fault scenarios are simulated in the relay using the embedded real-time simulator. Considering a zone 2 fault for example, MBDI logic first simulates candidate faults using the apparent impedance data at the relay location. The output of the embedded fault simulation returns expected RMS voltages at each bus for each candidate fault scenario. By comparing the embedded simulator solution with the measured real-time bus voltages at adjacent buses, the MBDI logic can confirm or reject whether a fault condition is truly present as described in [48] and [49].

A simple experimental-scale physical power system test bed is utilized to demonstrate the integrated MBDI/embedded real-time simulator prototype. The power system test bed includes transmission line models with parameters designed to be representative of a 100 mi, 5-bus, 345 kV system. The testbed system includes both transmission and distribution circuits and operating at a scaled-down 208 V and 41.6 V, respectively. The fault current on the transmission sections is limited to 6.7 A, with a nominal load current of 1.4 A. The MBDI algorithm is integrated as process four, shown in Fig. 5. A single line-to-ground fault is then applied at 100% of the transmission line length, corresponding to a zone 2 fault. The top waveform captured in Fig.13 shows the measured fault current scaled through a current transducer (CT) and the bottom waveform shows the output of the MBDI logic confirming the fault condition. These experimental results show that after the fault is detected, the proposed embedded real-time simulator is able to simulate candidate fault scenarios. The simulation output for the adjacent bus voltage magnitudes matches the corresponding measured values, allowing the MBDI logic to correctly send a supervisory confirmation of the zone 2 fault. The results further demonstrate that the proposed embedded real-time simulator can help facilitate implementation of advanced protection concepts, such as MBDI, and other applications where distributed real-time simulation is required.

V. CONCLUSION

The emergence of hardware and software accessible SoCs provide a unique opportunity for novel strategies of real-time simulation attached to the grid. This approach brings the computational power to support the simulation and assessment of complete distribution systems for multiple advanced smart grid applications. Consequently, this paper has presented the architecture and implementation of a flexible real-time simulator embedded in a Raspberry Pi 2 Model B device. Among multiple challenges in this design, it is important to highlight the computationally optimised power flow solution and the concurrent operation of processes with deterministic execution time. Moreover, the platform integrates simultaneous sampling acquisition in combination with the FFT calculated on the GPU to achieve a fast measurement and amplitude detection. This sampling process is scheduled by a customised Linux kernel that ensures the deterministic execution of the sample time, even at heavy loads by the remaining computational tasks. Other components of the real-time platform include the quasi-steady-state solver and the admittance matrix management and update, as a result of the external estimation of load conditions that reflect the locally measured variables. This platform was written in C code using the message-passing model implemented by MPI. In this way, internal processes can be assigned to individual cores or devices according to complexity requirements.

The results of the power flow solution time show the practical potential to solve large-scale systems in the embedded implementation. Additionally, real-time performance is presented based on the latency and accuracy of the electrical interface as this is the most time-critical process. Finally, the power flow solution results are compared with the reference solution obtained from an off-line simulator tool. The findings of this comparison show that the embedded solution provides accurate electrical information that can be used by specific-purpose applications. Given these results, we envision that the field implementation of the platform provides valuable information for next-generation algorithms that optimise many factors of smart grid operation. This novel approach is a promising alternative for traditional large-scale real-time simulators due to the low cost and high flexibility for field implementation.

Although the current development does not support the hardware-in-the-loop operation, the ongoing research is dealing with effective alternatives for electrical and logical interfaces to test external equipment. Currently, the research team is working on the use of the proposed embedded simulator as a core tool in adaptive protection relays based on stochastic techniques. Additional foreseen works are related to the integration of advanced distribution automation strategies and the intelligent segmentation of large-scale simulations to achieve distributed calculations and address the main limitation of temporal resolution.

REFERENCES

[1] V. Madani *et al.*, "Distribution automation strategies challenges and opportunities in a changing landscape," *IEEE Trans. Smart Grid*, vol. 6, no. 4, pp. 2157–2165, Jul. 2015.

[2] X. Yu, C. Cecati, T. Dillon, and M. G. Simões, "The new frontier of smart grids," *IEEE Ind. Electron. Mag.*, vol. 5, no. 3, pp. 49–63, Sep. 2011.

[3] R. Podmore and M. R. Robinson, "The role of simulators for smart grid development," *IEEE Trans. Smart Grid*, vol. 1, no. 2, pp. 205–212, Sep. 2010.

[4] R. F. Arritt and R. C. Dugan, "Distribution system analysis and the future smart grid," *IEEE Trans. Ind. Appl.*, vol. 47, no. 6, pp. 2343–2350, Nov./Dec. 2011.

[5] A. Monti, E. Santi, R. A. Dougal, and M. Riva, "Rapid prototyping of digital controls for power electronics," *IEEE Trans. Power Electron.*, vol. 18, no. 3, pp. 915–923, May 2003.

[6] W. Li, M. Ferdowsi, M. Stevic, A. Monti, and F. Ponci, "Cosimulation for smart grid communications," *IEEE Trans Ind. Informat.*, vol. 10, no. 4, pp. 2374–2384, Nov. 2014.

[7] M. Büscher *et al.*, "Towards smart grid system validation: Integrating the SmartEST and the SESA laboratories," in *Proc. IEEE 24th Int. Symp. Ind. Electron. (ISIE)*, Jun. 2015, pp. 1144–1150.

[8] K. L. Butler-Purry, G. R. Damle, N. D. R. Sarma, F. Uriarte, and D. Grant, "Test bed for studying real-time simulation and control for shipboard power systems," in *Proc. IEEE Electr. Ship Technol. Symp.*, May 2007, pp. 434–437.

[9] S. S. Biswas, J. H. Kim, and A. K. Srivastava, "Development of a smart grid test bed and applications in PMU and PDC testing," in *Proc. North Amer. Power Symp. (NAPS)*, Sep. 2012, pp. 1–6.

[10] C. Molitor *et al.*, "Multiphysics test bed for renewable energy systems in smart homes," *IEEE Trans. Ind. Electron.*, vol. 60, no. 3, pp. 1235–1248, Mar. 2013.

[11] M. Barnes *et al.*, "Microgrid laboratory facilities," in *Proc. Int. Conf. Future Power Syst.*, 2005, p. 6.

[12] R. H. Lasseter *et al.*, "CERTS microgrid laboratory test bed," *IEEE Trans. Power Del.*, vol. 26, no. 1, pp. 325–332, Jan. 2011.

[13] V. Salehi, A. Mohamed, A. Mazloomzadeh, and O. A. Mohammed, "Laboratory-based smart power system, part I: Design and system development," *IEEE Trans. Smart Grid*, vol. 3, no. 3, pp. 1394–1404, Sep. 2012.

[14] F. Huerta, J. K. Gruber, M. Prodanovic, and P. Matatagui, "Power-hardware-in-the-loop test beds: Evaluation tools for grid integration of distributed energy resources," *IEEE Ind. Appl. Mag.*, vol. 22, no. 2, pp. 18–26, Mar./Apr. 2016.

[15] D. Celeita, M. Hernandez, G. Ramos, N. Penafiel, M. Rangel, and J. D. Bernal, "Implementation of an educational real-time platform for relaying automation on smart grids," *Electr. Power Syst. Res.*, vol. 130, pp. 156–166, Jan. 2016.

[16] L. Meng, M. Savaghebi, F. Andrade, J. C. Vasquez, J. M. Guerrero, and M. Graells, "Microgrid central controller development and hierarchical control implementation in the intelligent microgrid lab of Aalborg University," in *Proc. IEEE Appl. Power Electron. Conf. Expo. (APEC)*, Mar. 2015, pp. 2585–2592.

[17] L. Vanfretti, M. Chenine, M. S. Almas, R. Leelaruji, L. Angquist, and L. Nordstrom, "SmarTS Lab—A laboratory for developing applications for WAMPAC systems," in *Proc. IEEE Power Energy Soc. General Meeting*, Jul. 2012, pp. 1–8.

[18] R. M. Reddi and A. K. Srivastava, "Real time test bed development for power system operation, control and cyber security," in *Proc. North Amer. Power Symp.*, Sep. 2010, pp. 1–6.

[19] Z. Haibo and G. Dandan, "The research and implementation of experimental simulation platform based on RTDS and EMS (OPEN-3000)," in *Proc. IEEE PES Innov. Smart Grid technol.*, vol. 5. May 2012, pp. 1–4.

[20] M. D. Omar Faruque *et al.*, "Real-time simulation technologies for power systems design, testing, and analysis," *IEEE Power Energy Technol. Syst. J.*, vol. 2, no. 2, pp. 63–73, Jun. 2015.

[21] P. A. Laplante and S. J. Ovaska, *Real-Time Systems Design and Analysis: Tools for the Practitioner*. Hoboken, NJ, USA: Wiley, 2012.

[22] H. T. Zhang and L. L. Lai, "An overview on smart grid simulator," in *Proc. IEEE Power Energy Soc. General Meeting*, Jul. 2012, pp. 1–6.

[23] S.-M. Lee, J. Kim, S.-M. Lee, S. Park, and B. J. Chung, "SGSim: A unified smart grid simulator," in *Proc. IEEE Power Energy Soc. General Meeting*, Jul. 2013, pp. 1–5.

[24] S. Schütte, "Simulation model composition for the large-scale analysis of smart grid control mechanisms," Ph.D. dissertation, Dept. Comput. Sci., Univ. Oldenburg, Oldenburg, Germany, 2013.

[25] X. Guillaud *et al.*, "Applications of real-time simulation technologies in power and energy systems," *IEEE Power Energy Technol. Syst. J.*, vol. 2, no. 3, pp. 103–115, Sep. 2015.

[26] D. Abbes, A. Martinez, G. Champenois, and B. Robyns, "Real time supervision for a hybrid renewable power system emulator," *Simul. Model. Pract. Theory*, vol. 42, pp. 53–72, Mar. 2014.

[27] R. Champagne, L.-A. Dessaint, and H. Fortin-Blanchette, "Real-time simulation of electric drives," *Math. Comput. Simul.*, vol. 63, nos. 3–5, pp. 173–181, Nov. 2003.

[28] O. Crăciun, A. Florescu, I. Munteanu, A. I. Bratcu, S. Bacha, and D. Radu, "Hardware-in-the-loop simulation applied to protection devices testing," *Int. J. Elect. Power Energy Syst.*, vol. 54, pp. 55–64, Jan. 2014.

[29] Y. Chen and V. Dinavahi, "FPGA-based real-time EMTP," *IEEE Trans. Power Del.*, vol. 24, no. 2, pp. 892–902, Apr. 2009.

[30] V. R. Dinavahi, M. R. Iravani, and R. Bonert, "Real-time digital simulation and experimental verification of a D-STATCOM interfaced with a digital controller," *Int. J. Elect. Power Energy Syst.*, vol. 26, no. 9, pp. 703–713, Nov. 2004.

[31] C. Larose *et al.*, "A fully digital real-time power system simulator based on PC-cluster," *J. Math. Comput. Simul.*, vol. 63, nos. 3–5, pp. 151–159, Nov. 2003.

[32] M. Montazeri-Gh, M. Nasiri, and S. Jafari, "Real-time multi-rate HIL simulation platform for evaluation of a jet engine fuel controller," *Simul. Model. Pract. Theory*, vol. 19, no. 3, pp. 996–1006, Mar. 2011.

[33] M. Monga *et al.*, "Real-time simulation of dynamic vehicle models using a high-performance reconfigurable platform," *Procedia Comput. Sci.*, vol. 9, pp. 338–347, Jan. 2012.

[34] C. Vlad, A. I. Bratcu, I. Munteanu, and S. Epure, "Real-time replication of a stand-alone wind energy conversion system: Error analysis," *Int. J. Elect. Power Energy Syst.*, vol. 55, pp. 562–571, Feb. 2014.

[35] T. O. Bachir, C. Dufour, J. Bélanger, J. Mahseredjian, and J. P. David, "A fully automated reconfigurable calculation engine dedicated to the real-time simulation of high switching frequency power electronic circuits," *Math. Comput. Simul.*, vol. 91, pp. 167–177, May 2013.

[36] M. Rakotozafy, P. Poure, S. Saadate, C. Bordas, and L. Leclere, "Real-time digital simulation of power electronics systems with neutral point piloted multilevel inverter using FPGA," *Electr. Power Syst. Res.*, vol. 81, no. 2, pp. 687–698, Feb. 2011.

[37] L. Ibarra, A. Rosales, P. Ponce, A. Molina, and R. Ayyanar, "Overview of real-time simulation as a supporting effort to smart-grid attainment," *Energies*, vol. 10, no. 6, p. 817, Jun. 2017.

[38] G. Lauss, M. Omar Faruque, K. Schoder, C. Dufour, A. Viehweider, and J. Langston, "Characteristics and design of power hardware-in-the-loop simulations for electrical power systems," *IEEE Trans. Ind. Electron.*, vol. 63, no. 1, pp. 406–417, Jan. 2016.

[39] M. Hernandez, G. Ramos, H. V. Padullaparti, and S. Santoso, "Statistical inference for visualization of large utility power distribution systems," *Inventions*, vol. 2, no. 2, p. 11, Jun. 2017.

[40] M. Hernandez, G. Ramos, H. V. Padullaparti, and S. Santoso, "Visualization of time-sequential simulation for large power distribution systems," in *Proc. IEEE Manchester PowerTech*, Jun. 2017, pp. 1–6.

[41] M. Hernandez, G. Ramos, H. V. Padullaparti, and S. Santoso, "Simulation-based validation for voltage optimization with distributed generation," in *Proc. IEEE Power Energy Soc. General Meeting (PESGM)*, Jul. 2017, pp. 1–5.
[42] Opal-RT Technologies. (2017). *ePHASORSIM—Electromechanical Real-Time Simulation*. [Online]. Available: https://www.opal-rt.com/systems-ephasorsim/
[43] Opal-RT Technologies. (2017). *Hardware Overview*. [Online]. Available: https://www.opal-rt.com/hardware-overview/
[44] T. A. Davis and E. P. Natarajan, "Algorithm 907: KLU, a direct sparse solver for circuit simulation problems," *ACM Trans. Math. Softw.*, vol. 37, no. 3, pp. 1–17, Sep. 2010.
[45] T. A. Davis and E. Natarajan, "Sparse matrix methods for circuit simulation problems," in *Scientific Computing in Electrical Engineering*. Berlin, Germany: Springer, 2012.
[46] W. H. Kersting, "Radial distribution test feeders," in *Proc. IEEE Power Eng. Soc. Winter Meeting*, vol. 2. Jan./Feb. 2001, pp. 908–912.
[47] Electric Power Research Institute. (Oct. 2016). *EPRI Test Circuits*. [Online]. Available: http://smartgrid.epri.com/SimulationTool.aspx
[48] M. Lwin, H. V. Padullaparti, and S. Santoso, "Model-based relaying supervision for mitigation of cascading outages," in *Proc. IEEE Power Energy Soc. General Meeting (PESGM)*, Jul. 2016, pp. 1–5.
[49] M. Lwin, H. V. Padullaparti, and S. Santoso, "Supervision of power swing blocking using model-based distributed intelligence relaying framework," in *Proc. North Amer. Power Symp. (NAPS)*, Sep. 2016, pp. 1–6.

MIGUEL E. HERNANDEZ (S'12) received the bachelor's degree in electronic engineering from Universidad Santo Tomas, Bogotá, Colombia, in 2011, and the M.Sc. degree in electrical engineering from the Universidad de los Andes, Bogotá, in 2014, where he is currently pursuing the Ph.D. degree with the Department of Electrical and Electronic Engineering, School of Engineering. His current research interests include real-time for power systems simulation, advanced distribution automation, and power electronics.

GUSTAVO A. RAMOS (M'04–SM'14) received the bachelor's degree in electrical engineering from Universidad Nacional, Manizales, Colombia, in 1997, and the M.Sc. and Ph.D. degrees in electrical engineering from the Universidad de los Andes, Bogotá, Colombia, in 1999 and 2008, respectively. He is currently an Associate Professor with the Department of Electrical and Electronic Engineering, School of Engineering, Universidad de los Andes.

MIN LWIN (S'12–M'17) received the B.S. degree in electrical engineering from the University of Illinois at Urbana–Champaign in 2008. He received the M.S.E. and Ph.D. degrees in electrical engineering from The University of Texas at Austin in 2013 and 2017, respectively. From 2008 to 2011, he was an Electrical Engineer with Sargent & Lundy. He is currently a Senior Engineer with GE Energy Consulting, Schenectady, NY, USA. His research interests include applications of machine learning and optimization to power systems and renewable energy integration.

PIYAPATH SIRATARNSOPHON received the B.S. degree in electrical engineering from the University of Virginia in 2014 and the M.S. degree in electrical engineering from the University of Michigan in 2016. He is currently pursuing the Ph.D. degree with The University of Texas at Austin. His research interests include power qualities and model-based distributed intelligence in power systems.

SURYA SANTOSO (F'15) received the B.S degree in electrical engineering from Satya Wacana Christian University, Salatiga, Indonesia, in 1992, and the M.S.E and Ph.D. degrees in electrical and computer engineering from The University of Texas at Austin in 1994 and 1996, respectively. He was a Senior Power Systems and Consulting Engineer with Electrotek Concepts, Knoxville, TN, USA, from 1997 to 2003. He joined the Faculty of The University of Texas at Austin in 2003, where he is currently a Professor of electrical and computer engineering with the Cockrell School of Engineering. His research interests lie in the broad area of transmission and distribution systems, modeling and simulation, and automated root-cause analysis of power quality disturbances.

He has co-authored the *Electrical Power Systems Quality*, now in its third edition (McGraw-Hill Education) and has authored the college textbook *Fundamental of Electric Power Quality* (Createspace). He is an Editor of the *Handbook of Electric Power Calculations*, the fourth edition (McGraw-Hill Education) and the Lead Editor of *Standard Handbook for Electrical Engineers*, the seventeenth edition (McGraw-Hill Education).

• • •