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Fixed Frequency Pulse-Width Modulation Based Integrated Sliding Mode Controller for Phase-Shifted Full-Bridge Converters

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ABSTRACT The conventional approach to designing controllers for the phase-shifted full-bridge (PSFB) converter is to design a linear compensator based on the small-signal model, which cannot provide the converter with strong robustness against parametric disturbances and consistent transient responses over a wide range of operating conditions. This paper proposed a fixed frequency pulse-width-modulation (PWM)-based integrated sliding mode (ISM) controller for the PSFB converter. By analyzing the phase-shifted modulation of the full bridge, the dynamic state-space model of the PSFB is established based on the simplified circuit model. On this basis, the sliding motion in state space, the existence condition for steady-state operation, and the indirect PWM control function are discussed. Meanwhile, a switch control is introduced to the control function, and a robustness condition for parametric disturbances is analyzed. The designed PWM ISM controller is applied to a 1-kW PSFB converter prototype. Experimental results verify the effectiveness of the proposed controller by comparison with the hysteresis-modulation-based sliding mode controller and the increment PID controller.

INDEX TERMS Phase-shifted full-bridge, sliding mode control, fixed frequency, pulse-width modulation, robustness.

I. INTRODUCTION

Due to its inherent zero-voltage-switching (ZVS) operation without additional devices, a phase-shifted full-bridge (PSFB) converter can operate at high frequencies with high efficiency and high power density by reducing switching losses, minimizing reverse recovery effects in rectifiers and reducing current spikes created by parasitic elements [1]. These properties make the PSFB converter a popular and suitable topology in isolated high power applications [2]. When used with renewable distributed generation, the input source is highly intermittent, and the output load is often unknown. Therefore, the power transfer in the converters is dynamic and variable [3], which requires the PSFB converter to have both a high degree of robustness and a satisfactory output performance.

Traditionally, the controller design for the PSFB converter employs linear control methods based on the small-signal model using a state-space averaging method [4]. Although the linear controller can, in practice, provide stable control to the converter for a specific operating point, it cannot provide a high degree of robustness under changing external operating conditions or disturbed internal system parameters [5]. Because the PSFB converter, as a switching circuit, is a typical nonlinear system, it is unfit for a linear control technique.

As microprocessors with reduced costs and increased processing capacities become more available, the digital implementation of nonlinear control methods in switching power converters design becomes easier [6], making such methods as sliding mode (SM) control more feasible. As a variable structure control method, SM control naturally adapts to a system's nonlinearities [7]. Thus, due to SM control's outstanding robustness with respect to parametric variations and external disturbances, this method has recently been used for designing controllers for DC/DC converters.

To suppress the steady-state error, an additional term representing the double-integration of the output error is introduced in order to construct the sliding surface of the SM controller for the power converters presented in [8]. Although increasing the order of a system's controller improves the steady-state accuracy, the system's stability is

weakened due to the introduction of the integral pole term. In [9] and [10], a second-order SM controller is presented in order to enable a faster transient converter response and provide stronger robustness against parametric uncertainties, where the second-order time derivative of sliding surface is a non-empty set. This feature forces the system's trajectory to reach an equilibrium point directly, instead of reaching the surface first and later moving along the surface towards an equilibrium point, as is the case in a traditional first-order SM controller. However, this method complicates the design of the SM controller, since there are more parameters that need to be calculated.

The switching frequency of the converter under natural SM control is intrinsically uncontrolled. Although SM control can be implemented by means of hysteresis modulation (HM) to limit the maximum switching frequency, the frequency is variable and sensitive to the converter's parameters and operating conditions [11]. Such variations complicate the design of the reactive components, since these are usually designed for a fixed switching frequency. Moreover, as the harmonic content of the switching frequency is not constant, the function of output filters is weakened [12]. To solve this problem, several researchers have made an attempt to regulate the switching frequency under SM control.

Yan *et al.* [10] and Repecho *et al.* [13] show that adaptively modifying the amplitude of the hysteresis band in the hysteresis modulator in the event of a change in the operating conditions alleviates the problem of frequency variation in the HM based SM controller. However, the switching frequency is not perfectly constant, since it still fluctuates on a small scale at steady-state operation. As shown in [8] and [14], fixed switching frequency can be achieved by comparing the control signal to the ramp waveform to generate discrete gate pulses with pulse-width modulation (PWM). The PWM based SM controller loses a portion of its inherent robustness and dynamic performance, especially at low frequency, due to replacing the original discrete SM control action with a duty cycle, which is a smooth analytic function. In [15], an implementation of the SM controller is applied to the Buck converter using an analog phase locked loop (PLL) for switching frequency control. This method considers the converter as an oscillator in a PLL, since the switching frequency is individually regulated at each cycle with respect to the previous cycle. This method fixes the switching frequency without designing hysteresis comparators, as is required in to the HM SM controller, and preserves the original robustness, as opposed to the PWM SM controller. However, introducing a PLL requires complicated circuitry with an external frequency generator and increases power consumption.

Many of the presently used converters controlled by the SM controller use basic topologies, such as buck and boost converters. These converters only have two substructures, corresponding to the two states of a switch, i.e., ''turn-on'' and ''turn-off.'' Since the PSFB converter has four switches operated with phase-shifted modulation, which leads to multi-substructures, attempting to directly introduce the one-dimensional SM control law to the PSFB converter encounters certain limitations. In this paper, by simplifying the switching logic of the PSFB converter, the phase-shifted operation of four switches can be simplified to a one switch action, which facilitates the design of an SM controller for PSFB converters. Next, based on the equivalent dynamic model, the equivalent PWM control function is described by redesigning the control law. This equivalent function can be directly used in counting the registers of a digital processer. To compensate for the robustness loss caused by the suppression of PWM control, a switch control is introduced, which forms the integrated control function with the PWM control. Furthermore, the existence condition and robustness condition are analyzed, which provide the basis for the selection of the sliding coefficients. Finally, a fixed frequency PWM based integrated sliding mode (ISM) controller for the PSFB converter is derived. The effectiveness of the proposed controller is validated by experimental results and comparisons with the traditional HM SM controller and the increment PID controller.

This paper is organized as follows. The operating principle and the equivalent state-space model of the PSFB converter are introduced in Section II. The proposed controller design for the PSFB converter is presented in Section III. A description of the experimental setup of a 1 kW PSFB converter and discussion on experimental results are given in Section IV. Section V presents the paper's conclusions.

II. DYNAMICAL MODEL OF PSFB

A. OPERATION PRINCIPLE OF PSFB

The topology and operating waveforms of the PSFB converter are shown in Fig. 1, where V_{i} is the input source, S_x indicates the semiconductor switch, which is itself composed of the active switch G_x, the antiparallel diode D_{px}, and the junction capacitanceC_{px}, L and C are respectively the inductor and capacitor of the output filter, i_{L} and i_{C} are respectively the currents through the inductor L and capacitor C, V_{o} is the voltage across the capacitor C, T_{s} denotes the switching period and T_{hs} is the half-switching period. To achieve ZVS, two legs of a full-bridge are operated with a phase-shifted angle, as shown in Fig. 1(b). At the same bridge, with the dead-time being ignored, the turn-on signals for the two active switches maintain a half-switching period and the lower switches are controlled complementarily with the upper switches. Meanwhile, the leading gate signals Q_1 and Q_3 are applied to switches S_1 and S_3 followed by the application of the lagging gate signals Q_2 and Q_4 to switches S_2 and S_4 by a phase angle of δ. If the phase angle δ is changed, then the converter alters the point when the AC output voltage v_{ab} continues at the primary side of transformer, which results in a change in the secondary voltage of transformer and therefore a change in the output voltage of the PSFB converter.

Let x_1 be the output voltage error, x_2 be the derivative of the voltage error, and let x_3 be the integral of the voltage error. Under the continuous current mode operation of the converter, the state variables x_1, x_2, and x_3 can be

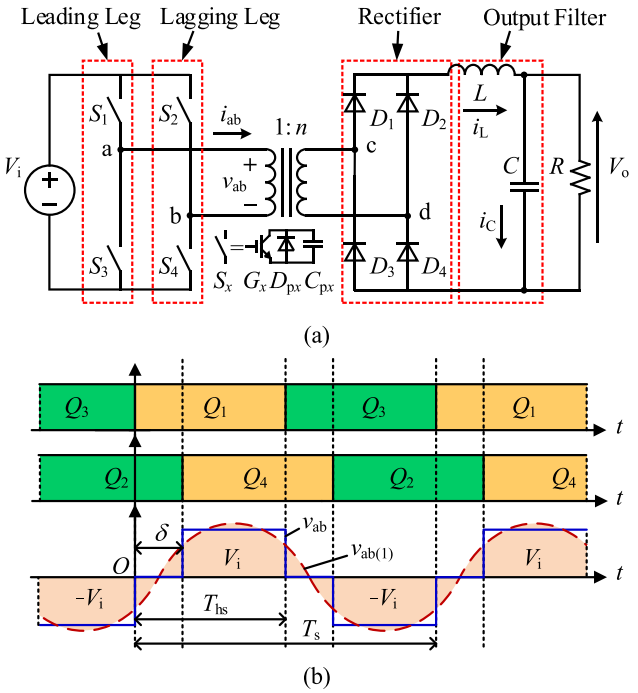

FIGURE 1. (a) Topology and (b) operating waveforms of the PSFB converter.

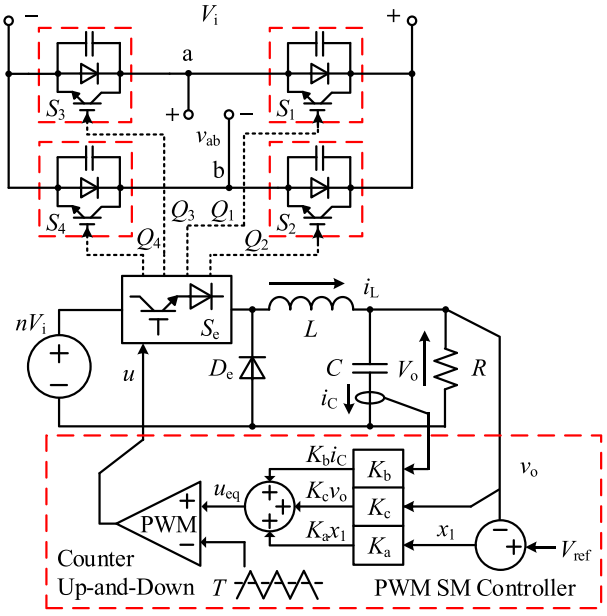

FIGURE 2. Simplified circuit model of PSFB and PWM based SM controller with digital pulse-width modulator.

expressed as

$$\begin{cases} x_1 = V_{\text{ref}} - v_o \\ x_2 = \dot{x}_1 = \frac{d(V_{\text{ref}} - v_o)}{dt} \\ \quad = \frac{v_o}{RC} - \int \left[\frac{(u_1 - u_2 - u_3 + u_4) n v_{\text{ab}}}{2LC} - \frac{v_o}{LC} \right] dt \\ x_3 = \int x_1 dt = \int (V_{\text{ref}} - v_o) dt \end{cases} \tag{1}$$

where n is the secondary to primary turns ratio of the transformer, and V_{ref}, v_{ab} and v_{o} are the reference output voltage, instantaneous primary voltage and instantaneous output voltage, respectively. The control inputs $u_1 - u_4$ stand for the states of switches $S_1 - S_4$. By taking the derivative of (1), the state-space equation can be expressed as follows

$$\begin{bmatrix} \dot{x}_1 \\ \dot{x}_2 \\ \dot{x}_3 \end{bmatrix} = \begin{bmatrix} 0 & 1 & 0 \\ -\frac{1}{LC} & -\frac{1}{RC} & 0 \\ 1 & 0 & 0 \end{bmatrix} \begin{bmatrix} x_1 \\ x_2 \\ x_3 \end{bmatrix} + \begin{bmatrix} 0 \\ \frac{V_{\text{ref}}}{LC} \\ 0 \end{bmatrix} + \begin{bmatrix} 0 & 0 & 0 & 0 \\ -\frac{n v_{\text{ab}}}{2LC} & \frac{n v_{\text{ab}}}{2LC} & \frac{n v_{\text{ab}}}{2LC} & -\frac{n v_{\text{ab}}}{2LC} \\ 0 & 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} u_1 \\ u_2 \\ u_3 \\ u_4 \end{bmatrix} \tag{2}$$

B. EQUIVALENT DYNAMICAL MODEL OF PSFB

The PSFB converter has a four-dimensional control input. In a single switching period, four different combinations of inputs correspond to four substructures, or operating phases, which are shown in Fig. 2. Four-dimensional inputs can be expressed in a Boolean matrix as

$$\mathbf{K} = \begin{bmatrix} 1 & 0 & 0 & 1 \\ 0 & 0 & 1 & 1 \\ 0 & 1 & 1 & 0 \\ 1 & 1 & 0 & 0 \\ 1 & 0 & -1 & 0 \end{bmatrix} \begin{matrix} u_1 \\ u_2 \\ u_3 \\ u_4 \\ v_{\text{ab}} \end{matrix} \tag{3}$$

where $v_{\text{ab}} = 1, 0$ and -1 denote V_{i}, 0 and $-V_{\text{i}}$, respectively. Based on Fig. 1 (b) and (3), we observe that when the two switches on the diagonal line of the full-bridge turn on, the input source V_{i} starts transferring power to the load R; and when the two switches on the horizontal line of the full-bridge turn on, the voltage source V_{i} stops transferring power. Thus, the simplified control input u can be defined as

$$u = \begin{cases} 1 = \text{“diagonal switches turn on”} \\ 0 = \text{“horizontal switches turn on”} \end{cases} \tag{4}$$

It should be noted that achieving phase-shifted modulation depends on the collaborative operation of the four switches in the full-bridge and follows a certain sequence of switching logic. Therefore, the simplified control input u should keep the logic unchanged.

Since the PSFB converter is a buck-derived topology, assuming that the components are ideal and ignoring the duty cycle loss in the primary, the PSFB converter is simplified to a buck circuit, as shown in Fig. 2. The simplified control input u is the gate signal that is applied to the equivalent switch S_{e}. We can easily derive that the switching period of u is T_{hs} and its duty cycle is D_{s} which is given by

$$D_s = \frac{180^\circ - \delta}{180^\circ} \tag{5}$$

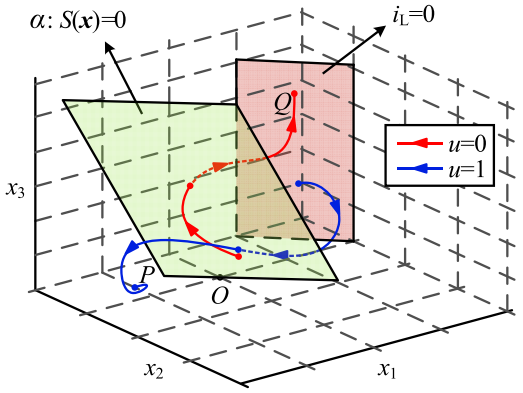

FIGURE 3. Phase trajectories of individual substructures corresponding to $u = 1$ and $u = 0$ for an arbitrary starting position.

Thus, the average output voltage of the converter in a switching period can be expressed as

$$V_o = nD_sV_{\mathrm{i}} \tag{6}$$

Similarly, the voltage error x_1, the derivative of the voltage error x_2, and the integral of the voltage error x_3 are selected as state variables. Equation (3) can be simplified as

$$\begin{aligned}\begin{bmatrix}\dot{x}_1\\ \dot{x}_2\\ \dot{x}_3\end{bmatrix} &= \begin{bmatrix}0 & 1 & 0\\ \frac{-1}{LC} & \frac{-1}{RC} & 0\\ 1 & 0 & 0\end{bmatrix}\begin{bmatrix}x_1\\ x_2\\ x_3\end{bmatrix} + \begin{bmatrix}0\\ -\frac{nV_{\mathrm{i}}}{LC}\\ 0\end{bmatrix}u + \begin{bmatrix}0\\ \frac{V_{\mathrm{ref}}}{LC}\\ 0\end{bmatrix}\\ &= \mathbf{Ax} + \mathbf{B}u + \mathbf{D}\end{aligned} \tag{7}$$

where $x = [x_1, x_2, x_3]^{\mathrm{T}}$

III. PWM BASED INTEGRATED SM CONTROLLER

A. CONTROL LAW

The output characteristic of the converter is exploited and taken into account in order to design the SM voltage controller. By analyzing the frequency of the complex field, the dynamic output voltage v_{o} of the PSFB converter in an open-loop can be expressed as

$$v_o(t) = unV_{\mathrm{i}} + (-1)^u A_m \cdot \exp\left(\frac{-t}{2\tau}\right) \cdot \cos(\omega t - \theta) \tag{8}$$

where the time constant τ, frequency ω, amplitude A_{m}, and primary phase angle of θ are determined by the converter parameters and initial conditions. According to (8), Fig. 3 graphically represents the phase trajectories of the individual substructures corresponding to $u = 1$ or $u = 0$ for an arbitrary starting position in state-space. As we can see from this figure, the trajectory converges to the equilibrium point $Q(V_{\mathrm{ref}}, 0, M)$ for $u = 0$, where M denotes the maximum limit of the integral. Similarly, the trajectory converges to the point $P(V_{\mathrm{ref}} - nV_{\mathrm{i}}, 0, M)$ for $u = 1$.

The sliding surface α is designed to pass through the origin O, i.e.,

$$\alpha : S(\mathbf{x}) = S(x_1, x_2, x_3) = 0 \tag{9}$$

By combining (1) and (9), we can conclude that

$$x_2 = H(x_1, 0, t) \tag{10}$$

Equation (10) indicates that when the system's operation is limited on the sliding surface, the state variable x_2 is determined by x_1. Since a reduced-order state variable is involved in the process of SM, SM control is actually a reduced-order control method. Normally, a controller composed of $(r-1)$th order sliding surface can achieve stable control of an rth order converter. Next, to assure the stability of the PSFB converter, the sliding surface function is designed as

$$S(\mathbf{x}) = k_1x_1 + k_2x_2 + k_3x_3 = \mathbf{Jx} \tag{11}$$

where k_1, k_2, and k_3 are sliding coefficients, and $\mathbf{J} = [k_1, k_2, k_3]^{\mathrm{T}}$. The sliding surface $S = 0$ divides the $x_1 - x_2 - x_3$ state-space into two regions. Each region can be specified with a switching state to drive the phase trajectory toward the sliding surface. From Fig. 3, we can observe that when the trajectory is above α, i.e., $S > 0$, the control input $u = 1$ will enable the trajectory to move toward the surface; when the trajectory is below α, i.e., $S < 0$, $u = 0$ will enable the trajectory to move toward the surface. Hence, the control law is designed as

$$\begin{aligned}u &= \frac{1}{2}[1 + sgn(S)]\\ &= \begin{cases}1 = \text{“diagonal switches turn on”}, & \text{for } S(x) > 0\\ 0 = \text{“horizontal switches turn on”}, & \text{for } S(x) < 0\end{cases}\end{aligned} \tag{12}$$

B. EXISTENCE CONDITION

Although the control law (12) ensures that the trajectory will be driven toward the sliding surface, it cannot provide the stability to ensure that the trajectory can be maintained on the sliding surface. Only when the trajectory slides on the surface and converges to the origin O can the system be considered stable. Next, an existence condition must be obeyed

$$\lim_{S\to 0} S(\mathbf{x}) \cdot \dot{S}(\mathbf{x}) < 0 \tag{13}$$

The time derivative of (11) is expressed as

$$\dot{S}(\mathbf{x}) = \mathbf{J}(\mathbf{Ax} + \mathbf{B}u + \mathbf{D}) \tag{14}$$

By combining (13) and (14), the existence condition for SM is

$$\begin{aligned}&\lim_{S\to 0} S(\mathbf{x}) \cdot \dot{S}(\mathbf{x}) < 0\\ &\Rightarrow \begin{cases}\alpha_1 = \mathbf{J}(\mathbf{Ax} + \mathbf{B} + \mathbf{D}) < 0, & \text{for } S(\mathbf{x}) \to 0^+\\ \alpha_2 = \mathbf{J}(\mathbf{Ax} + \mathbf{D}) > 0, & \text{for } S(\mathbf{x}) \to 0^-\end{cases}\end{aligned} \tag{15}$$

α_1 and α_2 can be rearranged in scalar representation, i.e.,

$$\begin{cases}\alpha_1 = k_3x_1 + \left(k_1 - \dfrac{k_2}{RC}\right)x_2 - k_2\left(\dfrac{nV_{\mathrm{i}} - v_o}{LC}\right)\\ \alpha_2 = k_3x_1 + \left(k_1 - \dfrac{k_2}{RC}\right)x_2 + \dfrac{k_2v_o}{LC}\end{cases} \tag{16}$$

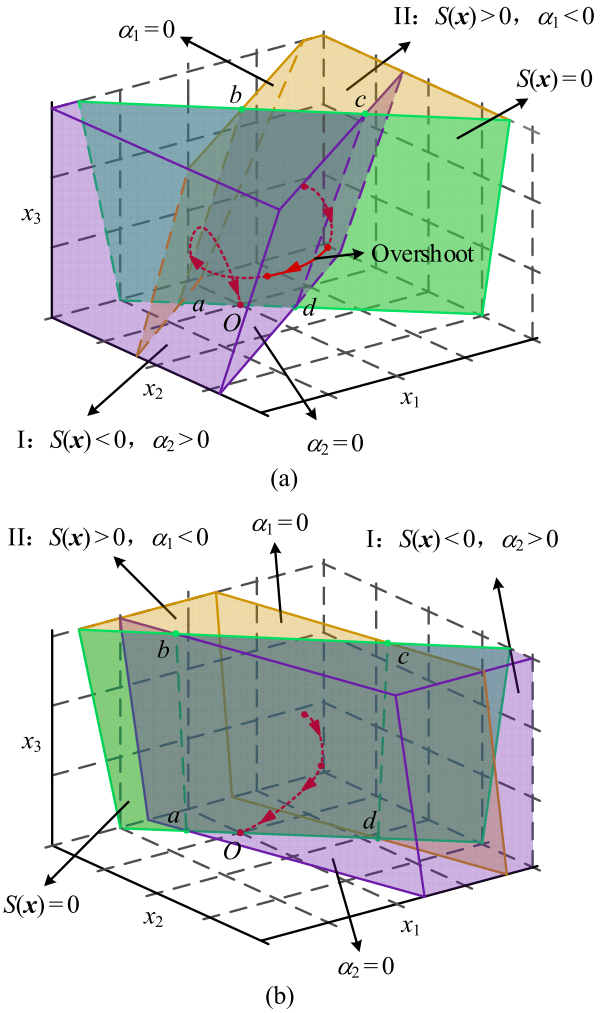

FIGURE 4. Existence regions of SM operation and phase trajectory in state-space for (a) $k_1 > 1/RC$ and (b) $k_1 < 1/RC$.

By substituting (16) into (15), the existence condition can be rearranged as follows

$$0 < \frac{k_3}{k_2}x_1 + \left(\frac{k_1}{k_2} - \frac{1}{RC}\right)x_2 + \frac{v_o}{LC} < \frac{nV_i}{LC} \tag{17}$$

To conveniently analyze the equation, we assume $k_2 = 1$. A graphic depiction of the existence regions can be seen in Fig. 4 for two respective cases: $k_1 > 1/RC$ and $k_1 < 1/RC$. In Fig. 4, region I represents $\alpha_2 > 0$, $S < 0$ and region II represents $\alpha_1 < 0$, $S > 0$. The SM operation occurs on the partial sliding surface covering both regions I and II. This partial surface is within *ab* and *cd*, where *ab* is the intersecting line of the two planes defined by $S = 0$ and $\alpha_1 = 0$, and *cd* is the intersecting line of the two planes defined by $S = 0$ and $\alpha_2 = 0$. For the case where $k_1 > 1/RC$, the trajectory will not enter SM operation and overshoot, landing outside of *abcd*, since it will slide to the origin O only when it is touching $S = 0$ within *abcd*, as shown in Fig. 4(a). For the case where $k_1 < 1/RC$, the trajectory on the surface is bounded within *abcd*, which means it will converge to the origin O without overshooting upon reaching the surface for the first time.

In practice, the sensitivity on the instantaneous load resistance decreases when the sliding coefficients are properly designed such that $k_1 > 1/R_{(\min)}C$, $R_{(\min)}$ is the minimum load resistance, Meanwhile, by introducing the actual operating conditions into (17), the design constraint can be tightened. According to the tightening method described in [11], by decomposing (17) into two inequalities and considering them as individual cases with respect to the polarity of the capacitor current flow, the conditions covering the range of input voltage and output load for which the PSFB converter is designed for is given by

$$\begin{cases} \dfrac{k_1}{k_2} - \dfrac{1}{R_{(\max)}C} < \min(\Delta_1, \Delta_2) \\ \Delta_1 = \dfrac{V_o}{L\left|i_{C(\text{peak})}\right|} + \dfrac{k_3 C(V_{\text{ref}} - v_o)}{k_2\left|i_{C(\text{peak})}\right|} \\ \Delta_2 = \dfrac{nV_{i(\min)} - V_o}{L\left|i_{C(\text{peak})}\right|} - \dfrac{k_3 C(V_{\text{ref}} - v_o)}{k_2\left|i_{C(\text{peak})}\right|} \end{cases} \tag{18}$$

where $R_{(\max)}$ is the maximum load resistance, $V_{i(\min)}$ is the minimum input voltage, and $|i_{C(\text{peak})}|$ is the peak capacitor current, which is the maximum inductor current ripple under steady-state operation.

C. EQUIVALENT PWM CONTROL AND SWITCH CONTROL

The control law (12) can be implemented directly to achieve SM control for the PSFB converter by introducing a hysteresis band, i.e., an HM based SM controller. Next, (12) is redefined as

$$u = \frac{1}{2}\left[1 + \text{sgn}(S)\right] = \begin{cases} 1, & \text{when } S(\mathbf{x}) > +\varepsilon \\ 0, & \text{when } S(\mathbf{x}) < -\varepsilon \end{cases} \tag{19}$$

where the bandwidth ε is an arbitrarily small value. With this modulation, if $S > +\varepsilon$, the diagonal switches turn on following the switching logic. Conversely, if $S < -\varepsilon$, the horizontal switches turn on following the switching logic. In the region $+\varepsilon > S > +\varepsilon$, the switches remain in their previous state. Thus, by introducing a region where no switching occurs, the maximum switching frequency under SM control is limited. Although the hysteresis band with the boundary condition provides a form of control to the switching frequency, it cannot fix the frequency, which leads to difficulties in both designing the converter and in selecting the components.

To achieve a fixed switching frequency, the SM control signal u is converted to the equivalent PWM signal, which regulates the output voltage of the converter as the duty cycle. However, if the discrete law (12) is directly converted to a continuous function, the physical significance of values of u between 0 and 1 and the process of pulse-width modulation are not clear. To solve this problem, we redesigned (12) as

$$u_T = u \cdot T = \begin{cases} T, & \text{the maximum turn-on time of } S_e \\ 0, & \text{the minimum turn-on time of } S_e \end{cases} \tag{20}$$

where T is the fixed switching period. It is obvious that the maximum turn-on time of switch S_e is T, which is equivalent to the event where switch S_e turns on. Conversely, the minimum turn-on time of switch S_e is 0, which is equivalent to the event where switch S_e turns off. Therefore, the controlling effect of (20) is equivalent to that of (12).

By substituting u_T for u in (14) and enforcing

$$\mathbf{J}(\mathbf{Ax}+\mathbf{B}u_T+\mathbf{D})=0 \tag{21}$$

solving for the equivalent PWM control function u_{eq} yields

$$\begin{aligned} u_{eq} &= -T\left[\mathbf{JB}\right]^{-1}\mathbf{J}\left[\mathbf{Ax}+\mathbf{D}\right] \\ &= T\left[\frac{v_o}{nV_i}+\frac{k_3LC}{k_2nV_i}(V_{ref}-v_o)-\frac{L}{nV_i}\left(\frac{k_1}{k_2}-\frac{1}{RC}\right)i_C\right] \end{aligned} \tag{22}$$

where u_{eq} is continuous and $0 < u_{eq} < T$. By substituting (22) into the inequality, the inequality becomes

$$0 < u_{eq} = T\left[\frac{k_3LC}{k_2nV_i}(V_{ref}-v_o)\frac{L}{nV_i}\left(\frac{k_1}{k_2}-\frac{1}{RC}\right)i_C+\frac{v_o}{nV_i}\right] < T \tag{23}$$

The physical significance of (23) is that in a constant time period T, the turn-on time of switch S_e is u_{eq}. In other words, the generation of u_{eq} is actually the pulse-width modulation. As a result, the duty cycle D_u of the equivalent PWM is

$$D_u = \frac{u_{eq}}{T} = \frac{1}{T}\left[K_a(V_{ref}-v_o)+K_bi_C+K_cv_o\right] \tag{24}$$

where $K_a = \frac{k_3LCT}{k_2nV_i}$, $K_b = -\frac{LT}{nV_i}\left(\frac{k_1}{k_2}-\frac{1}{RC}\right)$, $K_c = \frac{T}{nV_i}$.

It should be noted that (24) is similar to the PID controller, but they come from different sources. The former is obtained by employing the nonlinear control method based on the large-signal model; the latter is obtained by employing the linear control method based on the small-signal model, which cannot provide strong robustness in large-signal operations.

The equivalent function (22) can be directly used in the implementation of the proposed PWM ISM controller. In this paper, a TMS320F28335 is adopted as the digital control core. The core's counter works in the count up-and-down mode, and T is set as the value of the period register. The calculated u_{eq} is used as the count value of the phase-shifted angle, which is written to the counter compare register set, as shown in Fig. 2.

Since the actual switching frequency cannot be infinite, and the processing performed by a digital processor must be discrete, the equivalent control u_{eq} is an approximation of the original control u, which causes the SM controller to lose some of its inherent robustness against parametric disturbances. In consideration of the delay time of turning the switch on and off, the leak inductance of the transformer, and some other unmodeled dynamics, a switch control u_v is attached to the equivalent control u_{eq}, i.e.

$$\begin{cases} u_s = u_{eq}+u_v \\ u_v = T\left|x_1\right|\operatorname{sgn}(S) \end{cases} \tag{25}$$

where u_s is the integrated control function used as the eventual count value of the phase-shifted angle. The variable u_v is introduced in order to achieve robust control when the system has uncertain parameters. Owing to the robustness function $\operatorname{sgn}(S)$, strong chattering exists in the integrated control u_s. The chattering magnitude can be automatically reduced by the error $|x_1|$. As shown in (25), when the converter is entering a steady-state, both the state variable x_1 and the coefficient of $\operatorname{sgn}(S)$ approach zero, and the chattering is weakened as a result.

By substituting u for u_s in (14) and multiplying by $S(\mathbf{x})$ on the both side, we can derive

$$S(\mathbf{x})\cdot\dot{S}(\mathbf{x}) = \frac{-k_2nV_i}{LC}\left|x_1\right|\operatorname{sgn}(S)\cdot S(\mathbf{x}) \tag{26}$$

It can be demonstrated that when $S(\mathbf{x})\neq 0$, $S(\mathbf{x})\cdot\dot{S}(\mathbf{x}) < 0$ always holds, i.e., the existence condition (15) is obeyed. Hence, the integrated control function u_s can assure the stability of the system and the convergence of the trajectory on the sliding surface.

D. ROBUSTNESS ANALYSIS

The tightened condition (18) only considers the external operating conditions, such as input voltage and output load. However, the equivalent control u_{eq} contains not only the operating parameters V_i and R but also the design parameters L and C. Due to the errors of the components in production and the influence resulting from the nonlinear components in the circuit, the actual parameters of the PSFB are uncertain and vary with changing operating conditions. These uncertain parametric disturbances lead to the inaccuracy of the equivalent control u_{eq}. Therefore, this uncertainty should be considered in the SM controller's design.

Assume that L and $\hat{L}$ are the nominal value and the actual value of the inductance, respectively and that C and $\hat{C}$ are the nominal value and the actual value of the capacitance, respectively.

By making this assumption,

$$\begin{cases} \Delta L = \hat{L}-L \\ \Delta C = \hat{C}-C \end{cases} \tag{27}$$

where ΔL and ΔC are the disturbed values of the inductance and capacitance, respectively, and that

$$\begin{cases} \delta L = \Delta L/L \\ \delta C = \Delta C/C \end{cases} \tag{28}$$

where δL and δC are the error factor of the inductance and capacitance, respectively. Then, the equivalent control function (22), with the design parameters considered, can be expressed as

$$\begin{aligned} \hat{u}_{eq} = T\Bigg[&\frac{\hat{L}\hat{C}}{nV_i}\left(\frac{k_3}{k_2}-\frac{1}{\hat{L}\hat{C}}\right)(V_{ref}-v_o) \\ &-\frac{\hat{L}}{nV_i}\left(\frac{k_1}{k_2}-\frac{1}{R\hat{C}}\right)i_C+\frac{V_{ref}}{nV_i}\Bigg] \end{aligned} \tag{29}$$

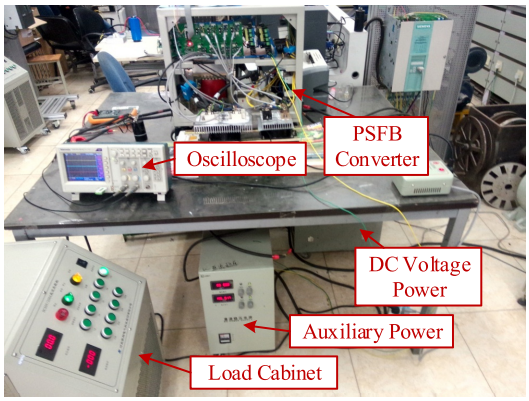

FIGURE 5. Experiment Setup.

By substituting (29) into (25) and (14), the time derivative of $S(\mathbf{x})$ can be expressed as

$$\dot{S}(\mathbf{x}) = i_C\left(\frac{\Delta L k_1}{LC} + \frac{k_2}{RC^2} - \frac{\hat{L}k_2}{LRC\hat{C}}\right) - x_1 k_3\left(\frac{\Delta L}{L} + \frac{\Delta C}{C} + \frac{\Delta L \Delta C}{LC}\right) - \frac{k_2 n V_i}{LC}|x_1|\,\mathrm{sgn}(S) \tag{30}$$

Equation (30) should obey the existence condition (15) to ensure the stability of system. Because $\Delta C << C$,

$$C\hat{C} = C(C + \Delta C) = C^2 + C\Delta C \approx C^2 \tag{31}$$

and we can simplify (30) based on (31), then

$$\dot{S}(\mathbf{x}) = i_C\left(\frac{k_1}{C} - \frac{k_2}{RC^2(1+\delta C)}\right)\delta L - x_1 k_3(\delta L + \delta C + \delta L \delta C) - \frac{k_2 n V_i}{LC}|x_1|\,\mathrm{sgn}(S) \tag{32}$$

By analyzing (32), we can observe that, in order to decrease the sensitivity of the system on the parameter L, the sliding coefficients k_1 and k_2 should satisfy

$$\frac{k_1}{C} - \frac{k_2}{RC^2(1+\delta C)} \approx 0 \tag{33}$$

In this situation, (32) can be further simplified as

$$\dot{S}(\mathbf{x}) = x_1 k_3(\delta L + \delta C + \delta L \delta C) - \frac{k_2 n V_i}{LC}|x_1|\,\mathrm{sgn}(S) \tag{34}$$

Next, according to the requirement of existence condition (15), when $S(\mathbf{x}) > 0$, $\dot{S}(\mathbf{x}) < 0$,

$$\frac{k_3}{k_2} > -\frac{nV_i}{LC(\delta L + \delta C + \delta L \delta C)} \cdot \frac{|x_1|}{x_1} \tag{35}$$

when $S(\mathbf{x}) < 0$, $(\mathbf{x}) > 0$,

$$\frac{k_3}{k_2} < \frac{nV_i}{LC(\delta L + \delta C + \delta L \delta C)} \cdot \frac{|x_1|}{x_1} \tag{36}$$

By combining (35) and (36), the robustness condition is expressed as follows

$$\frac{k_3}{k_2} < \frac{nV_i}{LC\,|\delta L + \delta C + \delta L \delta C|} \tag{37}$$

TABLE 1. Specifications of PSFB converter.

Description	Nominal value
IGBT 2MBI100VA (SEMIKRON)	I_{CE} = 100 A, V_{CSS} = 600 V
Rectifiers SKD210 (SEMIKRON)	I_D = 210 A, V_{RRM} = 600 V
Turns ratio	N_1 = 24 Ts, N_2 = 4 Ts
Inductance	L = 100 μH
Capacitance	C = 1000 μF
Input voltage	V_i = 270 V
Reference output voltage	V_{ref} = 28 V

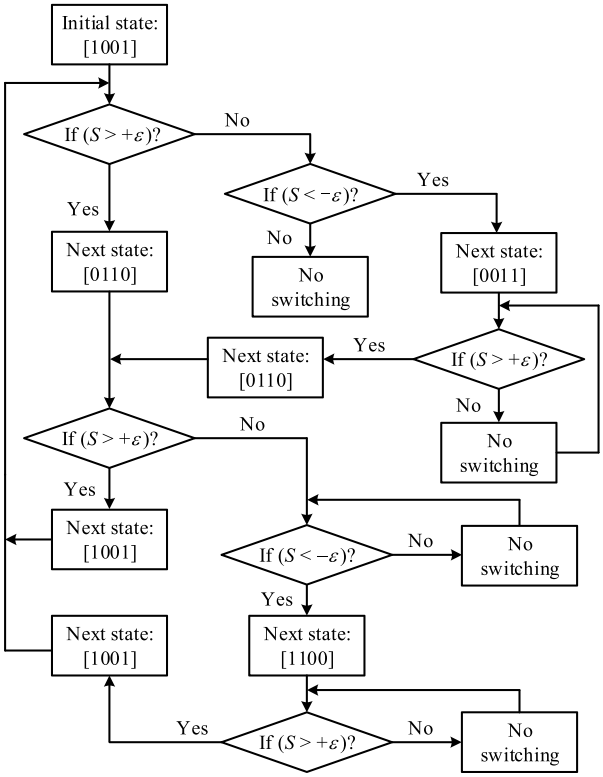

FIGURE 6. Program flow chart of HM SM control scheme with logic sequence structure for the PSFB converter.

To this point, the tightened existence condition (18) and the robustness conditions (33) and (37) form the basis for the selection of the sliding coefficients. Satisfying the above conditions assures the stability of system and its robustness against external operating condition variation and internal design parametric disturbance.

IV. EXPERIMENTAL RESULTS

A. EXPERIMENTAL SETUP

The proposed design approach and PWM ISM controller for the PSFB converter are verified through experiments. The experiment platform is shown in Fig. 5 and main parameters of the PSFB converter prototype with a rated output power P_o of 1 kW are listed in Table 1. The converter is designed to

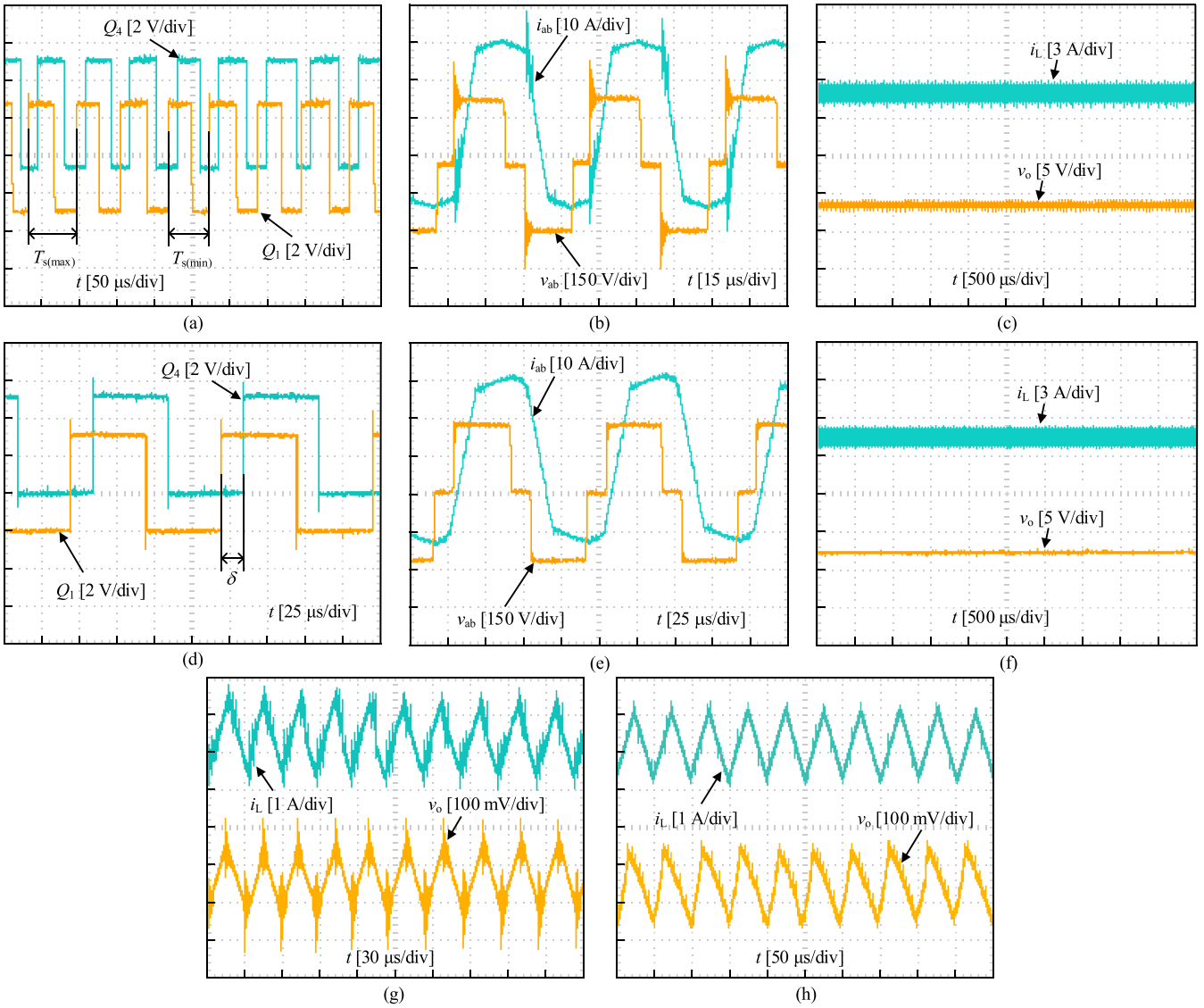

FIGURE 7. Experimental results of the PSFB converter at rated power for applying the HM SM controller and the proposed PWM ISM controller. (a) is gate pulses under HM SM control. (b) is operating waveforms in transformer under HM SM control. (c) is the inductor current i_L and capacitor voltage v_o under HM SM control. (d) is gate pulses under PWM ISM control. (e) is operating waveforms in transformer under PWM ISM control. (f) is the inductor current i_L and capacitor voltage v_o under PWM ISM control. (g) is ripples of i_L and v_o under HM SM control. (h) is ripples of i_L and v_o under PWM ISM control.

operate in continuous current mode with a maximum allowable capacitor voltage ripple factor of 0.01 and a maximum allowable inductor current ripple factor of 0.1.

According to Ackermann's Formula for designing static SM controllers [20], sliding coefficients are selected within the range determined by the conditions presented in (18), (33), and (37). To ensure the critically damped response of the system, the control parameters are selected as $K_a = 145.6$, $K_b = -0.647$ and $K_c = 9.71$.

To compare the proposed PWM ISM controller with a traditional HM SM controller, the design of an HM SM control scheme for the PSFB converter is given in Fig. 6, where the vector $[u_1u_2u_3u_4]$ denotes the control signals that are applied to the four switches of the full-bridge. As mentioned previously, the simplified control input u should keep the switching logic unchanged. Therefore, a logic sequence structure is introduced to the HM SM controller in order to restore the simplified control input to the original four-dimensional inputs.

The control system for the converter is implemented in a DSP of a TMS320F28335 with a sampling period of 50 μs. In practice, for digital implementation of HM SM control, the limit of the maximum switching frequency relates not only to the hysteresis bandwidth ε, but to the sampling frequency. In this paper, by selecting a proper ε and sampling period, the maximum switching frequency for HM SM controller is approximately 20 kHz. The fixed switching frequency for the proposed PWM ISM controller is 10 kHz.

The proposed PWM ISM controller for the PSFB is verified through experimental results and comparisons. Both a

comparison of the traditional HM SM controller with the proposed PWM ISM controller is given and the difference of the control effects between the proposed PWM ISM controller and classical increment PID are discussed.

B. STEADY-STATE PERFORMANCE

Fig. 7 shows the details of the driving signals, operating waveforms of the transformer, current ripples through inductor L, and voltage ripples across capacitor C in the PSFB converter with the HM SM controller and the proposed PWM ISM controller, where the converter is operated at the rated power.

For the HM SM controller, during steady-state operation, the period of the gate pulses, e.g., the gate signal of Q_1, fluctuates between the minimum switching time $T_{s(min)}$ and the maximum switching time $T_{s(max)}$ in Fig. 6 (a), where $T_{s(min)}$ and $T_{s(max)}$ of Q_1 are approximately 56 μs and 67 μs, respectively. In addition to this, the duty cycle of the gate pulses varies slightly, instead of maintaining a constant 50%. Due to the unfixed period and duty cycle caused by the HM SM controller, the phase-shifted modulation is not completely achieved, which prevents normal soft-switching operation and causes large spikes in the transformer, as shown in Fig. 7(b). Meanwhile, Fig. 7(c) shows strong chattering in the output waveforms caused by the sign function sgn(S). Chattering is composed of large ringing oscillations in the ripples of the current and voltage, as shown in Fig. 7(g), where the maximum peak-to-peak ripple voltage is approximately 346 mV. This value is beyond the acceptable range of voltage ripple, which requires a larger capacitor to filter.

By contrast, the proposed PWM ISM controller fixes the switching frequency of the PSFB converter, as shown in Fig. 7(d), where the switching period is fixed at 100 μs. Since the PWM ISM controller indirectly regulates the phase-shifted angle instead of directly generating the gate pulses, as opposed to the HM SM controller, the phase-shifted modulation is unchanged and the soft-switching operation is maintained. As shown in Fig. 7(e), there is no significant spike in either the current or the voltage in the transformer. Furthermore, by converting the discrete control law u into the continuous control function u_{eq}, the chattering is weakened during steady-state operation, as shown in Fig. 7(f). The voltage ripple also decreases, as shown in Fig. 7(h), where the maximum peak-to-peak ripple voltage is approximately 233 mV.

C. COMPARISON OF CHANGE IN SWITCHING FREQUENCY

Fig. 8 indicates that a change in the switching frequency occurs when the load or output power varies. For the HM SM controller, the average switching frequency is approximately 18.4 kHz at rated power of 1 kW and decreases by an average of at 1.2 kHz per 100-W reduce in the load. Conversely, the proposed PWM ISM controller fixes the switching frequency at 10 kHz naturally, since the discrete control signals are converted to the PWM duty cycle, which is solely determined by the phase-shifted angle. A fixed switching frequency

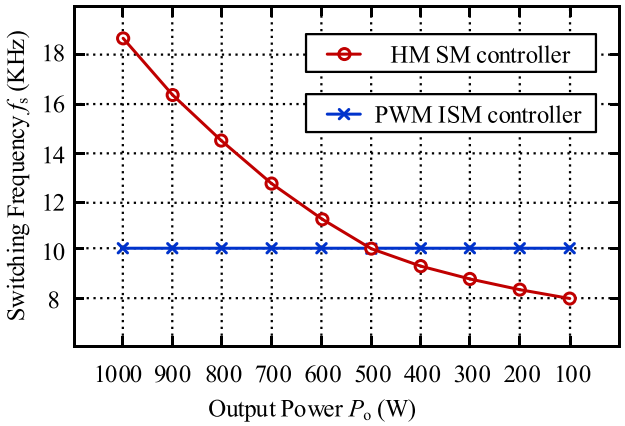

FIGURE 8. Experimental measured average switching frequency of the PSFB converter operating under load variation.

alleviates the difficulty and complexity in designing the transformer and filter for the PSFB converter, since it is inconvenient to select components based on a variable frequency.

D. DYNAMIC PERFORMANCE

The dynamic performance of the PSFB converter with the proposed PWM ISM controller and the traditional increment PID controller are compared experimentally.

First, a step change from 270 V to 330 V is applied to the input voltage. By comparing Fig. 9(a) with (d), we can see that the output voltage of the PSFB with the proposed PWM ISM controller stabilizes rapidly with less overshoot and with a smaller adjustment time than the increment PID controller.

Next, a step load change is applied on the output by alternatively switching the load between a heavy load of 33 A and a low load of 8 A. Fig. 9(b) and (e) show, respectively, the output waveforms of the converter with the classical increment PID controller and the proposed PWM ISM controller. For the increment PID controller, the voltage overshoot and adjustment time are approximately 3.87 V and 2.52 ms, respectively. Meanwhile, the dynamic response of the system is different under different operating conditions. Specifically, the lower the currents are, the more oscillatory the response is. This finding is observed because the linear controller is designed for a specific operating condition, which leads to different response behaviors when the converter is exposed to dissimilar operating conditions. In contrast, in the PWM ISM controller, the voltage overshoot and adjustment time decreased to approximately 2.91 V and 1.43 ms, respectively. Meanwhile, the output performance shows a consistent critically damped response for both increasing and decreasing loads. Therefore, the proposed PWM ISM controller endows the PSFB converter with strong robustness against the changes in its operating conditions.

E. COMPARISON OF ROBUSTNESS AGAINST PARAMETRIC VARIATIONS

To validate the robustness against parametric variations in the internal design and against unmodeled dynamics,

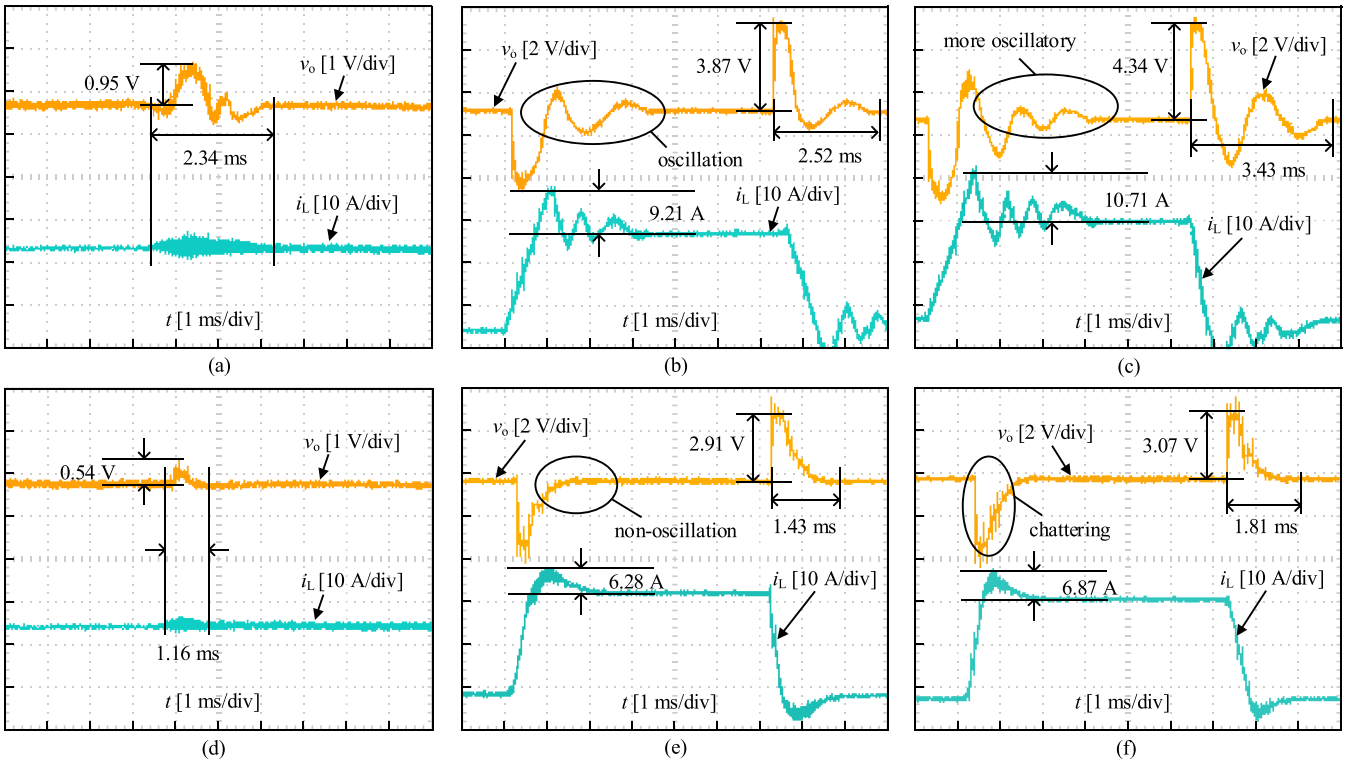

FIGURE 9. Experimental results of the PSFB converter for respectively using the proposed PWM ISM controller and the increment PID controller. (a) is step-input responses under increment PID control. (b) is step-load responses under increment PID control with scheme A. (c) is step-load responses under increment PID control with scheme B. (d) is step-input responses under PWM ISM control. (e) is step-load responses under PWM ISM control with scheme A. (f) is step-load responses under PWM ISM control with scheme B.

TABLE 2. Selection schemes of inductor and capacitor.

Description	Nominal value	Measured value	Static error
Scheme A	$L = 100\ \mu H$	$\hat{L} = 98.7\ \mu H$	$\Delta L = -1.3\ \mu H$
	$C = 1000\ \mu F$	$\hat{C} = 1030.5\ \mu F$	$\Delta C = 30.5\ \mu F$
Scheme B	$L = 100\ \mu H$	$\hat{L} = 114.4\ \mu H$	$\Delta L = 14.4\ \mu H$
	$C = 1000\ \mu F$	$\hat{C} = 1170.9\ \mu F$	$\Delta C = 170.9\ \mu F$

two schemes of selection for the inductor L and capacitor C are listed in Table 2 and compared by experimental results.

Scheme A selects a single inductor as L whose static inductance is 100 μH $\pm$ 10% and selects a single capacitor as C whose static capacitance is 1000 μF $\pm$ 10%. Scheme B selects two inductors, whose static inductances are respectively 100 μH $\pm$ 10% and 15 μH $\pm$ 10%, connected in series as L, and two capacitors, the static capacitance of which are respectively 1000 μF $\pm$ 10% and 150 μF $\pm$ 10%, connected in parallel as C. In fact, Scheme B is used to enlarge the variation of the parameters artificially.

Since the actual operating inductor and capacitor will be affected by other devices, e.g., semiconductor components, the final disturbed values ΔL and ΔC may be larger and more uncertain. The operating waveforms shown in Fig. 9(b) and (e) are measured under Scheme A. Fig. 9(c) and (f) show the measured operating waveforms under Scheme B, with all other experimental conditions unchanged. By comparing Fig. 9(b) with (c), we can see that, for the PID controller, when there is a larger variation (approximately 15% of the nominal value) of L and C, the output response becomes more oscillatory, the voltage overshoot increases by approximately 0.5 V, and the adjustment time is extended by approximately 0.9 ms. For the PWM ISM controller, the output response is basically uninfluenced by the parametric variations. This demonstrates an advantage of the proposed controller in terms of the robustness in its dynamic response with regard to parametric variations and uncertainties.

Additionally, it should be noted that there is dramatic jitter in dynamic response, which is chattering caused by the sign function sgn(S) in the switch control u_v. During the steady-state operation, the chattering is weakened. This is expected, since the error term $|x_1|$ automatically regulates the effect of u_v. When the system enters into a steady-state, the error is close to zero, and then the effect of switch control u_v is weakened, which in turn results in weaker chattering.

V. CONCLUSIONS

In this paper, a fixed frequency PWM based ISM controller for the PSFB converter has been presented. This controller

improves the robustness and output dynamic performance of the converter by introducing a nonlinear SM control method to a nonlinear switching system. The effectiveness of the PWM ISM controller is validated by experimentally comparing the proposed controller with a traditional HM SM controller and an increment PID controller.

The conclusions of this paper are as follows:

1) By simplifying the switching logic of the phase-shifted modulation, the PSFB converter is simplified to a Buck circuit. Since the four-dimensional inputs are equivalently converted into two switching states, the introduction of SM control to the PSFB converter is possible.
2) By converting the discrete control law into an equivalent PWM duty cycle that can be expressed as the phase-shifted angle, a fixed switching frequency under SM control is achieved. This solves the problem of changing switching frequencies present in the HM SM control method and enables the PSFB to maintain soft-switching operation.
3) Although the proposed controller is seemingly similar to the traditional PID controller, their sources are different. The former is derived from a nonlinear SM control method based on the large-signal model, which can provide the PSFB converter with strong robustness in the face of dynamic behavior at different operating conditions. The latter is derived from a classical linear control method based on the small-signal model. Since it is designed for a specific operating point, it cannot provide the PSFB converter with consistent output responses for all operating conditions.
4) To compensate for the loss of robustness in the face of disturbances and uncertainties, a switch control within a sign function is introduced to the control function. Meanwhile, the output chattering caused by sgn(S) is weakened automatically by the error term $|x_1|$.

Experimental results show that the output response of the PSFB converter with the proposed controller agrees with the theoretical design, i.e., that the PWM ISM controller can provide the PSFB converter with strong robustness against changing operating conditions and variations in design parameters. Furthermore, the switching frequency of PSFB under SM control is fixed.

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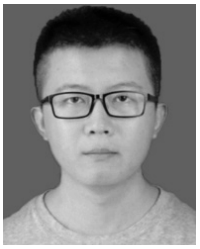

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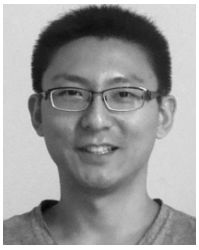

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