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A Temperature-Dependent SiC MOSFET Modeling Method Based on MATLAB/Simulink

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ABSTRACT In this paper, a modeling method based on MATLAB/Simulink for a temperature-dependent SiC MOSFET in the entire working region was proposed. Using a supplementary test circuit, the output characteristics of a device in the saturated region were extracted. Based on these characteristics, the model covered the output characteristics of the device in the whole working region. From the output curves, three main parameters essential for modeling were derived. Based on the Si lateral double-diffused MOSFET model, a temperature-dependent static model of SCT20N120 was established by adding a temperature-dependent compensation voltage source to simulate the temperature characteristics of the threshold voltage and a temperature-dependent compensation current source to compensate for the drain current error in the linear region due to the differences in structure and material between Si and SiC. In addition, based on the gate equivalent circuit, the dynamic model of the target device was established. The temperature-dependent static simulation results could simulate the actual measured values well. Furthermore, based on the comparison between the dynamic simulation results involving the device's turn-on and turn-off process losses and the actual transient state losses derived from a double-pulse test under the conditions of $V_{ds} = 300$ V, $I_d = 15$ A, $R_{g\_exton} = 18\ \Omega$, and $R_{g\_extoff} = 12\ \Omega$ at 200 °C, the maximum error was 6.7%.

INDEX TERMS SiC MOSFET, MATLAB/Simulink, whole working region, temperature-dependent model.

I. INTRODUCTION

After several decades of development, the use of Si power devices has approached the upper limit of the material characteristics. Compared with Si, SiC has the advantages of a wide bandgap, high breakdown electric field, high thermal conductivity, and high carrier saturation rate. Therefore, SiC power devices not only show a trend to replace Si power devices in the field of high-voltage and high-frequency devices, but also have high temperature reliability, a requirement which Si power devices could not fully meet in the fields of oil drilling, new energy vehicles, aerospace, and other extreme application environments.

With the large-scale commercialization of SiC power MOSFETs, domestic and foreign scholars have conducted a series of thorough studies on device modeling. Reference [1] established the SiC power MOSFET behavior model, which consisted of three fixed-value parasitic capacitances and a drain–source resistor whose value was under the control of the gate–source voltage. In order to simulate the switching process accurately, the parasitic inductors in the package were considered. The behavioral model established by [2] estimated the component losses by polynomial functions. The SPICE model proposed by [3] took into account the low-temperature characteristics of the device and the influence of the turn-off of negative voltage. Based on the Shockley transverse MOSFET model, [4] added the Forster RC network and simulated the device's self-heating properties. The model in [5] used a temperature-controlled voltage source to compensate for the temperature's influence on threshold voltage. Additionally, by using two temperature-controlled current sources in parallel with the standard MOSFET model, the influences of temperature on the carrier and avalanche effects were simulated. In [6] and [7], the Nth-power model was established to simulate the high voltage SiC power MOSFET, and the precision of the output curve was improved. The model presented in [8] divided the device's working region into three parts, calculated the voltage of each part, and analyzed the carrier drift in each part. Reference [9] established the physical model of SiC VDMOSFETs and simulated the uneven current distribution

in the JFET region by a nonlinear voltage source and resistor network. The main advantage of this model was to describe the characteristics of the device in the linear and saturated regions by a set of simple functions. In [10], a new model parameter extraction strategy was proposed. The parameters could be extracted from the device's datasheet without additional experimental testing. Reference [11] explained the low carrier mobility in the inversion layer by simulating the interface trap. Reference [12] established the 2D model by SILVACOATLAS software, which included the composite effect, bandgap narrowing, collision ionization, and lattice heating effect.

The modeling methods for SiC Power MOSFETs are mainly based on physical modeling or behavioral modeling. The former simulates the electrical characteristics and thermal behavior of the device by solving the physical equations. Its advantage is that the model has high precision, and the correlative parameters have corresponding physical meanings, whereas its disadvantage is that the model is complex, and the parameters are numerous and difficult to obtain. The latter usually adopts the method of mathematical fitting, without considering the complex physical mechanisms of the device, so the relevant model parameters have no actual physical meanings. Its advantage is that the model is simple and time-saving, while its disadvantage is that the accuracy of the simulation is low, especially when the device's operation is beyond the curve fitting conditions.

In this paper, a temperature-dependent SiC MOSFET modeling method based on MATLAB/ Simulink was proposed. It took into account the working characteristics of the device in the saturation region. By supplementary experiment, the saturation region part of the output characteristic curve, from which some essential parameters were extracted for modeling, was made available, so that the model could simulate the device's working characteristics in the whole working region. In this model, a compensation voltage source was added to simulate the temperature characteristic of the threshold voltage, and a compensation current source was attached to compensate for the material and structural differences between the lateral double-diffused Si MOSFET and the vertical double-diffused SiC MOSFET. The model belonged to the semi-physical model, which not only kept the physical meanings of most parameters, but also eliminated the dependence on some physical parameters that are difficult to obtain by data fitting, thus reducing the complexity of the model and enhancing its portability.

II. STATIC CHARACTERISTIC MEASUREMENT METHOD

The SiC MOSFET selected for modeling was SCT20N120 from ST Microelectronics. The initial measurement of the static characteristic curve adopted the test platform shown in Fig. 1. The device was placed on the heating plate, and a PT100 resistor was attached to the heating plate as a temperature reference. According to the test conditions offered by the datasheet, the temperature-dependent curves of SCT20N120's on-state resistance and threshold voltage

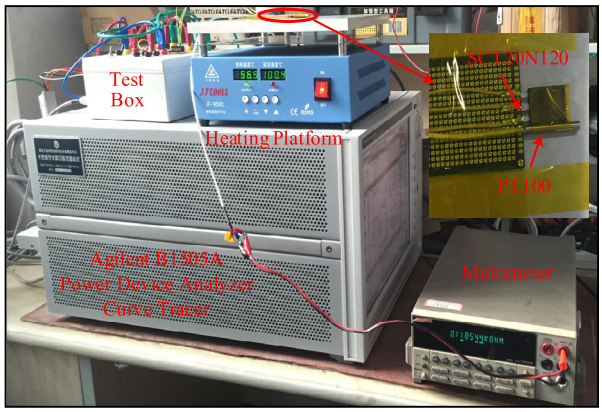


FIGURE 1. Static characteristic test platform for SiC MOSFET.

at different temperature points were measured by an Agilent B1505A power device analyzer and curve tracer.

However, due to the limitation of the measuring instrument's power and range, the whole output characteristic curve and transfer characteristic curve could not be obtained completely by the measuring instrument.

The device's working point is located in the cut-off region when it works in the off-state, whereas the device's working point is located in the linear region when it works in the on-state. In the SiC MOSFET's turn-on and turn-off processes, the working point inevitably passes through the saturation region. Although the resident time in the saturation region is very short, the voltage and current in the saturated region are high, so the loss is greater. In order to better simulate the characteristics of the device and establish an accurate model in the whole working region, the output characteristics of the device in the saturation region need to be obtained by a supplementary experiment.

The supplementary test circuit is shown in Fig. 2. To provide enough transient current, the DC power supply uses rectification circuit with a 1500-μF electrolytic capacitor pack in parallel with the output side, as shown in Fig. 3. Because the device's power dissipation is large in the saturation region, it is more appropriate to conduct the test with a single narrow drive pulse, to ensure the safety of the device.

III. STATIC MODEL ESTABLISHMENT PRINCIPLE

The static model of a SiC power MOSFET is shown in Fig. 4. The core unit is based on the traditional Si lateral double-diffused MOSFET, while the SiC power MOSFET generally uses the vertical double-diffused structure. To bridge the gap in material and structure, a compensation current source is added to compensate for the drain current I_d in the linear region, so that it can simulate the SiC power MOSFET behavior. In addition, to simulate the temperature characteristic of the threshold voltage V_{th}, a compensation voltage source is included.

A. MODELING OF MOS CORE UNIT

Without the influence of temperature, an essential analysis involving the I_d–V_{ds} relation is made for low-power

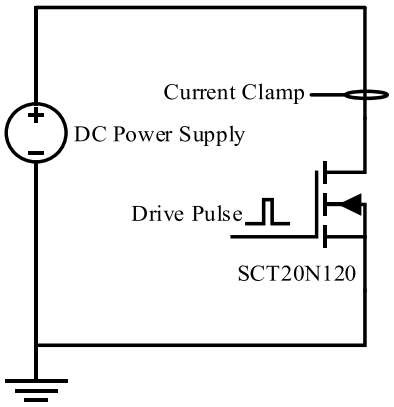


FIGURE 2. Static characteristic supplementary test circuit.

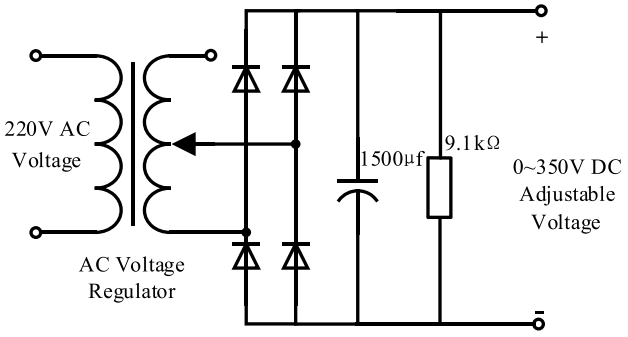


FIGURE 3. DC Power supply for supplementary test circuit.

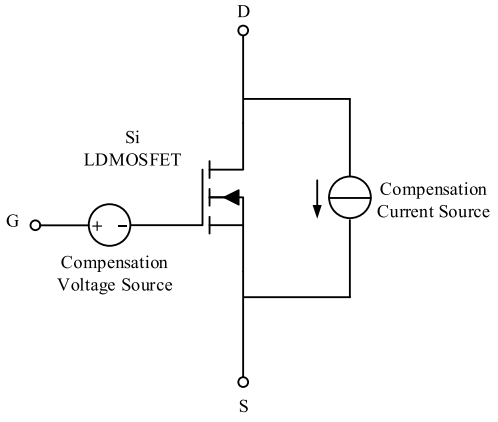


FIGURE 4. Static model of SiC MOSFET.

Si LDMOS, as shown in (1)–(3):

If $V_{gs} < V_{th}$,

$$I_d = 0. \tag{1}$$

If $V_{gs} > V_{th}$ and $0 < V_{ds} < V_{ds\_sat}$,

$$I_d = \frac{W}{L} K_p[(V_{gs} - V_{th})V_{ds} - \frac{(1+\alpha)\,V_{ds}^2}{2}]\,(1 + \lambda V_{ds}). \tag{2}$$

If $V_{gs} > V_{th}$ and $V_{ds} \geq V_{ds\_sat}$,

$$I_d = \frac{W}{2L(1+\alpha)} K_p(1 + \lambda V_{ds})(V_{gs} - V_{th})^2, \tag{3}$$

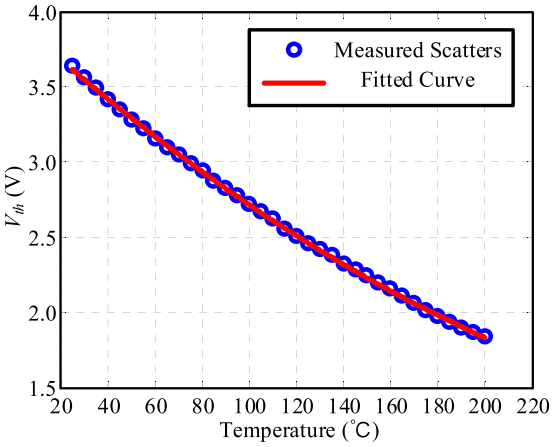


FIGURE 5. Fitting curve of threshold voltage temperature characteristic.

where W is the conducting channel's width; L is the conducting channel's length; K_p is the intrinsic transconductance parameter, where $K_p = \mu_n C_{ox}$, μ_n is the carrier mobility, and C_{ox} is the gate–oxide layer capacitance per unit area; α is the influence coefficient of the depleted layer volume charge on the saturated drain–source voltage V_{ds_sat}; λ is the channel length modulation coefficient, which indicates the influence of channel length modulation effect on drain current I_d; and V_{ds_sat} is the saturated drain–source voltage, which is the boundary point of the linear region and saturated region, expressed as

$$V_{ds\_sat} = \frac{(V_{gs} - V_{th})}{(1+\alpha)} \tag{4}$$

where V_{ds_sat} is saturated drain–source voltage, V_{gs} is gate driving voltage, and V_{th} is threshold voltage.

As the parameters involved in above equations cannot be obtained directly, it is necessary to determine these parameters, including α, K_p, and λ, before modeling.

The parameter α is the first to be determined. According to (4), it can be obtained if V_{ds_sat}, V_{gs} and V_{th} are available.

As V_{gs} has been determined in the design of the driving circuit and the ambient temperature T is known, the problem is simplified into determining the temperature-dependent function of the threshold voltage $V_{th,T}$ and the temperature-dependent function of the saturated drain–source voltage $V_{ds\_sat,T}$.

Based on the temperature characteristic scatter diagram of the threshold voltage, shown in Fig. 5, the following polynomial fitting function is used to obtain a fitted curve of $V_{th,T}$.

$$V_{th,T} = 1.784 \times 10^{-5} T^2 - 0.01417T + 3.958 \tag{5}$$

As the ambient temperature changes, $V_{ds\_sat,T}$ is no longer a single-variable function of driving voltage V_{gs}, but rather a two-variable function of V_{gs} and T.

Fig. 6 shows the saturated drain–source voltage diagrammatic curve with varying gate voltage at 25 °C, which also denotes the boundary between the linear region and saturation region, and the saturated drain–source voltage diagrammatic

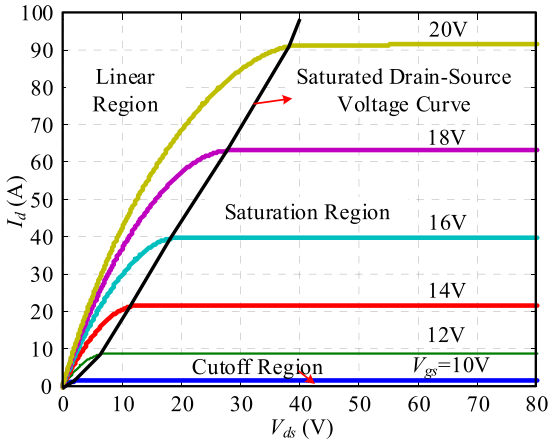


FIGURE 6. Saturated drain–source voltage curve with varying gate voltage at 25 °C.

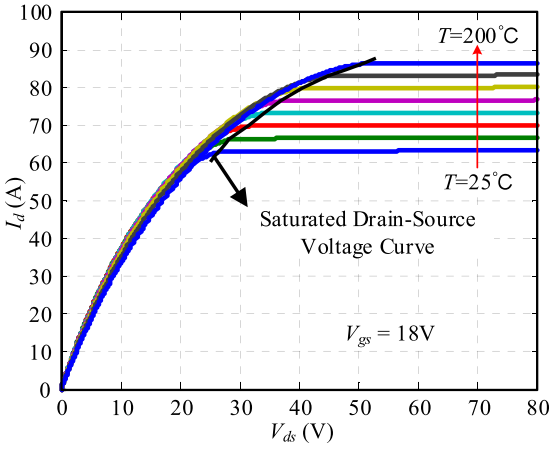


FIGURE 7. Saturated drain–source voltage curve with varying temperatures when V_{gs} = 18 V.

curve with a gate voltage of 18 V at various temperatures is shown in Fig. 7. With varying temperatures (25–200 °C) and gate voltages (10–20 V), a series of $V_{ds\_sat,T}$'s 3D scatters are extracted for fitting.

The following polynomial fitting function is used to obtain the fitted curve of $V_{ds\_sat,T}$, shown in Fig. 8.

$$V_{ds\_sat,T} = p_{00}+p_{10}T+p_{01}V_{gs}+p_{20}T^2+p_{11}TV_{gs}+p_{02}V_{gs}^2 + p_{30}T^3+p_{21}T^2V_{gs}+p_{12}TV_{gs}^2+p_{03}V_{gs}^3, \quad (6)$$

Where $p_{00} = -67.86$, $p_{10} = 0.2199$, $p_{01} = 13.43$, $p_{20} = -9.313 \times 10^{-4}$, $p_{11} = -0.02321$, $p_{02} = -0.9072$, $p_{30} = 1.737 \times 10^{-6}$, $p_{21} = 4.537 \times 10^{-5}$, $p_{12} = 8.812 \times 10^{-4}$, and $p_{03} = 0.02496$.

As T, V_{gs}, $V_{th,T}$ and $V_{ds\_sat,T}$ are available, the parameter, α, could be obtained according to (7).

$$\alpha = 1 - \frac{V_{gs} - V_{th,T}}{V_{ds\_sat,T}} \quad (7)$$

The parameter K_p is the second to be determined. Because both the conductivity channel width W and the conductivity

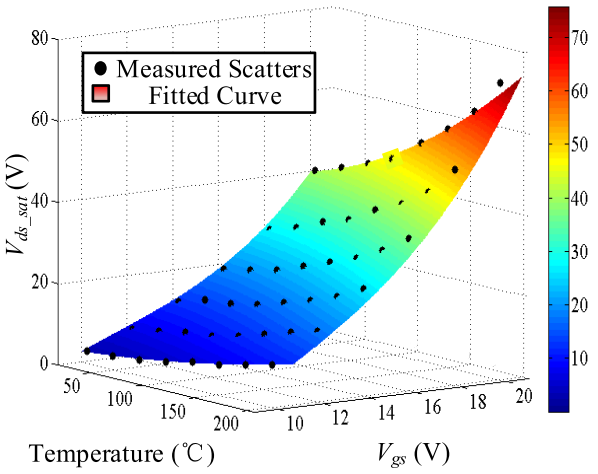


FIGURE 8. Saturated drain–source voltage fitting curve.

channel length L are constant, and W/L is a coefficient of K_p, it is not necessary to know the specific values of W and L; instead, the parameter K is introduced as the drain current scale coefficient to integrate the above three parameters, as shown in (8).

$$K = \frac{W}{L}K_p \quad (8)$$

Because the saturated drain–source voltage curve is the boundary between linear region and saturation region, the working point ($I_{d\_sat,T}$, $V_{ds\_sat,T}$) on the boundary curve also meets the static characteristic equations in linear region. Therefore, the expression of saturated current $I_{d\_sat,T}$, as shown in (9), could be derived by substituting the working point ($I_{d\_sat,T}$, $V_{ds\_sat,T}$) into (2).

$$I_{d\_sat,T} = K[(V_{gs} - V_{th,T})V_{ds\_sat,T} - \frac{(1+\alpha)V_{ds\_sat,T}^2}{2}] \times (1+\lambda V_{ds\_sat,T}) \quad (9)$$

As T, V_{gs}, $V_{th,T}$, and $V_{ds\_sat,T}$ are available, the parameter, K, could be obtained if $I_{d\_sat,T}$ is known.

The saturated drain current $I_{d\_sat,T}$ is also a two-variable function of T and V_{gs}. Similarly, the polynomial fitting function (10) is used to obtain the fitted curve shown in Fig. 9.

$$I_{ds\_sat,T} = p_{00}+p_{10}T+p_{01}V_{gs}+p_{20}T^2+p_{11}TV_{gs}+p_{02}V_{gs}^2 + p_{30}T^3+p_{21}T^2V_{gs}+p_{12}TV_{gs}^2+p_{03}V_{gs}^3, \quad (10)$$

where $p_{00} = 66.29$, $p_{10} = -0.2487$, $p_{01} = -15.19$, $p_{20} = 2.653\times10^{-4}$, $p_{11} = 0.03345$, $p_{02} = 0.9227$, $p_{30} = -7.898\times10^{-8}$, $p_{21} = -1.405 \times 10^{-5}$, $p_{12} = -6.779 \times 10^{-4}$, $p_{03} = -0.005493$.

By taking (10) into (9), the drain current scale coefficient K is (11), as shown at the bottom of the next page:

The parameter λ is the third to be determined. The channel length modulation effect makes the drain current in the saturated region increase with the rising drain–source voltage, rather than remaining constant. Thus, λ could be obtained by the output characteristic curve in the saturation region.

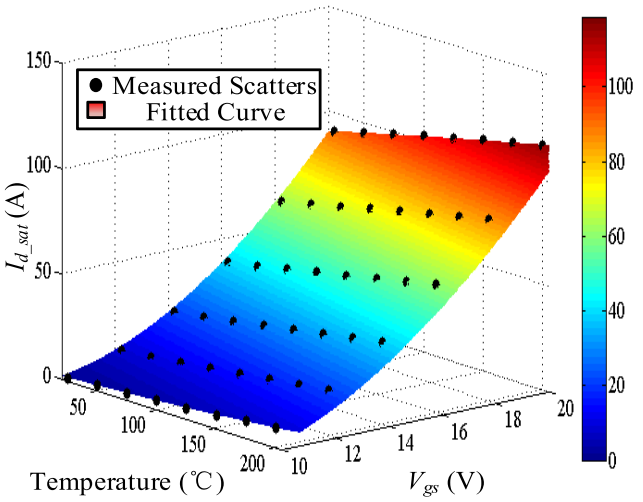


FIGURE 9. Saturated drain current fitting curve.

Define the saturation region output conductance G_{DS} as

$$G_{DS} \approx \left.\frac{dI_{d,T}}{dV_{ds,T}}\right|_{\text{saturation region}}. \tag{12}$$

The saturation-region drain current $I_{d,T}$ and the saturated drain current $I_{d\_sat,T}$ are respectively expressed as:

$$I_{d,T} = \frac{K}{2(1+\alpha)}(1+\lambda V_{ds,T})(V_{gs}-V_{th,T})^2 \tag{13}$$

$$I_{d\_sat,T} = \frac{K}{2(1+\alpha)}(V_{gs}-V_{th,T})^2. \tag{14}$$

According to (12)–(14), G_{DS} could also be expressed as:

$$G_{DS} = \lambda I_{d\_sat,T}. \tag{15}$$

As shown in Fig. 10, the geometric definition of G_{DS} in the saturation region is defined as:

$$tan\theta = G_{DS}. \tag{16}$$

A conversion is made to (15) for (17), shown as follows:

$$tan\theta = G_{DS} = \frac{I_{d\_sat,T}}{1/\lambda}. \tag{17}$$

Under the conditions of $V_{gs} = 20$ V and $T = 25$ °C, by reversely extending the output characteristic curve in the saturation region until forming an intersection with the horizontal axis, the value of λ, could be obtained according to the geometric definition of G_{DS}.

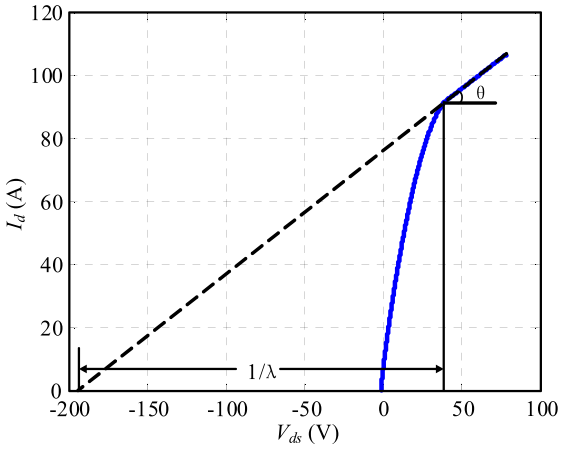


FIGURE 10. Schematic diagram of λ's geometric definition.

B. COMPENSATION FOR THRESHOLD VOLTAGE

To simulate the temperature characteristic of the threshold voltage, based on $V_{th,T}$ derived from (5), a temperature-controlled voltage source is added to the model, as shown in Fig. 4.

C. COMPENSATION FOR DRAIN CURRENT IN LINEAR REGION

The differences in the structure and working process between LDMOSFET and VDMOSFET are difficult to compensate by precise analytic functions. In addition, the difference in the materials between SiC and Si, and the immature processing technology of SiC power MOSFETs, make the compensation problem more complicated. In this paper, the mathematical method is used for compensation from the aspect of device behavior, which simplifies the problem.

Because the error mainly results from the gate–source voltage, drain–source voltage, and temperature, the following compensation function involving the above three factors is used to establish a compensation current source.

$$I_d = I_d'\left[1+\frac{(T+273)^{f(V_{gs})}}{25+273}+\frac{(T+273)^{g(V_{ds})}}{25+273}\right], \tag{18}$$

where I_d is the actual drain current in the linear region; I_d' is the mode's drain current in the linear region without compensation; $f(V_{gs})$ and $g(V_{ds})$ are the correction functions, the former of which can be obtained from the transfer characteristic curve to guarantee the fitting accuracy of the transfer characteristic and the threshold voltage, and the latter can be obtained from the output characteristic curve to ensure the fitting accuracy of the output characteristic and the conduction resistance.

$$K = \frac{I_{d\_sat,T}}{\left[(V_{gs}-V_{th,T})V_{ds\_sat,T}-0.5(1+\alpha)V_{ds\_sat,T}^2\right]\left(1+\lambda V_{ds\_sat,T}\right)} \tag{11}$$

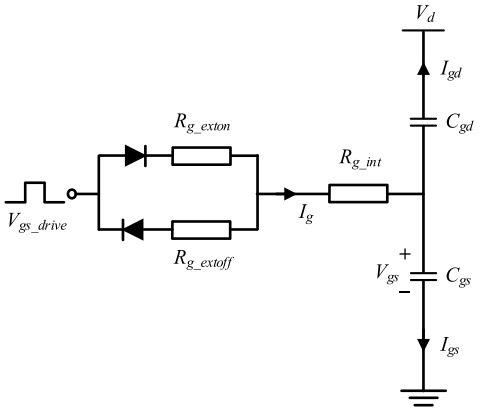


FIGURE 11. Gate equivalent circuit of SiC MOSFET.

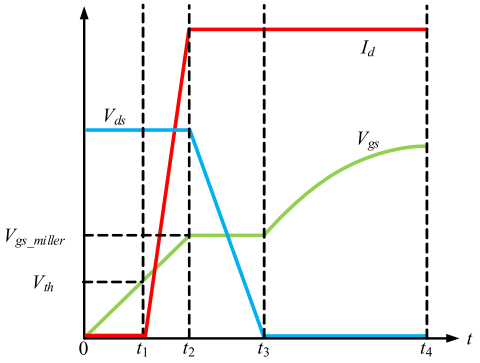


FIGURE 12. SiC MOSFET turn-on process under inductive load.

IV. DYNAMIC MODEL ESTABLISHMENT PRINCIPLE

The dynamic model of the SiC power MOSFET uses the gate equivalent circuit, as shown in Fig. 11. In the circuit, V_{gs_drive} is the gate driving voltage; R_{g_int} is the gate interior parasitic resistance; R_{g_exton} is the gate exterior turn-on resistance; R_{g_extoff} is the gate exterior turn-off resistance; Ig is the gate drive current; C_{gd} and C_{gs} respectively represent the gate–drain parasitic capacitance and the gate–source parasitic capacitance; I_{gd} and I_{gs} represent the current through C_{gd} and C_{gs}, respectively; V_d is the drain voltage; and V_{gs} is the voltage on C_{gs}.

If V_{gs_drive} is equivalent to the step excitation signal, then V_{gs} can be expressed as follows:

$$V_{gs} = V_{gs\_drive}(1 - e^{-t/\tau}) \tag{19}$$

where the time constant $\tau = (C_{gs} + C_{gd})(R_{g\_int} + R_{g\_ext})$.

The turn-on process of a SiC MOSFET with an inductive load is shown in Fig. 12.

During Period 1 (0–t_1), V_{gs} rises to V_{th} from 0 V. t_1 could be expressed as follows:

$$t_1 = (R_{g\_int} + R_{g\_exton})(C_{gs} + C_{gd}) \ln(\frac{V_{gs\_drive}}{V_{gs\_drive} - V_{th}}). \tag{20}$$

During Period 2 (t_1–t_2), V_{gs} rises to the miller platform voltage V_{gs_miller} from V_{th}, and I_d increases to the steady state value from 0 A. t_2 could be expressed as follows:

$$t_2 = (R_{g\_int} + R_{g\_exton})(C_{gs} + C_{gd}) \ln(\frac{V_{gs\_drive}}{V_{gs\_drive} - V_{gs\_miller}}) \tag{21}$$

During Period 3 (t_2–t_3), V_{gs} stays in V_{gs_miller}, and drain–source voltage V_{ds} begin falling at t_2 as the Miller capacitance C_{gd} is charged until V_{ds} reaches the on-state voltage. Here,

$$V_{gs\_miller} \approx V_{th} + \sqrt{\frac{I_d}{g_m}}, \tag{22}$$

and t_3 could be expressed as follows:

$$t_3 = \frac{(R_{g\_int} + R_{g\_exton})Q_{gd}}{(V_{gs\_drive} - V_{gs\_miller})} + t_2. \tag{23}$$

During Period 4 (t_3–t_4), V_{gs} rises to the gate drive voltage V_{gs_drive} from V_{gs_miller}. t_4 could be expressed as follows:

$$t_4 = (R_{g\_int} + R_{g\_exton})(C_{gs} + C_{gd}) + (t_3 - t_2). \tag{24}$$

The turn-off process of the SiC MOSFET with an inductive load is shown in Fig. 13. Similarly, the relevant time points are expressed as follows:

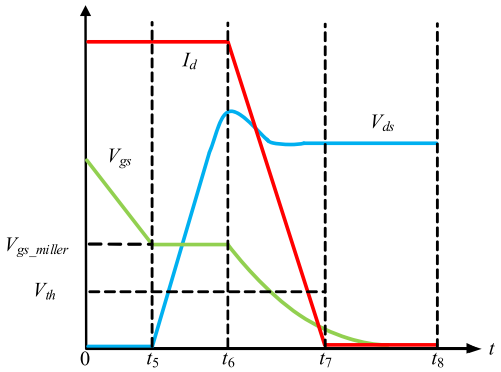


FIGURE 13. SiC MOSFET turn-off process under inductive load.

$$t_5 = (R_{g\_int} + R_{g\_extoff})(C_{gs} + C_{gd}) \ln(\frac{V_{gs\_drive}}{V_{gs\_miller}}) \tag{25}$$

$$t_6 = \frac{(R_{g\_int} + R_{g\_extoff})Q_{gd}}{V_{gs\_miller}} + t_5 \tag{26}$$

$$t_7 = (R_{g\_int} + R_{g\_extoff})(C_{gs} + C_{gd}) \ln(\frac{V_{gs\_miller}}{V_{th}}) + t_6 \tag{27}$$

$$t_8 = (R_{g\_int} + R_{g\_extoff})(C_{gs} + C_{gd}) + (t_6 - t_5). \tag{28}$$

V. SIMULATION AND EXPERIMENT ANALYSIS

In this section, the simulation results of the SiC MOSFET model are compared with the actual device's working characteristics, derived from a double-pulse test, to evaluate the accuracy of the model.

The SiC MOSFET model is shown in Fig. 14. The Mode module controls the switch between the static model and

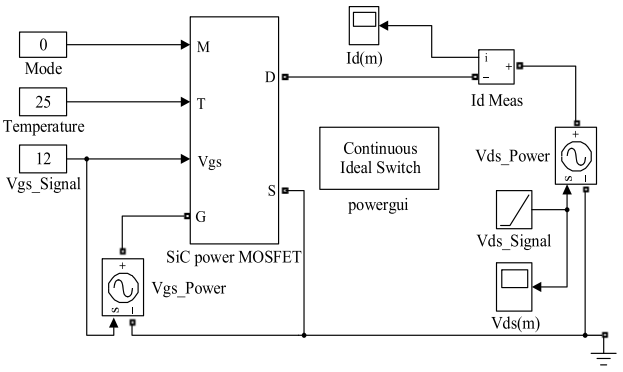


FIGURE 14. Simulink model of SiC MOSFET.

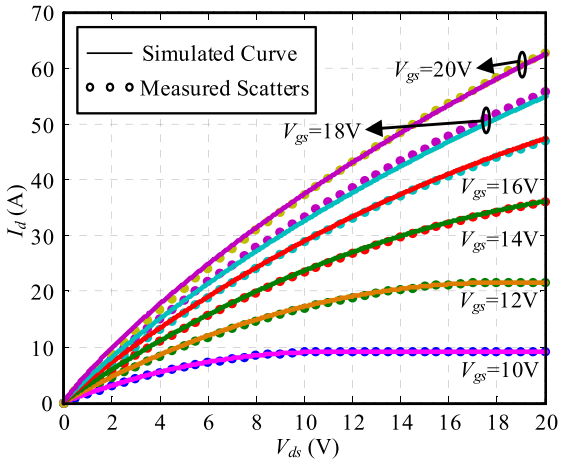


FIGURE 15. Comparison of output characteristic curves between experiment and simulation at 200 °C.

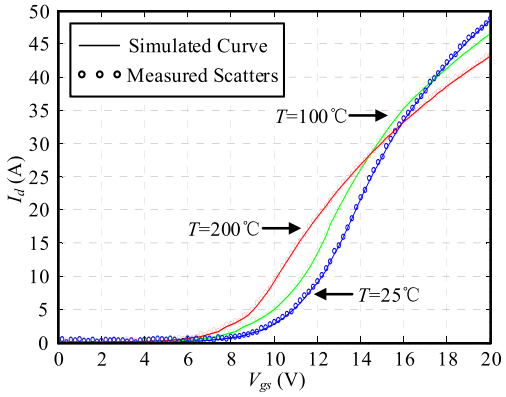


FIGURE 16. Comparison of transfer characteristic curves between experiment and simulation at 25 °C, 100 °C, and 200 °C.

the dynamic model; the Temperature module works as junction temperature adjuster; the V_{gs_signal} module generates the gate–source voltage driving signal; the V_{ds_signal} module supplies the drain–source voltage control signal; and the V_{gs_power} and V_{ds_power} modules respectively convert the control signals, V_{gs_signal} and V_{ds_signal}, to the relevant power supply.

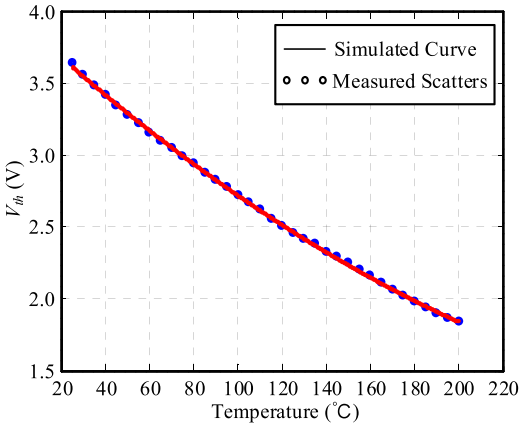


FIGURE 17. Comparison of threshold voltage temperature characteristic curves between experiment and simulation.

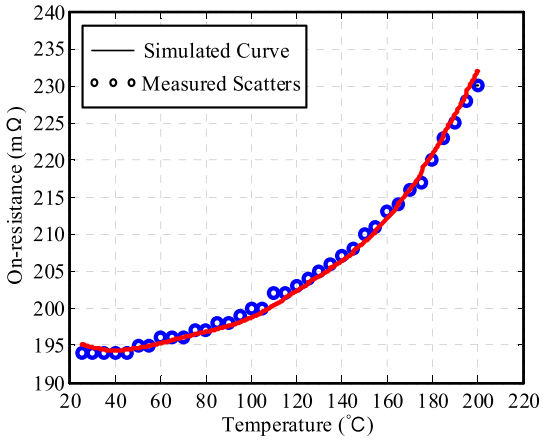


FIGURE 18. Comparison of on-resistance temperature characteristic curves between experiment and simulation.

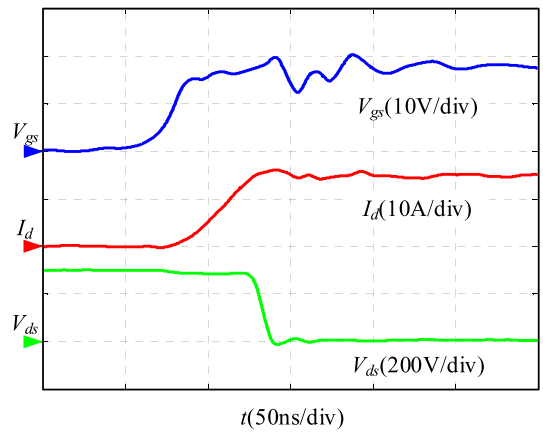


FIGURE 19. Experimental waveform of SCT20N120's turn-on process.

Fig. 15 shows the output characteristic curves of SCT20N120 model in comparison with the actual measured values at 200 °C.

Fig. 16 shows the transfer characteristic curves of the SCT20N120 model in comparison with the actual measured values at 25 °C, 100 °C, and 200 °C, respectively.

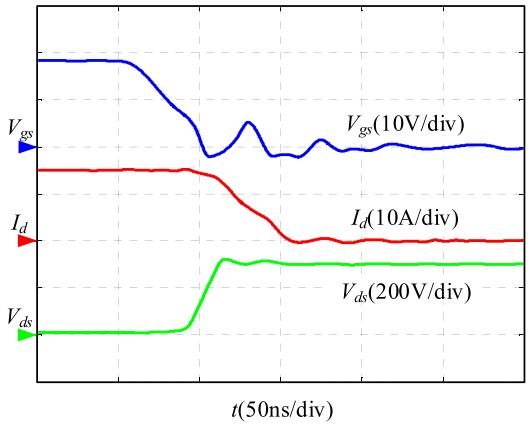


FIGURE 20. Experimental waveform of SCT20N120's turn-off process.

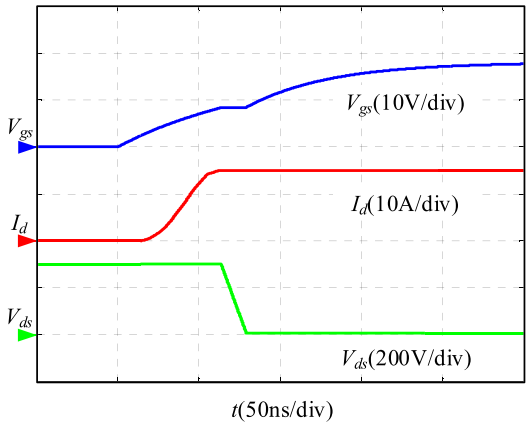


FIGURE 21. Simulation waveform of SCT20N120's turn-on process.

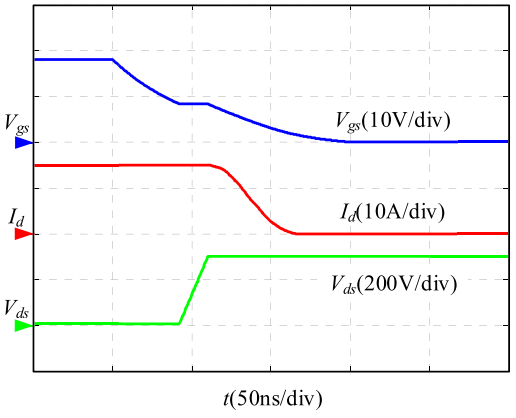


FIGURE 22. Simulation waveform of SCT20N120's turn-off process.

Fig. 17 shows the temperature characteristic curves of the SCT20N120 model's threshold voltage in comparison with the actual measured values.

Fig. 18 shows the temperature characteristic curves of the SCT20N120 model's on-resistance in comparison with the actual measured values.

Fig. 19–22 show the double-pulse experiment results of SiC MOSFET's turn-on and turn-off processes, and the

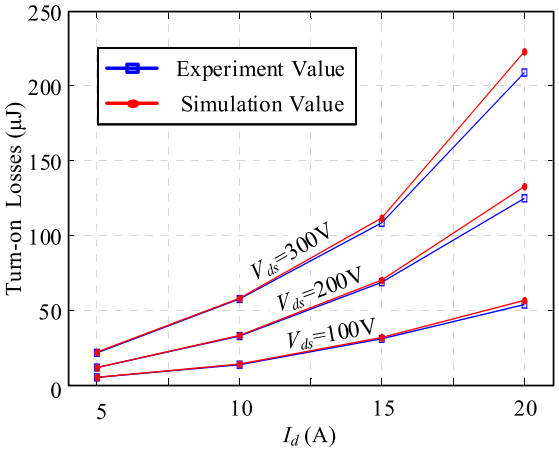


FIGURE 23. Comparison of turn-on losses between experimental results and simulation results.

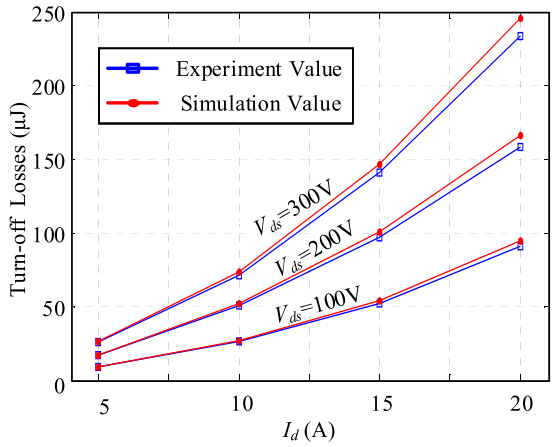


FIGURE 24. Comparison of turn-off losses between experimental results and simulation results.

simulation results of the model's turn-on and turn-off processes, respectively, under the condition that V_{ds} = 300 V, I_d = 15 A, R_{g_exton} = 18 Ω, and R_{g_extoff} = 12 Ω. The turn-on and turn-off losses of SCT20N120 are 108 μJ and 140 μJ, respectively, and the simulation results in Fig. 21–22 are 112 μJ and 146 μJ, respectively.

The comparisons of the turn-on and turn-off losses with changing V_{ds} and I_d between the experimental and simulation results are shown in Fig. 23–24. In the turn-on process, the maximum error is 6.7%, and it is 5.2% in the turn-off process.

VI. CONCLUSION

This paper proposed a modeling method based on MATLAB/Simulink for a temperature-dependent SiC MOSFET model in the whole working region.

The 1200-V, 20-A SiC MOSFET, SCT20N120 from ST Microelectronics, was selected as the target device for modeling. In order to obtain sufficient simulation precision, the output characteristics of the device in the saturated region were extracted using a supplementary test circuit, and thereby

the whole working region output characteristic curves of device were made available. From the curves, three main parameters essential for modeling were derived.

Based on the traditional Si lateral double-diffused MOSFET model, a temperature-dependent static model of SCT20N120 was established by adding a temperature-dependent compensation voltage source to simulate the temperature characteristics of threshold voltage, and a temperature-dependent compensation current source to compensate for the drain current error in the linear region due to the differences in structure and material. In addition, based on the gate equivalent circuit, a dynamic model of SCT20N120 was established.

The simulation results of the temperature-dependent static model involving the output characteristics, transfer characteristics, threshold voltage, and on-state resistance could simulate well the actual measured values. Furthermore, the simulation results of the dynamic model under the conditions of $V_{ds} = 300$ V, $I_d = 15$ A, $R_{g\_exton} = 18\ \Omega$, and $R_{g\_extoff} = 12\ \Omega$ at 200 °C indicated that the temperature-dependent dynamic model could simulate SCT20N120's turn-on and turn-off transient states losses with a maximum error of 6.7%.

REFERENCES

[1] P. Alexakis, O. Alatise, L. Ran, and P. Mawby, "Modeling power converters using hard switched silicon carbide MOSFETs and Schottky barrier diodes," in *Proc. 15th Eur. Conf. Power Electron. Appl. (EPE)*, Lille, France, 2013, pp. 1–9.

[2] A. Merkert, T. Krone, and A. Mertens, "Characterization and scalable modeling of power semiconductors for optimized design of traction inverters with Si- and SiC-devices," *IEEE Trans. Power Electron.*, vol. 29, no. 5, pp. 2238–2245, May 2014.

[3] K. Sun, H. Wu, J. Lu, Y. Xing, and L. Huang, "Improved modeling of medium voltage SiC MOSFET within wide temperature range," *IEEE Trans. Power Electron.*, vol. 29, no. 5, pp. 2229–2237, May 2014.

[4] S. Yin, T. Wang, K. J. Tseng, J. Zhao, and X. Hu, "Electro-thermal modeling of SiC power devices for circuit simulation," in *Proc. 39th Annu. Conf. IEEE Ind. Electron. Soc. (IECON)*, Nov. 2013, pp. 718–723.

[5] V. d'Alessandro *et al.*, "SPICE modeling and dynamic electrothermal simulation of SiC power MOSFETs," in *Proc. IEEE 26th Int. Symp. Power Semiconductor Devices ICs (ISPSD)*, Jun. 2014, pp. 285–288.

[6] N. Phankong, T. Funaki, and T. Hikihara, "A static and dynamic model for a silicon carbide power MOSFET," in *Proc. 13th Eur. Conf. Power Electron. Appl. (EPE)*, Sep. 2009, pp. 1–10.

[7] Y. Cui, M. Chinthavali, and L. M. Tolbert, "Temperature dependent Pspice model of silicon carbide power MOSFET," in *Proc. 27th Annu. IEEE Appl. Power Electron. Conf. Expo. (APEC)*, Feb. 2012, pp. 1698–1704.

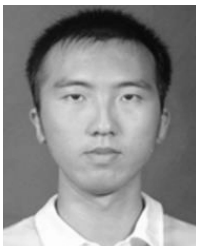
[8] M. Hasanuzzaman, S. K. Islam, L. M. Tolbert, and B. Ozpineci, "Design, modeling, testing, and spice parameter extraction of DIMOS transistor in 4 H-silicon carbide," *Int. J. High Speed Electron. Syst.*, vol. 16, no. 2, pp. 733–746, 2006.

[9] R. Fu, A. Grekov, J. Hudgins, A. Mantooth, and E. Santi, "Power SiC DMOSFET model accounting for nonuniform current distribution in JFET region," *IEEE Trans. Ind. Appl.*, vol. 48, no. 1, pp. 181–190, Jan./Feb. 2012.

[10] M. Mudholkar, S. Ahmed, M. N. Ericson, S. S. Frank, C. L. Britton, and H. A. Mantooth, "Datasheet driven silicon carbide power MOSFET model," *IEEE Trans. Power Electron.*, vol. 29, no. 5, pp. 2220–2228, May 2014.

[11] S. Potbhare, N. Goldsman, A. Lelis, J. M. McGarrity, F. B. McLean, and D. Habersat, "A physical model of high temperature 4 H-SiC MOSFETs," *IEEE Trans. Electron Devices*, vol. 55, no. 8, pp. 2029–2040, Aug. 2008.

[12] B. N. Pushpakaran, S. B. Bayne, and A. A. Ogunniyi, "Electro-thermal transient simulation of silicon carbide power MOSFET," in *Proc. 19th IEEE Pulsed Power Conf. (PPC)*, Jun. 2013, pp. 1–6.



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