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A 700MHz to 2.5GHz Cascode GaAs Power Amplifier for Multi-Band Pico-Cell Achieving 20dB Gain, 40dBm to 45dBm OIP3 and 66% Peak PAE

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ABSTRACT Recent development and technology advancement in wireless communication systems to accommodate higher data rate poses a great challenge for wideband operation. This is due to the employment of modulation scheme, such as OFDM, which is subject to high peak to average ratio. Hence communication systems, such as LTE have to operate in multiple operating bands at the moment in order to transmit the OFDM signals linearly with high gain. The power amplifier serves as the bottle neck for high gain linear operation over wide bandwidth. This paper addresses this issue and further presents a novel integrated feedback and analog pre-distortion linearization technique as a solution to achieve wideband flat gain and linear output power while preserving the power amplifier's power added efficiency (PAE). A maximally flat gain is achieved through the dual parallel feedback technique. The analog pre-distorter on the other hand introduces an optimum third order nonlinear signal components cancellation mechanism over wide frequency range. A prototype of 700 MHz to 2.5 GHz power amplifier is implemented in 0.25 μm PHEMT. It achieves an input and output return loss of less than -10 dB followed by flat power gain of 20 dB across the operating band, while sustaining an unconditional stability performance up to 20 GHz. With 1-dB compression point output power (P1dB) of 24.0 dBm, the PA delivers an OIP3 of more than 40 dBm with peak PAE of 66%. The fully integrated circuit consumes an area of 0.8 mm^2. The proposed circuit serves to be a good solution to be integrated as a part of the wideband transmitter system for picocell application.

INDEX TERMS Analog pre-distorter (APD), power amplifier, gallium–arsenide (GaAs), wideband, power added efficiency (PAE), picocell.

I. INTRODUCTION

As the demand for wide band, multi-standard and high data rate wireless systems increases, the need for power amplifier (PA) linearity and efficiency enhancement techniques have proliferated over the years [1]. The key challenge is to improve the transmit quality of the high data rate signal which is dependant to high Peak to Average Ratio (PAPR). The typical PAPR of an OFDM downlink signal is 11dB [2]. Hence the signals are often transmitted at backed off output power to preserve its quality. Reducing the backed off output power level improves the PA's efficiency and its operating bandwidth [3]. However, this has to be achieved without distorting the transmit signal.

The Doherty power amplification technique, Switch mode PAs, Chireix PAs, Envelope Elimination and Restoration (EE&R) and Envelope Tracking PAs are among the forerunners in improving the transmitter's efficiency and currently attracts great attention [4]–[8]. The Doherty PA improves the PA conversion efficiency by varying the modulation load impedance [9]. In [10], a linear Doherty power amplifier (PA) with adaptive bias circuit network for average power tracking (APT) operation is proposed where a

multi-level DC-DC converter for APT is integrated to the Doherty PA and linked with the carrier, peaking and driver amplifiers. Additionally a two-stage Doherty power amplifier (PA) with an asymmetric configuration has been designed with 0.25μm GaN SiC monolithic microwave integrated circuit technology in which two-section quarter-wave transformer was used to improve the linearity by cancelling the third order intermodulation product (IMD3) between the carrier and peaking amplifier frequency responses [11]. However, the design bottlenecks in limited bandwidth with non-flat gain across the operation band. The phase variation of the Doherty structure can be compensated using a dual-input method for the carrier and peaking amplifiers [12], but the proposed architecture is quite complex. To compensate the phase variation thus improving the linearity at reduced back off region, offset transmission line has been introduced to the peaking amplifier [13]. However the load modulation of the carrier amplifier is degraded due to the presence of low impedance to the peaking amplifier. To mitigate this, the offset line has been integrated to the carrier amplifier too [14]. The asymmetric structure also serves to be a preferred choice where varying the device sizes of the carrier and peaking amplifier are able to reduce the back-off output power [15]. Despite significant amount of work in reducing the back off output power, the performance achieved by Doherty PA is limited in terms of operating bandwidth.

On the other hand, the Envelope Tracking (ET) also promises efficiency improvement for the PA by reducing the power dissipation for systems with high PAPR. The ET modulator varies the supply voltage of the PA in accordance with the time varying envelope of the signal to keep the PA in consistent compression mode in order to achieve highest efficiency. A Dual Path Digital Pre-Distortion (DP-DPD) method is implemented in [16] to attain high efficiency. The proposed ET PA achieves overall PAE of 53% and 15.3dB gain for a 20MHz bandwidth modulated signal. However the efficiency achieved is narrowband and with lower gain. ET has also demonstrated high prospect for mobile applications since it improves the battery lifespan. Alternatively the envelope PA is integrated as a single CMOS integrated circuit but with off-chip bulky inductors [17]. However, the reported efficiency is still low as compared to GaAs technology. This is due to the low breakdown voltage of the CMOS transistor itself. Despite the low breakdown voltage, a fully integrated Class-J CMOS power amplifier with stacked-FET structure is developed and discussed in [18]. The influence of knee voltage is carefully considered in the analysis of second-harmonic losses in order to improve the broadband efficiency. The reported PA exhibits power-added efficiency (PAE) of 43.7% with a saturated output power of 22 dBm from 2.1 GHz to 4.8 GHz achieving a maximum gain of 17.4dB. However, the proposed design is highly sensitive to output matching hence unable to achieve a wide flat gain response with high linearity concurrently.

Recently, Analog Pre-Distortion (APD) is gaining significant attention as a suitable technique to improve the linearity of PAs by performing the pre-distortion at low power in the RF passband [19]. Furthermore, analog pre-distorter method does not require the baseband information of the incoming RF input signal therefore enables compact and small form factor which is essential for wireless communications [20]. In [21], analog pre-distorter which features two sub circuits for AM-AM & AM-PM is used to linearize the Class-J PA. The proposed method enables wideband efficiency from 1.7 to 2.05 GHz with an output power of 28dBm and delivers high PAE of 56%.

However, the bandwidth is still limited for wideband and multi-standard application and requires complex circuit topology. Another approach proposed by [22] uses advanced thermal models of power transistor and pre-distorter to minimize the temperature variations which effects the linearity performance of the PA. In [23], pre-distortion technique using neural network is proposed to compensate the temperature drift in a CMOS PA.

Long term memory effect which is due to the slow drift of the PA characteristics attributed by the charge trapping and de-trapping effects has been observed in GaN based PA technology [24]. To mitigate this effect, a combination of behavioural modelling using signal processing techniques and physics based models that control the coefficients of a typical DPD model is proposed [25]. A process, voltage and temperature (PVT) compensation technique is presented in [26], where an analog pre-distorter is incorporated at the feedback network of the cascode Class E PA. This method exhibits an inverse PVT represented by an empirical baseband transistor model that tracks the AM-AM characteristic of the cascode modulated PA. The limitation of this method is that it requires an extensive predetermined data of process variations, voltage and temperature characterization to develop the empirical model.

In order to achieve flat gain, high efficiency and high linearity operations for picocell application, this work presents a new wideband Class AB cascode power amplifier architecture. It consist of a dual stage parallel feedback and a cascaded Analog Predistorter (APD) that provides flat gain and high linearity with minimum trade-off with PA's efficiency. The fabricated wideband PA covers an operating bandwidth from 700MHz to 2.5GHz with an OIP3 of more than 40dBm across the bandwidth of operation.

The outline of this paper is organized as follows. In section II, the theory of operation of the wideband cascode Class AB concept is explained which includes the Linearization technique. The design methodology is given in section III, while section IV highlights the validation results of the PA. Finally, the conclusion is drawn in section V.

II. THEORY OF OPERATION

A. FLAT BROADBAND GAIN DESIGN

In this work, the cascode topology is used as it exhibits high output impedance, benefitting the increase of small signal gain over a wider bandwidth [27]. Fig.1 illustrates a

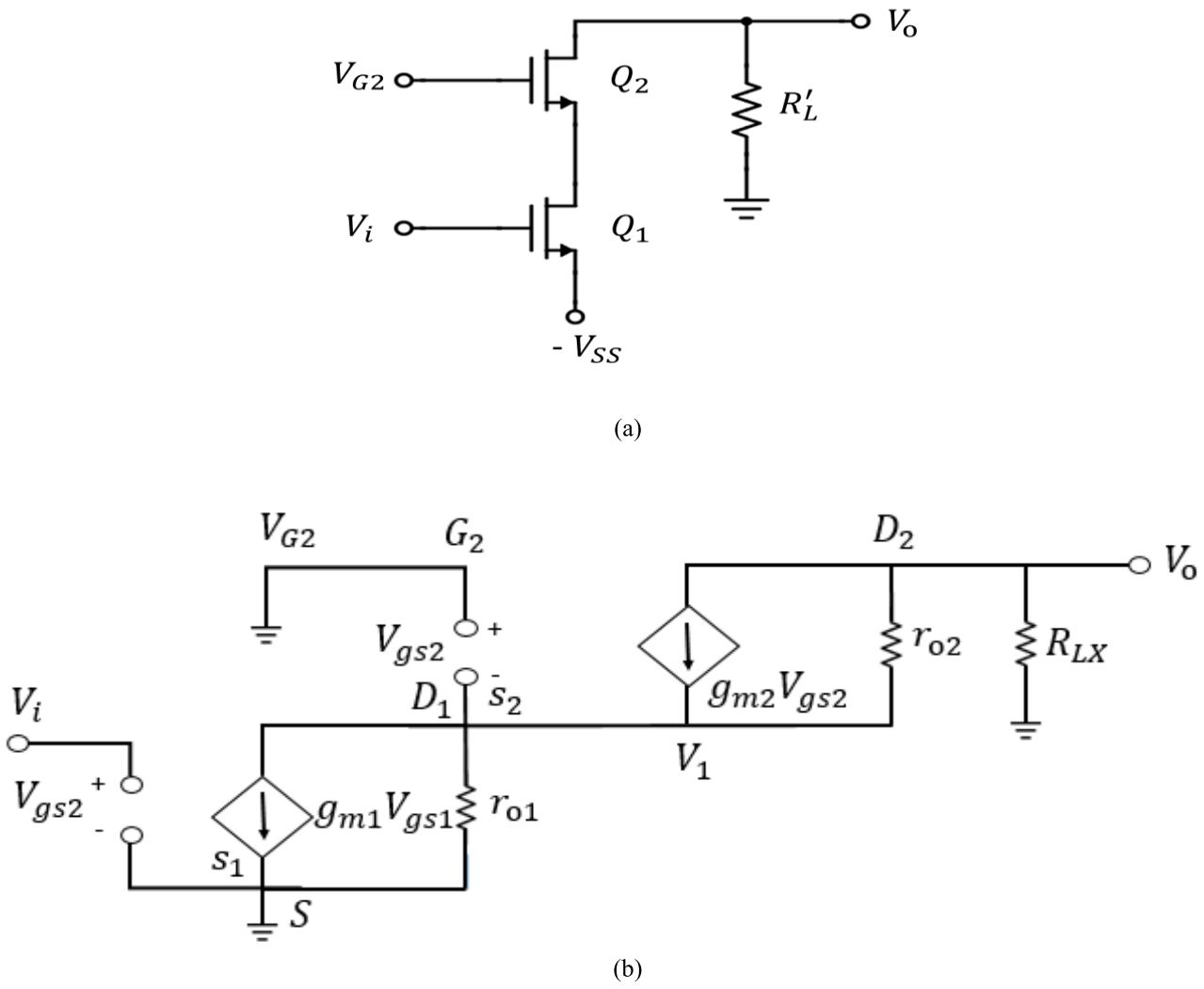

FIGURE 1. Cascode amplifier topology (a) schematic view and (b) small signal model.

typical cascode connection and its corresponding small signal model.

Referring to Fig.1 (b), the amplifier's voltage gain with load resistance R_{LX} can be expressed as follows.

At node V_o:

$$\frac{V_o - V_1}{r_{o2}} - g_{m2}V_1 = 0 \tag{1}$$

$$V_o - V_1 = (g_{m2}V_1)\, r_{o2} \tag{2}$$

$$V_o = g_{m2}V_1 r_{o2} + V_1 \tag{3}$$

$$V_o = V_1\,(1 + g_{m2}r_{o2})\,. \tag{4}$$

At node V_1:

$$\frac{V_1}{r_{o1}} + g_m V_1 + 0 = 0 \tag{5}$$

$$V_1 = -g_{m1}r_{o1}V_1 \tag{6}$$

$$\therefore\ V_o = -g_m r_{o1} V_1\,(1 + g_{m2}r_{o2}) \tag{7}$$

$$A_{Vo} = \frac{V_o}{V_i} = -g_{m1}r_{o1}\,(1 + g_{m2}r_{o2}) \tag{8}$$

$$A_{Vo} \cong -g_{m1}g_{m2}r_{o1}r_{o2} \tag{9}$$

where A_{Vo} is the open loop voltage gain. The voltage gain of the cascode amplifier is given as

$$A_V = A_{Vo} \times \frac{R_{LX} + R_o}{R_{LX}} \tag{10}$$

where R_o is the output impedance given as

$$R_o = r_{o1} + r_{o2} + g_{m2}r_{o1}r_{o2} \tag{11}$$

Hence,

$$A_V = (-g_{m1}g_{m2}r_{o1}r_{o2})\left[1 + \frac{r_{o1} + r_{o2} + g_{m2}r_{o1}r_{o2}}{R_{LX}}\right]. \tag{12}$$

Fig.2 illustrates the cascode amplifier with the dual stage shunt feedback system integrated to it and its corresponding large signal model.

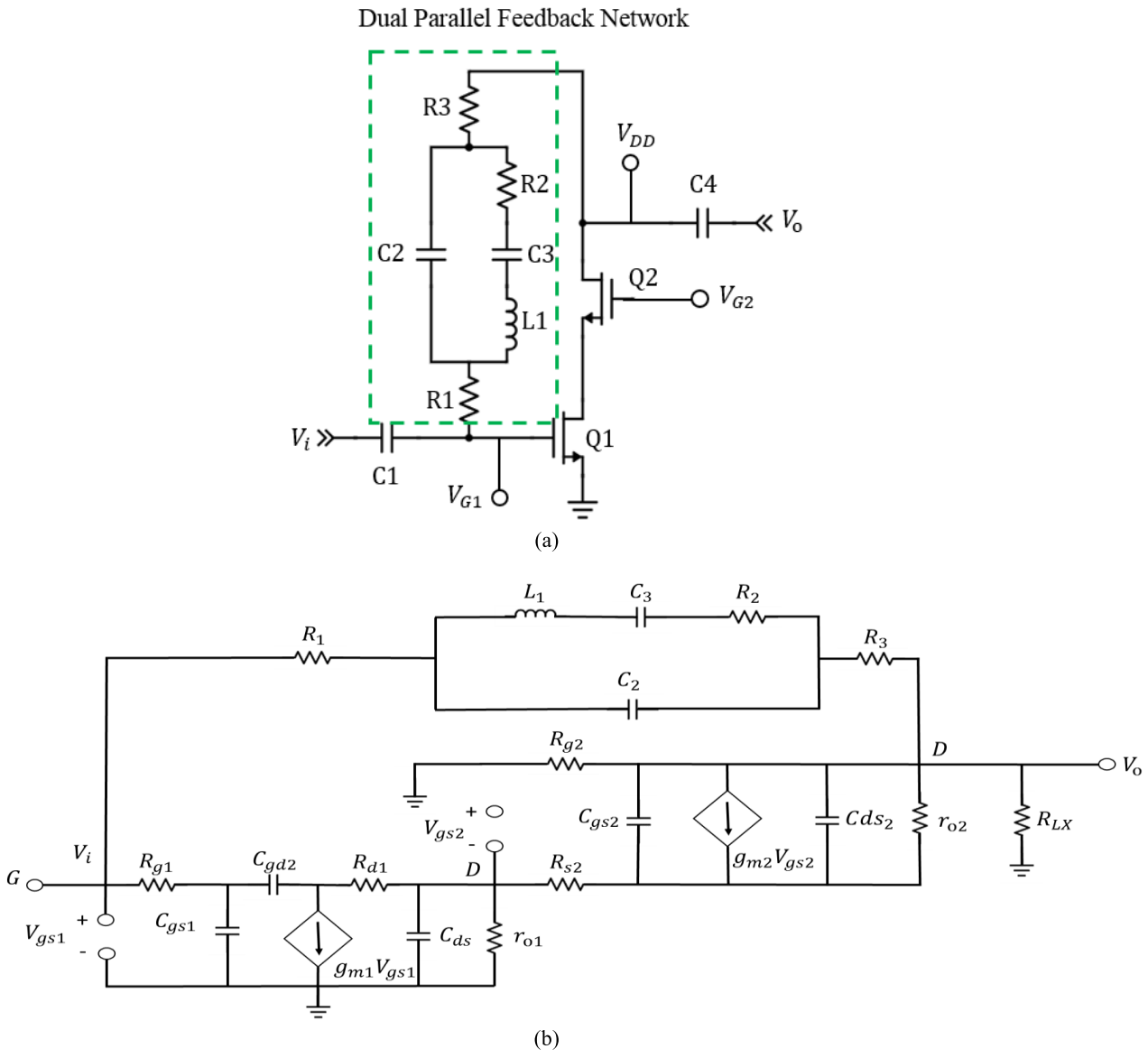

FIGURE 2. Cascode power amplifier (a) with dual stage parallel feedback network, (b) The equivalent large signal model.

The fundamental admittance matrix for a power amplifier with integrated feedback network is given as:

$$\begin{bmatrix} i_i \\ i_o \end{bmatrix} = \begin{bmatrix} \frac{1}{R_{fb2}} & \frac{-1}{R_{fb2}} \\ g_m - \frac{1}{R_{fb2}} & \frac{1}{R_{fb2}} \end{bmatrix} \begin{bmatrix} v_i \\ v_o \end{bmatrix} \tag{13}$$

where R_{fb2} denotes the parallel feedback. Using the above equations as a reference, the voltage gain A'_V of the network in Fig.2 (b) is derived as

$$A'_V = \frac{1}{M}\left(-2A_V + \frac{2R_L}{R_{fb2}}\right) \tag{14}$$

where

$$R_L = R_o // R_{LX} \tag{15}$$

and

$$M = 1 + \frac{2R_L}{R_{fb2}} + \frac{g_m R_L^2}{R_{fb2}} \tag{16}$$

of Fig.2, the feedback network R_{fb2} is derived as

$$R_{fb2} = R_3 + [(R_2 + j\omega\,(L_1 - C_3))\,//C_2] + R_1]. \tag{17}$$

Hence results

$$A'_V = \frac{1}{M}\left(-2A_V + \frac{2\,(R_o//R_{LX})}{R_3 + [(R_2 + j\omega\,(L_1 - C_3))//C_2)] + R_1}\right) \tag{18}$$

$$= \frac{1}{M}\left(-2A_V + \frac{2\left[\frac{R_L \times (r_{o1} + r_{o2} + g_{m2} r_{o1})}{R_{LX} + r_{o1} + r_{o2} + g_{m2} r_{o1} r_{o2}}\right]}{R_3 + \left[\frac{C_2(R_2 + j\omega(L_1 - C_3))}{C_2 + (R_2 + j\omega(L_1 - C_3))}\right] + R_1}\right) \tag{19}$$

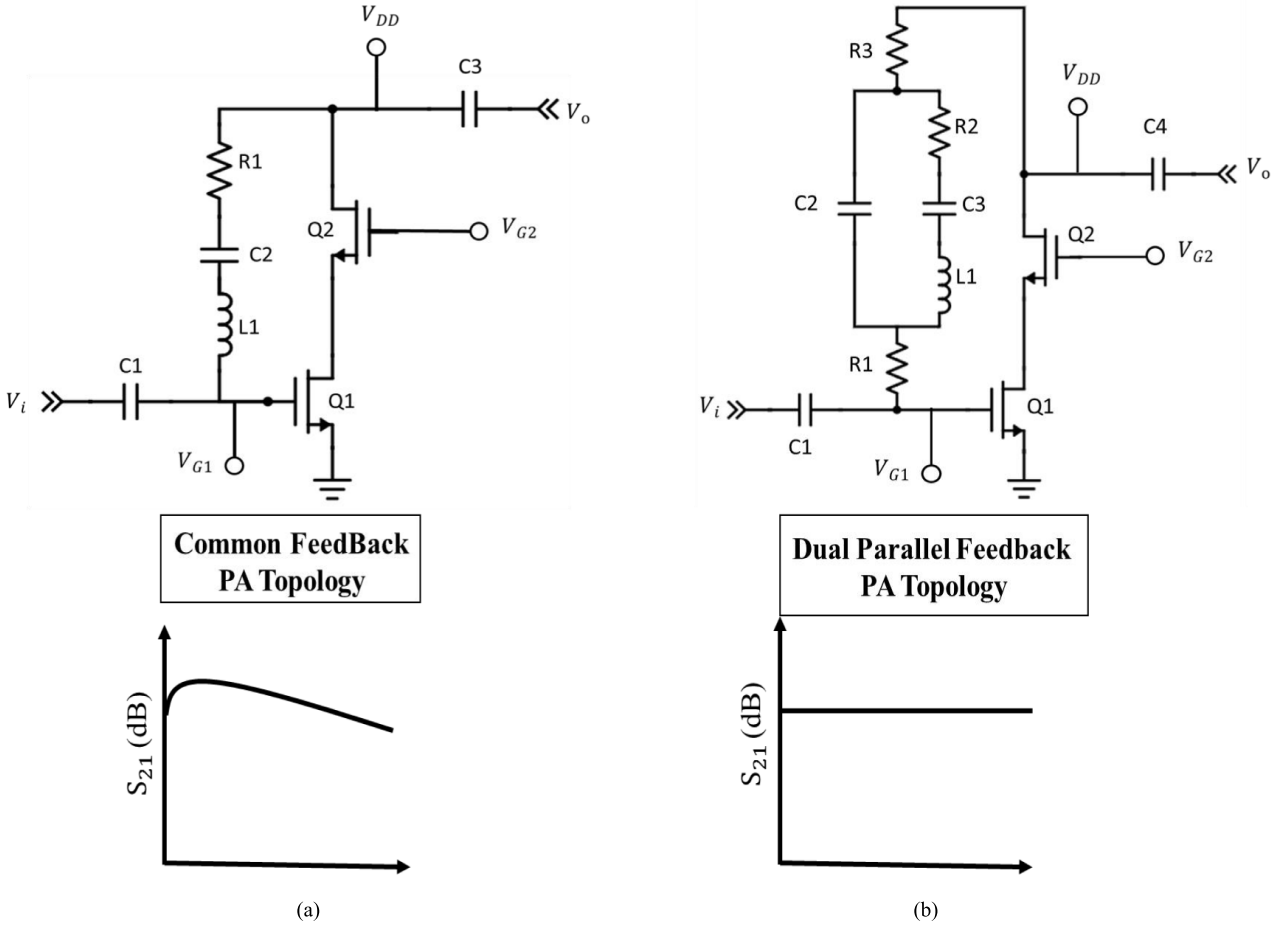

FIGURE 3. Gain vs frequency for two topologies. Wideband gain flatness is achieved with the aid of the dual stage parallel feedback network.

where M is

$$M = 1 + \frac{2\left[\frac{R_{LX}(r_{o1}+r_{o2}+g_{m2}r_{o1}r_{o2})}{R_{LX}+r_{o1}+r_{o2}+g_{m2}r_{o1}r_{o2}}\right]}{R_3+\left[\frac{C_2(R_2+j\omega(L_1-C_3))}{C_2+(R_2+j\omega(L_1-C_3))}\right]+R_1} + \frac{g_m\left[\frac{R_{LX}(r_{o1}+r_{o2}+g_{m2}r_{o1}r_{o2})}{R_{LX}+r_{o1}+r_{o2}+g_{m2}r_{o1}r_{o2}}\right]^2}{R_3+\left[\frac{C_2(R_2+j\omega(L_1-C_3))}{C_2+(R_2+j\omega(L_1-C_3))}\right]+R_1}. \quad (20)$$

The power gain is given as

$$S_{21} = A'_V\,(1+S_{11}) \quad (21)$$

where S_{11} represents the input return loss of the power amplifier. Hence in (19), the second part of the equation which is dependent to C_2 and L_1-C_3 contributes to the gain flatness extension across frequency. The corresponding gain plot (S_{21}) across frequency for a typical feedback PA topology and the dual stage parallel feedback topology is shown in Fig.3.

B. APD FOR BROADBAND LINEARITY

Signal distortion in RF power amplifiers are characterized in terms of AM-AM and AM-PM distortion. The AM-AM

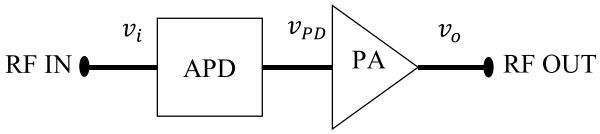

FIGURE 4. IMD3 Cancellation Analysis.

distortion is imputed to the device output resistance R_{ds}, circuit output resistance R_{out} and of non-linear capacitance C_{gs} and C_{gd}. C_{gs} and C_{gd} also contributes to AM-PM distortion [28]. The relationship between the nonlinear current characteristics generated due to C_{gs}/C_{gd} and the third order intermodulation product (IMD3) is represented by

$$IMD_G = 20\log\frac{I_{gs2\omega1-\omega2}}{I_{gs\omega1}} \quad (22)$$

$$IMD_D = 20\log\frac{I_{ds2\omega1-\omega2}}{I_{ds\omega1}} \quad (23)$$

where the $I_{gs2\omega1-\omega2}$ and $I_{ds2\omega1-\omega2}$ denotes the nonlinear current generated due to C_{gs} and C_{gd} respectively. Hence minimizing the above parasitic capacitance shall reduce the

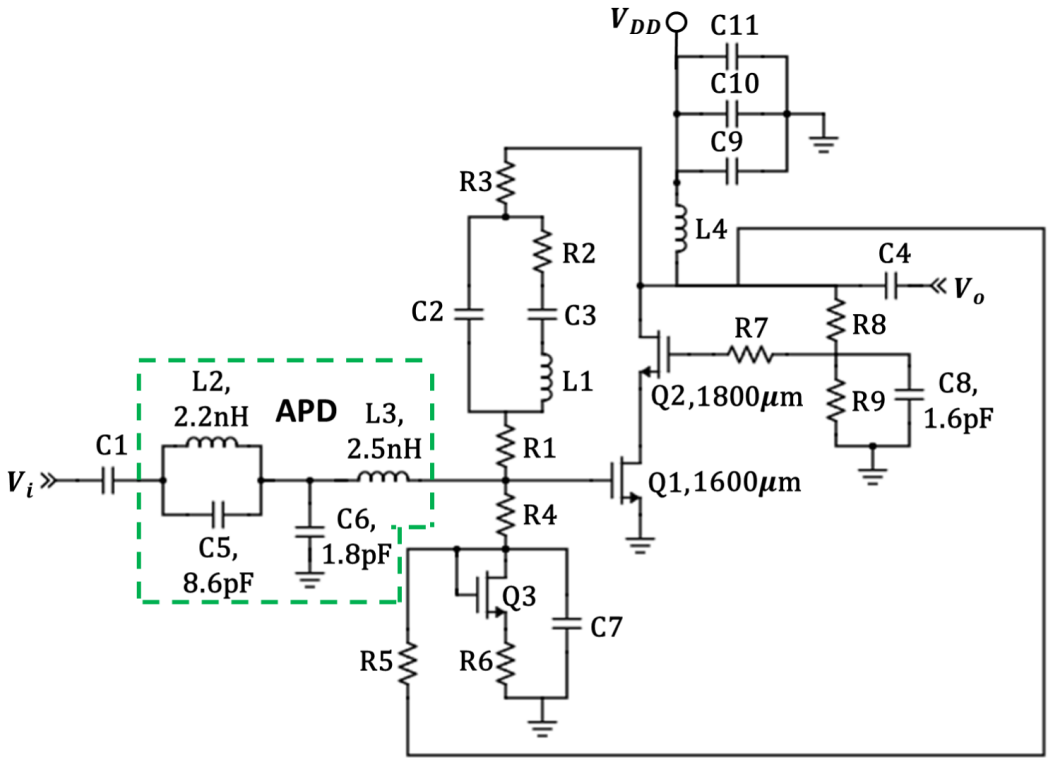

FIGURE 5. Schematic diagram of the broadband, flat gain and linear power amplifier.

third order intermodulation product thus improving PA's linearity performance. In this work, the analog predistortion linearization technique is employed to achieve this goal. Analog predistortion linearizer (APD) helps to achieve low distortion by providing opposite phase response at the RF input signal to compensate the nonlinearity of the intrinsic active device [29]. The cancellation produced by the integration of the APD to the PA generates IMD3 components which are equal in amplitude but 180° out of phase respective to each other. This operation can be explained with the aid of the following analysis utilizing the power series as shown in Fig.4.

The power series representing the configuration in Fig. 4 is given as

$$v_o = A'_{v0} + A'_{v1}v_{PD} + A'_{v2}v_{PD}^2 + A'_{v3}v_{PD}^3 + A'_{v4}v_{PD}^4 + A'_{v5}v_{PD}^5 + \ldots \quad (24)$$

$$v_{PD} = K_0 + K_1v_i + K_2v_i^2 + K_3v_i^3 + K_4v_i^4 + K_5v_i^5 + \ldots \quad (25)$$

where A'_v and K denotes the gain of the PA and APD respectively.

Taking into account the fundamental and the third order components only:

$$v_o = A'_{v1}\left[K_1v_i + K_3v_i^3\right] + A'_{v3}\left[K_1v_i + K_3v_i^3\right]^3. \quad (26)$$

Expanding (26) yields

$$v_o = A'_{v1}K_1v_i + \left[A'_{v1}K_3 + A'_3K_1^3\right]v_i^3 + A'_3K_3\left[3K_1^2v_i^5 + K_1K_3v_i^6 + 2K_1K_3v_i^7 + K_3^2v_i^8\right]. \quad (27)$$

To nullify the third order component in equation (27) which is the source of IMD3,

$$v_o = A'_{v1}K_3 + A'_{v3}K_1^3 = 0 \quad (28)$$

$$K_3 = \frac{-A'_{v3}K_1^3}{A'_{v1}}. \quad (29)$$

Equation (29) is normalized in terms of the first order linear gain, A'_{v1}/K_1^3 which leads to

$$K_3 = -A'_{v3}. \quad (30)$$

Equation (30) shows that the APD has to generate an opposite third order response component in order to achieve cancellation thus suppresses the sideband spectral regrowth. This is quantified in terms of opposite phase response generation between the APD and main amplifier across its fundamental output power [21]. Hence in this work, a phase predistorter has been integrated at the gate of the cascode power amplifier to improve its linearity performance.

III. DESIGN METHODOLOGY

Fig. 5 illustrates the schematic of the designed PA with integrated APD and dual parallel feedback network. The design

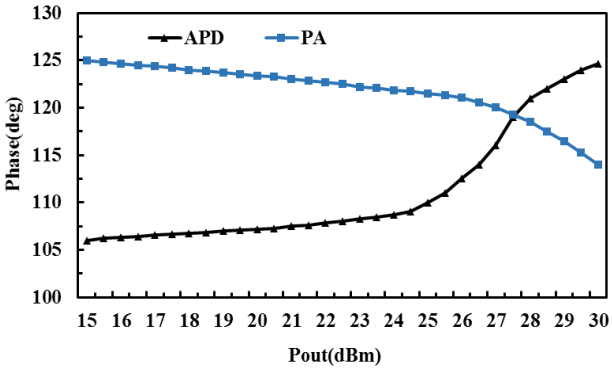

FIGURE 6. Phase response of the APD and Cascode PA.

objective of this PA is to achieve an operating bandwidth from 700MHz to 2.5GHz with corresponding power gain of more than 20dB and a quarter Watt maximum output power which corroborate for multiband LTE picocell base station application.

The cascode PA is biased for Class AB operation with a quiescent current of 40mA. The biasing point of the PA is optimized with an aid of a current mirror network in order to provide a stable biasing input to the PA. This network is represented by Q_3, R_4, R_6 and C_7 in Fig. 5. Active biasing is more robust and less sensitive to process variation of the threshold voltage (V_{th}) [30]. R_4 and R_5 forms a constant current source for Q_3.

As mention in the previous section, the APD aids in linearizing the PA via phase cancellation method in order to minimize the spectral regrowth. Referring to Fig. 5, the APD network is represented by a dual stage network which consist of parallel LC (L_2 and C_5) and series LC (L_3 and C_6) which is responsible to generate the opposite phase response to the PA. This is illustrated in Fig. 6 which depicts the phase plots of the APD and PA respectively.

As observed in Fig. 6, the APD generates a positive phase response (phase increase as output power increases) to counter the negative phase response generated by the cascode PA. The cascode PA generates negative phase response due to the dominance of its capacitance C_{gs}, whereas the APD is dominated by its inductance. C_5 and C_6 are needed in order to reduce the input reflection therefore eases system integration. The outcome of the proposed linearization techniques is quantified in terms of Amplitude-Amplitude Modulation (AM-AM) and Amplitude Modulation-Phase Modulation (AM-PM) plots as illustrated in Fig. 7. AM-AM illustrates the changes of the magnitude of the PA's power gain whereas AM-PM represents the changes of phase of the PA's power gain across output power.

In Fig. 7(a) it can be observed that the gain flatness is achieved across output power up to 24dBm followed by a phase deviation of less than 3° that verifies the linearization process. An AM-PM distortion of 5° or more is equally significant to gain compression of 1dB or more [31].

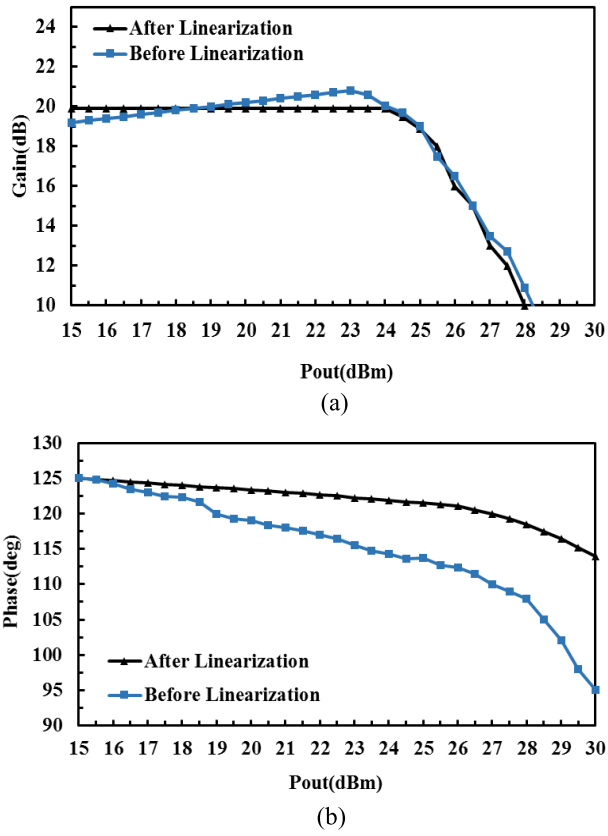

FIGURE 7. Simulated (a) AM-AM Profile and (b) AM-PM profile at center frequency of 1.5GHz.

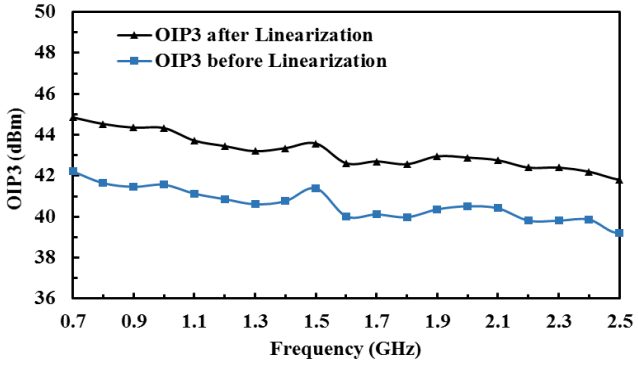

FIGURE 8. Simulated OIP3 plot comparison before and after linearization.

Fig. 8 illustrates the third order intercept point (OIP3) of the PA prior and after linearization. The OIP3 improves 2.5 dB across the operating bandwidth. This corresponds to the AM-AM and AM-PM improvement achieved in Fig. 7. Optimum IMD3 cancellation occurs at 1.5GHz, which is eminent through the OIP3 peaking.

Besides linearization and wideband operation, stability performance of the PA is another important design criteria that have been emphasized in this work. This is quantified in terms of the K-factor parameter as shown

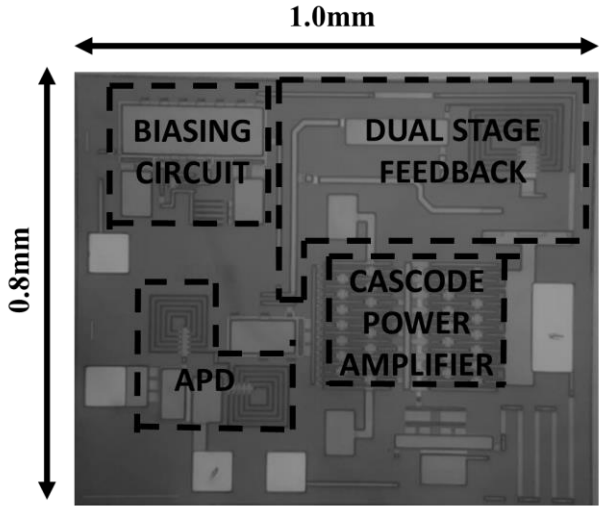

FIGURE 9. Photomicrograph of the wideband Power Amplifier with integrated APD.

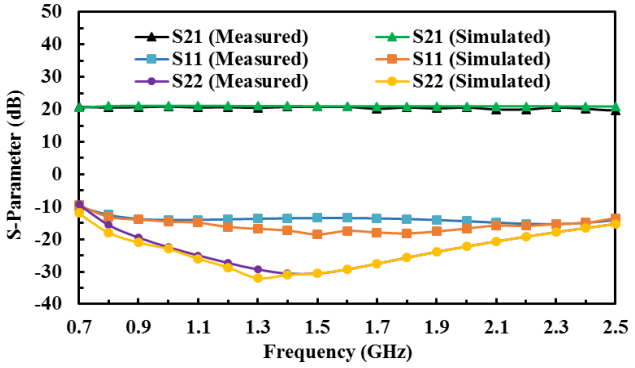

FIGURE 10. S-Parameter results of the wideband PA design. Flat gain of 20dB is achieved for 1.8GHz bandwidth.

in [32]

$$K = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |\Delta|^2}{2\,|S_{12}S_{21}|} \tag{31}$$

where

$$\Delta = S_{11}S_{22} - S_{12}S_{21}. \tag{32}$$

The design goal of this work is to achieve an unconditional stability, where K > 1. This is achieved by mainly ensuring $|S_{11}|$ and $|S_{22}|$ is less than 1 across the frequency. The proposed architecture observes unconditional stability up to 20GHz.

IV. MEASUREMENT RESULTS

The fully integrated wideband power amplifier circuit is fabricated with $0.25\mu m$ PHEMT technology occupying a die area of 0.8mm^2. Fig. 9 illustrates the photomicrograph of the chip.

The simulated and measured small-signal S-parameter performance of the wideband PA is illustrated in Fig. 10. The

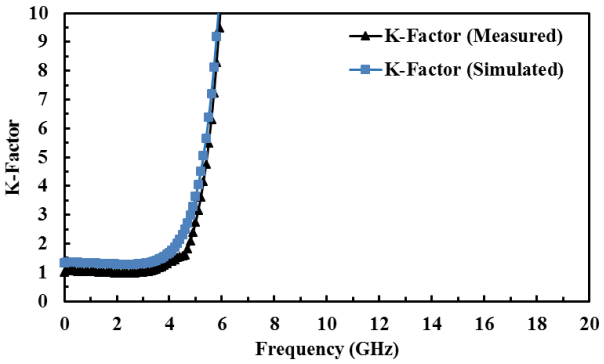

FIGURE 11. Simulated and measured stability of the wideband PA.

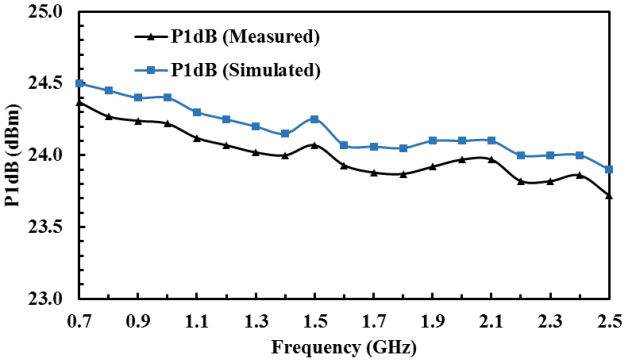

FIGURE 12. Simulated and measured P1dB of the wideband PA.

drain supply voltage of the PA is 5V and it is biased at class-AB. It can be observed in Figure 10 that there is a good correlation between the simulated and measured results from 700MHz up to 2.5GHz. The S_{11} and S_{22} of less than −10dB indicates that the PA exhibits low mismatch loss across the desired operating bandwidth. This low mismatch at the input and output is attributed by the proposed feedback network integrated to the input matching network. The feedback network also contributes to PA's maximally flat gain of 20dB from 700MHz to 2.5GHz.

Despite high gain operation, yet the PA exhibits unconditionally stable characteristics from DC up to 20GHz as depicted in Fig. 11. This is represented by the value of K factor higher than 1. The stability beyond 10GHz is contributed by the secondary feedback network represented by capacitor C_2 in Fig. 5.

The 1-dB compression output power (P1dB) across the operating frequency is plotted in Fig. 12. In an average, the achieved P1dB is 24dBm, with peak value of 24.5dBm at 700MHz. Fig. 13 depicts the measured AM-AM performance of the wideband PA. A gain variation of less than 1dB is achieved across the output power at 700MHz, 1.5GHz and 2.5GHz. This is achieved through the third order distortion (IMD3) cancellation mechanism introduced by the APD linearizer.

Further validation on the effectiveness of the proposed APD linearization is conducted through OIP3 measurement.

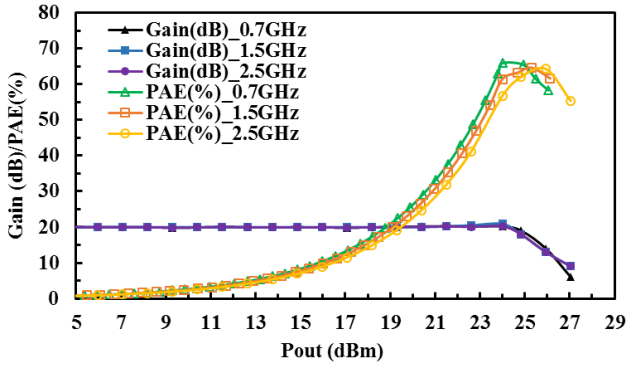

FIGURE 13. Measured AM – AM performance of the wideband PA. The maximum output power is 27dBm across the operating bandwidth.

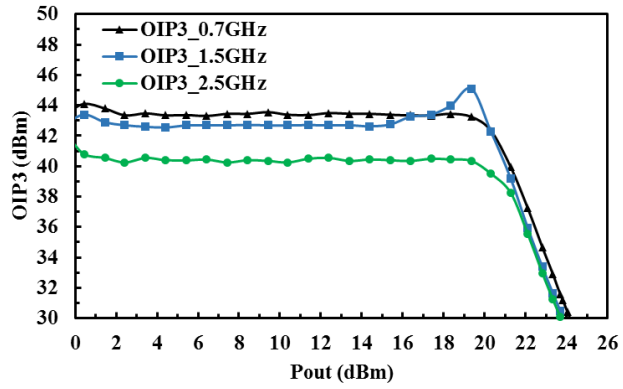

FIGURE 14. Measured OIP3 performance across output power.

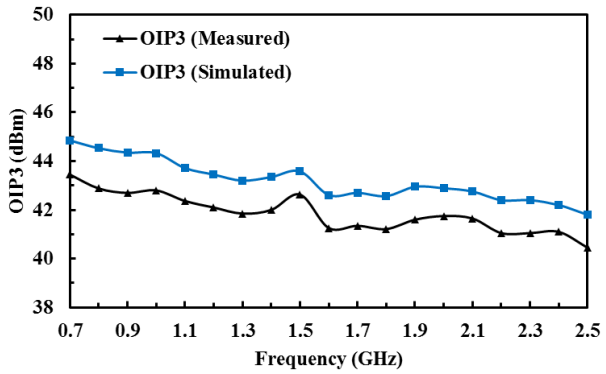

FIGURE 15. Simulated and measured OIP3 of the wideband PA across frequency at 19dBm output power.

Fig. 14 illustrates the OIP3 performance across the output power. The OIP3 was measured with two signal tones with a deviation of 1MHz. With the aid of the APD, the PA achieves more than 40dBm OIP3 across the bandwidth up to 21.5dBm at 700MHz and 1.5GHz followed by 20.5dBm at 2.5GHz. Interestingly, it can be observed in Figure 14 that the OIP3 plot for 1.5GHz peaks at 19dBm with a corresponding value of 45dBm. At this point, an optimum IMD3 cancellation is achieved. The OIP3 plot across the operating frequency at output power of 19dBm is illustrated in Fig. 15. These plot

TABLE 1. Performance summary of the proposed wideband PA.

Parameters	Results
Technology	0.25 µm GaAs E-pHEMT
Die Size	800 µm × 1000 µm
Supply Voltage	5.0 V
Class	AB
Frequency	700MHz to 2.5 GHz
Gain	20 dB ± 0.5 dB
S_{11}	< -10 dB
S_{22}	< -10 dB
Max Linear Output Power	24.5 dBm at 700MHz to 23.9 dBm at 2.5 GHz
OIP3	45 dBm
PAE	66% at 700MHz to 56% at 2.5 GHz
Stability	Unconditionally Stable up to 20 GHz

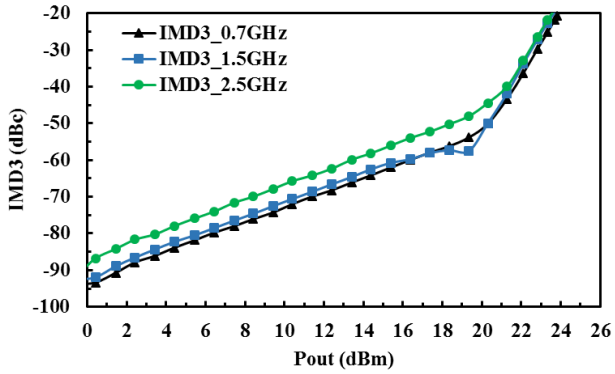

FIGURE 16. Measured IMD3 performance across output power.

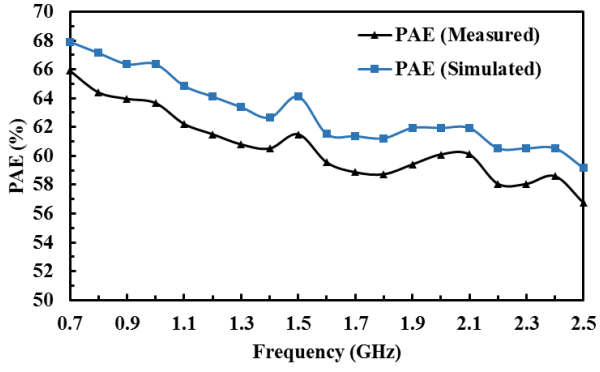

FIGURE 17. Simulated and measured PAE at P1dB of the wideband PA.

confirms the linearity at the major frequency points along the bandwidth.

Fig. 16 further validates the linearity performance of the PA across output power as indicated by the measured IMD3 results.

The corresponding PAE performance is plotted in Fig. 17. PA delivers more than 55% PAE from 700MHz to 2.5GHz

TABLE 2. Comparison with published power amplifiers.

Reference	Freq (GHz)	Vdd(V)	Idd(mA)	Gain(dB)	OIP3(dBm)	P1dB(dBm)	ACLR(dBc)	PAE%
21	1.7-2.05	3.3	-	35.8	-	28.0	-30.0	40.5 -55.8
33	0.5 – 2.0	40.0	500.0	20.0	47.0	35.0	-	15.8
34	0.7- 2.0	1.2	2.0	21.2	13.5	3.01	-	NA
35	0.2-0.6	5.0	115.0	13.0	41.4	21.8	-	26.3
36	0.1-1.0	5.0	90.0	20.2	34.2	21.8	-	33.6
37	1.85	4.0	-	14.2	-	26.5	-33.3	35.4
38	0.82-0.92	3.6	-	26.6	-	26.0	-30.2	23.0-25.3
39	1.95	3.3	-	-	-	27.0	-38.0	29.0
40	1.95	6.8	-	-	-	26.5	-38.0	42.0
41	0.88	5.0	391.0	30.0	-	25.6	-45.0	18.8
42	1.95	3.4	-	28.5	-	26.0	-32.5	26.6
43	2.4	4.2	-	16.3	-	24.3	-45.0	42.0
44	1.88	3.3	-	24.6	-	24.2	-41.0	38.6
45	1.9	3.6	-	14.0	-	23.8	-31.0	24.0
46	1.7-2.0	4.0	-	18.3	-	26.5	(-35.3) – (-37.1)	38.6 – 35.1
47	1.8-2.2	5.0	120.0	28.0-25.0	43	-	-50	46.0
This work	0.7-2.5	5.0	80.0	20.0+/-0.5	45	24.0	-	>55.0

which confirms a Class-AB operation. A PAE of more than 60% is achieved from 700MHz to 1.6GHz and 1.9GHz to 2.1GHz. The PAE also peaked at 1.5GHz which shows an optimum operation, the APD linearizer preserves the PA's efficiency.

Table 1 summarize the measured performances of the proposed wideband PA. As compared to the state of the art wideband power amplifiers published as shown in Table 2, the proposed PA exhibits a relatively high and flat gain linear performance at above 23.9dBm output power with low current consumption and excellent PAE.

V. CONCLUSION

A novel topology of fully integrated GaAs wideband linear power amplifier has been presented. Through an insightful analysis and the use of a dual stage parallel feedback network, a flat gain for 1.8GHz bandwidth is achieved. The stringent linearity specifications is met via APD linearizer without degrading the PA's efficiency. More than 40dBm OIP3 is achieved at 5dB backoff output power from the 1dB compression point. Peak OIP3 of 45dBm is achieved at 1.5GHz. The small die area of 0.8mm^2 benefits the manufacturing cost. The result highlights the potential application of the proposed PA multiband picocell transmitter where it is capable to operate linearly for wideband operation comparatively with the reported state of the art works in Table 2.

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