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The Evolution of Channelization Receiver Architecture: Principles and Design Challenges

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ABSTRACT This paper presents a broadband receiver architecture with series and parallel channelization. The proposed architecture decomposes the broadband incident spectrum into multiple channels, and achieves fast switching time, while using the single synthesizer with a fixed local oscillator (LO) frequency. Channelized receiver is a good candidate for critical RF processing tasks, such as data conversion, broadband radio, and spectrum analysis. The key feature of the proposed channelized receiver is the decomposition of the broadband frequency spectrum through parallel band partition and series channel selection. Relevant design challenges of the channelization receiver are discussed. In addition, the radio impairments determining the key performance of the radio are analyzed. The prototype receiver front-end was designed and implemented in 45 nm CMOS technology to demonstrate the effectiveness of the proposed architecture. The receiver front-end prototype splits an input spectrum of dc-40 GHz into four sub-bands with 10 GHz IF bandwidth and dissipates the average power of 33 mA and 60 mA from RF and LO blocks, respectively, while achieving <5 dB NF and <-145 dBc/Hz phase noise.

INDEX TERMS Channelization, broadband, wideband, receiver, cognitive radio, spectrum sensing, software-defined radio.

I. INTRODUCTION

Plethora of wireless communication standards exist in the radio frequency regime. The number of wireless devices will be increased rapidly in the future due to numerous wireless sensors and wearable devices. Thus, future communication devices need to operate under spectral crowding and reduced channel capacity. Under the spectrum congested environment, Cognitive Radio (CR) [1] attempts to achieve an efficient spectrum utilization and, therefore, have drawn strong attentions from the scientific community.

CR requires broadband spectrum analysis with the frequency agility. Direct time-domain sampling and digitization over a multi-GHz bandwidth is a straightforward approach denoted as Software-Defined Radio (SDR). SDR [2], [3] puts very stringent requirements on the ADC in terms of dynamic range, speed, and noise. Then, it is not a reality yet even with the state-of-the-art technologies [4].

Frequency channelization is an attractive alternative to direct time-domain sampling and digitization of the full input spectrum. Channelization receiver decomposes the broadband input signal into multiple channels. Channelized signals are subsequently digitized by multiple ADC with the relaxed requirements on the performance.

R. Gharpurey and P. Kinget [5] proposed the iterative down conversion architecture to achieve the frequency channelization and the agile spectrum analysis. T.-L. Hsieh et al. [6] utilized the iterative down conversion architecture to the Ultra Wide-Band (UWB) radio system to detect the in-band interferences acutely. In [7], 3-way iterative down conversion is presented to improve the channel-to-channel signal leakage and minimize the number of iterative down conversion under the same frequency channelization condition.

All the reported works [5]–[7] utilize the iterative down conversion as a vehicle to achieve the frequency channelization. As the number of channels to be decomposed increases, the number of iterative down conversion increases leading to worse channel-to-channel signal leakage and spurious performance. The bandwidth of the input spectrum to be analyzed is limited by the bandwidth of the low noise amplifier (LNA) and the first-stage mixer in the signal path. Without any

pre-filtering in the RF front-end, the dynamic range (DR) performance of the receiver is severely impaired by the interferences and jammers.

In this paper, we propose the channelization receiver architecture adopting series and parallel channelization. The front end of the channelization receiver decomposes the input spectrum into contiguous and equidistant sub-bands that are mapped into the same frequency spectrum. The back-end performs an iterative down conversion and completes the channelization. The proposed architecture performs the frequency decomposition in two-dimensional space and thus increases the operation bandwidth and DR of the receiver. Each sub-band can be optimized separately due to the parallel decomposition in the front-end of the channelization receiver and can provide better figure of merit than previous published methods. The bandwidth of the incident spectrum at the back-end is reduced by the number of the partition in the front-end. Doubly terminated ladder filter along with harmonic rejection mixer iteratively down-converts the signal with much less spurious and leakage signal. LO signal for each mixer is provided through on-chip frequency dividers whose first stage is injection locked to 40GHz off-chip reference source.

This paper is organized as follows. Section II reviews several channelized receiver architectures and their limitations. In Section III, the principle of the proposed channelization receiver is presented followed by the discussion of the design challenges and system impairments in Section IV. The prototype DC-40GHz receiver front-end is implemented in the mainstream CMOS technology and the simulation results of the prototype receiver front-end are provided in Section V. Concluding remarks are given in Section VI.

II. RF CHANNELIZATION RECEIVER: PRIOR WORK

A. FREQUENCY SYNTHESIZER BASED RECEIVER FOR RF CHANNELIZATION

Before exploring the properties of the prior works in the channelization receiver architecture, it is helpful to discuss why the conventional frequency synthesizer based receiver is not suitable for the broadband spectrum analysis with the frequency scanning agility.

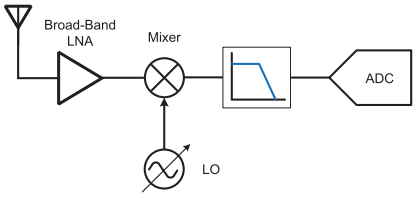

FIGURE 1. Frequency synthesizer based receiver for RF channelization: single path.

Fig. 1 shows the direct conversion receiver with the single signal path. Sequential spectrum scanning is performed with the PLL's frequency sweep. Many difficulties lie in this architecture to achieve the broadband operation with fast frequency scanning. First of all, PLL with broadband reference frequency generation is not trivial. For instance,

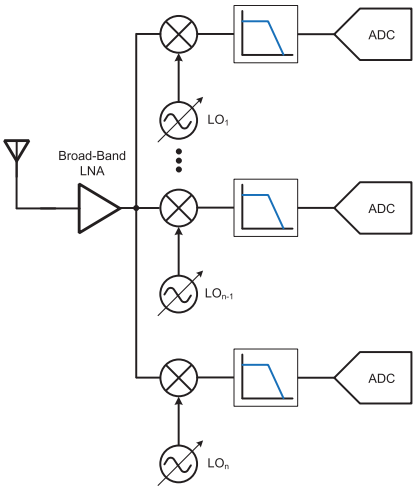

FIGURE 2. Frequency synthesizer based receiver for RF channelization: parallel path.

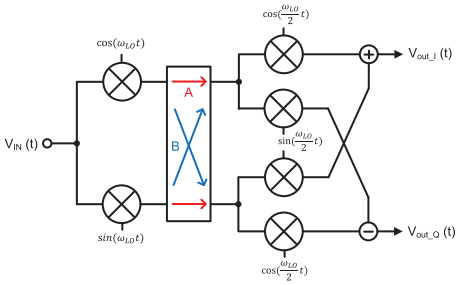

FIGURE 3. Cascaded mixer for the single-side-band frequency conversion.

the work in [8] adopts two PLLs, five single-sideband (SSB) mixers, and two multiplexers for 3.1-10.6GHz UWB radio system. Secondly, even though a single PLL can provide the broadband spectrum scanning, the hopping time between the channels limits the total scanning time. Given the number of total channel N, let the frequency hopping time and analysis time are T_{hop} and $T_{analysis}$, respectively. The total time for scanning is expressed by

$$T_{total} = N \cdot \left(T_{hop} + T_{analysis}\right). \tag{1}$$

To improve the hopping time, the bandwidth of the PLL needs to be widened but the maximum bandwidth is dictated by the Gardener's stability limit, roughly one-tenth of the PLL reference frequency [9].

Fig. 2 shows the direct conversion receiver with multiple down-conversion mixers and PLLs for the broadband spectrum scanning. The spectrum scanning time is reduced by the number of parallel paths (M). However, a large loading due to the parallel down converter lowers the bandwidth of the broadband LNA. Chip size grows linearly as the number of parallel path is increased. Moreover, multiple PLLs on the same chip incur spurious coupling leading to unwanted spurs.

B. ITERATIVE DOWN CONVERTER FOR RF CHANNELIZATION

Channelization receiver [5]–[7], [10] based on the iterative down conversion solves the aforementioned problems

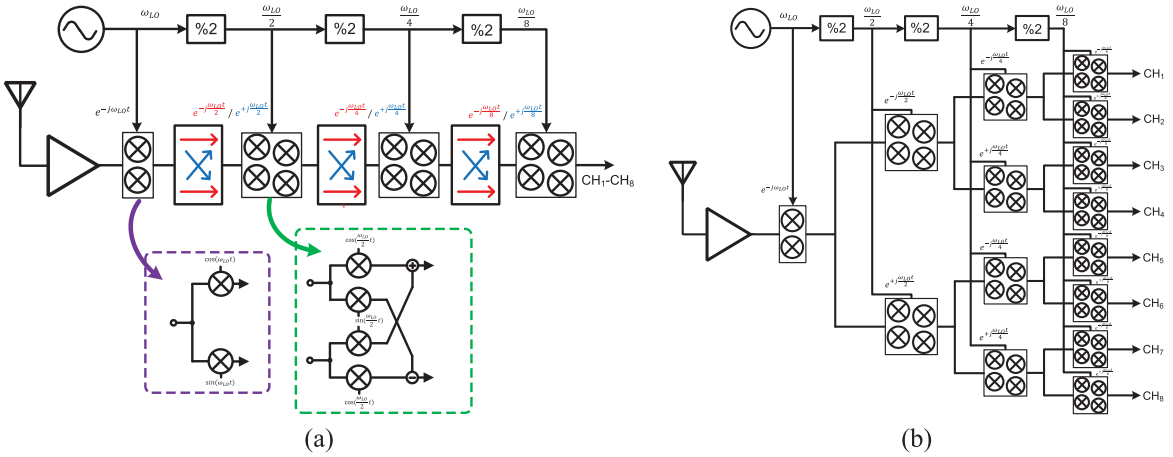

FIGURE 4. (a) Block diagram of the sequential channelizer and (b) block diagram of the concurrent channelizer [5].

with the frequency synthesizer based receiver. Channelization through iterative down conversion is best illustrated with the cascaded mixing stage shown in Fig. 3. First mixing stage is the I/Q mixer used as a simple down-converter. Subsequent mixing stage is the complex I/Q mixer (or double quadrature mixer). Inter-stage switch is utilized to determine the polarity of the complex mixing stage. For the direct path (state A), the outputs of the final stage are derived as (2), shown at the bottom of this page. With the state B in Fig. 3, the quadrature outputs are given by (3), shown at the bottom of this page.

Thus, according to the switch configuration, cascaded mixer stages generate the effective LO of $\omega_{LO} \pm \frac{\omega LO}{2}$. With N down conversion stages, the effective LO (ω_{eff}) is then

$$\omega_{eff} = \omega_{LO} \pm \frac{\omega LO}{2} \pm \frac{\omega LO}{4} \pm \cdots\cdots \pm \frac{\omega LO}{2^{N-1}}. \quad (4)$$

Through the iterative down conversion, the input spectrum is bifurcated in each stage [6]. Selection of the upper- or the lower-side-band with respect to each LO frequency is achieved by the switch configuration. The number of iterative down converter determines the channel number and its spacing ($M = 2^{N-1}$ and $BW_{channel} = \frac{BW}{M}$). The input spectrum is channelized and the entire spectrum is scanned sequentially with the proper selection of each down (up) conversion stage. The PLL only needs to operate at the single reference frequency, obviating the need for broadband reference frequency generation. Frequency divider and SSB mixer generate sub-harmonics of the reference frequency and these sub-harmonics as well as the reference frequency from the PLL is the LO signal of iterative down (up) conversion mixer. Frequency hopping time between the channels is not dictated by the loop behavior of PLL. The bifurcation process during each stage is very fast due to the open-loop switch's ON/OFF. The block diagram of the receiver in Fig. 4(a) illustrates the implementation of 8 channelization with 4 iterative down converters.

Instead of the bifurcation process due to the switch set-up, concurrent channelizer in Fig. 4(b) bisects the channels for each down convertor and unfolds them. The benefit with the approach is the concurrency due to the unfoldment of all the channels. However, the area of the channelization receiver is increased linearly in accordance with the number of channels.

3-way iterative down conversion technique proposed in [7] is based on the observation that the lower frequency spectrum does not require iterative down conversion but the low pass filtering to be channelized. Iterative down conversion for this low frequency channel is effectively moving the channel up and down and thus it is creating unnecessary spurious and signal leakages due to harmonics and image signals.

III. PROPOSED CHANNELIZATION RECEIVER

As a counterpart of CR in the military regime, Electronic Warfare (EW) receiver requires fast frequency spectrum anal-

$$\begin{aligned}
v_{out_I,down}(t) &= v_{in}(t) \cdot \left[\cos(\omega_{LO}t)\cos\left(\frac{\omega_{LO}t}{2}\right) + \sin(\omega_{LO}t)\sin\left(\frac{\omega_{LO}t}{2}\right)\right] = v_{in}(t) \cdot \cos\left(\frac{\omega_{LO}t}{2}\right). \\
v_{out_Q,down}(t) &= v_{in}(t) \cdot \left[\sin(\omega_{LO}t)\cos\left(\frac{\omega_{LO}t}{2}\right) - \cos(\omega_{LO}t)\sin\left(\frac{\omega_{LO}t}{2}\right)\right] = v_{in}(t) \cdot \sin\left(\frac{\omega_{LO}t}{2}\right). \quad (2) \\
v_{out_I,up}(t) &= v_{in}(t) \cdot \left[\sin(\omega_{LO}t)\cos\left(\frac{\omega_{LO}t}{2}\right) + \cos(\omega_{LO}t)\sin\left(\frac{\omega_{LO}t}{2}\right)\right] = v_{in}(t) \cdot \cos\left(\frac{3\omega_{LO}t}{2}\right). \\
v_{out_Q,up}(t) &= v_{in}(t) \cdot \left[\cos(\omega_{LO}t)\cos\left(\frac{\omega_{LO}t}{2}\right) - \sin(\omega_{LO}t)\sin\left(\frac{\omega_{LO}t}{2}\right)\right] = v_{in}(t) \cdot \sin\left(\frac{3\omega_{LO}t}{2}\right). \quad (3)
\end{aligned}$$

ysis with high dynamic range. In this work, we aim to develop 20MHz-40GHz broadband channelization receiver with >1GHz spectrum analysis bandwidth to support the next-generation EW receiver in order to achieve electronic intelligence gathering. The target minimum detectable signal and dynamic range for this receiver is −70dBm and 80dB, respectively. With the help of the gain control in the receiver, the entire system is predicted to operate from −70dBm to +10dBm.

The proposed channelization receiver adopts the zero-IF topology for the baseband demodulation. Frequency operation from 20MHz to 40GHz along with >1GHz spectrum analysis bandwidth dictates the number of channels to be less than 40. Then, we chose 32 channels due to binary frequency scaling of the iterative down conversion process. To perform I/Q processing, six $(\log_2(32) + 1)$ down conversions are required. The PLL only needs to operate at 40GHz and the frequency divider chain generates 20GHz to 0.625GHz in a binary fashion. With the I/Q processing at the baseband, the analysis bandwidth amounts to 1.25GHz, which satisfies the >1GHz target bandwidth.

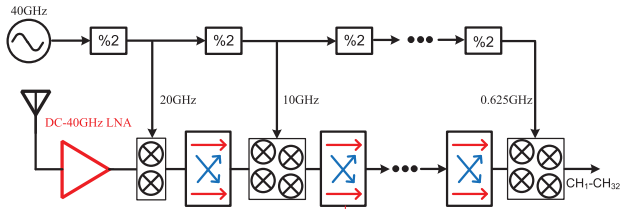

FIGURE 5. Block diagram of the sequential 40GHz bandwidth channelization receiver.

The initial system architecture based on this system requirement results in the architecture shown in Fig. 5. The bottleneck with this approach, which is identical to the sequential iterative down conversion receiver, is the necessity of the broadband and high performance front-end (LNA and first-stage mixer) for 20MHz-40GHz operation bandwidth. For the design of the LNA, distributed amplifier (DA) might be able to achieve the required bandwidth [11]–[13]. However, the implementation of the DA comes with large area and power penalty. Its noise figure (NF) is poor due to the limited quality factor of the on-chip passive devices. The dynamic range of the receiver is severely degraded due to the void of pre-filtering.

In order to overcome the aforementioned problems with the approach in Fig. 5 (similarly, Fig. 4). We propose the channelization receiver utilizing series and parallel channelization shown in Fig. 6. Series channelization refers to the iterative down conversion of the back-end, which is similar to the conventional approach. Instead of processing the broadband 20MHz-40GHz signal without any pre-filtering, coarse channelization (or band segmentation) is performed with parallel front-end signal paths. The proposed architecture performs the frequency decomposition in two-dimensional space and thus improves the dynamic range performance of the receiver. Total number of channelization (M) depends on the band segmentation (N_{band}) and the iterative down conversion (N_{idc}) as shown below.

$$M = N_{band} \cdot 2^{N_{idc}-1}. \tag{5}$$

The number of parallel front-end is determined by several requirements including the system operating condition. In this work, four band sections are adopted to fully utilize the divide-by-2 operation in the LO path. Support of 10GHz $(= \frac{BW}{N_{band}})$ operation bandwidth for each band is also reasonable from the bandwidth coverage, out-of-band interference rejection, and performance optimization perspectives.

The front-end performance is optimized for each band segmentation and thus can provide better figure of merit than DC-40GHz single-path front-end solution. Off-chip bandpass and low-pass filters provide good rejection for out-of-band blockers and relax the linearity requirements for each path's LNA and mixer. For instance, the uppermost path in Fig. 6 requires 30-40GHz operating LNA and single-stage mixer with the LO frequency of 30GHz. The down conversion mixer in this path converts the signal to DC-10GHz bandwidth that is further handled by the back-end serial channelizer.

The iterative down conversion for the back-end performs the channelization of the DC-10GHz signal after the front-end maps the decomposed input spectrum into the same frequency range. All the mixers except the first stage is the double quadrature mixer with quadrature RF and LO due to the previous mixing action and divide-by-2 flip-flops, respectively. The first stage mixer, however, has two modes of operation. For 20MHz-10GHz input spectrum, the front-end only amplifies the input signal without the down-conversion. The first stage mixer of the back-end is the first down-conversion and therefore works as an I/Q mixer with quadrature LO only. For other bands (10GHz-40GHz), the first stage mixer of the back-end performs the double quadrature mixing.

All the LO signals for each mixer are derived from the 40GHz reference signal except 30GHz LO for the 30-40GHz band. In our work, 30GHz LO is generated by the SSB mixing operation of 10GHz and 20GHz LO signals, which are available already. Alternatively, iterative down conversion with 20GHz and 10GHz LO can be utilized instead of generating 30GHz LO signal due to the double quadrature mixing. The former approach is adopted here since it does not impair the receiver's minimum detectable signal performance as long as the phase noise of the SSB mixing is sufficiently good. The latter approach, on the other hand, directly impacts the noise figure of the system since the LNA's gain is limited at this high frequency and the noise folding due to iterative down conversion severly degrades the noise figure.

IV. DESIGN CHALLENGES AND SYSTEM IMPAIRMENTS

A. MINIMUM DETECTABLE SIGNAL AND DYNAMIC RANGE

The target minimum detectable signal (MDS) and dynamic range (DR) of the broadband receiver is −70dBm and 80dB,

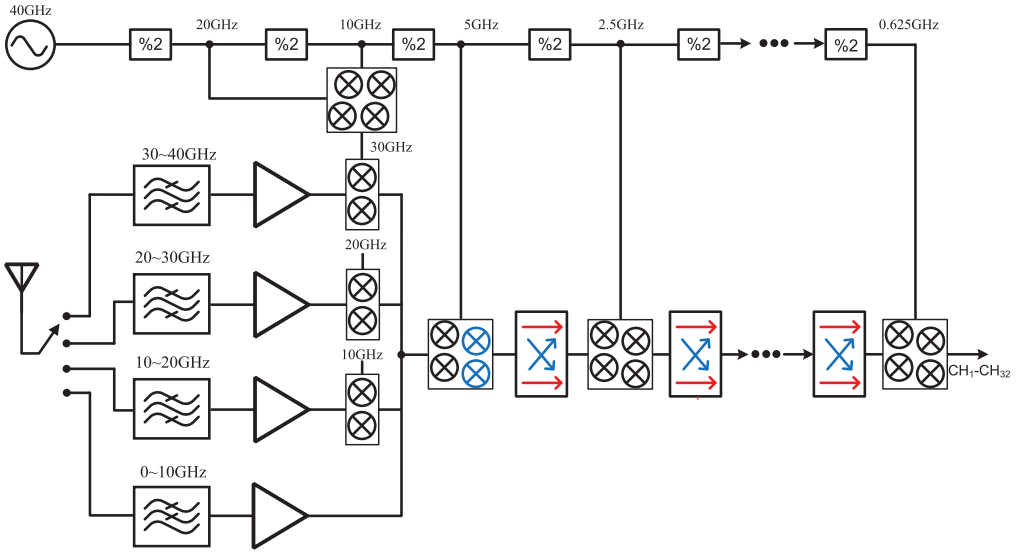

FIGURE 6. Block diagram of the proposed 40GHz bandwidth channelization receiver.

respectively. To ensure the target MDS with broadband operation, thermal noise, non-linearity, and phase noise needs to be considered together and the requirement can be stated as follows.

$$N_R + N_{rm} + P_{2nd} + P_{3rd} \leq -70dBm, \tag{6}$$

where N_R is the receiver thermal noise power, N_{rm} is the noise power due to reciprocal mixing, and P_{2nd} and P_{3rd} are the inter-modulation power due to 2_{nd}- and 3_{rd}-order non-linearity of the receiver whose noise powers due to each sources are determined based on the following relations.

$$N_R\,[dBm] = -174 + 10 \cdot \log_{10}(BW) + NF + IL, \tag{7}$$
$$N_{rm}\,[dBm] = P_{jam} + PN_R + 10 \cdot \log_{10}(BW) + IL, \tag{8}$$
$$P_{2nd}\,[dBm] = 2P_{jam} - IIP_2 + IL, \tag{9}$$
$$P_{3rd}\,[dBm] = 3P_{jam} - 2IIP_3 + IL, \tag{10}$$

where NF is the receiver noise figure, IL is the insertion loss of the font-end module, PN_R is the phase noise of the receiver, P_{jam} is the interference (jammer) power incident along with the weak desired signal, and BW is the analysis bandwidth.

80dB of DR is impractical from the receiver performance as well as the ADC performance perspective that is to digitize the channelized spectrum. For instance, weak desired signal at −70dBm along with +10dBm interferences require 50dBm of IIP_3 and 90dBm of IIP_2 in order to reduce the in-band inter-modulation power below the desired signal. The required linearity performance is not achievable even with the passive device circuits such as passive attenuator [14]. From the ADC performance perspective, minimum ENOB required is 13 bit with 1.25GSample/s. State of the art ADC in recent literature obtains approximately 9dB ENOB only with >1GSample/s sampling rate [15], [16]. Then, the receiver gain line-up needs an adjustment for different input power

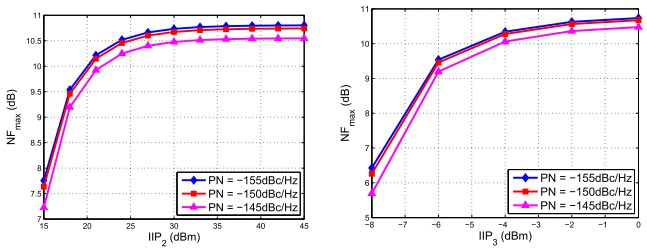

FIGURE 7. With far-out phase noise as a parameter, maximum NF allowed versus: (a) IIP_2 and (b) IIP_3 .

ranges and instantaneous DR is targeted for 40dB with the single gain line-up.

To define the target specifications with the single gain line-up, IIP_2 (& IIP_3), NF, and PN_R are calculated with (6) as a constraint. The insertion loss (IL) of the front-end module is assumed 2dB. Then, with the far-out phase noise of the receiver as a parameter, maximum allowed NF versus IIP_2 and IIP_3 are plotted in Fig. 7(a) and Fig. 7(b), respectively. In Fig. 7(a), the noise contribution due to IIP_3 is assumed negligible, and vice versa in Fig. 7(b). The allowed maximum NF becomes quickly degraded when IIP_2 and IIP_3 gets lower than 20dBm and −6dBm, respectively. It can be found also that the effect of reciprocal mixing due to the phase noise of the receiver is minimal as long as the far-out phase noise (PN_R) is lower than −145dBc/Hz. With PN_R = −145dBc/Hz, IIP_2 = 20dBm, and IIP_3 = −6dBm, the receiver NF needs to be <8dB to satisfy the target MDS. There exists an additional noise degradation due to the reciprocal mixing of the phase noise spectrum by the in-band thermal noise (N_o) itself. Added noise density due to the phase noise is calculated by [17].

$$N_{PN} = N_o \cdot \int_{-\infty}^{\infty} S_{LO}(\omega)\, d\omega, \tag{11}$$

where $S_{LO}(\omega)$ is the phase noise of the receiver. With -145 dBc/Hz of phase noise derived from the reciprocal mixing of the interferences, the added noise density is minimal with less than 0.1dB loss in the MDS.

The derived target specification above is to guarantee the target MDS and instantaneous DR of 40dB with the single gain line-up. With the help of variable gain in the receiver signal chain, the overall DR of 80dB needs to be satisfied with reasonable ADC ENOB and sampling rate. Based on the high-speed ADC works in the recent literature [15], [16], we assume 8bit ENOB and 3GSample/s with 3dBm full-scale (FS). Quantization noise floor of the ADC is then -47dBm. With the signal power at the MDS level, receiver gain prior to A/D conversion should be sufficiently high such that the the noise due to the receiver dominates the detection SNR and the degradation due to the quantization noise is minimal. Then, the receiver gain of minimum 39dB positions the receiver noise power at -31dBm. Quantization noise power is 16dB lower than the receiver noise and, thus, the added noise due to the ADC is less than 0.1dB. On the other hand, when the receiver handles the large input signal, the receiver gain needs to be lowered not to saturate the receiver nor overload the ADC. To allow any envelope variation of the received signal, the receiver gain needs to be -13dB or below. As a result of these considerations, Fig. 8 depicts the variable gain requirement for the proposed receiver with 8bit ADC (i.e., 50dB dynamic range).

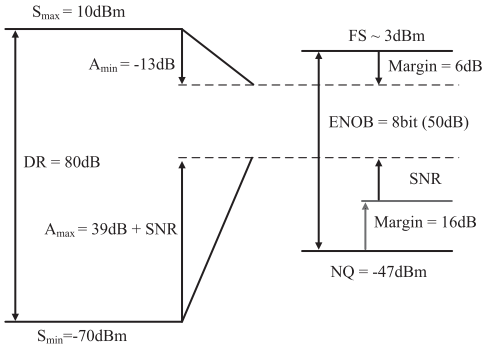

FIGURE 8. Variable gain requirement for the proposed receiver.

B. IMAGE REJECTION

The proposed receiver adopts the direct-conversion (zero-IF) architecture with cascaded down conversion. Direct-conversion receiver in general requires relaxed quadrature accuracy since the quadrature mismatch superposes a small fraction of the spectrally inverted desired signal on to itself [4]. With super-heterodyne receiver architecture, on the other hand, the receiver has to endure unwanted channel signal that can be +40dB higher than the desired signal strength.

With gain mismatch of g and phase mismatch of θ, the image rejection ratio, or the residual side-band suppression ratio (RSB), is widely known and is expressed below [18].

$$RSB_{single} = \frac{1 - 2(1+g)\cos(\theta) + (1+g)^2}{1 + 2(1+g)\cos(\theta) + (1+g)^2}. \quad (13)$$

Under small imbalance conditions (e.g., $g < 0.1$, $\theta < 3^\circ \cdot \pi/180$rad/s), The RSB can be approximated as

$$RSB_{single} \approx \frac{(g)^2 + (\theta)^2}{4}. \quad (14)$$

25dBc of image rejection is readily achievable with single down conversion mixer. For instance, $g < 0.1$ (0.8dB), $\theta < 3^\circ \cdot \pi/180$rad/s gives 25.3dBc from (13). On the other hand, with the proposed channelization receiver, the image rejection performance needs a careful attention due to the cascaded down conversion nature. To quantify the effect of cascaded down-conversion, complex I/Q mixer (2nd mixer in Fig. 3) is analyzed with imbalance conditions for both the RF and LO signals. The image rejection ratio of the complex mixer is derived and is shown in (12), at the bottom of this page. Note that (12) is considered to be the image rejection ratio of the cascaded down-conversion in Fig. 3.

Under small imbalance conditions for the cascaded down converter, the cascaded RSB is approximated as

$$RSB_{cascaded} \approx \frac{(g_1+g_2)^2 + (\theta_1+\theta_2)^2}{4}. \quad (15)$$

If the number of the iterative down conversion is N (= 5 in our work), (15) is extended to the following.

$$RSB_{general} \approx \frac{\left(\sum_{i=1}^{N} g_i\right)^2 + \left(\sum_{i=1}^{N} \theta_i\right)^2}{4}. \quad (16)$$

Imbalances (i.e., gain and phase mismatches) due to each mixer stage are random processes and are statistically independent to each other. Then, under the assumption that variance of each mixer stage's gain and phase mismatches are the same, the root-mean-square (rms) values of the total gain and phase mismatch are given by

$$\sigma_{g,total} = \sqrt{\sigma_{g_1}^2 + \sigma_{g_2}^2 + \cdots + \sigma_{g_N}^2} = \sqrt{N}\sigma_g \quad (17)$$

$$\sigma_{\theta,total} = \sqrt{\sigma_{\theta_1}^2 + \sigma_{\theta_2}^2 + \cdots + \sigma_{\theta_N}^2} = \sqrt{N}\sigma_\theta \quad (18)$$

Thus, each mixer stage needs to have $1/\sqrt{(N)}$ better mismatch parameter with N cascaded down conversion. For instance, in order to achieve 25dBc of image rejection for the proposed receiver, each mixer stage needs to have $g < 0.045$ (0.4dB), $\theta < 1.34^\circ \cdot \pi/180$rad/s with 5 down conversion stages.

$$RSB_{cascaded} = \frac{1 - 2(1+g_1)(1+g_2)\cos(\theta_1+\theta_2) + [(1+g_1)(1+g_2)]^2}{1 + 2(1+g_1)(1+g_2)\cos(\theta_1-\theta_2) + [(1+g_1)(1+g_2)]^2}. \quad (12)$$

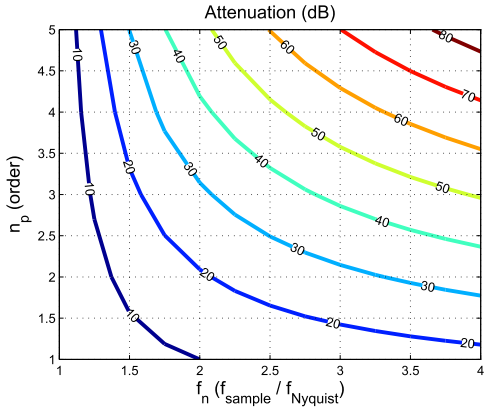

FIGURE 9. Attenuation of the out-of-band blocker at $f_s - f_{BW}$ as a function of the filter order and the ADC sampling rate.

C. CHANNEL SELECTION

Channel selection filtering can be performed in RF domain, analog (baseband) domain, or the combination of both. In practical implementation, the required quality factor ($Q = \frac{\omega_o}{BW}$) of the channel selection filter is prohibitively large at RF domain where the filtering is in the form of band-pass with high center frequency (ω_o). Thus, most of the channel selection is performed in the analog domain for zero-IF receivers [4], [19], [20].

Channel selection filter then helps to attenuate the close-in blockers and prevents the overloading of the ADC. In addition, the limitation of the baseband signal bandwidth before sampling avoids the degradation in SNR due to the aliasing of the out-of-channel blockers and noise. If the signal bandwidth and the sampling frequency are f_{BW} and f_s, respectively, the power of the blocker signal located at $f_s - f_{BW}$ should be sufficiently suppressed with the channel selection filter. All-pole filter and Nyquist rate ADC are discussed here to determine the order of the baseband lowpass filter. The attenuation of a Butterworth lowpass filter has a constant roll-off of 20dB/decade/pole and thus, the attenuation at the $f_s - f_{BW}$ frequency can be expressed as follows.

$$L(f) = 10 \cdot \log_{10}\left(1 + \left(\frac{f_s - f_{BW}}{f_c}\right)^{2n_p}\right), \tag{19}$$

where n_p and f_c are the order and the cut-off frequency of the baseband filter. f_c needs to be identical to the signal bandwidth (f_{BW}) of each I/Q outputs, which is 0.625GHz in this proposed channelization receiver. Fig. 9 shows the filtering effect of the blocker signal at $f_s - f_{BW}$ versus the filter order (n_p) and the normalized sampling frequency ($f_n = \frac{f_s}{2f_{BW}}$). 4th order Butterworth filter and 3GSample/S Nyquist ADC provide 46dB of filtering for the out-of-band jammer at the worst-case anti-aliasing frequency. With instantaneous target DR of 40dB, this filter order is plausible as the channel selection filter as well as the anti-aliasing filter of the ADC.

D. HARMONIC REJECTION

Frequency translation due to the mixer stage is achieved by various mechanisms. Linear, time-invariant system cannot generate any new spectral components and thus, mixer must be either non-linear or time-varying system [21], [22]. Mixers based on the non-linearity (e.g., square-law mixer) is not used for high performance receiver due to the poor conversion gain and noise level. Mixer utilizing the switching operation is superior to the former in its performance. However, odd harmonics of LO frequency is frequency translated and corrupts the baseband signal spectrum.

Harmonic rejection mixer [23], [24] is the remedy for the spectrum corruption due to the odd harmonic frequency components but require 3-path phase shifted LO signals. Also, the harmonic rejection ratio is typically limited to <40dB and places the fundamental limitation. 3-phase ($-45°$, $0°$, and $+45°$) and amplitude scaled ($1/\sqrt{2}$, 1, and $1/\sqrt{2}$) LO signals can in principle reject the $8k+3$ and $8k+5$ harmonics ($k = 0, 1, 2, \ldots$). With the 3-phase LO signal with the given relationship, LO signal for the harmonic rejection mixer can be represented by

$$\rho_0(t) = \sum_{n=1}^{\infty} a_n \cdot \exp(jn\omega_o t), \tag{20}$$

$$\rho_1(t) = \frac{1}{\sqrt{2}} \cdot \rho_0\left(t - \frac{T}{8}\right), \tag{21}$$

$$\rho_2(t) = \frac{1}{\sqrt{2}} \cdot \rho_0\left(t + \frac{T}{8}\right), \tag{22}$$

where T is the period of LO signal. Then, the effective LO signal of the harmonic rejection mixer is derived as below.

$$\begin{aligned}\rho(t) &= \rho_0(t) + \rho_1(t) + \rho_2(t), \\ &= \sum_{n=1}^{\infty} a_n \left[1 + \sqrt{2} \cdot \cos(\frac{n}{4}\pi)\right] \cdot \exp(jn\omega_o t).\end{aligned} \tag{23}$$

For $n = 8k + 3$ and $n = 8k + 5$, there exists no harmonic components. Only for other odd harmonics, mixer properly translates the desired RF signal to IF signal. Besides the fundamental harmonic, the first undesired harmonic is at 7_{th}, which can be easily filtered out. Similar to the finite image rejection ratio due to mismatches, harmonic rejection ratio is limited and their rejection ratios for the 3_{rd} and the 5_{th} are shown in Fig. 10. As can be seen from Fig. 10, Satisfying >40dB of harmonic rejection is not trivial and require precise matching performance ($\alpha < 0.01$ (0.09dB), $\theta < 0.5° \cdot \pi/180$rad/s) for the 3_{rd} and the 5_{th} harmonics.

The parallel channelization (band segmentation) in the proposed architecture limits the blocker signal at the harmonic frequency and eases the harmonic rejection requirement of the following mixers. The blockers at the harmonic frequency of the back-end channelizer is then attenuated by the LNA, mixer, and off-chip front-end module. In addition, the input spectrum of the back-end serial channelization stage is limited to DC-10GHz. The back-end serial channelizer operates

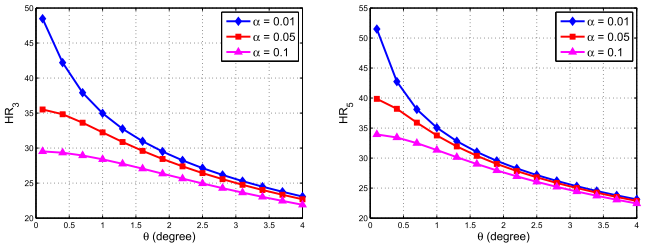

FIGURE 10. Harmonic rejection ratio with gain (α) and phase (θ) mismatches: (a) 3_{rd} harmonic and (b) 5_{th} harmonic.

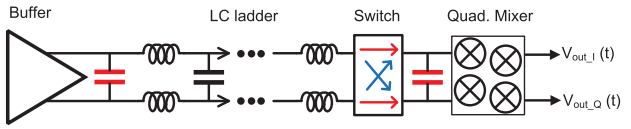

FIGURE 11. Block diagram of the back-end unit.

at the reduced input bandwidth and thus, can utilize the harmonic rejection mixer with minimum power penalty.

After four parallel bands are combined through the on-chip switches, there exists the buffer stage with doubly terminated ladder filter as shown in Fig. 11. The purpose of the buffer stage is to endure large parasitics at the combining node due to many parallel connections and long signal routings. Ladder filter is incorporated as the buffer stage load network and provides wide bandwidth by nulling out the parasitics of the buffer output and the mixer input. The filter provides the filtering for the out-of-band blockers and limits the noise bandwidth for the following mixer stage as well. The blocker frequency for the 3_{rd} harmonic of the first mixer at the back-end is 15GHz. With the 5 ladder filter stages implemented in our work, the blocker is attenuated by 17.7 dB from (19). Then, harmonic rejection mixer at the back-end operates with more benign matching requirement. The receiver requirements discussed in this section are summarized in Table 1.

V. SIMULATION RESULTS

The prototype receiver front-end was designed and implemented in TSMC 45nm RF CMOS technology. Fig. 12 illustrates system architecture of the channelized receiver front-end and its LO chains. The broadband input is partitioned into 4 channelized sub-bands with 10GHz BW. Off-chip source is used to inject the 40GHz reference clock signal and two-stage divide-by-2 generates the required 20GHz and 10GHz LO signals for band2 and band1, respectively. The 30GHz LO signal for band3 is generated through SSB mixing operation.

LNAs for each sub-bands are implemented as a two-stage amplifier. Band2 and band3 LNAs are inductively generated common-source amplifiers [25], [26] and their frequency responses are stagger-tuned to cover 10GHz band coverage. Band1 and band0 LNAs are inverter-type complementary MOS amplifiers [27] due to their good power-efficiency and

TABLE 1. Receiver system budget.

Parameter	Specifications	Noise Power [dBm]	Contribution [%]
NF (dB)	8*	-75	31.5
Phase Noise (dBc/Hz)	-145	-82	6
IIP_2 (dBm)	25	-82	4.8
IIP_3 (dBm)	-6	-76	24.3
RSB (dBc)	25	-95.3	0.3
Harmonic Rej. (dBc)	50◇	-80.5	8.5
Filter Order	4	-76.4	22.2
ENOB (ADC)	8	-86†	2.4
MDS (dBm)	**-70**	**-70.1**	**100**

* Includes the insertion loss (IL) of the front-end module
◇ With 10dB of filtering due to the front-end module
† Quantization noise power referred to the receiver input

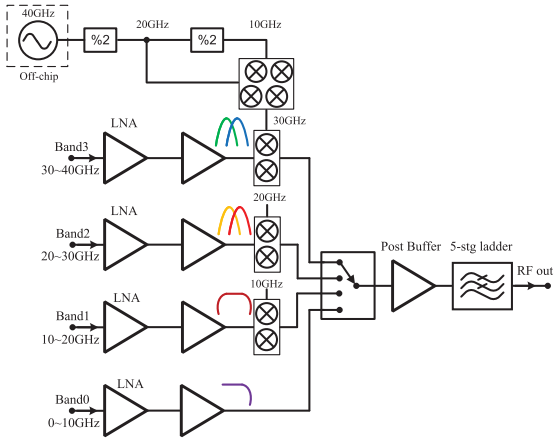

FIGURE 12. Schematic of the channelization receiver front-end.

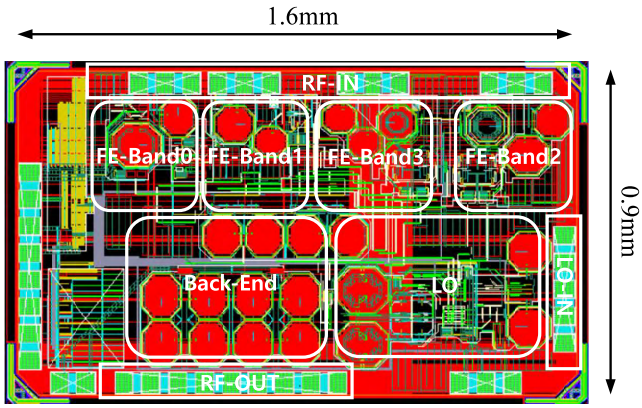

FIGURE 13. Chip layout of the channelization receiver front-end.

linearity property. Mixers for band1-band3 adopts the same topology of the complementary Gilbert-Cell mixer with current reuse. 4 to 1 RF switch subsequently selects the desired sub-band. Post-amplifier and 5-stage ladder low-pass filter limits the high frequency signals and noise as well for the following back-end stages, which are not included in this prototype.

Fig. 13 shows the chip layout of the channelized receiver front-end. The system occupies 1.6mm by 0.9mm including the pads. Front-end sub-bands and LO blocks are placed to minimize the interconnection between RF and LO

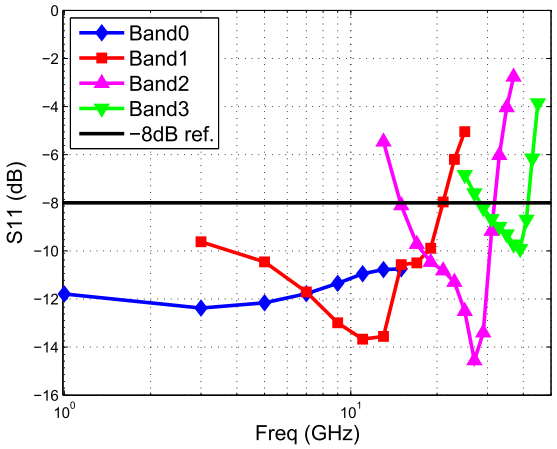

FIGURE 14. S_{11} of the channelization receiver front-end.

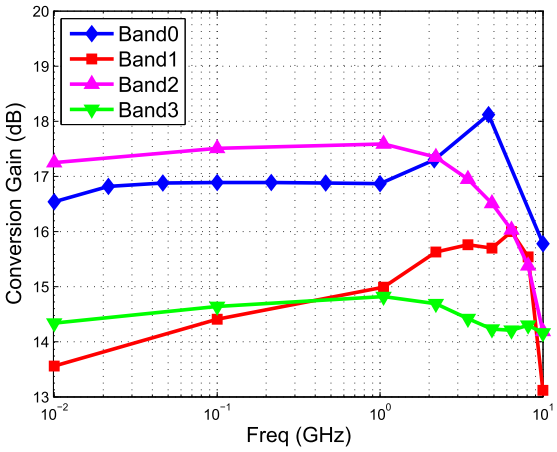

FIGURE 15. Conversion-gain of the channelization receiver front-end.

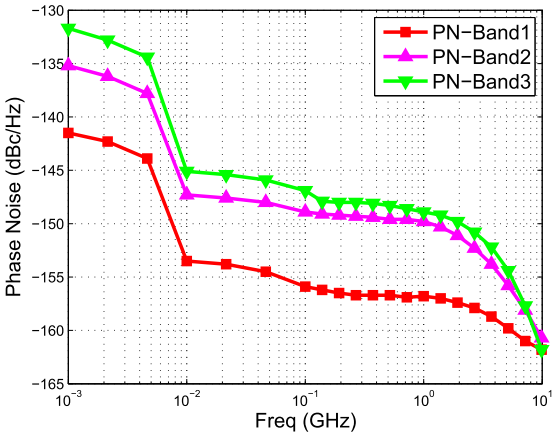

FIGURE 16. Phase Noise of the channelization receiver front-end.

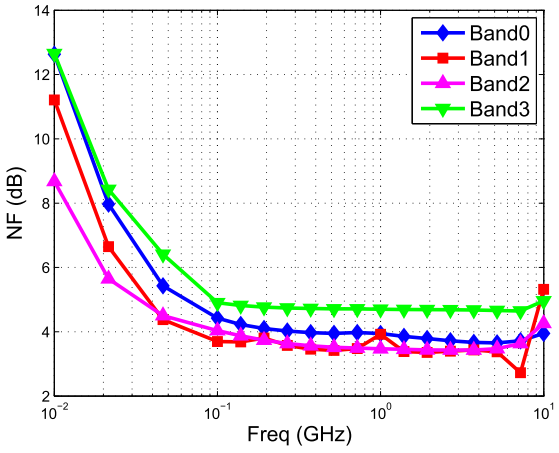

FIGURE 17. NF of the channelization receiver front-end.

for band 2 and band3. The 5-stage ladder filter requires 4 inductors for each I/Q stage and occupies most of the back-end area.

Fig. 14 shows the simulated impedance match (S_{11}) of the proposed channelization receiver front-end. The S_{11} of the band0-band2 shows better than −10dB and band3 marginally meets −8dB at the edge of the band. Simulated conversion-gain of 4 sub-bands are shown in Fig. 15. The conversion gain shows >13dB. Within each sub-bands, the gain variation is less than 3dB.

The phase noise of the channelization receiver-front end is simulated with noisy external signal generator[1] as shown in Fig. 16. The target specification of −145dBc/Hz is satisfied for >10MHz offset frequencies for all sub-bands.

Fig. 17 shows the simulated noise figure of the channelized receiver front-end. NF is less than 5dB when it is thermal noise limited. The flicker noise corner (3dB above the flat region, $NF_{thermal} = NF_{flicker}$) is observed around 20-40MHz IF frequencies.

[1]The phase-noise was obtained from the data sheet of Keysight Technologies analog signal generator E8257D PSG and was used in simulations.

VI. CONCLUSIONS

This paper has presented a broadband channelization receiver architecture along with its design challenges and system analysis. The proposed channelization receiver architecture adopts the parallel band partition at the front-end and the series channelization at the back-end. The parallel band partition at the front-end relaxes the signal condition due to the interferences and eases the optimization per sub-band. The serially channelized receiver back-end enables the agile frequency scanning and simple LO signal chain consisting of successive divide-by-2 and the single SSB mixer. System analysis with consideration of multitude receiver impairments shows that the spectrum agile frequency spectrum receiver with −70dBm minimum detectable signal and 40dB instantaneous dynamic range is achievable with 8bit ENOB ADC.

The prototype receiver front-end is implemented in TSMC 45nm CMOS technology as a proof of concept for the broadband receiver front-end solution. The receiver front-end shows <5dB NF and <−145dBc/Hz phase noise performance, which meet the target specifications for the spectrum sensing receiver. With 1.1V supply, the prototype receiver

front-end dissipates 33mA and 60mA from the signal-path and LO path, respectively when each band's current consumption is averaged.

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