IEEE Access
Multidisciplinary | Rapid Review | Open Access Journal

Received September 20, 2017, accepted October 23, 2017, date of publication October 26, 2017,
date of current version November 14, 2017.

Digital Object Identifier 10.1109/ACCESS.2017.2766671

A Stochastic Flash Analog-to-Digital Converter Linearized by Reference Swapping

MIN-KI JEON, WON-JUN YOO, CHAN-GYU KIM, AND CHANGSIK YOO, (Member, IEEE)
Department of Electronic Engineering, Hanyang University, Seoul 04763, South Korea

Corresponding author: Changsik Yoo (csyoo@hanyang.ac.kr)

This work was supported by the Samsung Research Funding Center of Samsung Electronics under Project SRFC-IT1501-01.

ABSTRACT The linearity of a stochastic flash analog-to-digital converter (ADC) with two groups of comparators is improved by reference swapping. If the input offset of a comparator is larger than the linear input range of its comparator group, the reference voltage of the comparator is swapped with the reference voltage of the other comparator group. The reference swapping doubles the number of comparators providing a meaningful result in determining the ADC output. A stochastic flash ADC linearized by the reference swapping has been implemented in a 65-nm CMOS process. The peak signal-to-noise + distortion ratio is 39 dB, which is 3-dB higher than that without the reference swapping.

INDEX TERMS Analog-to-digital converter (ADC), CMOS, flash ADC, stochastic signal processing.

I. INTRODUCTION

Because the input offset and noise of comparators limit the achievable resolution of conventional analog-to-digital converters (ADCs), transistors and passive devices such as resistors and capacitors are often designed to be much larger than their minimum allowed sizes. The remaining input offset can be cancelled by an offset cancelling circuit, which requires additional power consumption, silicon area, and clock cycles depending on the architecture of the ADC. In a stochastic flash ADC, on the other hand, the device mismatch is utilized to obtain a linearized transfer characteristic with sufficiently a large number of comparators [1]–[7]. Because random variation is not a concern in a stochastic flash ADC, it may allow a fully synthesizable design, which is highly desirable in a scaled CMOS technology [6].

The basic architecture of a stochastic flash ADC is shown in Fig. 1(a), where all the comparators have the same reference voltage V_{REF} and the outputs of all the comparators are summed together to obtain the digital output. If a sufficiently large number of comparators are used, the probability density function (PDF) of the comparator input offset V_{OS} would be Gaussian by the central limit theorem, as shown in Fig. 1(b). Then, the transfer characteristic of the stochastic flash ADC is most linear for analog input smaller than the standard deviation (σ) of the comparator input offset, as shown in Fig. 1(c). If the input offset of a comparator is larger than σ, its output is outside the linear range and becomes meaningless in determining the ADC digital output. For this reason, a large number of comparators have to be used in a stochastic flash ADC to obtain the desired level of linearity, although many of them are wasted [4].

Several schemes have been proposed to allow a stochastic flash ADC to have the desired level of linearity with a reasonable number of comparators. If the inverse Gaussian transformation is applied to the digital output code of a stochastic flash ADC, its distorted transfer characteristic can be linearized by simple digital post-processing logic [6], [7]. In [4], two groups of comparators are used whose reference voltages are separated by 2σ, as shown in Fig. 2(a). Then, the PDF of the comparator reference + input offset is nearly uniform in the linear input range, meaning there was improved linearity, as shown in Fig. 2(b). The group-1 (group-2) comparators in the shaded region of Fig. 2(b) always provide "1" ("0") output for analog input in the linear range; therefore, their outputs are meaningless in determining the digital output code. In [5], the positive and negative inputs of the comparators in the shaded region are swapped with each other to invert the polarity of the input offset. This PDF folding is an effective way of improving the linearity of a stochastic flash ADC because the number of comparators providing meaningful output is doubled.

In this paper, a stochastic flash ADC with two groups of comparators is linearized by adaptively swapping the reference voltage of the comparators. The reference voltage of a comparator of one comparator group is swapped with the reference voltage of the other comparator group if its

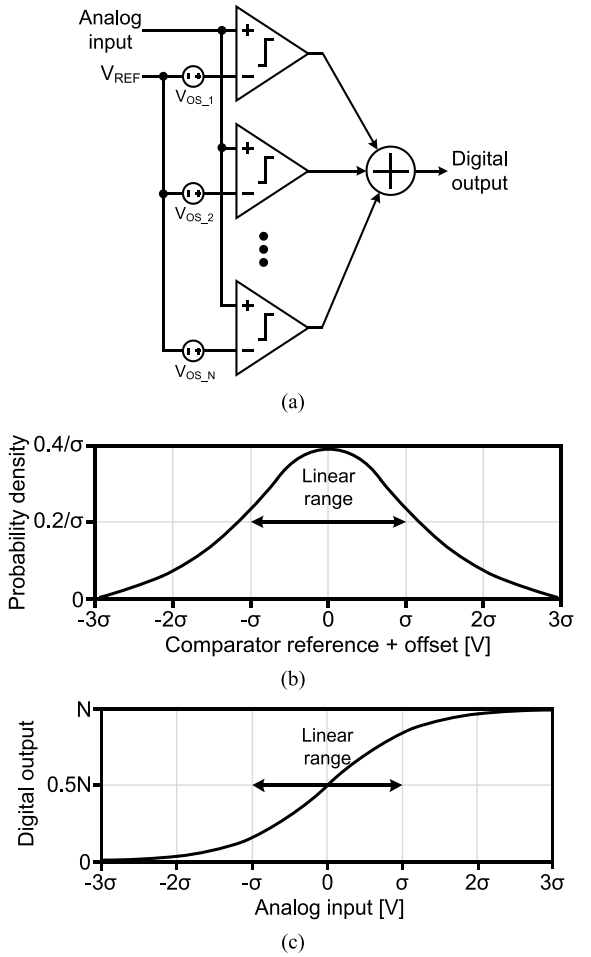


FIGURE 1. (a) Basic architecture of a stochastic flash ADC, (b) probability density function (PDF) of the comparator reference + offset voltage where the comparator reference V_{REF} is assumed to be zero, and (c) the transfer function.

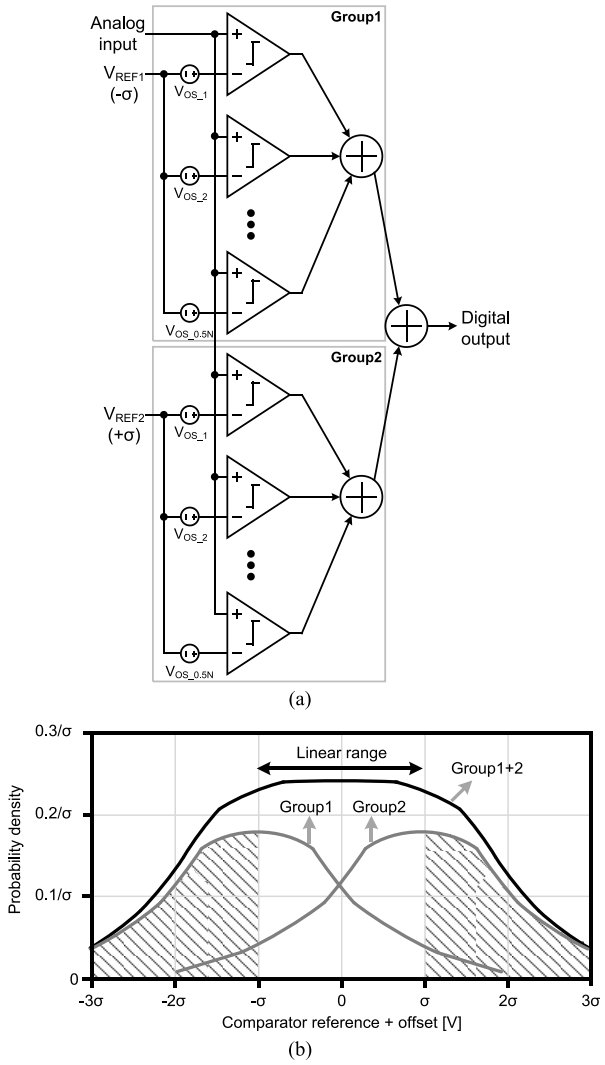


FIGURE 2. (a) Stochastic flash ADC with two groups of comparators and (b) the PDF of the sum of the comparator reference and the input offset of the comparator.

input offset is outside the linear input range. The reference swapping provides the same level of linearization as the PDF folding proposed in [5] with simple hardware. Section II discloses the operation principle and the circuit implementation. The experimental results are given in Section III. Finally, Section IV concludes this paper.

II. STOCHASTIC FLASH ADC LINEARIZED BY REFERENCE SWAPPING

The proposed stochastic flash ADC has two groups of comparators, and the reference levels of the comparators in group-1 and group-2 are $-\sigma$ and σ, respectively, where σ is the standard deviation of the comparator input offset. The PDF of the sum of the comparator reference and its input offset can be drawn as shown in Fig. 3(a) and Fig. 3(b) for group-1 and group-2, respectively. Each group has 4,095 comparators; therefore, there are 8,190 comparators in total.

In group-1, the outputs of the comparators with negative input offset (in the shaded region of Fig. 3(a)) are always "1" for analog input in the linear input range. In group-2, the outputs of the comparators with positive input offset (in the shaded region of Fig. 3(b)) are always "0" for analog input in the linear input range. Therefore, the comparators in the shaded regions (the group-1 comparators with negative input offset and the group-2 comparators with positive input offset) provide meaningless outputs in determining the ADC digital output code. To let them have meaningful outputs, the reference voltage of the group-1 and group-2 comparators in the shaded region is swapped from $-\sigma$ to $+\sigma$ and from $+\sigma$ to $-\sigma$, as shown in Fig. 3(a) and Fig. 3(b), respectively. With this reference swapping, the PDF of the reference + input offset of the two group comparators appears as drawn in the solid line of Fig. 3(c). The reference swapping doubles the number of comparators providing meaningful output for the ADC digital output code, as shown in Fig. 3(c).

For the reference swapping, it is first determined whether the input offset is positive or negative at power-up. For the comparators in group-1, both the positive and negative inputs are connected to the reference level $-\sigma$. If the output of

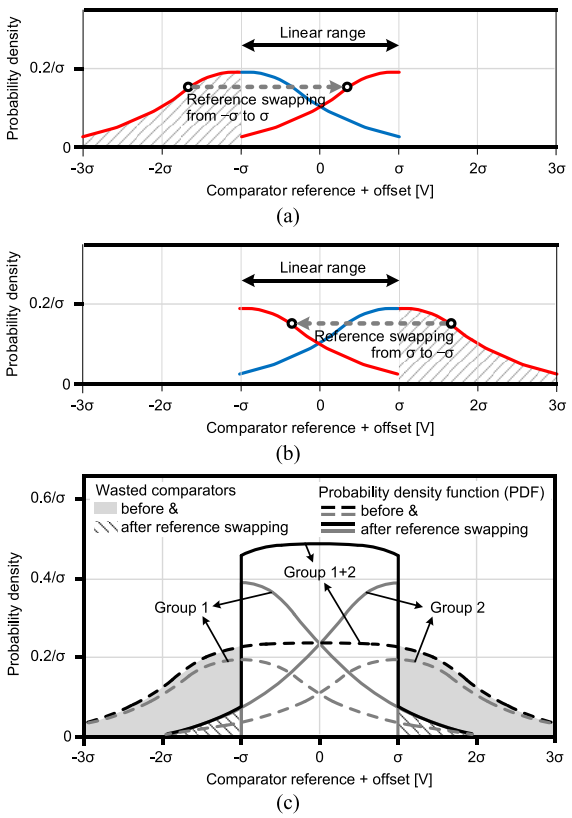


FIGURE 3. Swapping of the reference for the comparators of (a) group-1, (b) group-2, and (c) the PDF before and after the reference swapping.

a comparator is "1", it means the comparator has negative input offset and is in the shaded region. The reference level is then swapped to $+\sigma$. For the comparators in group-2, both the positive and negative inputs are connected to the reference level $+\sigma$. The reference level is swapped to $-\sigma$ for the comparators whose output is "0", meaning the input offset is positive. After this reference swapping is completed, normal ADC operation begins with two groups of comparators and adaptively swapped reference levels.

Fig. 4(a) shows the operation timing of the proposed stochastic flash ADC. The comparator and reference swapping control logic for group-1 and group-2 are shown in Fig. 4(b) and Fig. 4(c), respectively. During the reference swapping period determining whether to keep or swap the reference, the calibration enabling signal *CAL* is set to be "1" and the reset signal *RESETB* is initially "0" to set the reference swapping signal *SWAP* to be "0". Both the positive and negative inputs of the comparators of group-1 (group-2) are connected to $-\sigma$ ($+\sigma$). If the input offset of a group-1 (group-2) comparator is negative (positive), its output V_{OUTP} would be "1" ("0"). Then, the reset signal *RESETB* and the calibration enabling signal *CAL* are set to be "1" and "0", respectively, enabling the latch consisting of the NAND gate and the inverter to store the comparison result in the latch. For the reference swapping, one NAND gate, one inverter, and six transmission gates are additionally required per comparator.

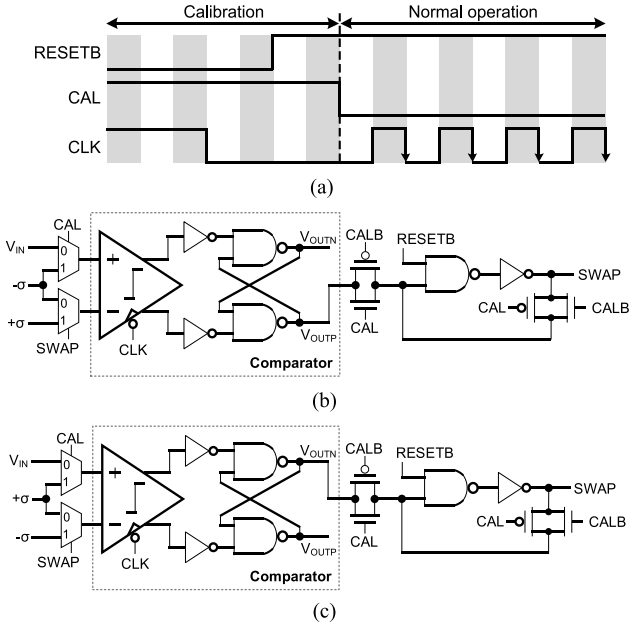


FIGURE 4. (a) Timing diagram of the proposed stochastic flash ADC and the architecture of the comparator and reference swapping control logic for (b) group-1 and (c) group-2.

The comparators of group-1 and group-2 have different reference voltages, which means their input common-mode levels are different if conventional single-ended comparators are used. Different input common-mode levels may result in different shapes of the PDF of the reference + input offset for group-1 and group-2 comparators. To fully exploit the benefit of two comparator group architecture in improving the linearity of a stochastic flash ADC, it is desirable for the two comparator groups to have the same PDF of reference + input offset. To allow this, the comparators are designed as fully differential ones to have the same input common-mode level regardless of reference voltage.

We have evaluated the strong-ARM latch-based structure shown in Fig. 5(a) and the proposed one shown in Fig. 5(b) to see which one is more suitable for this work [8]. The drain nodes of the input transistors $M_1 \sim M_4$ of the strong-ARM latch-based comparator in Fig. 5(a) are discharged to 0-V when *CLK* is "1". When *CLK* becomes "0", the input difference is evaluated and initially the input transistors operate in the saturation region. In contrast, the drain nodes of the input transistors $M_1 \sim M_4$ of the comparator used in this work (shown in Fig. 5(b)) are pre-charged to V_{DD} when *CLK* is "1". When *CLK* becomes "0", the input difference is evaluated and initially the input transistors operate in the linear region, meaning there is a smaller gain of the input transistors $M_1 \sim M_4$. Because the mismatch of the other transistors is divided by the gain of the input transistors when referred to the input, the comparator in Fig. 5(b) shows a larger input offset, as seen in the simulated probability density in Fig. 5(c) [8]. While the comparators for a conventional flash ADC are required to have as small input offset as possible, a stochastic flash ADC can have better linearity with a larger

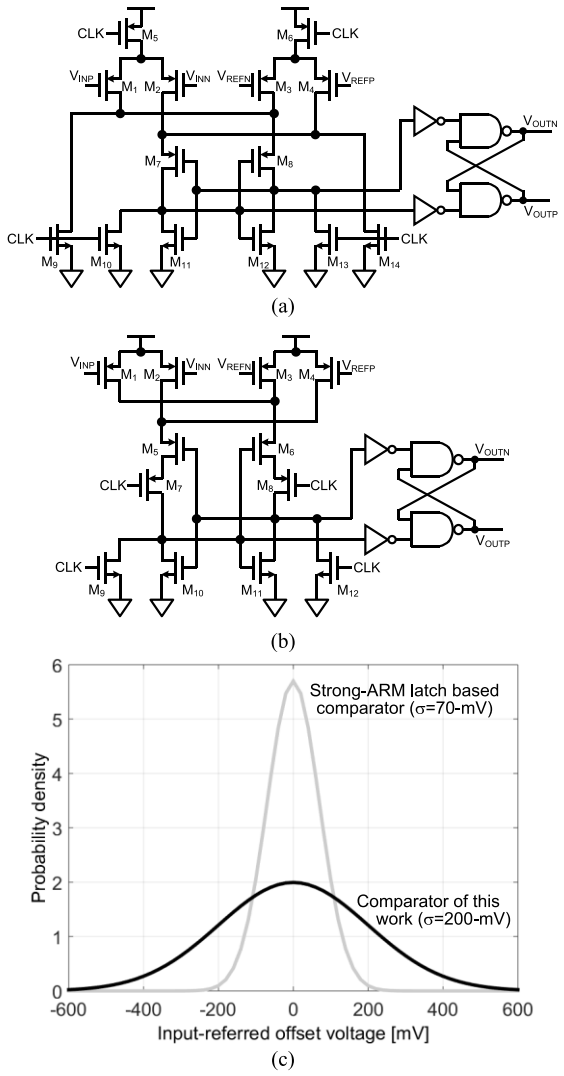


FIGURE 5. **(a) A four-input fully differential comparator with strong-ARM latch architecture, (b) the comparator used in this work with larger input offset, and (c) the simulated probability density of the input-referred offset voltage.**

comparator input offset and thus the comparator in Fig. 5(b) is chosen for this work. All the transistors are sized to be at minimum size.

Because the comparator outputs of a stochastic flash ADC can have many sparkles, the Wallace tree adder shown in Fig. 6(a) counts the number of "1" outputs from the 8,190 comparator outputs instead of using a conventional thermometer-to-binary decoder. Registers are inserted after every two consecutive full-adders (FA) to create a pipeline structure for the maximum operation frequency. The FA in the Wallace tree adder can be considered as a three-to-two bit-compressor where the three inputs should have the same bit weight. The outputs of the comparators are first re-timed by F/Fs and applied to eight 1024-input adders. The 1024-input adder shown in Fig. 6(b) has a regular structure and counts the number of "1"s in the input to generate the corresponding 11-bit binary output code which is then applied to the back-end adder. The back-end adder, consisting of seven addition

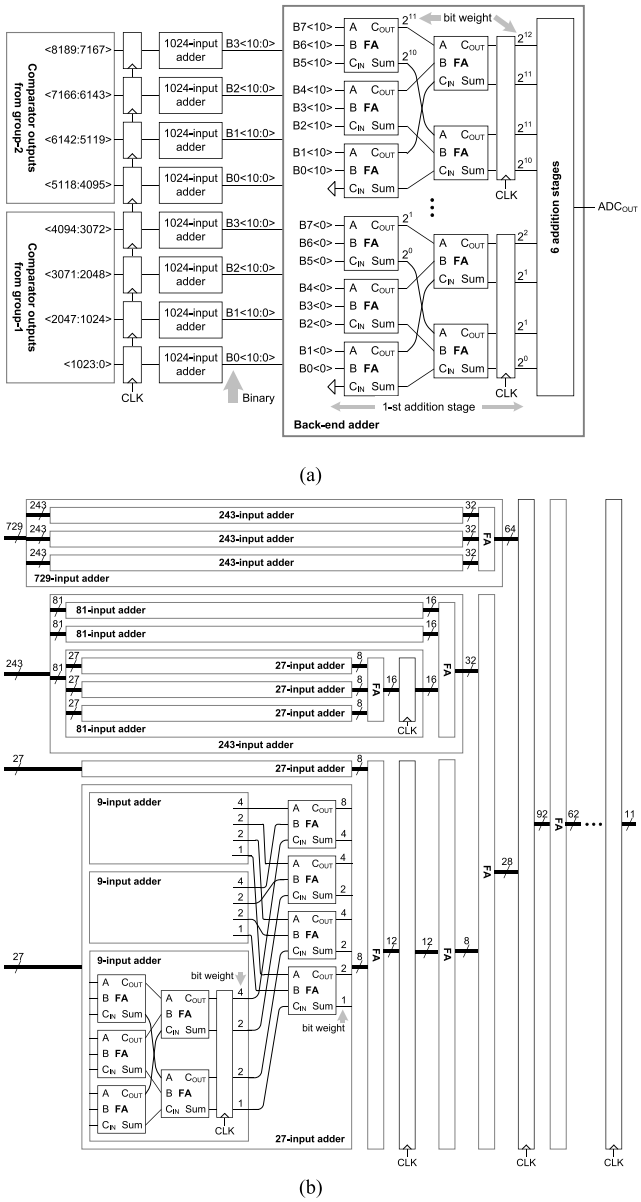


FIGURE 6. **Architecture of (a) the Wallace tree adder and (b) the 1024-input adder.**

stages, as shown in Fig. 6(a), adds the bits with the same bit weight to generate the final binary digital output ADC_{OUT}.

III. EXPERIMENTAL RESULTS

To verify the effectiveness of the proposed reference swapping in improving the linearity of a stochastic flash ADC, a prototype chip has been implemented in a 65-nm CMOS process. The chip microphotograph is shown in Fig. 7, and the active silicon area is 0.756-mm^2. The stochastic flash ADC operates with a 0.9-V supply voltage and consumes 33-mW and 63.9-mW, respectively at a 100-MS/s and 200-MS/s sampling rate.

Fig. 8 shows the measured spectrum of the ADC output for a 5.11-MHz sinusoidal input with a 100-MS/s sampling rate. The linearity of the stochastic flash ADC is obtained

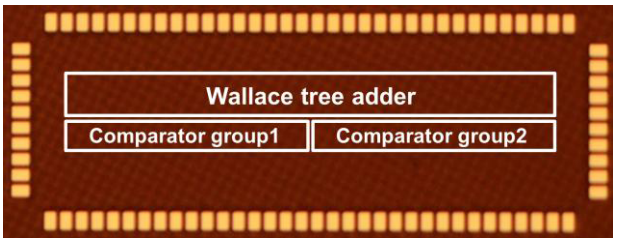


FIGURE 7. Chip microphotograph.

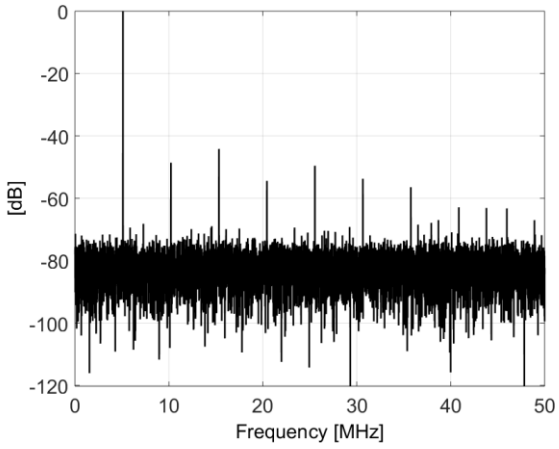


FIGURE 8. Output spectrum for a 5.11-MHz sinusoidal input.

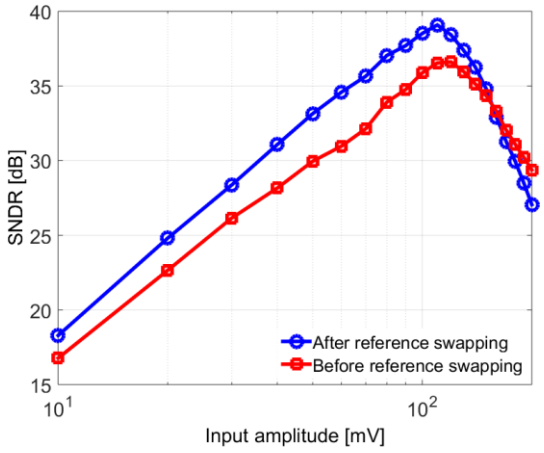


FIGURE 9. Measured SNDR of 1.08-MHz sinusoidal input versus the input amplitude before and after the reference swapping.

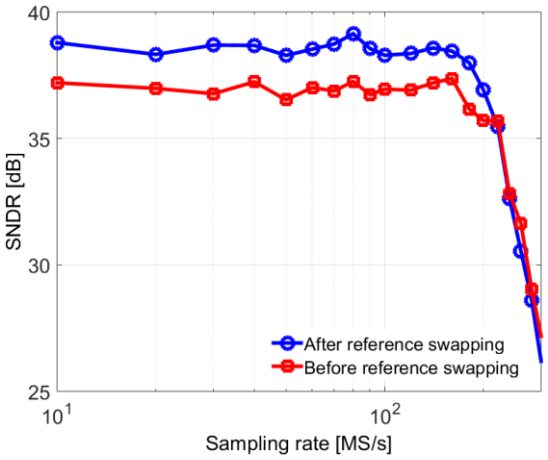


FIGURE 10. Peak SNDR versus the sampling rate for a 1.08-MHz sinusoidal input before and after the reference swapping.

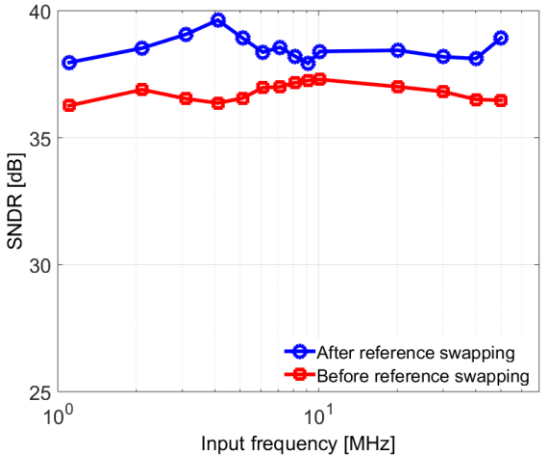


FIGURE 11. Peak SNDR versus the input frequency with 100-MS/s sampling rate.

from the stochastic distribution of the comparator input offset. Because the distribution may not be perfectly symmetric due to the finite number of comparators, even-order harmonics are observed in the output spectrum although the stochastic flash ADC has a fully differential architecture.

As a function of the amplitude of the 1.08-MHz sinusoidal input, the SNDR is measured before and after the reference swapping, as shown in Fig. 9. The maximum SNDR is improved to 39-dB from 36-dB. Therefore, the effective number of bits (ENOB) is 5.7-bit and 6.2-bit, respectively before and after the reference swapping. From the SNDR measured for a 1.08-MHz sinusoidal input versus the sampling rate shown in Fig. 10, the maximum sampling rate is limited to be less than 200-MS/s. The maximum sampling rate is thought to be limited by the operation speed of the Wallace tree adder. At 100-MS/s, the SNDR is measured as a function of the sinusoidal input frequency before and after the reference swapping, as shown in Fig. 11. It can be seen that the proposed stochastic flash ADC shows comparable performance up to the Nyquist input frequency.

The performance of the proposed stochastic flash ADC is compared with other stochastic ADCs in Table 1. The proposed stochastic flash ADC shows the highest SNDR and ENOB and the second largest linear input range. Although the stochastic flash in [7] shows the largest linear input range by employing 8-groups of comparators and applying the inverse Gaussian transformation, it requires calibration to generate multiple reference levels spaced by the standard deviation of the input offset of comparators.

TABLE 1. Performance comparison of stochastic flash ADC.

	This work	[3]	[4]	[6]	[7]
CMOS [nm]	**65**	90	180	90	130
Linearization tech.	**2-group comp. w/ reference swapping**	-	2-group comp.	Inverse Gaussian	8-group comp. w/ inverse Gaussian
Peak SNDR [dB]	**39**	23.97	33.59	35.89	32.8
ENOB [bit]	**6.2**	3.7	5.3	5.7	5.2
# of comp.	**8,190**	63	7,680	2,047	2,040
Supply [V]	**0.9**	1.2	0.9	1.2	1.0
Input range [$mV_{pp,diff}$]	**440**	100	280	280	800
Area [mm^2]	**0.756**	0.04	0.43	0.18	0.51
Power [mW]	**33**	23	0.631	34.8	87
Sampling rate [MS/s]	**100**	1,500	8	210	320
FoM* [pJ/conv.step]	**4.5**	1.2	2.0	3.2	7.4

FoM=(Power/2^{ENOB})f_S

IV. CONCLUSION

The linearity of a stochastic flash ADC with two groups of comparators is improved by adaptively swapping the reference levels between the two groups. A stochastic flash ADC with 8,190 comparators has been implemented in a 65-nm CMOS process whose SNDR is improved to 39-dB from 36-dB by the proposed reference swapping. This means the number of comparators providing meaningful output is doubled.

ACKNOWLEDGMENT

The CAD tools and chip fabrication service were provided by the IC Design Education Center (IDEC), Korea.

REFERENCES

[1] A.-J. Annema, B. Nauta, R. van Langevelde, and H. Tuinhout, "Analog circuits in ultra-deep-submicron CMOS," *IEEE J. Solid-State Circuits*, vol. 40, no. 1, pp. 132–143, Jan. 2005.

[2] A.-J. Annema, B. Nauta, R. van Langevelde, and H. Tuinhout, "Designing outside rail constraints," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2004, pp. 134–135.

[3] T. Sundström and A. Alvandpour, "Utilizing process variations for reference generation in a flash ADC," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 56, no. 5, pp. 364–368, May 2009.

[4] S. Weaver, B. Hershberg, P. Kurahashi, D. Knierim, and U.-K. Moon, "Stochastic flash analog-to-digital conversion," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 57, no. 11, pp. 2825–2833, Nov. 2010.

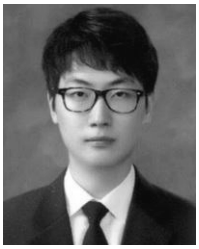
[5] S. Weaver, B. Hershberg, and U.-K. Moon, "PDF folding for stochastic flash ADCs," in *Proc. IEEE Int. Conf. Electron., Circuits, Syst. (ICECS)*, Dec. 2010, pp. 770–773.

[6] S. Weaver, B. Hershberg, and U.-K. Moon, "Digitally synthesized stochastic flash ADC using only standard digital cells," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 61, no. 1, pp. 84–91, Jan. 2014.

[7] A. Fahmy, J. Liu, T. Kim, and N. Maghari, "An all-digital scalable and reconfigurable wide-input range stochastic ADC using only standard cells," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 62, no. 8, pp. 731–735, Aug. 2015.

[8] B. Razavi, "The StrongARM latch [a circuit for all seasons]," *IEEE Solid-State Circuits Mag.*, vol. 7, no. 2, pp. 12–17, Mar. 2015.

MIN-KI JEON received the B.S., M.S., and Ph.D. degrees from Hanyang University, Seoul, South Korea, in 2010, 2012, and 2017, respectively, all in electronic engineering. He is currently with AnaPass Inc., Seoul. His research interests include high-speed interface circuit design.



WON-JUN YOO received the B.S. and M.S. degrees in electronic engineering from Hanyang University, Seoul, South Korea, in 2015 and 2017, respectively. Since 2017, he has been with SK Hynix, Icheon, South Korea, as a Senior Researcher.

CHAN-GYU KIM received the B.S. degree in electronic engineering from Konkuk University, Seoul, South Korea, in 2015, and the M.S. degree in information display engineering from Hanyang University, Seoul, South Korea, in 2017. Since 2017, he has been with LG Electronics, Pyeongtaek, South Korea.

CHANGSIK YOO (M'00) received the B.S. (Honors), M.S., and Ph.D. degrees from Seoul National University, Seoul, South Korea, in 1992, 1994, and 1998, respectively, all in electronic engineering. From 1998 to 1999, he was with the Integrated Systems Laboratory, Swiss Federal Institute of Technology, Zürich, Switzerland, as a Research Staff. From 1999 to 2002, he was with Samsung Electronics, Hwasung, South Korea, as a Senior Engineer. Since 2002, he has been a Professor with Hanyang University, Seoul. His main research interest is the mixed-mode CMOS integrated circuit design. He served as a Technical Committee Member for several international conferences, such as the IEEE International Solid-State Circuits Conference, the IEEE VLSI Circuits Symposium, and the IEEE European Solid-State Circuits Conference. He was an Associate Editor of the IEEE Microwave and Wireless Components Letters.