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# High-Isolation CMOS T/R Switch Design Using a Two-Stage Equivalent Transmission Line Structure

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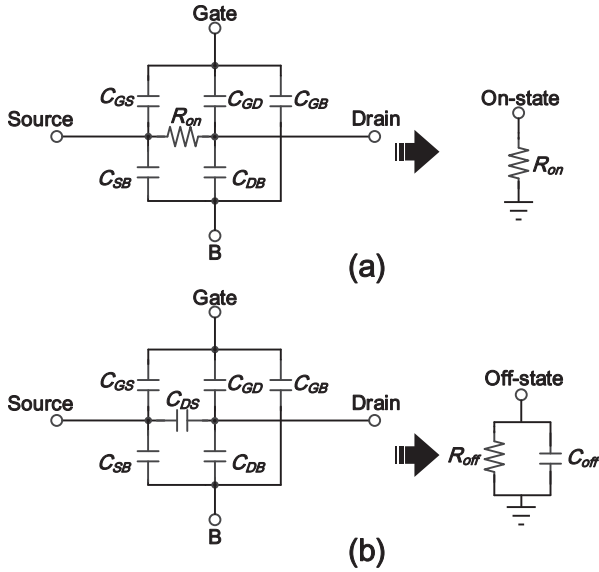
**ABSTRACT** A fully integrated Ku-band transmit/receive (T/R) switch based on a two-stage equivalent transmission line structure has been designed using a 180-nm complementary metal-oxide-semiconductor (CMOS) process. An analysis shows a relation between the series inductance and turn-on resistance for high isolation. A stack structure with feed-forward capacitors was chosen as a means of improving the power-handling capability of the switch. A low insertion loss (IL) of the switch was achieved by eliminating series transistors. The measured minimum ILs of the switch in the transmitter (TX) and receiver (RX) modes are 2.7 dB and 2.3 dB, respectively. The measured isolations in the TX and RX modes are greater than 34 and 25 dB, respectively, from 15 to 18 GHz. The design reaches a measured input 1-dB power compression point ( $IP_1dB$ ) of 22 dBm at 17 GHz. The switch achieves stringent isolation, insertion loss, and power-handling capability requirements along with the capability of full integration, demonstrating its great potential for use in fully integrated CMOS T/R chips.

**INDEX TERMS** CMOS transmit/receive (T/R) switch, lumped equivalent transmission line structure, insertion loss, isolation, power-handling capability, full integration.

## I. INTRODUCTION

At present, increasing numbers of RF components are being integrated using the standard CMOS process to satisfy requirements of low cost and small size for wireless consumer markets. However, RF switches are still mainly realized using the gallium arsenide (GaAs) process [1], [2] or the silicon-on-insulator (SOI) CMOS process [3], [4] due to the insulation provided by GaAs substrates and the possibility of high resistivity of SOI substrates, which are beneficial for achieving high isolation and low insertion loss. This mix of processes for different components prevents integration progress toward a true single-chip radio. Furthermore, the high wafer costs of the GaAs process and the SOI CMOS process make it difficult to meet reduced cost requirements. Fueled by the recent explosion in wireless internet technologies, rapidly growing communication markets are driving the development of reliable, high-performance and economical RF systems on one chip. An RF CMOS switch has the natural advantages of a high integration capacity and a low cost, but its insertion loss and power-handling capability are severely

limited by the conductivity of the silicon substrate and the low breakdown voltage of the transistor. Various switches have been implemented using CMOS process. Due to the limitation of the CMOS process and high IL, the operating bandwidth of conventional series-shunt switch is limited to low GHz application and hardly used in the millimeter-wave regime [5]. For high frequency applications, the loss due to shunt arm severely degrades the IL while the lack of shunt arm results in a low isolation [6]. To overcome this issue, the travelling-wave concept switch [7] and matching-network switch [8] are widely used. In both switches, in order to enhance the isolation,  $\lambda/4$  transmission lines are used instead of series transistors. However, the  $\lambda/4$  transmission lines occupy larger chip area. Moreover, the travelling-wave concept switch uses double-shunt transistors to get high isolation, whereas the double-shunt transistors increase the IL; the matching-network switch uses a shunt inductor to resonate out the parasitic capacitance of the transistor in the off-state to realize low IL, whereas only one shunt transistor does not guarantee enough isolation value [9].



**FIGURE 1.** Simplified small signal equivalent circuit models for MOSFETs under: (a) on-state. (b) off-state.

In this work, a Ku-band T/R switch based on an equivalent transmission line structure is designed using a 180 nm CMOS process. Equivalent transmission line is created by cascading series inductor, shunt capacitor and transistor’s parasitic capacitance to synthesize a  $\Pi$  network which works as a equivalent  $\lambda/4$  transmission line [10]. A two-stage  $\Pi$  structure is adopted to greatly improve the isolation. The double-shunt transistors in two-stage  $\Pi$  structure are absorbed into the impedance matching network to decrease IL. Stacked transistors with feed-forward capacitors are used to improve the power-handling capacity.

This paper is organized as follows. Section II evaluates the isolation and design of the proposed T/R switch. The results of experimental measurements are discussed in Section III. Finally, the paper is concluded in Section IV.

## II. DESIGN AND ANALYSIS

Fig. 1 shows simplified small signal equivalent circuit models of MOSFETs under the on and off states [10].  $C_{GS}$ ,  $C_{GD}$ ,  $C_{DS}$ ,  $C_{DB}$ ,  $C_{SB}$  and  $C_{GB}$  are parasitic capacitances of the transistor. For a transistor with a grounded source, when the gate-source voltage  $V_{gs}$  is higher than the threshold voltage  $V_{th}$ , the transistor is turned on and can be modeled as a small on-resistance  $R_{on}$  as shown in Fig. 1(a). Otherwise, the transistor is turned off and functions as an off-capacitance  $C_{off}$  as shown in Fig. 1(b) [11]. The on-resistance  $R_{on}$  and off-capacitance  $C_{off}$  can be expressed depend on model parameters [6], [12].

$$\begin{cases} R_{on} = \frac{1}{\mu_n C_{ox} \frac{W}{L} (V_{gs} - V_{th})} & (1) \\ C_{off} = C_{DS} + \frac{C_{GS} \times C_{GD}}{C_{GS} + C_{GD}} & (2) \end{cases}$$

$C_{ox}$  denotes the gate capacitance per unit area,  $W$  and  $L$  is the width and length of transistor respectively.

Given this on-off nature of the transistor, the conventional T/R switch structure using a  $\lambda/4$  transmission line [8] can be replaced with the equivalent transmission line structure to reduce the chip size [10]. Fig. 2(a) presents the developed switch schematic based on lumped element  $\Pi$  networks, in which the influence of parasitic junction capacitance is decreased to achieve satisfactory performance [13]. The module can be switched between the TX and RX modes with suitable control of the operating conditions of the transistors  $M_1$  and  $M_2$ . In the TX mode, as shown in Fig. 2(b), the transistor  $M_1$  is turned off and modeled as an off-capacitance  $C_{off1-1}$ . Therefore, the transistor  $M_1$ , together with  $L_{1-1}$  and  $C_{1-1}$ , acts as a equivalent  $\lambda/4$  transmission line to allow the transmitted signal from the Tx port to pass through it to the antenna port. At the same time, the transistor  $M_2$  operates in the opposite condition and is regarded as a on-resistance  $R_{on2-1}$ . The inductor  $L_{2-1}$  and the capacitor  $C_{2-1}$  form a parallel resonant tank that prevents the transmitted signal from leaking into the Rx port. The capacitors  $C_{1-1}$  and  $C_{2-1}$  can be merged into a single shunt capacitor  $C$  for their parallel connection. The entire circuit in the TX mode consists of a series of equivalent  $\Pi$  networks connected to a parallel resonant tank. The same approach can be used to analyze the operation in the RX mode, as shown in Fig. 2(c).

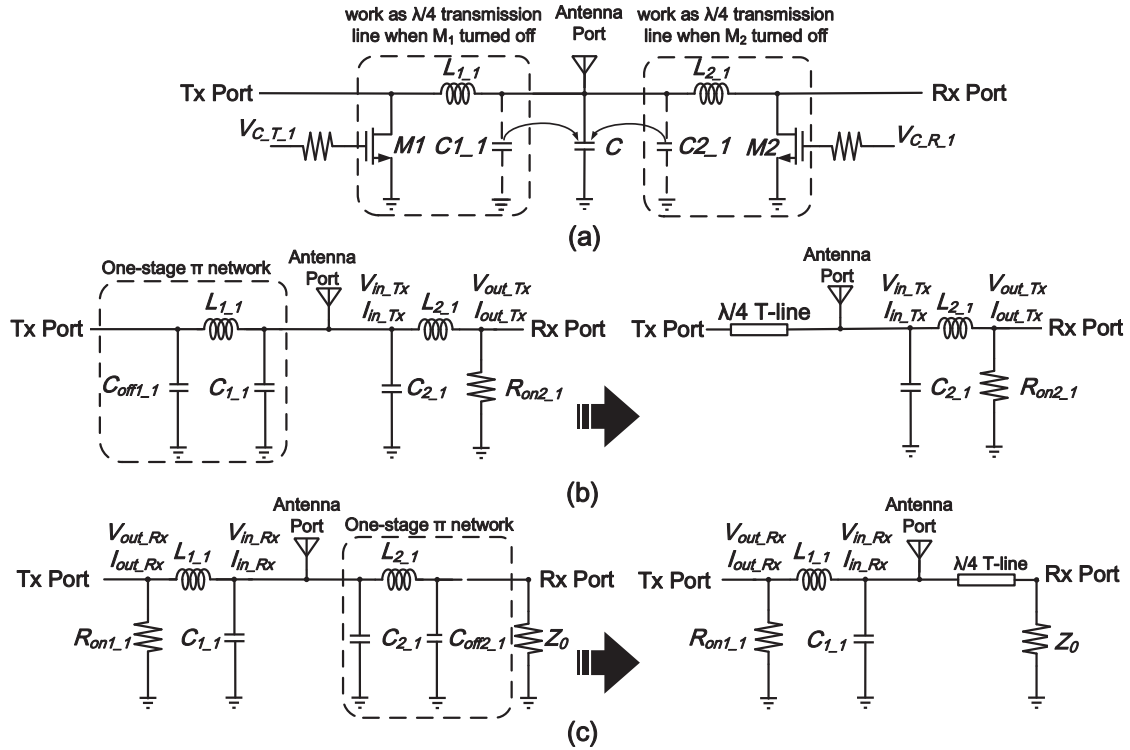
### A. ISOLATION ANALYSIS OF A ONE-STAGE $\Pi$ -TYPE T/R SWITCH

The Tx port of the switch is usually connected to a power amplifier (PA), and the Rx port is usually connected to a low noise amplifier (LNA). In the TX mode, to protect the LNA, the power leaking into the Rx port should be no more than the maximum allowed input power of the LNA; meanwhile, the transmitted signal is typically at a high power level. For this reason, the T/R switch should have high isolation between the Tx and Rx ports. Fig. 2(b) and (c) show the equivalent circuits for the estimation of the isolation in the TX mode and RX mode, respectively. In Fig. 2(b), for easy evaluation of the isolation of the switch, under the assumption that the  $\Pi$  network in the Tx-Antenna branch functions as a  $\lambda/4$  T-line with a characteristic impedance of  $Z_0$  and the antenna port is terminated with a matched impedance  $Z_0$ , the three-port network is transformed into a two-port network. Therefore, the isolation of the switch in the TX mode can be calculated as follows:

$$ISO = -20 \log \left| \frac{V_{out\_TX}}{V_{in\_TX}} \right| \quad (3)$$

The relationship between  $V_{out\_TX}$  and  $V_{in\_TX}$  can be expressed by using an ABCD matrix, as shown in (4) and (5), as shown at the bottom of the next page:

$$\begin{bmatrix} V_{out\_TX} \\ I_{out\_TX} \end{bmatrix} = \begin{bmatrix} A & B \\ C & D \end{bmatrix} \begin{bmatrix} V_{in\_TX} \\ I_{in\_TX} \end{bmatrix} \quad (4)$$



**FIGURE 2.** Switch schematics based on one-stage  $\Pi$  networks: (a) Small-signal equivalent circuit. (b) Small-signal equivalent circuit in the TX mode. (c) Small-signal equivalent circuit in the RX mode.

Because the inductor  $L_{2,1}$  and the capacitor  $C_{2,1}$  form a parallel resonant tank at the operating frequency,

$$\omega L_{2,1} \approx \frac{1}{\omega C_{2,1}} \approx Z_0 \quad (6)$$

The ABCD matrix given in (5) can be simplified to

$$\begin{bmatrix} A & B \\ C & D \end{bmatrix} = \begin{bmatrix} 1 + \frac{j\omega L_{2,1}}{R_{on2,1}} & j\omega L_{2,1} \\ \frac{1}{Z_0} + \frac{j\omega L_{2,1}}{Z_0 R_{on2,1}} + j\omega C_{2,1} & \frac{j\omega L_{2,1}}{Z_0} \end{bmatrix} \quad (7)$$

Thus, the isolation in (3) is calculated as follows:

$$\begin{aligned} ISO &= -20 \log \left| \frac{V_{out\_TX}}{V_{in\_TX}} \right| \\ &= -20 \log \left| \frac{2}{A + B/Z_0 + CZ_0 + D} \right| \\ &= -20 \lg 2 + 20 \lg \left| 2 + j \left( \frac{2\omega L_{2,1}}{R_{on2,1}} + \frac{2\omega L_{2,1}}{Z_0} + \omega C_{2,1} Z_0 \right) \right| \\ &\approx 20 \lg \frac{\omega L_{2,1}}{R_{on2,1}} \end{aligned} \quad (8)$$

The isolation value depends on the ratio of the impedance of inductor  $L_{2,1}$  to the on-resistance  $R_{on2,1}$  of the transistor,

namely,  $\omega * L_{2,1} / R_{on2,1}$ . At 16.5 GHz, when the antenna terminal impedance  $Z_0$  is 50  $\Omega$ ,

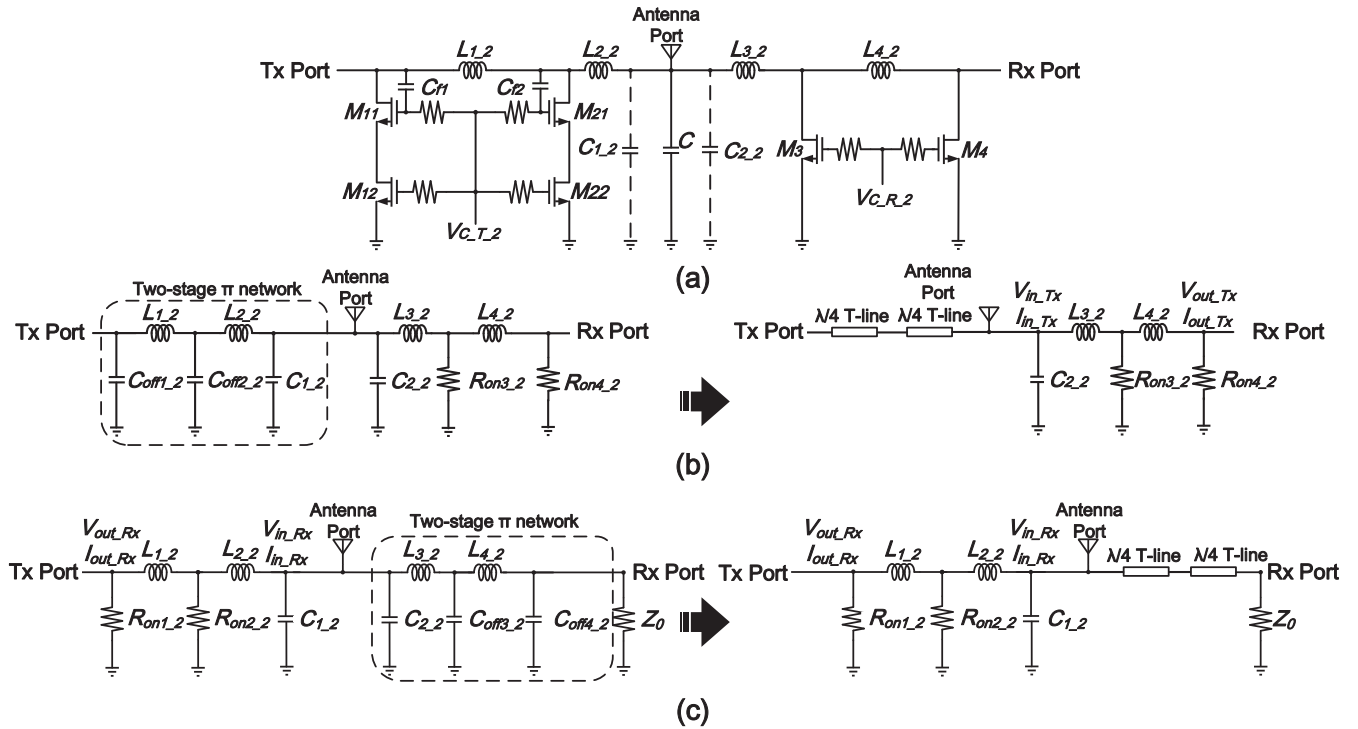
$$\begin{cases} C_{off1,1} = C_{1,1} = C_{2,1} = 193 \text{ fF} & (9) \\ L_{1,1} = L_{2,1} = 483 \text{ pH} & (10) \end{cases}$$

For the 180 nm bulk CMOS process used in the design, in order to realize an off-capacitance value  $C_{off1,1}$  of 193 fF, the total gate width of  $M_1$  is chosen to be 192  $\mu m$ , with a gate length of 180 nm. Due to the symmetry of the switch in the TX and RX modes, as shown in Fig. 2(b) and (c), the total gate width of  $M_2$  is also 190  $\mu m$ , corresponding to an  $R_{on2,1}$  of 4  $\Omega$ . Therefore, the isolation result as expressed in (8) is usually approximately 20~24 dB at 16.5 GHz, which is not sufficiently high to protect the LNA. In general, the isolation of a T/R switch in the TX mode is required to be greater than 30 dB [9], [14], [15].

### B. ISOLATION ANALYSIS OF A TWO-STAGE $\Pi$ -TYPE T/R SWITCH

To increase the isolation between the Tx and Rx ports in the TX mode, a design for a two-stage  $\Pi$ -type T/R switch is proposed, as shown in Fig. 3(a). Because of the use of two-stage

$$\begin{aligned} \begin{bmatrix} A & B \\ C & D \end{bmatrix} &= \begin{bmatrix} 1 & 0 \\ 1/Z_0 & 1 \end{bmatrix} \begin{bmatrix} 1 & 0 \\ j\omega C_{2,1} & 1 \end{bmatrix} \begin{bmatrix} 1 & j\omega L_{2,1} \\ 0 & 1 \end{bmatrix} \begin{bmatrix} 1 & 0 \\ 1/R_{on2,1} & 1 \end{bmatrix} \\ &= \begin{bmatrix} 1 + \frac{j\omega L_{2,1}}{R_{on2,1}} & j\omega L_{2,1} \\ \frac{1}{Z_0} + \frac{j\omega L_{2,1}}{Z_0 R_{on2,1}} + j\omega C_{2,1} + \frac{1 - \omega^2 L_{2,1} C_{2,1}}{R_{on2,1}} & 1 - \omega^2 L_{2,1} C_{2,1} + \frac{j\omega L_{2,1}}{Z_0} \end{bmatrix} \end{aligned} \quad (5)$$



**FIGURE 3.** Switch schematics based on two-stage  $\Pi$  networks: (a) Small-signal equivalent circuit. (b) Small-signal equivalent circuit in the TX mode. (c) Small-signal equivalent circuit in the RX mode.

$\Pi$  networks while the inductor  $L_{3,2}$  and the capacitor  $C_{2,2}$  form a parallel resonant tank at the operating frequency, the following expressions hold:

$$\begin{cases} R_{on4,2} = 2R_{on3,2} & (11) \end{cases}$$

$$\begin{cases} L_{3,2} \approx L_{4,2} & (12) \end{cases}$$

$$\begin{cases} \omega^2 L_{3,2} C_{2,2} \approx 1 & (13) \end{cases}$$

The ABCD matrix for Fig. 3(b) as expressed in (14), as shown at the bottom of this page, is still used to calculate the isolation. Thus, the isolation for Fig. 3(b) is calculated as follows:

$$\begin{aligned} ISO &= -20 \log \left| \frac{V_{out\_TX}}{V_{in\_TX}} \right| \\ &= -20 \log \left| \frac{2}{A + B/Z_0 + CZ_0 + D} \right| \\ &\approx -20 \lg 2 + 20 \lg \left| \frac{4\omega^2 L_{3,2}^2}{R_{on4,2}^2} \right| \\ &= 20 \lg 2 + 40 \lg \frac{\omega L_{3,2}}{R_{on4,2}} \end{aligned} \quad (15)$$

The  $\Pi$  networks in Fig. 2(b) and Fig. 3(b) have the same characteristic impedance  $Z_0$ ; therefore,

$$\begin{cases} L_{2,1} = L_{3,2} & (16) \end{cases}$$

$$\begin{cases} R_{on2,1} = R_{on4,2} & (17) \end{cases}$$

As seen from a comparison of (8) and (15), the two-stage  $\Pi$ -type T/R switch has a better isolation value, which is  $20 \lg(\omega * L_2 / R_{on2})$  larger than that of its one-stage  $\Pi$ -type counterpart. The IL and isolation between two configurations using 180 nm triple-well CMOS technology have been simulated with the Agilent's simulation software advanced design system (ADS). As shown in Fig. 4, between 14 and 25 GHz, although the IL of two-stage  $\Pi$ -type configuration is 0.8 dB larger than one-stage configuration, the two-stage configuration has an isolation value that is 20~25 dB higher than that of its one-stage counterpart which is in agreement with the theoretical calculations. Switches have a trade-off between insertion loss and isolation. The two-stage configuration has high isolation at the cost of an insertion loss higher than that of the one-stage configuration. Between the desired

$$\begin{aligned} \begin{bmatrix} A & B \\ C & D \end{bmatrix} &= \begin{bmatrix} 1 & 0 \\ 1/Z_0 & 1 \end{bmatrix} \begin{bmatrix} 1 & 0 \\ j\omega C_{2,2} & 1 \end{bmatrix} \begin{bmatrix} 1 & j\omega L_{3,2} \\ 0 & 1 \end{bmatrix} \begin{bmatrix} 1 & 0 \\ 1/R_{on3,2} & 1 \end{bmatrix} \begin{bmatrix} 1 & j\omega L_{4,2} \\ 0 & 1 \end{bmatrix} \begin{bmatrix} 1 & 0 \\ 1/R_{on4,2} & 1 \end{bmatrix} \\ &= \begin{bmatrix} 1 + \frac{4j\omega L_{3,2}}{R_{on4,2}} - \frac{2\omega^2 L_{3,2}^2}{R_{on4,2}^2} & 2j\omega L_{3,2} - \frac{2\omega^2 L_{3,2}^2}{R_{on4,2}} \\ \frac{4j\omega L_{3,2}}{R_{on4,2}} + \frac{1}{Z_0} - \frac{1}{R_{on4,2}} + j\omega C_{2,2} - \frac{2\omega^2 L_{3,2}^2}{R_{on4,2}^2} & -1 + \frac{2j\omega L_{3,2}}{Z_0} - \frac{2\omega^2 L_{3,2}^2}{Z_0 R_{on4,2}} \end{bmatrix} \end{aligned} \quad (14)$$

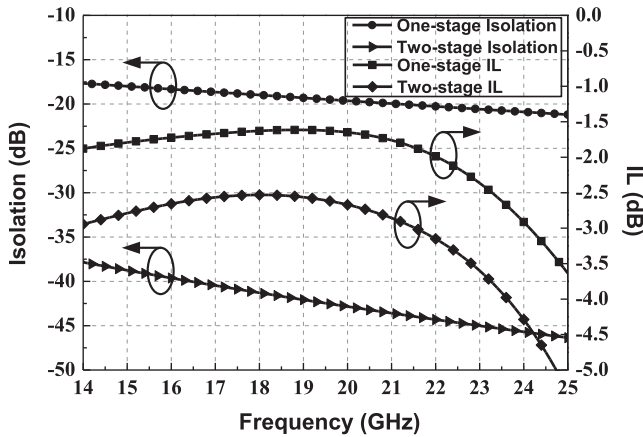


FIGURE 4. Simulated isolation and IL results for the two-stage  $\Pi$ -type and one-stage  $\Pi$ -type configurations.

frequency 15-17 GHz, in order to achieve larger than 30 dB isolation value, the two-stage  $\Pi$ -type configuration is chosen with an acceptable IL around 2.5 dB [16].

### C. IMPROVEMENT OF THE POWER-HANDLING CAPABILITY

The power-handling capability is the main bottleneck for a T/R switch fabricated using the standard CMOS process. In the TX mode, the switch needs to be able to handle a high transmitted power. Therefore, the stacked transistors technique is used to prevent undesirable channel formation and to enable the switch to withstand higher voltage swings by dividing the large voltage swing at the antenna port between two transistors, which is beneficial for achieving a low breakdown voltage in standard CMOS devices [17].

The linearity of the switch is decided by two kinds of voltage level limitations. One is the threshold voltage and the other is the breakdown voltage [18]. The  $V_{ds}$  of each stacked transistors should be smaller than the breakdown voltage for reliable operation. But due to the gate coupling effect and the substrate coupling effect, the voltage cannot be evenly distributed on each transistor. Under normal conditions, the transistor nearer to the input source is subjected to a larger voltage swing than the other one. As shown in Fig. 5(a), the peak-to-peak voltage swing across  $M_{11}$  is around 3.6 V which is 1.2 V higher than that across  $M_{12}$ . This uneven distribution increases the risk of damage to the transistor nearer to the input source due to exceeding the highest breakdown voltage. As a result, the linearity and power-handling capability of the switch degrades. To realize an even voltage distribution, feed-forward capacitors (FFCs)  $C_{f1}$  and  $C_{f2}$ , as shown in Fig. 3, are used to increase the conductance across the gate and drain of the first transistors,  $M_{11}$  and  $M_{21}$  [19], [20]. Fig. 5 shows a comparison of the simulated results with and without FFCs. With the help of FFCs of 288 fF, the voltage drop difference between transistors  $M_{11}$  and  $M_{21}$  is reduced from 1.2 V to 0.4 V at 16 GHz, indicating that an even voltage distribution is

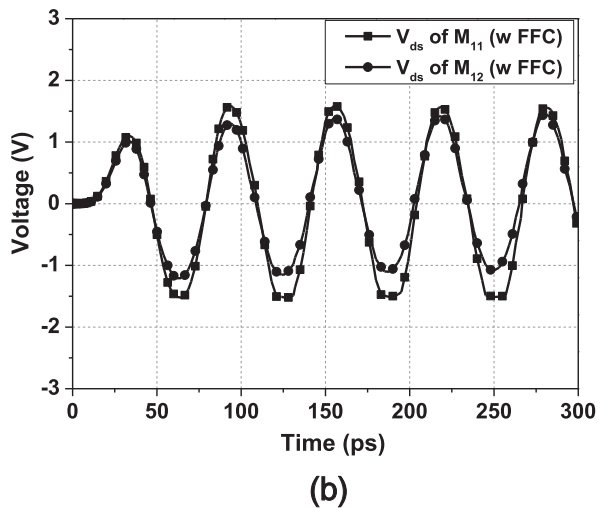
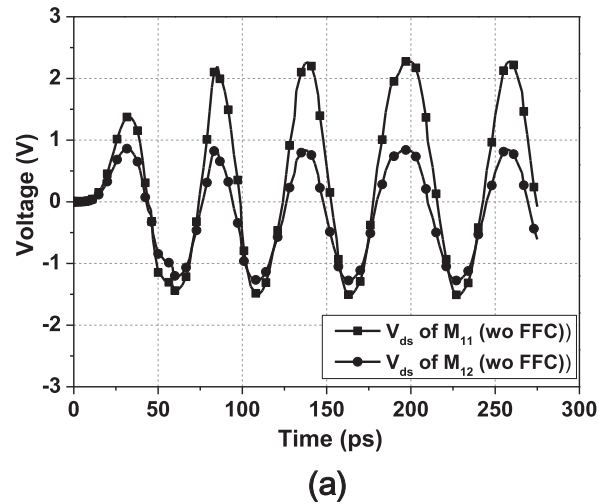


FIGURE 5. Simulation comparison between voltage drops on each stacked transistors: (a) without FFC and (b) with FFC.

realized. This modification of the voltage distribution enables the stack to endure a larger voltage drop before the breakdown of the first transistor. Meanwhile, due to the elimination of series transistors in the entire circuit, an effective trade-off between a high power-handling capability in the TX mode and a low insertion loss in the RX mode can be achieved.

### III. EXPERIMENTAL RESULTS

The proposed T/R switch based on the two-stage  $\Pi$ -type configuration was implemented using standard 180 nm triple-well CMOS technology. The buried deep N-well in triple-well process separates the body of nMOS from the substrate [21]. Therefore, the substrate coupling effect can be reduced. At the same time, the added deep N-well layer creates two pn-junction diodes to prevent a breakdown in isolation between the p-well, deep n-well and p-substrate [22]. For compact chip size and high isolation, the off-state capacitance value used to constitute equivalent  $\lambda/4$  transmission

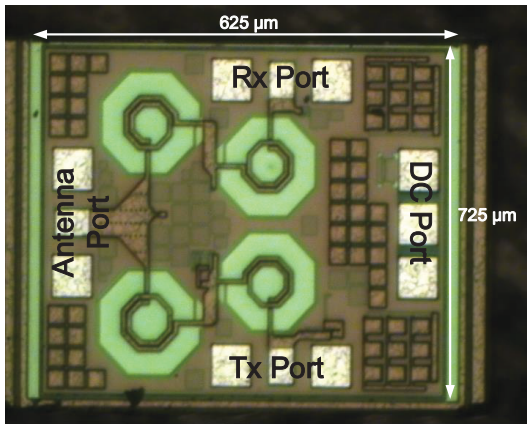


FIGURE 6. Microscopic image of the fabricated T/TR switch chip.

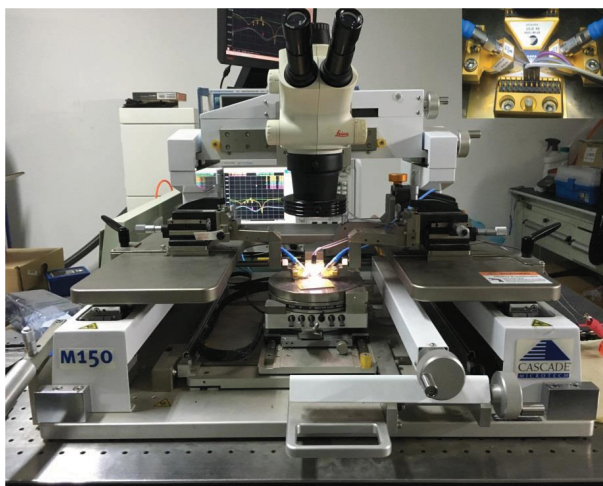
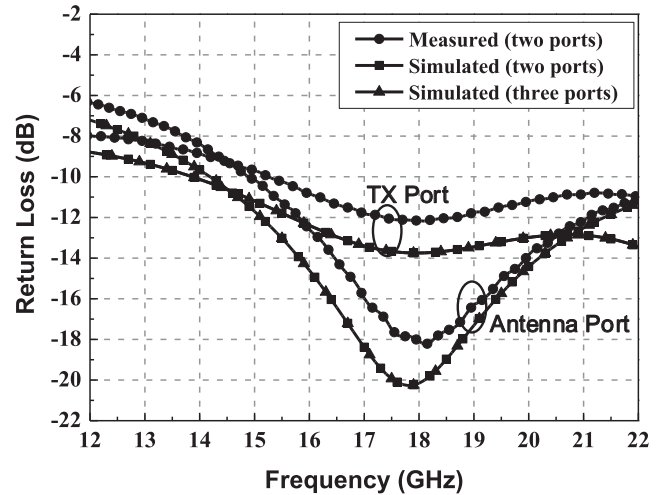


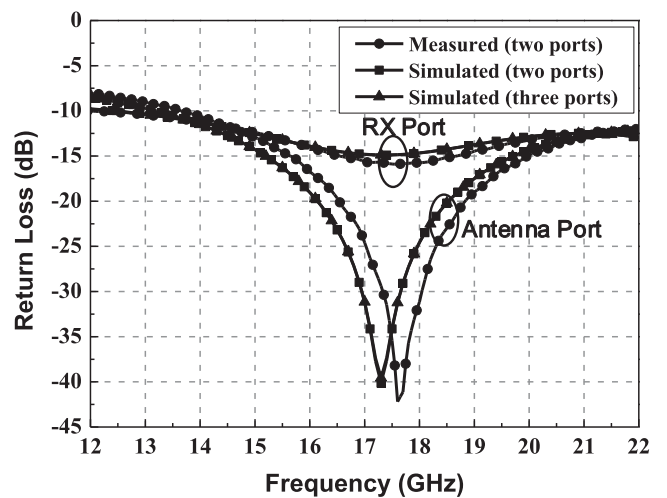
FIGURE 7. Photograph of the T/TR switch chip test bench.

lines should be decided firstly. The off-state capacitance value of 193 fF is chosen that equal to 50 Ω at 16 GHz. Then, the balance between the power-handling capability and IL should be made. The T/R switch needs to undergo high output power in the TX mode and achieve low IL in the RX mode, respectively. The stacked structure increases the power-handling capability with inevitable drawback of IL increasing. So the stacked structure is only employed in the TX channel. Finally, a trade-off is needed to consider between linearity and isolation. In order to improve the linearity, the FFCs are used. But large FFCs increase the total conductance of the stack that degrades the isolation [19]. Therefore, the FFCs of 288 fF are chosen to make a balance between the linearity and isolation. Table 1 lists the transistor dimensions and passive element values of the proposed T/R switch.

The fabricated CMOS T/R switch, as shown in Fig. 6, had a die area of 625 μm \* 725 μm, including three sets of ground-signal-ground (GSG) pads and one set of pass-ground-pass (PGP) pads. Measurements were conducted on the chip using a vector network analyzer and a Cascade probe



(a)



(b)

FIGURE 8. Measured versus simulated return loss results in (a) TX mode and (b) RX mode.

TABLE 1. Circuit element values of the proposed T/R switch.

Circuit Element	Element Value
$M_{11}, M_{12}$	384 μm / 180 nm
$M_{21}, M_{22}$	768 μm / 180 nm
$M_3$	384 μm / 180 nm
$M_4$	192 μm / 180 nm
$L_{1,2}, L_{2,2}, L_{3,2}, L_{4,2}$	475 nH
$C_{f1}, C_{f2}$	288 fF
$C$	370 fF
$V_{C\_T\_2}$	1.8 V (on), 0 V (off)
$V_{C\_R\_2}$	1.8 V (on), 0 V (off)

station, as shown in Fig. 7. Limited by the test conditions, the parameters of the switch in different modes were obtained only by applying a pair of RF probes to two ports, with

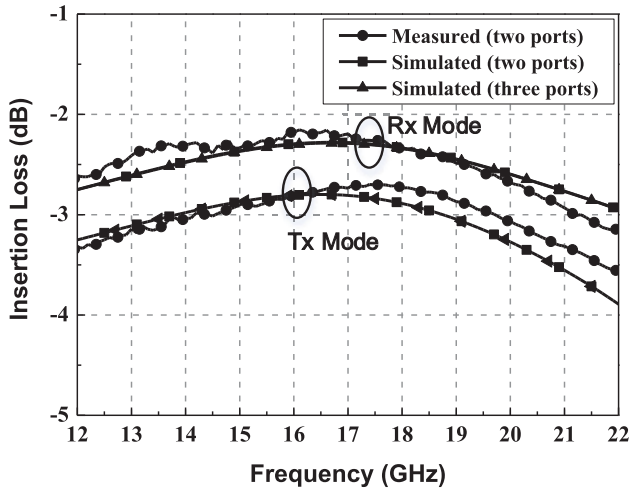


FIGURE 9. Measured versus simulated insertion loss results in the TX mode and the RX mode.

one idle open port, which should have been set to  $50 \Omega$ . Therefore, the measured results will differ from those in the case of a  $50 \Omega$  load termination, especially the isolation results. However, from a comparison of the measured and simulated results, the performance of the T/R switch can be deduced. Such comparisons were performed between the measured results, simulated two-port results with an idle open port and simulated three-port results with the remaining port terminated at  $50 \Omega$ .

The return losses in both modes, as shown in Fig. 8, are better than 10 dB at 15-22 GHz. When simulated IL, no matter the third port is opened or connected to  $50 \Omega$ , it is shorted by adjacent small on-resistance  $R_{on4,2}$  or  $R_{on1,2}$  as shown in Fig. 3(b) and (c) that is only  $4 \Omega$ . Therefore, the two-ports and three-ports simulated IL results are the same. As shown in Fig. 9, from 15 to 18 GHz, the measured RX-mode IL (between the Ant and Rx ports) is approximately 2.3 dB, and the TX-mode IL (between the Ant and Tx ports) is 2.7 dB, consistent with the simulation. The measured isolations in the RX and TX modes are plotted in Fig. 10, from which isolations of 25 dB in the RX mode and 34 dB in the TX mode are observed. The measured isolations in both modes are close to those simulated under the two-port condition because of the identical load conditions but show a discrepancy from the simulated three-port condition. The potential cause of this discrepancy is that the transmitted or received power that should have mainly gone into the port with the  $50 \Omega$  load is instead reflected back because of the idle open port and leaks into the isolation port. Therefore, the measured isolation of the switch is 6 dB worse than that simulated under the three-port condition. In practical application, all of the switch ports will be matched to bring the isolation results closer to those simulated under the three-port condition. The measured  $P_{out}$  values in the TX mode are plotted versus  $P_{in}$  in Fig. 11, from which an  $IP_{1dB}$  of 22 dBm at 17 GHz can be extracted.

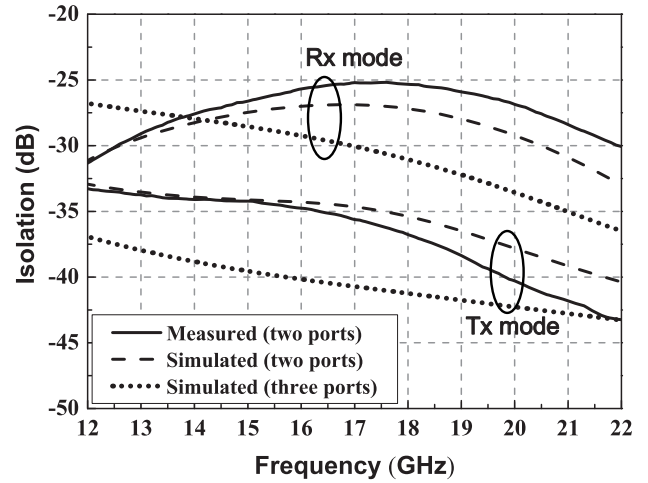


FIGURE 10. Measured versus simulated isolation results in the TX mode and the RX mode.

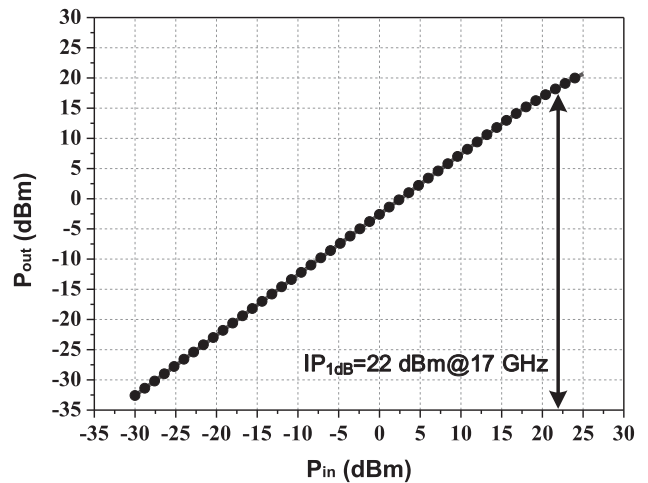


FIGURE 11. Measured  $IP_{1dB}$  results at 17 GHz.

The performance of the proposed T/R switch is summarized in Table 1 together with the performance characterizations of other reported CMOS switches. Compared with the others, the T/R switch designed here demonstrates an acceptable insertion loss, high isolation and good power-handling capability. It is recognized that the IL performance of this work is a little higher for high efficiency RF transceiver applications. In order to realize full integrated transceiver and achieve low-cost, some sacrifices in circuit performance may be inevitable [27]. This is the price to pay for minimum size and cost using CMOS process, particularly using low-cost 180 nm process with  $f_t/f_{max}$  of 53 GHz/56 GHz [28]. When the advanced process such as  $0.13\text{-}\mu\text{m}$ , 90 nm, and 65 nm CMOS process used to realize this high isolation switch, as the channel length of CMOS transistor becomes smaller, the on-resistance  $R_{on}$  decreases and results in lower IL [8]. Because of ease integration, the high-isolation T/R switch designed here has been integrated in the Ku band 4-element phased array transceiver [29].

**TABLE 2. Comparison of the proposed Ku-band cmos T/R switch with other reported works.**

Ref	Process	Freq (GHz)	IL (dB)	ISO (dB)	ISO-IL (dB)	IP <sub>1dB</sub> (dBm)	Return Loss (dB)	Chip Size (mm <sup>2</sup> )	Topology
[23]	0.18- $\mu$ m BiCMOS	17.2-27.3	>4.5 (RX) >6.7 (TX)	>16 (RX) >18.2 (TX)	>11.5 (RX) >11.5 (TX)	15.4@24 GHz	<8	1.15	LC networks
[24]	45-nm SOI CMOS	14-18	0.6-0.78	15-18	14.4-17.2	31.5@14 GHz	<-15	0.009*	Stacked transistors
[25]	90-nm triple-well CMOS	24	3.5 (RX) 3.4 (TX)	16 (RX) 22 (TX)	12.5 (RX) 19.6 (TX)	28.7@24 GHz	<-7	0.0176*	Floating well
[26]	0.13- $\mu$ m CMOS	15	1.8 (TX)	17.8	16	21.5@15 GHz	<-7	0.25	Impedance transformer
This work	0.18- $\mu$ m triple-well CMOS	15-18	>2.3 (RX) >2.7 (TX)	>25 (RX) >34 (TX)	>22.7 (RX) >31.3 (TX)	22@17 GHz	<-10 (RX) <-10 (TX)	0.45	2-stage $\Pi$ -type networks

\* Core area size without testing pads.

#### IV. CONCLUSION

The Ku-band T/R switch topology has been presented and analysed. The switch based on equivalent transmission line structure absorbs parasitic capacitors into the impedance matching structure. Since the developed switch achieves high isolation and good power-handling capability, it can be easily customized to integrate with other components using the standard CMOS process to realize a T/R module on one chip.

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