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A Design Strategy for AM/PM Compensation in GaN Doherty Power Amplifiers

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ABSTRACT This paper presents the theoretical analysis of phase distortion (AM/PM) mechanisms in Gallium Nitride (GaN) Doherty power amplifiers (DPAs) and a novel approach to optimize the tradeoff between linearity and efficiency. In particular, it is demonstrated how it is possible to mitigate the AM/PM by designing a suitable mismatch at the input of the active devices, based on the identification of constant AM/PM and gain contour circles. The proposed theory is experimentally confirmed by source- and load-pull measurements and further validated through the design and realization of a 7 GHz 10 W DPA based on GaN monolithic technology.

INDEX TERMS Doherty power amplifiers, gallium nitride, linearity, electronically tunable networks.

I. INTRODUCTION

Power amplifiers (PAs) are the most critical components in microwave radios, since their linearity strongly affects the quality of the transmitted signal, and their power consumption strongly influences the overall system power budget [1], [2].

To cope with the users' demand for increasingly higher data-rates, modern wireless communication systems adopt complex digital modulation schemes that pose severe linearity constraints on the PA forcing the operation at an average output power that is far from the maximum, i.e. in back-off (BO) condition. This in turns poses challenging requirements on efficiency that should be maintained as high as possible also in BO, in contrast with the usually poor BO efficiency of classical class-AB PAs. To overcome this limitation, the Doherty Power Amplifier (DPA) architecture has emerged as the most suitable solution to achieve high BO efficiency [3]–[6]. Since fabricated DPAs are rather non-linear [7]–[10], they are typically employed in conjunction with digital predistortion (DPD), in order to fulfill linearity constraints [11]. In particular, while amplitude distortion (AM/AM) can be effectively modelled with static models [12] and thus compensated by simple memoryless DPDs (e.g. look-up-table), phase distortion (AM/PM) is a major issue of DPA [10] and leads to the adoption of complex and powerful DPDs.

Such combination of DPD and DPA techniques proved to effectively yield notable BO efficiency enhancement with respect to class-AB solutions in the base-station market, where the required power levels are in the order of hundreds of watts. However, a very different scenario occurs instead in point-to-point microwave links, where power levels are usually limited to tens of watts. In this framework, the adoption of complex DPD-based linearizers could be not convenient in terms of overall power budget and, as a consequence, the effective advantages of DPAs with respect to class-AB PAs are still questionable [13].

The development of efficient DPAs topologies with minimal distortions, allowing for minimum-complexity DPD schemes to be employed, is therefore crucial to enable the widespread adoption of the DPA architecture in this field of applications. Moreover, the need of low-distortion DPAs is expected to be further emphasized by the introduction of the 5G mobile standard, due to the foreseen adoption of antenna arrays based on a large number of low power integrated PAs working at carrier frequencies in the microwave and millimetre-wave range [14].

This work proposes a novel design approach to optimize the trade-off between power gain and linearity in Gallium Nitride (GaN [15]) DPAs. The theoretical analysis, based on a simplified representation of the DPA architecture, led to a novel formulation for the amplitude to phase modulation distortion (AM/PM) generation mechanism, underlying its relationship with the input matching condition of the devices. Based on this result, constant AM/PM contours can be derived and used, in conjunction with constant gain ones, to find an optimum mismatching condition for AM/PM reduction. The proposed approach is experimentally validated with source- and load-pull measurements on a GaN device, and tested by the design and characterization of a demonstrator, a GaN Microwave Monolithic Integrated Circuit (MMIC) DPA, first presented by Giofrè *et al.* [16]. The MMIC is equipped with electronically controlled switches, which also provide the possibility to modify the input matching conditions of the devices and thus to verify the effect of mismatch on the amplifier behavior. Both MMICs are designed at 7 GHz targeting 10W output power, in accordance with microwave backhaul specifications [17]. They include only one stage: this choice, even if yielding to low power gain, was made to avoid any possible cross-effect that a driver stage may introduce, affecting the validity of the results in terms of theory verification.

II. PHASE DISTORTION IN GaN DPAs

Amplitude (AM/AM) and phase distortion (AM/PM) are two key parameters, defining the linearity of a power amplifier. While in class-AB PAs both AM/AM and AM/PM can be minimized simultaneously, for example by proper choice of bias point [9], in Doherty PAs this becomes difficult, or even impossible, due to the effect of load modulation [10]. As a consequence, in DPAs, AM/PM represents the major issue from the linearization point of view, since, contrary to AM/AM, it requires non-static DPD schemes [18].

A. AM/PM ANALYSIS

The proposed approach is based on some results available in literature [7]–[10], [19]–[23], of which a brief compendium is reported in the following for sake of clarity. Then, a novel formulation, underlying the relationship between AM/PM and the active devices' input matching conditions, is reported. Finally, based on this theoretical analysis, an effective design tool to trade-off between AM/PM and gain is introduced.

The theoretical analysis relies on a simplified device model similar to that presented in [8] and [10]. The simplifying assumptions follow the results obtained in [21], where, through a rigorous Volterra-series-based analysis, it was demonstrated that the sources of AM/PM distortion in a device can be mainly ascribed to the device intrinsic non-linear capacitors and the variation of the gain (i.e. of the transconductance g_m) from expansion to compression as input power increases.

The simplified PA scheme of Fig. 1(a) can be adopted for both the Main and the Auxiliary amplifiers of a DPA.

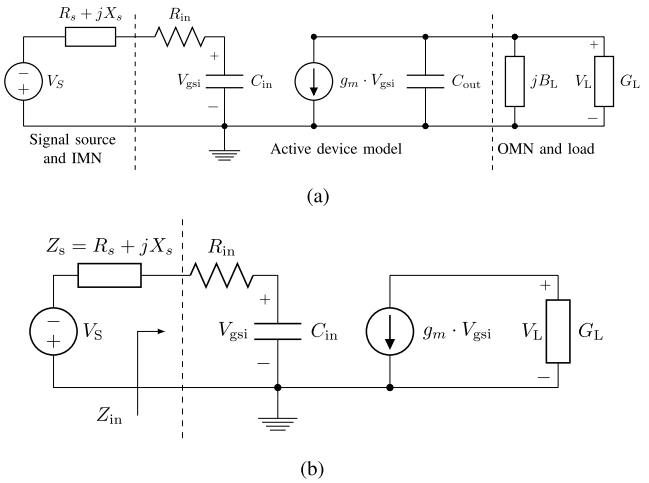

FIGURE 1. Power amplifier model: (a) first circuit, with Miller approximation applied and (b) final circuit.

The active device is modelled through a voltage controlled current source $g_m \cdot V_{gsi}$, while an input resistance R_{in} is inserted to account for both the device resistive parasitics and the losses introduced by the stabilization network. The device intrinsic capacitances are represented with an input and output equivalent capacitances, C_{in} and C_{out}, obtained according to Miller's approximation as [8], [24]:

$$C_{in} = C_{gs} + C_{gd}\left(1 + \frac{g_m}{G_L}\right) \tag{1}$$

$$C_{out} = C_{ds} + C_{gd}\left(1 + \frac{G_L}{g_m}\right) \tag{2}$$

where G_L is the equivalent load conductance, and C_{GS}, C_{DS}, and C_{GD} are the intrinsic device capacitances. The output matching network (OMN) is assumed to be lossless and is represented by a susceptance B_L in parallel to the load G_L. The input matching network (IMN) is modeled by a complex impedance $Z_S = (R_S + jX_S)$ in series with the input RF source V_S.

A further model approximation can be achieved by considering linear capacitances and transconductance. This assumption allows to directly figure out the link between causes and effects in the AM/PM mechanisms, with negligible loss in accuracy with respect to a complete non-linear model, as demonstrated in [7] and [25]. Moreover, at the operating frequency, and under the linear approximation assumption, it is possible to find the proper value of B_L that compensates the reactive behavior of C_{out}. This assumption is supported by the fact that the G_L/g_m ratio is much lower than unity in the frequency range where device acts as an amplifier [8]. The resulting simplified model to be considered is shown in Fig. 1(b).

By applying Kirchhoff's voltage law (KVL) at the circuit in Fig. 1(b) the phase of the output voltage V_L (with respect

to the input signal V_S) is obtained as:

$$\angle V_L = \text{atan}\left(\frac{R_S + R_{in}}{X_S - \dfrac{1}{\omega \cdot C_{in}}}\right) = \text{atan}\left(\frac{R_S + R_{in}}{X_S - \dfrac{G_L}{\omega[(C_{gs} + C_{gd})G_L + C_{gd}g_m]}}\right) \quad (3)$$

Any element of (3) that varies with the applied input power generates AM/PM distortion. In particular, it is possible to classify the sources of phase distortion in two categories:

1) *Technological*: These contributions are related to the active device physics, and thus common in all kind of current-mode amplifiers and mainly related to the variation of g_m, C_{gs}, and C_{gd} with the input power level.
2) *Behavioral*: these contributions are related to the particular PA architecture considered. In the specific case of the DPA, the load G_L is not constant, but modulated as a function of input power by the interaction between the main and auxiliary currents summing at the common node [3]. In particular, the load of the Main device swings from $G_{Lopt}/2$ to G_{Lopt}, while that of the Auxiliary device from infinity to $G_{Lopt,Aux}$. Therefore, in contrast with what happens in classical current mode class AB PA, a DPA would be still affected by a remarkable AM/PM, even if the adopted active devices were devoid of nonlinearities.

In [8] and [10], it was shown that the AM/PM of a DPA can be studied considering the AM/PM of the Main device alone.

Furthermore, according to the proposed model, the phase of the output voltage given by (3) shows an increasing monotonic behavior with respect to the load conductance G_L, that is in agreement with what experimentally shown in [20].

On these bases, the maximum AM/PM variation in a DPA can be evaluated as the difference between the phase of the output voltage at saturation and that in small-signal condition:

$$AM/PM = \angle V_L|_{G_L=G_{Lopt}} - \angle V_L|_{G_L=G_{Lopt}/2} \quad (4)$$

which is function of Z_S (see (3)), i.e., of the input matching network.

B. AM/PM VS. INPUT MATCHING FORMULATION

Referring to Fig. 1(b), the input impedance of the Main device is given by:

$$Z_{in}(G_L) = R_{in} - j\frac{G_L}{\omega[(C_{gs} + C_{gd})G_L + C_{gd}g_m]} \quad (5)$$

In a DPA such input impedance varies as the output conductance G_L is actively modulated by the Auxiliary device. Therefore, when designing the input matching network, it is possible to assure a conjugate matching condition only for a predefined value of G_L, i.e., only for a certain level of modulation. Assuming that the device is matched at saturation, that is when $G_L = G_{Lopt}$, then the impedance Z_S required to fulfill the complex conjugate matching condition is:

$$Z_S|_{match} = R_{in} + j\frac{G_{Lopt}}{\omega[(C_{gs} + C_{gd})G_{Lopt} + C_{gd}g_m]} \quad (6)$$

Substituting this value into (3) and then evaluating (4), the following equation can be obtained to describe the maximum AM/PM variation of a DPA:

$$AM/PM|_{match} = \text{atan}\left(\frac{\frac{G_{Lopt}}{(C_{gs}+C_{gd})G_{Lopt}+C_{gd}g_m} - \frac{G_{Lopt}}{(C_{gs}+C_{gd})G_{Lopt}+2C_{gd}g_m}}{2R_{in}\omega}\right) = \text{atan}\left(\frac{\frac{C_{gd}g_m G_{Lopt}}{4R_{in}\omega}}{\frac{(C_{gs}+C_{gd})^2 G_{Lopt}^2}{2} + \frac{3}{2}(C_{gs}+C_{gd})C_{gd}g_m G_{Lopt} + C_{gd}^2 g_m^2}\right) \quad (7)$$

Now, if a certain amount of mismatch with respect to the case of (6) is tolerated, two more degrees of freedom to improve the AM/PM distortion are gained. Introducing the additive quantity $Z_m = R_m + jX_m$ to represent the amount of mismatch, Z_S becomes

$$R_S = R_{in} + R_m \qquad X_S = \frac{G_{Lopt}}{\omega[(C_{gs} + C_{gd})G_{Lopt} + C_{gd}g_m]} + X_m \quad (8)$$

Then, by using these values in (3) and (4) and after some algebra rearrangement, the maximum AM/PM variation accounting for the presence of Z_m (i.e., in the mismatch case) turns out to be:

$$AM/PM|_{mismatch} = \text{atan}\left(\frac{2R_{in}(2R_{in} + R_m)\tan\Phi}{(2R_{in} + R_m)^2 + X_m(X_m + 2R_{in}\tan\Phi)}\right) \quad (9)$$

where $\Phi = AM/PM|_{match}$ is the AM/PM value resulting from (7), when the input of the Main device is matched at saturation.

The quantity resulting from (9) can be either higher or lower than Φ: this AM/PM formulation highlights the existing link between phase distortion and input matching condition of the Main device. It also allows to evaluate the achievable AM/PM improvement by accepting some mismatch (i.e., gain reduction).

C. EXPERIMENTAL VALIDATION OF THE PROPOSED FORMULATION

To validate the theoretical analysis, a dedicated source-pull measurement campaign was carried out. A single 8x150 μm GaN HEMT device from United Monolithic Semiconductors (more details in Section III), was experimentally characterized emulating the loading condition and hence the behavior of the Main stage of a DPA [9]. To this aim, two source-pull characterizations of the device were performed (at 7 GHz): the first with constant $G_{Lopt}/2$ load and

the second with constant G_{Lopt} load. In both cases, the phase of the output voltage with respect to the phase of the source was measured and the maximum AM/PM distortion was evaluated according to (4). The values of the device small-signal model, $R_{\mathrm{in}} = 1.9\,\Omega$, $C_{\mathrm{gs}} = 2.1\,\mathrm{pF}$, $C_{\mathrm{gd}} = 0.1\,\mathrm{pF}$ and $g_{\mathrm{m}} = 220\,\mathrm{mS}$, extracted from Scattering parameter measurements, were then used to calculate the theoretical AM/PM distortion. The real part of the optimum output conductance is G_{Lopt} =22 mS and, using (7), the AM/PM when the device is matched at the input to this value is 24°. In Fig. 2, the comparison between the measured and calculated constant AM/PM contours for different input impedances is shown: despite the simplifications adopted to extract the mathematical model, the agreement between the theoretical and the experimental curves is remarkable, thus indicating that the proposed theoretical approach is able to well approximate the actual evolution of the AM/PM in a DPA either with or without mismatch.

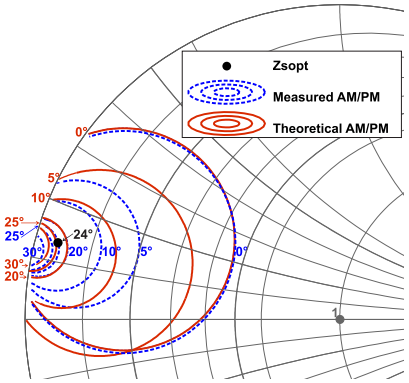

FIGURE 2. Comparison between measured and theoretical constant AM/PM curves for different input matching conditions.

D. AM/PM vs. MATCHING CONTOURS

Fig. 3 reports the same theoretical constant AM/PM contours of Fig. 2, together with the constant mismatch (i.e., constant insertion loss *IL*) contour curves, calculated as

$$IL = 10\log_{10}\left(1 - \left|\frac{Z_{\mathrm{S}} - Z_{\mathrm{Sopt}}}{Z_{\mathrm{S}} + Z^{*}_{\mathrm{Sopt}}}\right|^{2}\right) \tag{10}$$

IL quantifies the gain reduction resulting from mismatching the input impedance with respect to the matched case. As can be seen from Fig. 3, the proposed AM/PM formulation represents an effective design tool to identify the input mismatch that provides an optimum trade-off between AM/PM reduction and gain. For example, by accepting a gain reduction of 0.5 dB or 1 dB, the AM/PM can be reduced of 7° or 10°, respectively, while with 3 dB loss the AM/PM can be lowered down to 7.5°.

E. MATCHING IMBALANCE COMPENSATION

The introduction of some input mismatch in the Main path, if not properly compensated, leads to some drawback onto

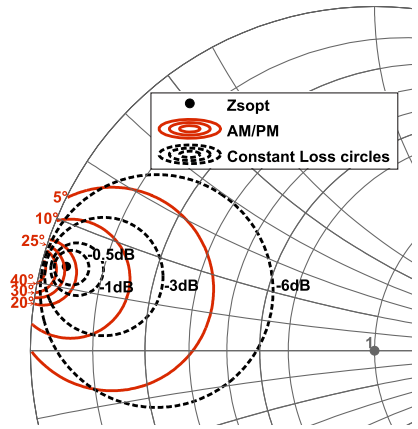

FIGURE 3. Constant AM/PM and mismatch contour curves. These contours can be used in the design phase to optimize the trade off between AM/PM and gain.

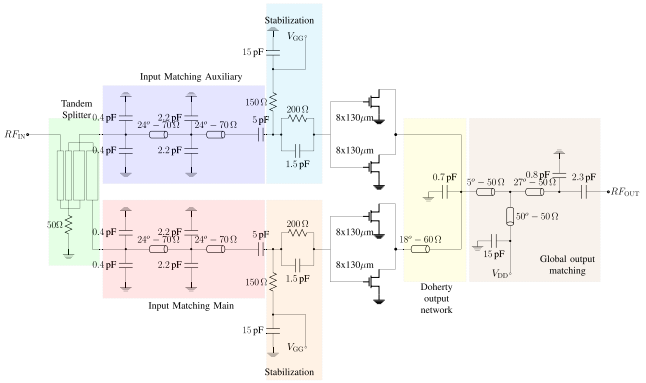

FIGURE 4. Electrical scheme of the DPA-F [13].

the other DPA features. In particular, it can cause either a worse load modulation, due to an early turning-on of the Auxiliary amplifier, or a phase imbalance between Main and Auxiliary paths. Both effects can be prevented by adding the same amount of mismatch at the input of the Auxiliary device. Therefore, once selected the input impedance for the best trade-off between AM/PM distortion and gain reduction, also the Auxiliary input matching network must be carefully optimized to keep the proper phase relation between the Main and Auxiliary output currents.

III. DPA DEMONSTRATORS

In order to validate the theoretical results at MMIC level, two GaN MMIC DPA modules based on the same technology were designed and characterized. The first (in the following referred as DPA-F), is a standard AB-C DPA, first presented by Giofrè *et al.* [13]. The second (referred as DPA-R), presented in [16], is a modified version of the same DPA, that includes electronically reconfigurable elements (HEMT switches) in the input network. In the following, the major design features of both DPAs are summarized.

The electrical schemes of the two modules are reported in Fig. 4 and Fig. 5. For both DPAs the 0.25 μm gate-length GaN

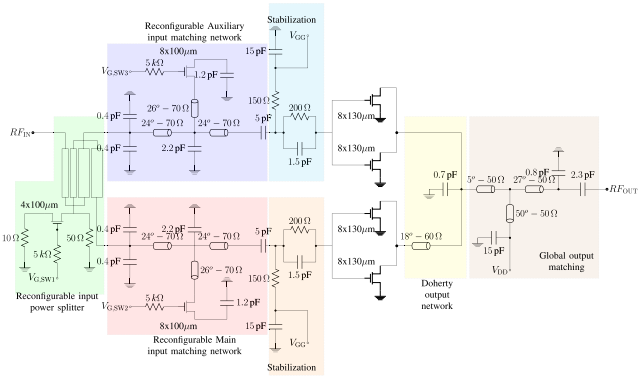

FIGURE 5. Electrical scheme of the DPA-R [16].

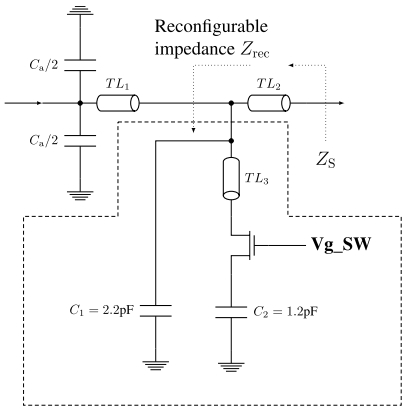

FIGURE 6. Reconfigurable IMN.

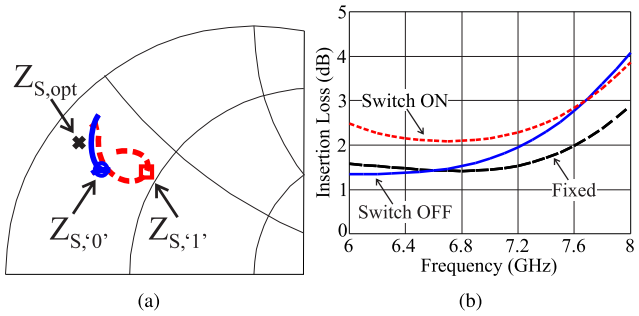

FIGURE 7. Reconfigurable IMN: (a) simulated impedance Z_S (see Fig. 6) and (b) simulated insertion loss (IL) in the OFF (blue) and ON (red dashed) state of the switch. In (b) the IMN IL of DPA-F is also reported (black long-dash), demonstrating that the switch does not introduce additional losses.

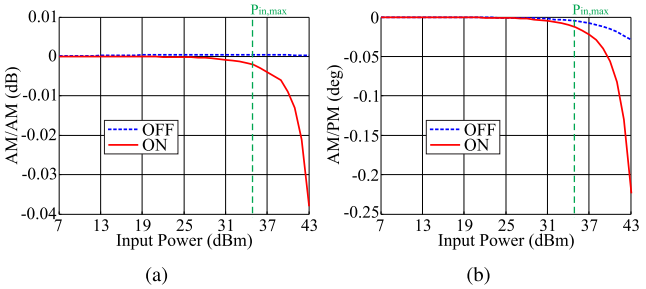

FIGURE 8. Simulated AM/AM (a) and AM/PM (b) of the reconfigurable IMN in the OFF (blue) and ON (red dashed) state of the switch.

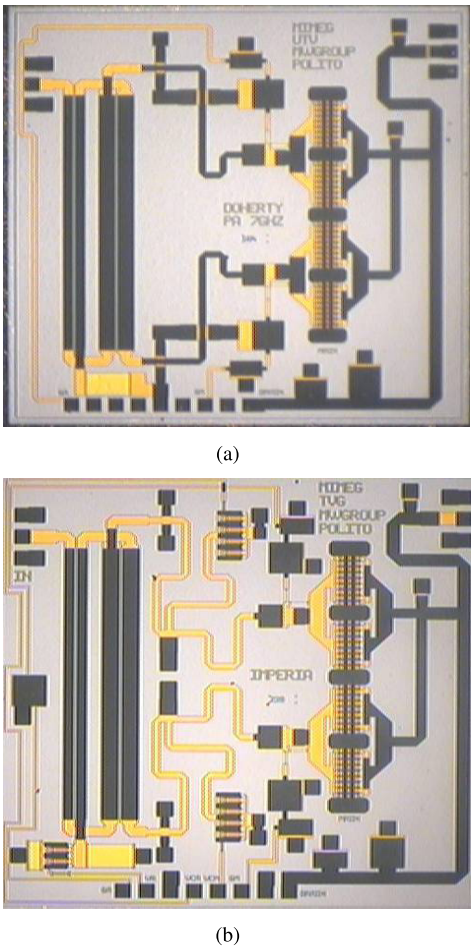

FIGURE 9. Microscope picture of the implemented DPAs: (a) DPA-F and (b) DPA-R. Chip size is 3 mm × 3 mm for both MMICs.

on SiC HEMT process (GH25-10) [26] from United Monolithic Semiconductors (UMS) was adopted, targeting a center frequency of 7 GHz and an output power of 10 W (40 dBm). Being the focus of this work the experimental verification of the presented theory, only the power stage has been designed, with a resulting low gain (7 dB). Accounting for the losses introduced by the output combiner, and for the available foundry models, the basic device selected was a $8\times130\,\mu$m HEMT, showing at 7 GHz an output power of ∼3 W in class-AB bias condition ($V_{DD} = 25$ V, $I_D = 33$ mA for $V_{GG} = -3.2$ V). Thus, to achieve the required output power, two of these devices are combined in a $2\times8\times130\,\mu$m macro-cell, adopted to implement both the Main and the Auxiliary stages, for a total DPA active periphery of $4\times8\times130\,\mu\text{m} = 4.16$ mm.

Concerning DPA-R, the reconfigurable elements adopted in the input networks are GaN HEMT switches, directly integrated in the same monolithic circuit of the DPA. Both the Main and Auxiliary IMNs can be independently modified by acting on two switches according to the structure shown

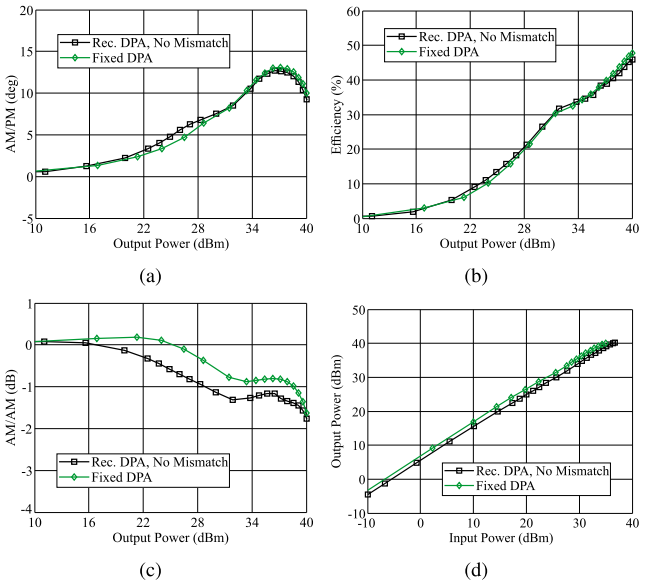

FIGURE 10. CW measurement results at 7 GHz. Reconfigurable DPA with no mismatch (black and squares) and fixed DPA (green and diamonds).

in Fig. 6: the two shunting capacitances of 2.2 pF, already present in DPA-F (see Fig. 4), are replaced with the structure reported in the dotted box in Fig. 6, implementing a reconfigurable capacitor.

When the switch is open (OFF state), the impedance Z_{rec} is given by the parallel of the fixed capacitance C_1 and the equivalent capacitance of the open-terminated transmission line TL_3. When the switch is closed (ON state), the equivalent capacitance changes due to the loading effect of C_2.

The adoption of such a variable capacitor allows to mismatch independently the Main and/or the Auxiliary devices of roughly 1 dB, by changing the impedance seen by the devices (Z_S in Fig. 6), as shown in Fig. 7. From the device point of view, when the switch is OFF, the matching network synthesizes a gate termination ($Z_{S,\text{'0'}}$) close to optimum impedance $Z_{S,\text{opt}}$. Conversely, when the switch is turned ON, the synthesized termination ($Z_{S,\text{'1'}}$) is shifted toward the centre of the Smith Chart, hence mismatching the corresponding stage.

For the switch implementation, an $8\times100\,\mu$m HEMT was selected, while the ON and OFF states are set providing 0 V and -25 V at the gate terminal, respectively. The device size and bias were properly selected to minimize distortion and losses introduced by the input network, which results negligible for the whole input power range, as reported in Fig. 8.

IV. EXPERIMENTAL RESULTS

The fabricated MMICs, shown in Fig. 9, were characterized with single-tone CW stimulus at 7 GHz, in order to verify the proposed design method and the agreement between measured and simulated results, the latter obtained exploiting the device foundry models. In all tests, the drain bias of the Main amplifier is 25 V, 80 mA, while that of the Auxiliary is 25 V, with gate voltage of -6.5 V.

Fig. 10 compares the measured AM/PM and efficiency *vs.* output power for both DPA-F and DPA-R, the latter in the matched configuration (all switches OFF, same conditions of DPA-F). The two MMICs show very similar performance, confirming that the introduction of the switches enables to test the proposed theory with a negligible degradation of performance.

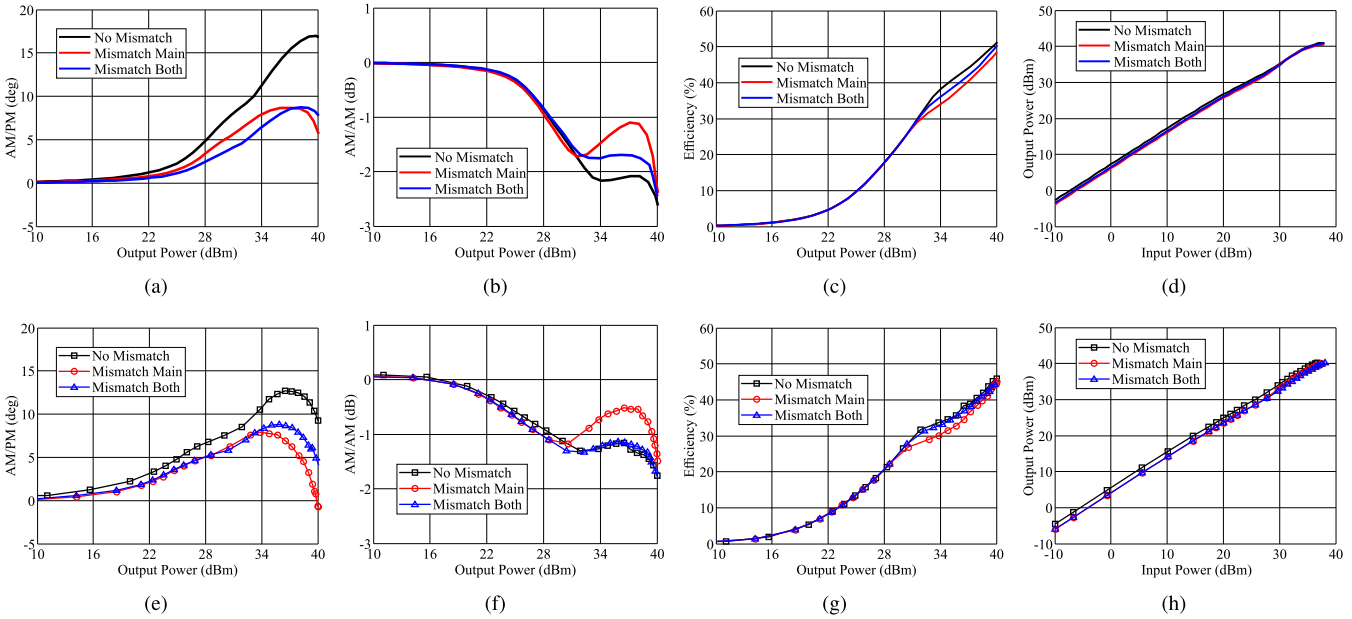

FIGURE 11. Reconfigurable DPA. Simulated (a-d) and measured (e-h) CW results at 7 GHz in different switch configurations: matched (black and squares), main mismatched (red and circles), main and auxiliary mismatched (blue and triangles).

Fig. 11 reports a summary of the CW results (measured and simulated) obtained on DPA-R in the three switch configurations of interest: 1) with no mismatch, 2) with 1 dB of mismatch introduced on the Main PA only (Main IMN switch ON, Auxiliary IMN switch OFF), and 3) with the same amount of mismatch on both Main and Auxiliary PAs (both IMN switches ON). A third switch, not discussed in this paper, controls the input splitting and it is in OFF state in these measurements, corresponding to equal splitting. Moreover, the case with mismatch on the Auxiliary only is also not discussed, because it is not related to a clear theoretical advantage in terms of linearity. More details on these other states can be found in [16].

The agreement between measurements and simulations is rather good, confirming the proposed theoretical approach relating input mismatch to DPA performance.

Phase distortion, reported in Fig. 11(a) and Fig. 11(e), is effectively reduced by input mismatch: the measured maximum value with no mismatch is around 13°, while it is reduced to 8° by introducing mismatch in the input path of the Main stage, corresponding to a relative AM/PM reduction of more than 30%. However, the mismatch applied to the Main PA only, significantly changes the AM/AM and reduces the back-off efficiency of around 4%-points, as shown in Fig. 11(b, f) and Fig. 11(c, g), respectively. Mismatching, instead, both the Main and Auxiliary PA leads to AM/AM and efficiency levels very similar to the condition without any mismatch, while AM/PM reduction is still presents, as it is 9° (see Fig. 11(e)). Evaluating the effect of this AM/PM reduction in terms of modulated signal measurement is a difficult task, because other effects comes into play especially with wideband modulations: further work is being done to address this aspect.

Finally, Fig. 11(d, h) show the output power *vs*. input power: in all configurations, the 10 W output power target is achieved, while the gain decreases, as expected, of around 1.5 dB when mismatch is applied.

V. CONCLUSIONS

A novel theoretical formulation of the AM/PM distortion in GaN DPAs has been presented, showing its relation with the input matching condition of the devices. Based on the proposed theoretical analysis, a design strategy for AM/PM reduction has been introduced and demonstrated by source-pull measurements on a real GaN device. To further confirm the theoretical results, two 7 GHz 10 W GaN MMIC DPA were fabricated and characterized: a switch-based reconfigurable module, to assess the effect of introducing input mismatch on the Main and Auxiliary stages, and an equivalent standard module to prove that the impact of the switches on DPA performances is negligible. CW characterization results demonstrate the effectiveness of the proposed strategy in improving the DPA linearity, significantly reducing the AM/PM distortion, and thus relaxing predistortion requirements.

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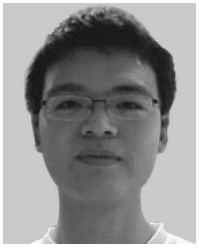

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