IEEE Access
Multidisciplinary | Rapid Review | Open Access Journal

Received August 7, 2017, accepted September 5, 2017, date of publication September 26, 2017, date of current version October 25, 2017.

Digital Object Identifier 10.1109/ACCESS.2017.2756985

A 2.4/5.2-GHz Concurrent Dual-Band CMOS Low Noise Amplifier

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This work was supported by MOHE FRGS under Grant 0153AB-L001.

ABSTRACT A concurrent dual-band low-noise amplifier (LNA) targeted for W-LAN IEEE 802.11 a/b/g standards is designed using 0.13-μm CMOS process. To attain the power-constrained simultaneous noise and input matching at 2.4 and 5.2 GHz, cascode common source inductive degeneration topology is adopted. The LNA achieves input reflection coefficients of −16.8 and −19.4 dB, forward gains of 19.3 and 17.5 dB at 2.4 and 5.2 GHz, respectively. Furthermore, the LNA exhibits noise figures of 3.2 and 3.3 dB with input 1-dB compression points of −29.6 and −28.2 dBm, while third-order input intercept points of −20.1 and −18.1 dBm at 2.4 and 5.2 GHz, respectively. The LNA dissipates 2.4 mW of power from a 1.2-V supply.

INDEX TERMS CMOS, concurrent dual-band, low noise amplifier (LNA), low power consumption, high gain.

I. INTRODUCTION

Growth of wireless applications require communication systems with more bandwidth and data rate. Since narrow band systems cannot cater to these requirements, a wideband system has been introduced to operate at a range of frequencies between 2.4 to 5.2 GHz. However, this wideband system introduces an out-of-band interference which degrades the sensitivity of the system [1], [2]. To alleviate this issue, an alternative approach is to design a narrow-band system that can operate at two different frequencies simultaneously. For the case of 802.11b/g and 802.11a, data rate of up to 54 Mbps can be attained for the design of a concurrent dual-band receiver at 2.4 and 5.2 GHz, respectively.

The LNA, whose function is to amplify simultaneously the low power signal and inhibit degradation of signal-to-noise ratio, is typically the first block in a receiver system. To achieve multiband operation, a switching LNA [3]–[5] is introduced to operate one band at a time. However, this configuration leads to lagging and to overcome this issue, a parallel LNA [6] is designed to manage two bands of operation, simultaneously. Despite the advantage, the parallel LNA results in larger footprint and higher power consumption. To overcome this issue, a concurrent dual-band LNA with a smaller footprint and lower power consumption is designed to manage two bands of operation, simultaneously. For this concurrent dual-band LNA requirement, dual-band input and output matching networks are needed.

In this paper, various dual-band matching networks of the LNA have been reviewed and analyzed. To achieve the dual-band input and output impedance matching, a combination of bandpass and band-stop filters is utilized. This combination of filters may cause unbalanced amplitude of the gain, which is detailed out in the analysis leading to a new dual-band output matching network. The proposed solution is not only capable of eliminating the usage of a band-stop filter but also achieves a balanced and relatively high gain at the desired frequencies of operation.

In addition, this research work shows detailed guidelines on how to achieve the balanced noise figure at both operating frequencies. The LNA is designed by combining a typical narrow-band LNA topology with a dual-band input matching network and a proposed dual-band output matching network for Wireless Local Area Network/Bluetooth (WLAN/BT) applications using RF CMOS process.

This paper is organized as follows. Section II analyzes the conventional and the proposed dual-band output matching network. Section III discusses the complete design of a concurrent dual-band LNA. Simulation results are then presented in Section IV.

II. DUAL-BAND OUTPUT MATCHING NETWORK

A. CONVENTIONAL DUAL-BAND OUTPUT MATCHING NETWORK

Previously reported dual-band LNAs [1], [2], [7]–[14] have been implemented using output matching network

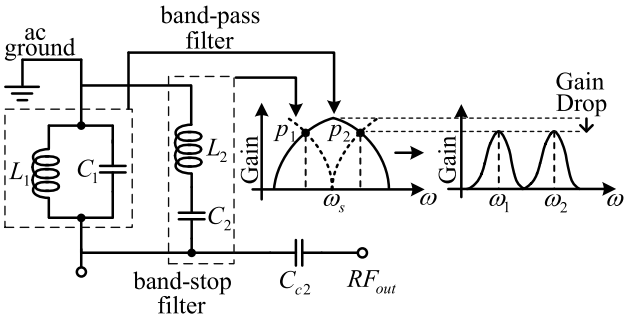

FIGURE 1. Conventional output matching network.

comprising of a parallel combination of bandpass and band-stop filters. The matching network is illustrated in Fig.1, where L_1 and C_1 forms the bandpass filter while L_2 and C_2 forms the band-stop filter. With the filters shunted to ac ground, the signal is coupled to the output by capacitance C_{c2}. The bandpass and the band-stop filters create a pass band and a stop band at the resonant frequency ω_s, respectively, giving rise to two passbands as depicted in Fig.1. The operating frequencies of these passbands occur at the two intersecting points p_1 and p_2 of these two filters.

The output impedance of network shown in Fig. 1 can be expressed as

$$Z_{out} = \left(j\omega L_1 \| \frac{1}{j\omega C_1}\right) \| \left(j\omega L_2 + \frac{1}{j\omega C_2}\right), \tag{1}$$

which is further simplified to yield

$$Z_{out} = \frac{j\omega L_1(1-\omega^2 L_2 C_2)}{1-\omega^2(L_2C_2+L_1C_1+L_1C_2)+\omega^4 L_2C_2L_1C_1}. \tag{2}$$

From (2), the characteristic equation is given by

$$\omega^4 L_2C_2L_1C_1 - \omega^2(L_2C_2+L_1C_1+L_1C_2)+1=0. \tag{3}$$

(3) is the fourth order polynomial which can be solved by taking the sum of roots and the product of the roots [9]. Hence, the sum of the roots S and the product of roots P are given by

$$S = {\omega_1}^2 + {\omega_2}^2 = -\frac{y}{x} \tag{4}$$

$$P = {\omega_1}^2{\omega_2}^2 = \frac{z}{x} \tag{5}$$

where

$$x = L_2C_2L_1C_1 \tag{6}$$

$$y = -(L_2C_2+L_1C_1+L_1C_2) \tag{7}$$

$$z = 1. \tag{8}$$

By substituting (6) and (7) into (4) yields

$$S = \frac{1}{L_1C_1} + \frac{1}{L_2C_2} + \frac{1}{L_2C_1} \tag{9}$$

and substituting (6) and (8) into (5) results in

$$P = \frac{1}{L_2C_2L_1C_1}. \tag{10}$$

In addition, the resonant frequency of the band-stop filter gives

$$\omega_s = \frac{\omega_1+\omega_2}{2} = \frac{1}{\sqrt{L_2C_2}} \tag{11}$$

where ω_s occurs as the average of the two operating radian frequencies ω_1 and ω_2. Assuming either value of L_2 or C_2 is known, (11) can be solved. Then (10) can be arranged as

$$L_1C_1 = \frac{1}{L_2C_2P}. \tag{12}$$

Therefore, substituting (12) into (9) yields the capacitance C_1. With known C_1, L_1 can be calculated from (12).

As illustrated in Fig.1, one critical drawback of applying the conventional output matching network is the significant drop in the gain of the LNA at the operating frequencies. Furthermore, if the resonant frequency ω_s' is slightly lower or higher than ω_s, the LNA produces an uneven gain. For $\omega_s' > \omega_s$, the LNA produces a lower gain at higher frequency. In contrast, the LNA exhibits a lower gain at lower frequency if $\omega_s' < \omega_s$. This behavior is illustrated in Fig. 2. In order to overcome these limitations, a new dual-band output matching network is proposed in the following section.

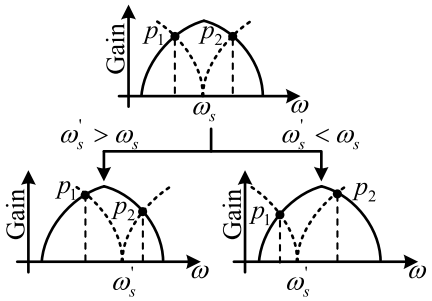

FIGURE 2. Band-stop filter behavior.

B. PROPOSED DUAL-BAND OUTPUT MATCHING NETWORK

To achieve balanced and high gain at both operating frequencies, a new dual-band output matching network comprising two bandpass filters connected in series is proposed as shown in Fig. 3. The two bandpass filters (L_1, C_1) and (L_2, C_2) resonate at 2.4 and 5.2 GHz, respectively. To an advantage, this approach further eliminates the use of a band-stop filter.

The output impedance of the proposed matching network shown in Fig. 3 can be expressed as

$$Z_{out} = \left(j\omega L_1 \| \frac{1}{j\omega C_1}\right) + \left(j\omega L_2 \| \frac{1}{j\omega C_2}\right) \tag{13}$$

and with further simplification, (13) results in

$$Z_{out} = \frac{j\omega(L_1+L_2-\omega^2L_1L_2C_2-\omega^2L_1C_1L_2)}{\omega^4L_1C_1L_2C_2-\omega^2(L_1C_1+L_2C_2)+1}. \tag{14}$$

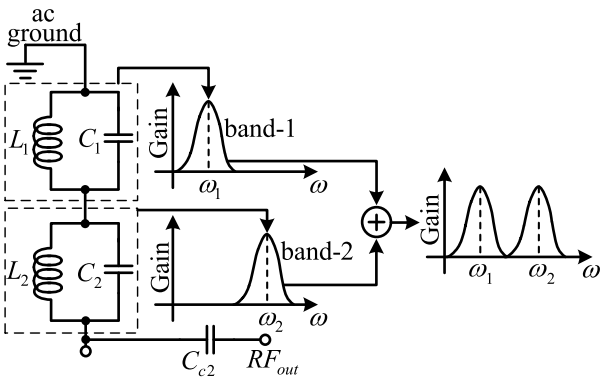

FIGURE 3. Proposed output matching network.

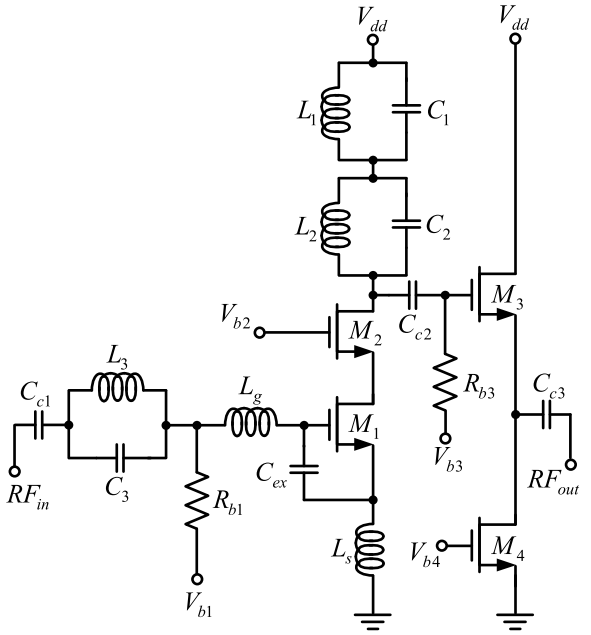

FIGURE 4. Schematic of the proposed concurrent dual-band LNA.

From (14), the characteristic equation is given by

$$\omega^4 L_1 C_1 L_2 C_2 - \omega^2 (L_1 C_1 + L_2 C_2) + 1 = 0 \tag{15}$$

and by solving (15), yields

$$\omega_1 = \frac{1}{\sqrt{L_1 C_1}} \tag{16}$$

$$\omega_2 = \frac{1}{\sqrt{L_2 C_2}}. \tag{17}$$

The component values for (L_1, C_1) and (L_2, C_2) are then obtained from (16) and (17), respectively.

III. CONCURRENT DUAL-BAND LNA DESIGN

The schematic of the proposed concurrent dual-band LNA is designed using a cascode common source amplifier topology with inductive degeneration as shown in Fig. 4. M_1 and M_2 are used as common source and common gate amplifiers, respectively, which are connected in a cascode configuration. To further improve the isolation between the input and the output, M_3 and M_4 (i.e buffer stage) are used as a source follower and a current source, respectively. The common source (CS) transistor M_1 with inductive degeneration is used by Shaeffer and Lee [15] to achieve power constrained noise optimization LNA. Further improvement has been proposed in the PCSNIM technique by adding the external capacitance C_{ex} between the gate and the source of M_1. The use of C_{ex} is introduced by Andreani and Sjoland [16] to minimize the noise figure at low power consumption. It was then theoretically investigated by Nguyen *et al.* [17] in the PCSNIM technique. To achieve the dual-band input impedance matching, a parallel network, comprising inductance L_3 and capacitance C_3 are in series with the narrow band LNA input matching network, comprising source inductance L_s, gate inductance L_g and gate to source external capacitance C_{ex} [1], [2]. In addition, coupling capacitances C_{c1}, C_{c2}, and C_{c3} are at the input and at the output of the cascode stage and the output of the buffer stage, respectively.

In this work, a proposed dual-band output matching network differs from the conventional dual-band output matching network as it utilizes a parallel combination of a bandpass filter and a band-stop filter while the proposed network has two bandpass filters connected in series to achieve the dual-band output impedance matching simultaneously.

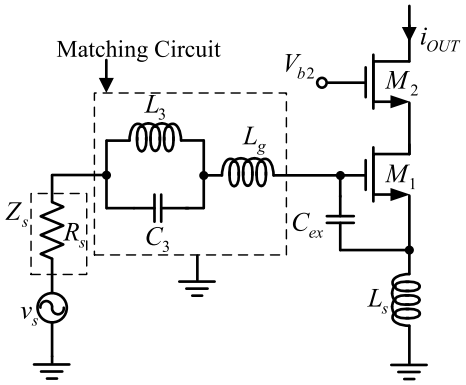

FIGURE 5. Schematic of inductively source degenerated CS LNA with a dual-band input matching network.

A. INPUT STAGE NOISE OPTIMIZATION

According to Friis law, the noise performance of the overall receiver system is dominated by the input stage of the LNA. The noise analysis is shown in Fig. 5. Furthermore the simplified small-signal equivalent model is extracted in Fig. 6. As the input stage contains a CS amplifier, the detailed noise analysis is reviewed in Appendix A. From Fig. 6, the optimum source impedance can be modified from Z_{opt} (A14) as

$$Z_{\text{opt}} = \left\{ \frac{\alpha\sqrt{\frac{\delta}{5\gamma}(1-|c|^2)} + j\left(\frac{C_t}{C_{gs}} - \alpha|c|\sqrt{\frac{\delta}{5\gamma}}\right)^2}{\omega C_{gs}\left\{\frac{\alpha^2\delta}{5\gamma}(1-|c|^2) + \left(\frac{C_t}{C_{gs}} - \alpha|c|\sqrt{\frac{\delta}{5\gamma}}\right)^2\right\}} - j\omega L_t - \frac{j\omega L_3}{1-\omega^2 L_3 C_3} \right\} \tag{18}$$

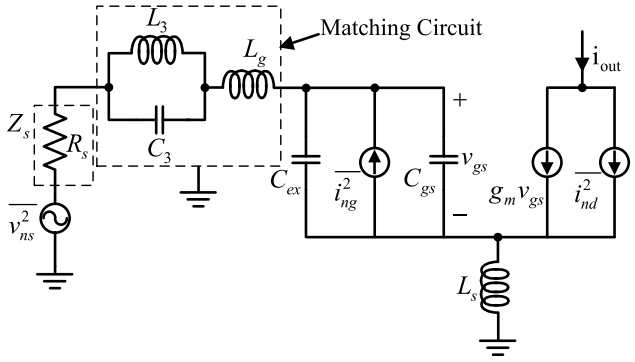

FIGURE 6. Small-signal equivalent circuit for noise calculations of Fig. 5.

where

$$C_t = C_{gs} + C_{ex} \tag{19}$$
$$L_t = L_s + L_g. \tag{20}$$

From (18), the real and the imaginary parts can be separated as follows:

$$\mathrm{Re}[Z_{\mathrm{opt}}] = \frac{\alpha\sqrt{\frac{\delta}{5\gamma}(1-|c|^2)}}{\omega C_{gs}\left\{\frac{\alpha^2\delta}{5\gamma}(1-|c|^2)+\left(\frac{C_t}{C_{gs}}-\alpha|c|\sqrt{\frac{\delta}{5\gamma}}\right)^2\right\}} \tag{21}$$

$$\mathrm{Im}[Z_{\mathrm{opt}}] = -\left(-\frac{K_c}{\omega C_t}+\omega L_t+\frac{\omega L_3}{1-\omega^2 L_3 C_3}\right) \tag{22}$$

where

$$K_c = \frac{\frac{C_t}{C_{gs}}\left(\frac{C_t}{C_{gs}}-\alpha|c|\sqrt{\frac{\delta}{5\gamma}}\right)^2}{\frac{\alpha^2\delta}{5\gamma}(1-|c|^2)+\left(\frac{C_t}{C_{gs}}-\alpha|c|\sqrt{\frac{\delta}{5\gamma}}\right)^2}. \tag{23}$$

It is assumed that the value of K_c is approximately close to 1 for a CMOS process [17]–[19]. From Fig. 5, the input impedance of the LNA is derived in Appendix B, given as

$$Z_{\mathrm{in}} = \frac{g_m L_s}{C_t} + j\{-\frac{1}{\omega C_t}+\omega L_t+\frac{\omega L_3}{1-\omega^2 L_3 C_3}\}. \tag{24}$$

It can be seen in (24) that the source inductive degeneration forms the real part in the input impedance which in turn helps to reduce the discrepancy between the real parts of the optimum noise impedance and the input impedance of dual-band LNA. The condition that allows the simultaneous noise and input matching is given by [17], [20]–[22] as

$$Z_{\mathrm{in}} = {Z_{\mathrm{opt}}}^*. \tag{25}$$

From (21)-(24), (25) can be satisfied when the following conditions are met [21]:

$$\mathrm{Re}[Z_{\mathrm{in}}] = \mathrm{Re}[Z_s] \tag{26}$$
$$\mathrm{Re}[Z_{\mathrm{opt}}] = \mathrm{Im}[Z_s] \tag{27}$$
$$\mathrm{Im}[Z_{\mathrm{in}}] = -\mathrm{Im}[Z_s] \tag{28}$$
$$\mathrm{Im}[Z_{\mathrm{opt}}] = \mathrm{Im}[Z_s]. \tag{29}$$

Assuming K_c is close to 1, the imaginary part of Z_{opt} and the imaginary part of Z_{in} are almost equal with the opposite sign, hence (28) and (29) are satisfied. From (26) and (27), the real part of Z_{in} and Z_{opt} should match to source impedance (Z_s = 50 Ω + j0 Ω) for the simultaneous noise and input matching of dual-band LNA. However, it is clear from (21) that the noise matching cannot be achieved at both operating frequencies simultaneously because the real part of Z_{opt} is distributed between two different frequencies [18]. Hence, to obtain a balanced noise performance at both operating frequencies, (21) is rewritten as

$$\mathrm{Re}[Z_{\mathrm{opt}}] = \frac{\alpha\sqrt{\frac{\delta}{5\gamma}(1-|c|^2)}}{\omega_{av} C_{gs}\left\{\frac{\alpha^2\delta}{5\gamma}(1-|c|^2)+\left(\frac{C_t}{C_{gs}}-\alpha|c|\sqrt{\frac{\delta}{5\gamma}}\right)^2\right\}} \tag{30}$$

where

$$\omega_{av} = \frac{\omega_1+\omega_2}{2}. \tag{31}$$

The optimum noise performance, in this case, has been obtained at both frequencies concurrently, validating the approach of dual-band input noise optimization.

B. INPUT STAGE DESIGN METHODOLOGY

The qualitative description of the input stage for the dual-band LNA, using power-constrained simultaneous noise and input matching with balanced noise performance, would be as follows: First, choose the optimum transistor width W_{M_1,opt,P_D} based on the power-constrained noise optimization given by [15]

$$W_{M_1,opt,P_D} = \frac{3}{2\omega_{av} L C_{ox} R_s Q_{L,opt,P_D}} \tag{32}$$

where L is the effective channel length of M_1, C_{ox} is the oxide capacitance, R_s is the source impedance and Q_{L,opt,P_D} is the input circuit optimum quality factor. Subsequently, to determine the DC bias V_{GS} is calculated to give fixed power dissipation. Now, L_s and C_{ex} can be obtained by satisfying

$$\mathrm{Re}[Z_{\mathrm{in}}] = \frac{g_m L_s}{C_t} = 50\Omega \tag{33}$$

with known L_s and C_{ex}, L_g can be determined from the following expression [21]

$$j\omega L_t + \frac{1}{j\omega C_t} = 0. \tag{34}$$

With the imaginary part of (24) is equal to zero, which is simplified to be

$$\frac{1}{j\omega C_t} + j\omega L_t + \frac{j\omega L_3}{1-\omega^2 L_3 C_3} = 0 \tag{35}$$
$$\omega^4 L_t C_t L_3 C_3 - \omega^2(L_t C_t + L_3 C_3 + L_3 C_t) + 1 = 0. \tag{36}$$

The resulting fourth order polynomial from (36) can be solved by taking the sum of the roots S and the product of the roots P,

yielding

$$S = \omega_1{}^2 + \omega_2{}^2 = -\frac{b}{a} \tag{37}$$

$$P = \omega_1{}^2.\omega_2{}^2 = \frac{c}{a} \tag{38}$$

where

$$a = L_t C_t L_3 C_3 \tag{39}$$

$$b = -(L_t C_t + L_3 C_3 + L_3 C_t) \tag{40}$$

$$c = 1. \tag{41}$$

From (38), L_3C_3 can be obtained as

$$L_3 C_3 = \frac{1}{P L_t C_t} \tag{42}$$

and by substituting (42) into (37) yields

$$C_3 = \frac{P C_t}{S P L_t C_t - P - 1}. \tag{43}$$

Therefore, L_3 can be determined from (42)

$$L_3 = \frac{1}{P L_t C_t C_3}. \tag{44}$$

C. CASCODE STAGE

The cascode stage improves the stability of the amplifier by shielding the input transistor M_1 from the voltage variations at the output. The width W_2 of M_2 determines the operating conditions with a minimal change in the width W_1 of M_1 at a fixed current [24]. It was found that the generated noise power from the cascode stage increases as the width of cascode stage increases. Hence, to reduce the noise contribution from M_2, the width of M_2 is minimized. Furthermore, the smaller W_2 also reduces the capacitance at the intermediate node between M_1 and M_2. Despite the two disadvantages, due to the Miller effect, smaller W_2 results in a noise mismatch and larger value of R_n. Thus, W_2 should be kept equal to W_1 [23], [24].

D. BUFFER STAGE

The last stage in the design of the dual-band LNA is the output buffer. This buffer is incorporated into the overall LNA design in order to match the output impedance to a network analyzer for measurement purpose. The source follower M_3 as shown in Fig. 4, translates the high impedance path at the gate of M_3 to the low impedance path at the source of M_3. This condition can be achieved by biasing transistor M_3 to yield $1/g_{m_3} = 50\ \Omega$.

IV. SIMULATION RESULTS

A concurrent dual-band LNA, as shown in Fig. 4, is simulated using 0.13-μm CMOS technology at 2.4 and 5.2 GHz for BT/WLAN applications, respectively. The core of the LNA dissipates a total current of 2.0 mA from 1.2 V supply. Fig. 7 shows the simulated forward gain S_{21}, input reflection coefficient S_{11}, noise figure NF and minimum noise figure NFmin of the LNA up to 6 GHz.

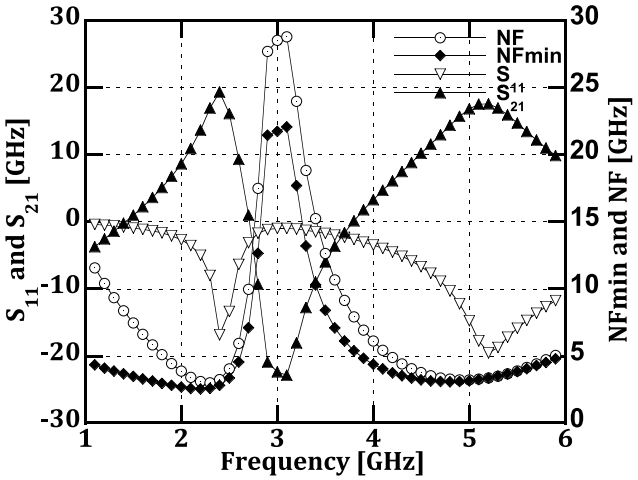

FIGURE 7. Simulated forward gains, input return losses, NFs and NFmins at 2.4 and 5.2 GHz.

TABLE 1. Performance summary of the LNA.

Frequency	2.4 GHz	5.2 GHz	Units
S_{21}	19.3	17.5	dB
S_{11}	-16.8	-19.4	dB
NF	3.2	3.3	dB
NFmin	2.8	3.3	dB
P_{1dB}	-29.6	-28.2	dBm
IIP3	-20.1	-18.1	dBm
Supply Voltage	1.2		V
DC Current	2.0		mA
CMOS Technology	0.13		μm

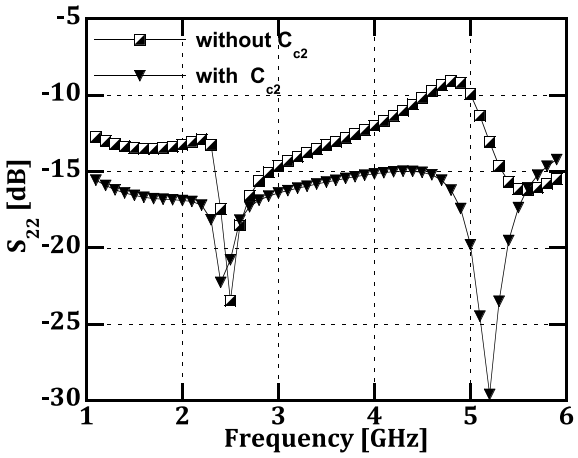

FIGURE 8. Output return losses with and without C_{c2} at 2.4 and 5.2 GHz.

The LNA achieves forward gains of 19.3 and 17.5 dB, input return losses of 16.8 and 19.4 dB at 2.4 GHz and 5.2 GHz, respectively. The simulated NFs are 3.2 dB and 3.3 dB, while NFmins are 2.8 dB and 3.3 dB at 2.4 GHz and 5.2 GHz, respectively. It is observed that the forward gains and the noise figures of the LNA are almost balanced at the corresponding operating frequencies (2.4 and 5.2 GHz) with a difference of only 1.8 dB for the forward gain and 0.1 dB

TABLE 2. Comparison of the concurrent dual-band LNAs operating in same frequency bands.

Ref.	Tech. [μm]	Freq. [GHz]	S11 [dB]	S21 [dB]	NF [dB]	IIP3 [dBm]	Power [mW]	Area [mm^2]
* [2]	0.35 CMOS	2.4 5.2	-25.0 -15.0	9.4 15.5	2.3 4.5	0.0 5.6	10.0	0.64†
[7]	0.18 CMOS	2.4 5.2	-12.7 -9.5	21.0 7.6	2.5 5.7	- -	10.0	-
[8]	0.18 CMOS	2.6 5.2	-20.0 -22.0	15.0 9.5	0.6 0.8	0.0 7.0	3.6	-
* [11]	0.18 CMOS	2.4 5.2	- -	14.2 14.6	4.4 3.7	-3.4 -2.7	7.2	0.83†
* [12]	0.18 CMOS	2.4 5.2	-15.0 -18.0	14.0 22.0	2.4 2.5	-0.2 -6.3	9.3	0.34†
* [13]	0.18 CMOS	2.4 5.2	-13.1 -10.5	12.9 8.2	3.7 3.7	-4.0 -1.0	7.6	0.90†
This Work	0.13 CMOS	2.4 5.2	-16.8 -19.4	19.3 17.5	3.2 3.3	-20.1 -18.1	2.4	-

* Measured data; †Including pads; ‡Excluding pads

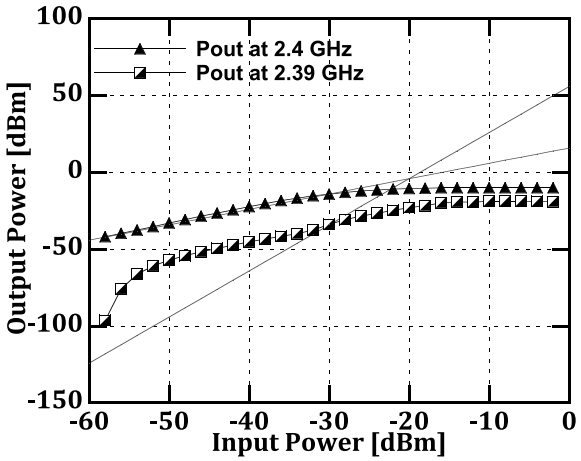

FIGURE 9. Simulated output power with respect to the input power at 2.4 GHz.

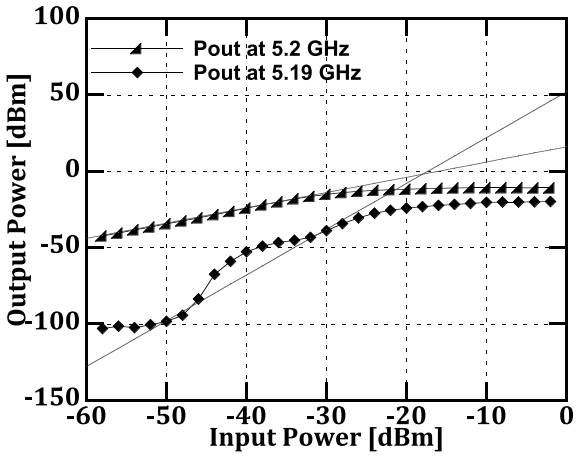

FIGURE 10. Simulated output power with respect to the input power at 5.2 GHz.

for the noise figure. On the other hand, the minimum noise figures occur at 2.2 and 4.9 GHz, denoted by ω_{1n} and ω_{2n}, respectively. The simplified relationship between ω_1, ω_2 and ω_{1n}, ω_{2n} is given by [19] as

$$\left(\frac{\omega_{1n}}{\omega_1}\right)^2 = K_c \tag{45}$$

$$\left(\frac{\omega_{2n}}{\omega_2}\right)^2 = K_c. \tag{46}$$

For simultaneous noise and input matching to be fulfilled, K_c expression in (45) and (46) should be close to 1. From (45), K_c is equal to 0.84 and from (46), K_c is equal to 0.88. The fact that K_c approximates to 1 signifies the close proximity between the operating frequencies of the concurrent dual-band LNA and the frequencies where the minimum NFs occur. If (45) and (46) do not yield a value of K_c close to 1, the design of the concurrent dual-band LNA cannot fulfill the simultaneous noise and input matching.

From Fig. 8, the output return losses without C_{c2} are 24.3 and 14.1 dB, while the output return losses with C_{c2} are 23.5 and 27.8 dB at 2.4 and 5.2 GHz, respectively. Power performances of the dual-band LNA are shown in Fig. 9 and Fig. 10 at 2.4 GHz and 5.2 GHz, respectively. An input 1-dB compression point P_{1dB} and an input third-order intercept point IIP3 are -29.6 and -20.1 dBm at 2.4 GHz as observed in Fig. 9. In the other hand, P_{1dB} and IIP3 are -28.2 and -18.1 dBm at 5.2 GHz, as shown in Fig. 10.

Table 1 summarizes the simulated performance of the concurrent dual-band LNA as depicted in Fig. 4. Table 2 compares the performance of this concurrent dual-band with previously published concurrent dual-band LNAs working in S and C-bands. The forward gains, noise figures and power dissipation are comparable with previously published concurrent dual-band LNAs.

V. CONCLUSION

A concurrent dual-band LNA with a modified output matching network is presented in this paper along with a comprehensive analysis to study the noise performance at its input. The effectiveness of the design has been demonstrated through simulated high forward gain and balanced noise

figure performance at the operating frequencies. The proposed concurrent dual-band LNA can be expanded at other frequencies for multi-band RF systems.

APPENDIX A
NOISE PARAMETERS OF CS AMPLIFIER

The noise of the LNA is a measure of noise factor F, which is the ratio of the total output noise power to the noise power at the source, is given by [23]

$$F = \frac{N_{total}}{N_{source}}. \tag{A1}$$

The noise performance of an LNA is directly related to an input matching. The transistor M_1 is used at the input of the LNA as depicted in Fig. 4.

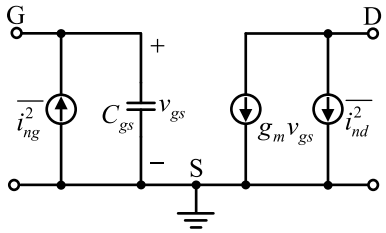

FIGURE 11. Small-signal model of CS amplifier with drain thermal noise current and gate induced noise current.

To analyze the noise of a two port network, an equivalent circuit can be modeled as shown in Fig. 11. v_{gs} and C_{gs} are the voltage and the capacitance between the gate and source of M_1, respectively, whereas g_m is transconductance. From the figure, the mean squared drain noise current is given by [23]–[25]

$$\overline{i_{nd}^2} = 4kT\gamma g_{do}\Delta f \tag{A2}$$

and a mean squared gate noise current [26] is

$$\overline{i_{ng}^2} = 4kT\delta g_g \Delta f \tag{A3}$$

where k is Boltzmann constant, T is the absolute temperature and Δf is the bandwidth. The parameters γ and δ are constants associated with a drain and a gate noise current, respectively. Here, g_{do} is the drain-source conductance when the drain-source voltage V_{DS} is equal to zero and shunt conductance g_g is given by

$$g_g = \frac{\omega^2 C_{gs}^2}{5g_{do}}. \tag{A4}$$

The gate induced noise current is partially correlated to the drain thermal noise current with a correlation coefficient c given by [15], [27], [28]

$$c = \frac{\overline{i_{ng} i_{nd}^*}}{\sqrt{\overline{i_{ng}^2}\,\overline{i_{nd}^2}}} \approx -0.395j \tag{A5}$$

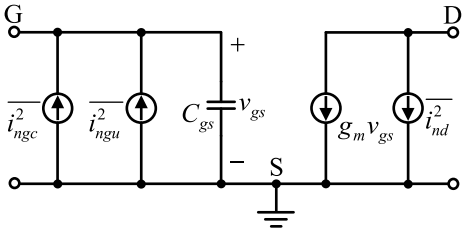

FIGURE 12. Representation of a gate induced noise current as combination of a correlated and uncorrelated gate induced noise currents.

As shown in Fig. 12, the gate induced noise current can be represented by a combination between correlated and uncorrelated gate noise currents given by

$$\overline{i_{ng}^2} = 4kT\delta g_g \Delta f |c|^2 + 4kT\delta g_g \Delta f (1 - |c|^2) \tag{A6}$$

$$\overline{i_{ng}^2} = \overline{i_{ngc}^2} + \overline{i_{ngu}^2} \tag{A7}$$

where

$$\overline{i_{ngc}^2} = 4kT\delta g_g \Delta f |c|^2 \tag{A8}$$

$$\overline{i_{ngu}^2} = 4kT\delta g_g \Delta f (1 - |c|^2). \tag{A9}$$

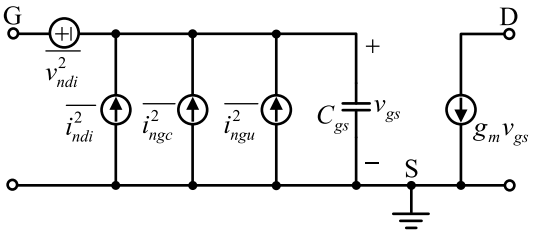

FIGURE 13. Replacement of drain thermal noise current with input noise voltage and input noise current.

As shown in Fig. 13, the drain noise current is referred to the input by two noise sources, namely the mean squared noise voltage $\overline{v_{ndi}^2}$ and the mean squared noise current $\overline{i_{ndi}^2}$. The ratio between the two is equal to the admittance at the input given by [25]

$$\frac{\overline{i_{ndi}^2}}{\overline{v_{ndi}^2}} = (j\omega C_{gs})^2. \tag{A10}$$

In general, the noise factor can be expressed as follows [29]

$$F = F_{min} + \frac{R_n \left| Y_s - Y_{opt} \right|^2}{G_s} \tag{A11}$$

where Y_s and Y_{opt} are the source admittance and the optimum source admittance while F_{min}, R_n and G_s are the minimum noise factor, the noise resistance and the source conductance, respectively. Notethat, F_{min} can be achieved at the optimum source admittance condition, i.e. $Y_s = Y_{opt}$. After some elaborative algebraic derivations [25], the noise parameters of the CS amplifier can be expressed as

$$R_n = \frac{\overline{v_{ndi}^2}}{4kT\Delta f} = \frac{\gamma}{\alpha}\frac{1}{g_m} \tag{A12}$$

$$Y_{\text{opt}} = \frac{1}{Z_{\text{opt}}} = G_{opt} + jB_{opt} \tag{A13}$$

$$Z_{\text{opt}} = \frac{\alpha\sqrt{\frac{\delta}{5\gamma}(1-|c|^2)} + j\left(1-\alpha|c|\sqrt{\frac{\delta}{5\gamma}}\right)^2}{\omega C_{gs}\left\{\frac{\alpha^2\delta}{5\gamma}(1-|c|^2) + \left(1-\alpha|c|\sqrt{\frac{\delta}{5\gamma}}\right)^2\right\}} \tag{A14}$$

$$F_{min} = 1 + \frac{2}{\sqrt{5}}\frac{\omega}{\omega_T}\sqrt{\gamma\delta(1-|c|^2)} \tag{A15}$$

where $\omega_T = 2\pi f_T = g_m/C_{gs}$ and f_T is the transistor's cutoff frequency. Note that, the effects of M_2 on the noise and frequency response are neglected, as well as the parasitic resistances at the gate, the body, the source and the drain terminal, and gate-drain capacitance of M_1.

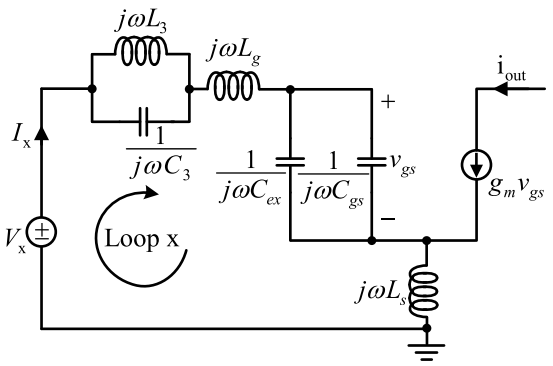

FIGURE 14. Small-signal model for the input impedance of dual-band LNA.

APPENDIX B
DERIVATION OF THE INPUT IMPEDANCE FOR A CONCURRENT DUAL-BAND LNA

The small-signal model for the input impedance of the dual-band LNA as shown in Fig. 14. The input impedance can be determine by taking the ratio of test voltage V_{x} to the test current I_{x}. Writing KVL equation across loop x yields

$$V_{\text{x}} = \left\{ I_{\text{x}}.\left(j\omega L_3 \| \frac{1}{j\omega C_3}\right) + I_{\text{x}}.j\omega L_g + I_{\text{x}}.\left(\frac{1}{j\omega C_{gs}} \| \frac{1}{j\omega C_{ex}}\right) + (I_{\text{x}} + g_m v_{gs}).j\omega L_s \right\} \tag{B1}$$

where

$$v_{gs} = I_{\text{x}}.\frac{1}{j\omega(C_{gs}+C_{ex})}. \tag{B2}$$

By substituting (B2) into (B1) gives

$$V_{\text{x}} = \left\{ I_{\text{x}}.\left\{ \frac{j\omega L_3}{j^2\omega^2 L_3 C_3 + 1} + j\omega(L_g + L_s) + \frac{1}{j\omega(C_{gs}+C_{ex})} + g_m\frac{j\omega L_s}{j\omega(C_{gs}+C_{ex})} \right\} \right\}. \tag{B3}$$

Arranging and simplifying (B3), results in input impedance Z_{in} in terms of the real and the imaginary part given by

$$Z_{\text{in}} = \frac{V_{\text{x}}}{I_{\text{x}}} = \underbrace{\frac{g_m L_s}{C_t}}_{\text{Real Part}} + j\underbrace{\left\{ -\frac{1}{\omega C_t} + \omega L_t + \frac{\omega L_3}{1-\omega^2 L_3 C_3} \right\}}_{\text{Imaginary Part}}. \tag{B4}$$

ACKNOWLEDGMENTS

The authors would like to thank Universiti Teknologi PETRONAS (UTP) for providing the graduate assistantship (GA) for this work. They also gratefully acknowledge Silterra Malaysia Sdn. Bhd. for the use of 0.13-μm CMOS process design kit (PDK).

REFERENCES

[1] H. Hashemi and A. Hajimiri, "Concurrent dual-band CMOS low noise amplifiers and receiver architectures," in *VLSI Circuits Symp. Dig.*, Jun. 2001, pp. 247–250.

[2] H. Hashemi and A. Hajimiri, "Concurrent multiband low-noise amplifiers-theory, design, and applications," *IEEE Trans. Microw. Theory Techn.*, vol. 50, no. 1, pp. 288–301, Jan. 2002.

[3] W.-S. Wuen and K.-A. Wen, "Dual-band switchable low noise amplifier for 5-GHz wireless LAN radio receivers," in *IEEE Int. 45th Midwest Circuits Syst. Symp. Dig.*, Aug. 2002, pp. II-258–II-261.

[4] V. Vidojkovic, J. van der Tang, E. Hanssen, A. Leeuwenburgh, and A. van Roermund, "Fully-integrated DECT/Bluetooth multi-band LNA in 0.18 μm CMOS," in *Proc. Int. Circuits Syst. Symp.*, May 2004, pp. I-565–I-568.

[5] M. T. Mustaffa, A. Zayegh, and T. Z. A. Zulkifli, "A reconfigurable LNA for multi-standard receiver using 0.18 μm CMOS technology," in *IEEE Student Res. Develop. Conf. Dig.*, Nov. 2009, pp. 238–241.

[6] S. Wu and B. Razavi, "A 900-MHz/1.8-GHz CMOS receiver for dual-band applications," *IEEE J. Solid-State Circuits*, vol. 33, no. 12, pp. 2178–2185, Dec. 1998.

[7] E. Kargaran and B. Madadi, "Design of a novel dual-band concurrent CMOS LNA with current reuse topology," in *Int. Netw. Inf. Conf. Tech. Dig.*, vol. 1. 2010, pp. 386–388.

[8] G. Zhiqiang, L. Dawei, L. Xiaowei, and Z. Zhongzhao, "The design of dual-band CMOS low noise amplifier for wireless applications," in *IEEE Acad. Int. Optoelectron. Microelectron. Technol. Symp. Dig.*, Oct. 2011, pp. 344–347.

[9] S. Datta, K. Datta, A. Dutta, and T. K. Bhattacharyya, "Fully concurrent dual-band LNA operating in 900 MHz/2.4 GHz bands for multi-standard wireless receiver with sub-2 dB noise figure," in *Int. Emerg. Trends Eng. Conf. Tech. Dig.*, vol. 1. 2010, pp. 731–734.

[10] C. P. Moreira, E. Kerheve, P. Jarry, and D. Belot, "A concurrent fully-integrated LNA for W-LAN IEEE 802.11b/g/a applications," in *IEEE Microw. Conf. Dig.*, Sep. 2006, pp. 1552–1555.

[11] S. Wang and B.-Z. Huang, "A high-gain CMOS LNA for 2.4/5.2-GHz WLAN applications," *Prog. Electromagn. Res. C*, vol. 21, pp. 155–167, May 2011.

[12] Y. P. Zhang, K. W. Chew, and P. F. Wong, "Analysis and design of a fully integrated CMOS low-noise amplifier for concurrent dual-band receivers," *Int. J. RF Microw. Comput.-Aided Eng.*, vol. 16, no. 5, pp. 444–453, Sep. 2006.

[13] Y.-J. Hong, S.-F. Wang, P.-T. Chen, Y.-S. Hwang, and J.-J. Chen, "A concurrent dual-band 2.4/5.2 GHz low-noise amplifier using gain enhanced techniques," in *IEEE Asia–Pacific Electromagn. Compat. Symp. Dig.*, May 2015, pp. 231–234.

[14] Y.-T. Lin, T. Wang, and S.-S. Lu, "Fully integrated concurrent dual-band low noise amplifier with suspended inductors in SiGe 0.35 μm BiCMOS technology," *Electron. Lett.*, vol. 44, no. 9, pp. 563–564, Apr. 2008.

[15] D. K. Shaeffer and T. H. Lee, "A 1.5-V, 1.5-GHz CMOS low noise amplifier," *IEEE J. Solid-State Circuits*, vol. 32, no. 5, pp. 745–759, May 1997.

[16] P. Andreani and H. Sjoland, "Noise optimization of an inductively degenerated CMOS low noise amplifier," *IEEE Trans. Circuits Syst. II, Analog Digit. Signal Process.*, vol. 48, no. 9, pp. 835–841, Sep. 2001.

[17] T.-K. Nguyen, C.-H. Kim, G.-J. Ihm, M.-S. Yang, and S.-G. Lee, "CMOS low-noise amplifier design optimization techniques," *IEEE Trans. Microw. Theory Techn.*, vol. 52, no. 5, pp. 1433–1442, May 2004.
[18] Y.-C. Hsiao, C. Meng, and C. Yang, "Design optimization of single-/dual-band FET LNAs using noise transformation matrix," *IEEE Trans. Microw. Theory Techn.*, vol. 64, no. 2, pp. 519–532, Feb. 2016.
[19] H.-W. Chiu, S.-S. Lu, and Y.-S. Lin, "A 2.17-dB NF 5-GHz-band monolithic CMOS LNA with 10-mW DC power consumption," *IEEE Trans. Microw. Theory Techn.*, vol. 53, no. 3, pp. 813–824, Mar. 2005.
[20] T.-K. Nguyen, N.-J. Oh, C.-Y. Cha, Y.-H. Oh, G.-J. Ihm, and S.-G. Lee, "Image-rejection CMOS low-noise amplifier design optimization techniques," *IEEE Trans. Microw. Theory Techn.*, vol. 53, no. 2, pp. 538–547, Feb. 2005.
[21] T.-K. Nguyen and S.-G. Lee, "Noise and gain optimization technique for RF-integrated CMOS low noise amplifier," in *Proc. IEEE Conf. Electron Devices Solid-State Circuits*, Dec. 2003, pp. 221–224.
[22] T.-K. Nguyen, Y.-M. Su, and S.-G. Lee, "A power constrained simultaneous noise and input matched low noise amplifier design technique," in *Proc. Int. Circuits Syst. Symp.*, vol. 4. May 2004, pp. 23–26.
[23] J.-S. Goo, H.-T. Ahn, D. J. Ladwig, Z. Yu, T. H. Lee, and R. W. Dutton, "A noise optimization technique for integrated low-noise amplifiers," *IEEE J. Solid-State Circuits*, vol. 37, no. 8, pp. 994–1002, Aug. 2002.
[24] J.-S. Goo, K.-H. Oh, C.-H. Choi, Z. Yu, T. H. Lee, and R. W. Dutton, "Guidelines for the power constrained design of a CMOS tuned LNA," in *Proc. Int. Conf. Simulation Semiconductor Process. Devices (SISPAD)*, Seattle, WA, USA, Sep. 2000, pp. 269–272.
[25] T. H. Lee, *The Design of CMOS Radio-Frequency Integrated Circuits*, 1st ed. Cambridge, U.K.: Cambridge Univ. Press, 1998, ch. 11.
[26] A. Van der Ziel, *Noise in Solid State Devices and Circuits*. New York, NY, USA: Wiley, 1986.
[27] D. K. Shaeffer and T. H. Lee, "Comment on corrections to 'A 1.5-V, 1.5-GHz CMOS low noise amplifier,'" *IEEE J. Solid-State Circuits*, vol. 41, no. 10, p. 2359, Oct. 2006.
[28] N.-J. Oh, "Corrections to 'CMOS low-noise amplifier design optimization techniques,'" *IEEE Trans. Microw. Theory Techn.*, vol. 55, no. 6, p. 1255, Jun. 2007.
[29] H. A. Haus *et al.*, "Representation of noise in linear twoports," *Proc. IRE*, vol. 48, no. 1, pp. 69–74, Jan. 1960.

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