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Comprehensive Analysis of Gate-Induced Drain Leakage in Emerging FET Architectures: Nanotube FETs Versus Nanowire FETs

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ABSTRACT In this paper, we have performed a comprehensive analysis of the gate-induced drain leakage (GIDL) in emerging nanotube (NT) and nanowire (NW) FET architectures. We demonstrate that the additional lateral band-to-band-tunneling (L-BTBT) in the NTFETs owing to the core gate increases their OFF-state current compared with the NWFETs. The increased L-BTBT results in a significantly degraded performance of NTFETs when the gate lengths are scaled to the sub-10-nm regime. Therefore, the enhanced gate control offered by the NT architecture is detrimental from L-BTBT GIDL perspective. We show that although the core gate leads to a considerable increase in the gate capacitance of NTFETs, their dynamic performance improves compared with NWFETs due to the enhanced effective drive current owing to the NT architecture. In addition, we also provide the necessary design guidelines for the NTFETs and NWFETs with respect to spacer dielectric constant, intrinsic material bandgap, effective oxide thickness, supply voltage, and NT diameter from L-BTBT GIDL perspective.

INDEX TERMS Nanotube, nanowire, band-to-band-tunneling (BTBT), gate induced drain leakage (GIDL).

I. INTRODUCTION

Gate-all-around (GAA) nanowires (NW) are considered to be the most promising alternative for ultimate scaling of the conventional metal-oxide-semiconductor FETs (MOSFETs) [1]–[3]. Although the effective gate control in the NW reduces the short channel effects, it also leads to a considerable overlap between the channel region valence band and the drain region conduction band in the OFF-state [4]–[12]. This band overlap facilitates a lateral band-to-band-tunneling (L-BTBT) of electrons from the channel to the drain increasing the OFF-state current considerably. The conventional gate-induced drain leakage (GIDL) current is mainly attributed to electron-hole pair generation by the tunneling of valance band electrons into the conduction band in gate-to-drain overlapped region via BTBT and trap assisted tunneling (TAT) mechanism [13], [14]. However, the conventional GIDL due to gate-drain overlap is dominant at large and negative gate voltages ($V_{GS} << 0$ V) [4]–[12]. Therefore, L-BTBT significantly degrades the performance of the NWFETs and hinders their scaling to the sub-10 nm regime [4]–[12]. In addition, L-BTBT is larger in the NWMOSFETs compared with the NW junctionless (JL) FETs [9]–[12], [15]–[18] which were proposed to alleviate the need for ultra-steep junctions and complex thermal budgets [5]–[12].

However, the JLFETs exhibit a reduced ON-state current due to a lower source/drain doping ($N_D = 1 \times 10^{19}$ cm^{-3}). Therefore, junctionless accumulation mode FETs (JAMFETs) with a heavily doped source/drain ($N_D = 1 \times 10^{20}$ cm^{-3}) were proposed [19]–[21] for increasing ON-state current of JLFETs. However, it was demonstrated in [9] that L-BTBT is also larger in NWJAMFETs compared to the NWJLFETs. Therefore, to mitigate the L-BTBT in NWJAMFETs and NWMOSFETs, a dual metal stacked gate (DMSG) architecture was proposed [6]. Furthermore, a NWJLFET with a P^+ core and N^+ shell was also proposed to reduce L-BTBT induced parasitic bipolar junction transistor (BJT) action and achieve efficient volume depletion in NWJLFETs [10].

Recently, a core gate was proposed in the GAA NW MOSFETs to further improve the gate control [22]–[28]. This nanotube (NT) architecture offers the best possible gate control. Therefore, NT MOSFETs and tunnel FETs exhibit a better performance compared to their

TABLE 1. Parameters used for the device simulation.

Parameter	NTFET	NWFET
Core Gate diameter (d_{core})	5 - 20 nm	-
Gate contact thickness (t_{gc})	5 nm	-
Effective oxide thickness (EOT)	0.67 nm [27]	0.67 nm [27]
Silicon Film thickness (t_{Si})	8 nm [27]	8 nm [27]
Gate length (L_G)	7 - 16 nm [27]	7 - 16 nm [27]
Length of spacer (L_S)	10 nm	10 nm
Spacer thickness (t_S)	5 nm	5 nm
Source/Drain doping ($N_{S/D}$)	$N_D = 1 \times 10^{20}$ cm^{-3}	$N_D = 1 \times 10^{20}$ cm^{-3}

NW counterparts [22]–[28]. Although the inclusion of a core gate in nanowire architecture leads to an improved ON-state current in NTMOSFETs, L-BTBT GIDL was not considered in [22]–[28]. Since L-BTBT significantly degrades the performance and hinders the scaling of NWFETs, it becomes necessary to investigate the impact of L-BTBT even in NWFETs with a core gate i.e. NTFETs and compare the impact of L-BTBT in NTFETs and NWFETs for future technology nodes. Furthermore, the dynamic performance of the NTFETs has also not yet been studied.

Therefore, in this work, we study the impact of L-BTBT on NTFETs and perform a comparative analysis of GIDL between NT and NWFETs for future technology nodes. We demonstrate that the core gate leads to an additional L-BTBT in NTFETs resulting in an increased OFF-state current compared with NWFETs. Therefore, NTFETs exhibit a degraded ON-state to OFF-state current ratio compared with NWFETs in the sub-10 nm regime. In addition, we show that in spite of the significant increase in the gate capacitance in NTFETs owing to the core gate, its dynamic performance is improved compared with NWFETs owing to the enhanced drive current in NTFETs. In addition, we also provide the necessary design guidelines for the NTFETs and NWFETs with respect to spacer dielectric constant, intrinsic material band gap, effective oxide thickness, supply voltage and nanotube diameter from L-BTBT GIDL perspective.

II. DEVICE STRUCTURE AND SIMULATION PARAMETERS

The cross-sectional view of the nanotube (NT) FETs: NTMOSFET and NTJAMFET and nanowire (NW) FETs: NWMOSFET and NWJAMFET are shown in Fig. 1. The NTFET consists of a core gate (core gate diameter = 20 nm [25]) which is tied to the outer gate. The contact to this core gate is taken at the drain end [22], [23], [25]–[28]. Therefore, a portion of the core gate also extends below the drain as shown in Fig. 1(a) and (b). We have taken a small gate contact thickness to reduce the Miller capacitance (and the delay) due to gate-drain overlap in the NTFETs. Furthermore, silicon NT have been experimentally realized [29] and the NTFETs can be fabricated using the process steps outlined in [22]–[24]. In addition, we have used SiO_2 gate sidewall spacers in all the device simulations since a gate sidewall spacer is essential for the formation of the NTFETs [22]–[24]. The parameters used for the NT and NWFETs are listed in table I. A channel length of 16 nm, an effective oxide thickness of 0.67 nm (t_{ox} = 1.5 nm: 0.5 nm SiO_2 and 1 nm HfO_2), a nanowire diameter of 8 nm and a supply voltageV_{DD} = 0.8 V has

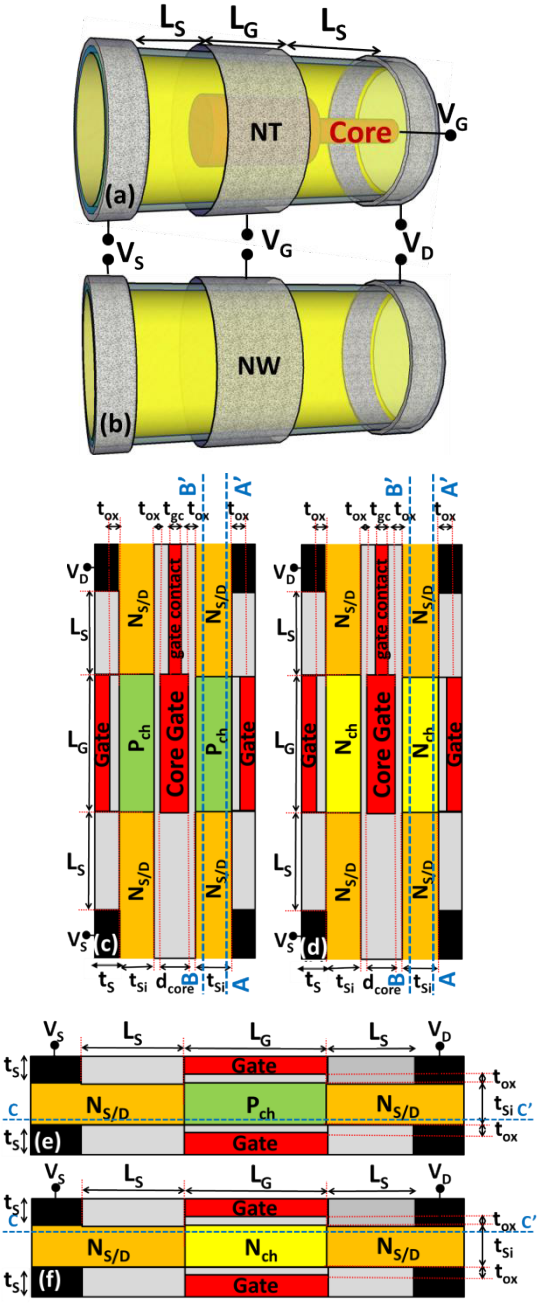

FIGURE 1. 3-D view of (a) nanotube (NT) FET and (b) nanowire (NW) FET depicting that NTFETs are essentially NWFETs with a core gate. Cross-sectional view of (c) NTMOSFET and (d) NTJAMFET and (e) NWMOSFET and (f) NWJAMFET. Cutline B-B′ has been taken 1 nm below the Si-SiO_2 interface adjacent to the core gate while cut lines A-A′ and C-C′ have been taken 1 nm below the Si-SiO_2 interface adjacent to the outer gate.

been used in our simulations as per the ITRS projections for the 8/7 nm technology node [4], [30]. A gate work function of 4.4 eV and 4.6 eV and a channel doping of $N_A = 1 \times 10^{16}$ cm^{-3} (P_{ch}) and $N_D = 1 \times 10^{18}$ cm^{-3} (N_{ch}) has been used for NT and NW MOSFETs and JAMFETs, respectively.

III. SIMULATION RESULTS AND DISCUSSIONS

Sentaurus TCAD (release I-2013.12) [31] was used to perform 3-D device simulations. Both field- and

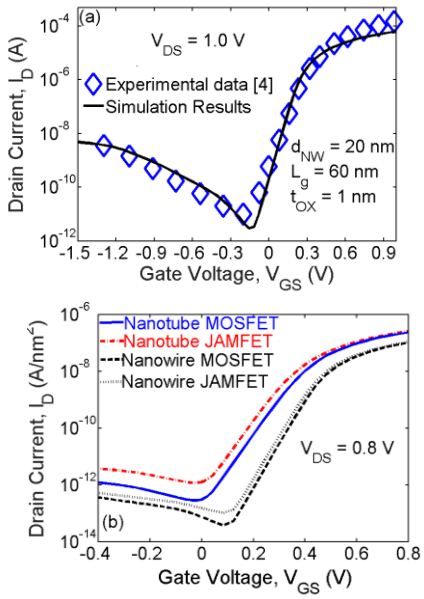

FIGURE 2. (a) Calibration of the simulation set-up by reproducing experimental results of [4] and (b) transfer characteristics of NT and NWFETs. The values of tunneling mass of electrons $m_e = 0.4\ m_0$ and holes $m_h = 0.65\ m_0$ and the effective density of states for holes $g_v = 0.66$ and electrons $g_c = 2.1$ were calibrated to match the experimental results.

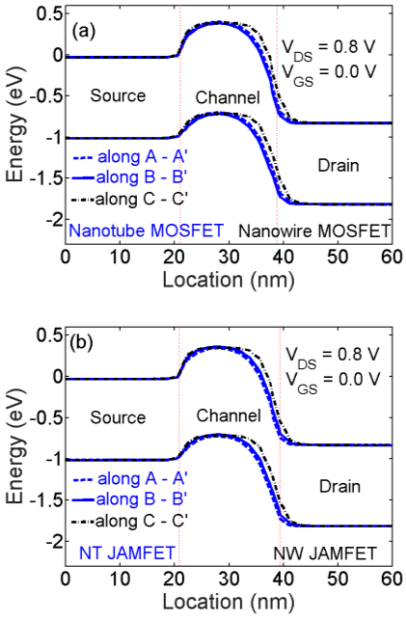

FIGURE 3. Energy band profiles of (a) NT and NWMOSFET and (b) NT and NWJAMFET. The cut lines A-A′, B-B′ and C-C′ have been taken 1 nm away from the Si-SiO_2 interface.

doping-dependent mobility degradations were taken into account using Lombardi mobility model and Philips unified mobility model. Shockley-Read-Hall (SRH), Auger recombination model and Fermi-Dirac statistics were also included. Band gap narrowing (BGN) model was invoked to consider the heavily doped source/drain extension regions. In addition, L-BTBT was considered using a non-local BTBT model. The quantum confinement effects are insignificant for silicon film thickness greater than 7 nm [32] and therefore, were not included in simulations. Furthermore, the simulation set-up was calibrated by reproducing the experimental results of NWMOSFET [4] as shown in Fig. 2(a) [6]. Furthermore, we have not included the direct tunneling model to consider the gate leakage in our simulations as also done in [4], and [33]. Since all the previous studies on nanotube MOSFETs are simulation based [22]–[28] and do not include BTBT models to account for L-BTBT GIDL, we have not calibrated our simulation results with previously reported results on NTMOSFETs [22]–[28] and used a simulation set-up which is calibrated to the experimental results of the NWMOSFETs for simulating NTFETs. Also, as can be observed from Fig. 2(a), there is a mismatch between the ON-state current (I_D at $V_{GS} = V_{DS} = 1.0$ V) value obtained from TCAD simulations (1.6×10^{-5} A) and the experimental data (3.1×10^{-5} A) obtained from [4]. However, it may be noted that the main objective of this paper is to compare the L-BTBT GIDL in NTFETs and NWFETs rather than showing the exact values of the current. Therefore, we have considered an abrupt doping profile at the source-channel and channel-drain interface to consider the worst case scenario for L-BTBT [6] and not considered any gate overlap effects in the drain region.

The transfer characteristics of the NT (and NW) MOSFET and JAMFET are compared in Fig. 2(b). Since the current carrying capacity depends on number of modes which is proportional to the cross-sectional area, the value of the drain current is normalized by dividing it with the effective silicon cross sectional area (i.e. $\pi \left(\frac{t_{Si}}{2}\right)^2$ for NW and $\pi \cdot t_{Si}\,(d_{core} + 2 \cdot t_{ox} + t_{Si})$ for NT) for a fair comparison. The ON-state current is higher in the NTFETs compared with the NWFETs due to an enhanced volume inversion and accumulation in the NT MOSFET and JAMFET, respectively [22], [23]. However, the OFF-state current of the NT MOSFET and JAMFET is higher than the NW MOSFET and JAMFET by nearly an order of magnitude. Furthermore, the OFF-state current of NW and NT MOSFET is lower than the NW and NT JAMFET, respectively.

The increased OFF-state current in the NTFETs is attributed to the presence of the core gate. The core gate leads to a significant proximity between the channel region valence band and the drain region conduction band close to the Si-SiO_2 interface (along cutline B-B') as shown in Fig. 3. This band alignment in the silicon film adjacent to the core gate facilitates L-BTBT. Therefore, in addition to the L-BTBT due to the outer surrounding gate (along cutline A-A') in the NTFETs, the core gate also contributes to the L-BTBT GIDL as shown in Fig. 4. However, only the outer surrounding gate (along cutline C-C') contributes to the L-BTBT in the NWFETs (Fig. 4). Therefore, the additional L-BTBT GIDL owing to the core gate in NTFET increases the OFF-state current compared with the NWFET. The L-BTBT

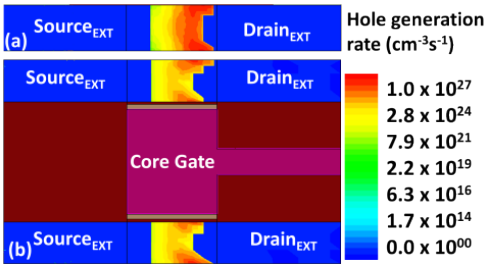

FIGURE 4. Hole generation rate contour plot of (a) NW and (b) NT JAMFET in the OFF-state ($V_{DS} = 1.0$ V, $V_{GS} = 0.0$ V).

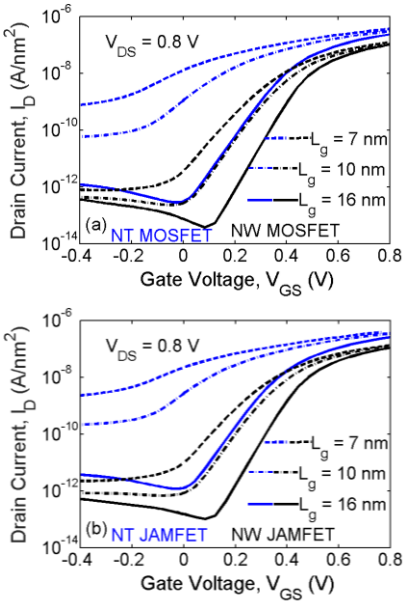

FIGURE 5. Impact of gate length scaling on (a) NT and NW MOSFET and (b) NT and NW JAMFET.

induced increase in the OFF-state current also degrades the sub-threshold slope of the NT MOSFET (82 mV/dec) and JAMFET (89.3 mV/dec) compared with the NW MOSFET (64.1 mV/dec) and JAMFET (65.2 mV/dec). Therefore, the enhanced gate control offered by NT architecture is detrimental from L-BTBT GIDL perspective.

Furthermore, the impact of gate length scaling on the performance of the NT and NWFETs is shown in Fig. 5. The OFF-state current of NTFETs increases significantly as compared to the NWFETs when the channel length is reduced to 7 nm. It may be noted that the threshold voltage also shifts for NTFETs with $L_g = 7$ nm reducing the OFF-state voltage to ~ -0.2 V. The performance degradation in NTFETs is attributed to the reduction in the source to channel barrier height and the additional L-BTBT GIDL due to the core gate as shown in Fig. 6. Therefore, L-BTBT GIDL is detrimental for the scaling of NTFETs and needs to be alleviated.

Since a gate-sidewall spacer is indispensable in NTFETs [22]–[24], we have also compared the performance of NT and NWFETs with different spacers in Fig. 7.

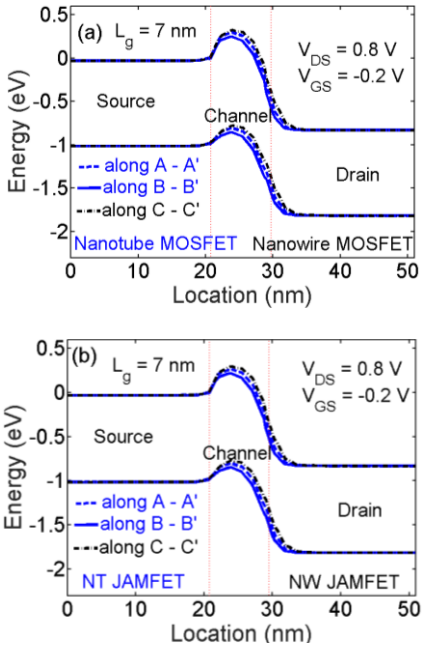

FIGURE 6. Energy band profiles of (a) NT and NWMOSFET and (b) NT and NWJAMFET for $L_g = 7$ nm.

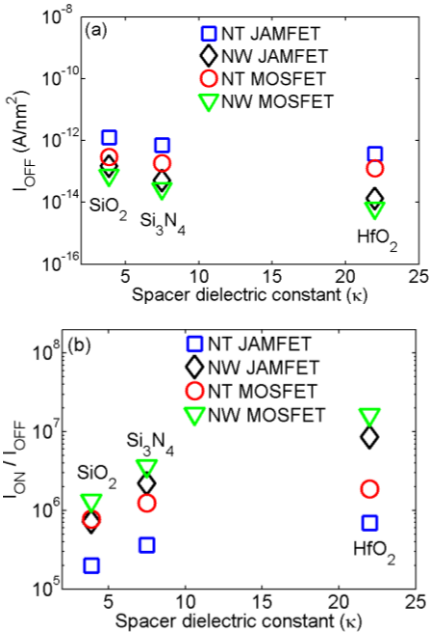

FIGURE 7. Variation of (a) OFF-state current (I_{OFF}) and (b) I_{ON}/I_{OFF} of NT and NW FETs with different spacers.

The inclusion of HfO_2 spacer in NT and NWFETs reduces the OFF-state current increasing the ON-state to OFF-state current ratio (I_{ON}/I_{OFF}). This reduction in the OFF-state current is attributed to the increased tunneling width owing to the attenuation in the transition of the bands due to the inclusion of high-κ spacer as shown in Fig. 8.

However, the inclusion of high-κ spacer may degrade the dynamic performance of the NT and NWFETs due to the increased fringing field. As shown in Fig. 9, the total

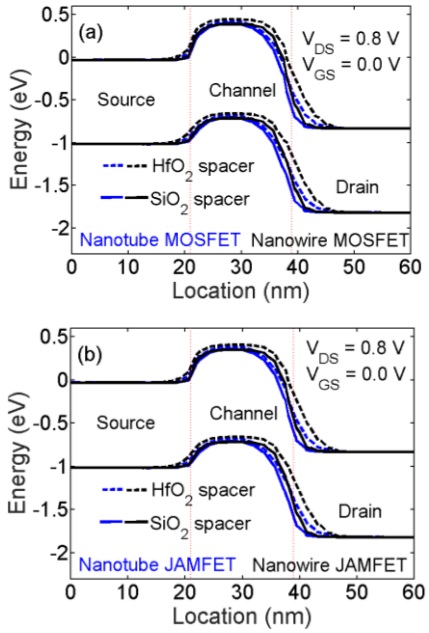

FIGURE 8. Energy band profiles taken at a cutline A-A′ for NT and C-C′ for NW (a) MOSFET and (b) JAMFET with different spacers.

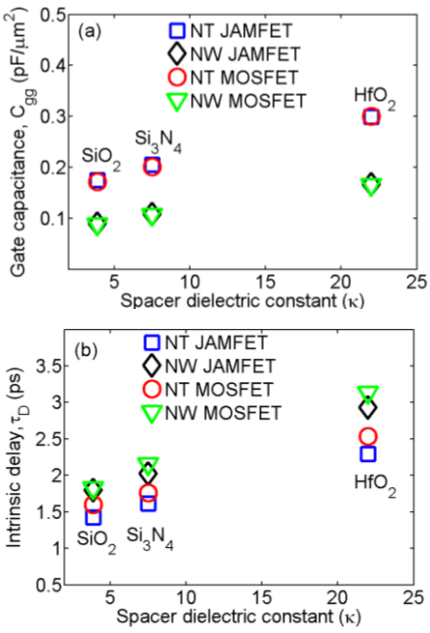

FIGURE 9. Variation of (a) gate capacitance (C_{gg}) and (b) intrinsic delay (τ_D) of the NT and NW FETs with different spacers.

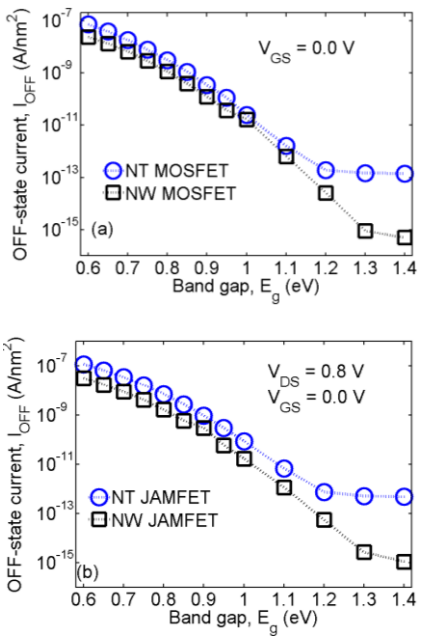

FIGURE 10. Variation of OFF-state current (I_{OFF}) of NT and NW (a) MOSFET and (b) JAMFET with the intrinsic material band gap (E_g).

gate capacitance (C_{gg}) is increased by nearly two times in the NTFETs compared to the NWFETs owing to the core gate. However, the intrinsic delay, calculated using the effective drive current method [34] as done in [7]–[9], for the NWFETs is ∼1.3 times larger than the NTFETs owing to the increased drive current offered by the NT architecture. Therefore, the intrinsic delay is improved in the NTFETs inspite of increased gate capacitance. In addition, an increase in the spacer dielectric constant increases the intrinsic delay due to an increase in the outer fringe capacitance owing to larger fringing fields. Therefore, the improvement in I_{ON}/I_{OFF} by the inclusion of high-κ spacer can be traded-off with an increased delay in NT and NWFETs.

In addition, the L-BTBT depends significantly on the intrinsic material band gap (E_{g0}). Therefore, the OFF-state current of NTFETs and NWFETs with different E_{g0} have been compared in Fig. 10. The effective band gap is calculated as: $E_{g,eff} = E_{g0} - dE_{g0}$ (BGN factor); with an error of ±0.00085 % [31]. As observed from Fig. 10, the L-BTBT enhanced OFF-state current reduces with increasing band gap. Although the tunneling current also depends on the effective tunneling mass, the OFF-state current of Ge ($E_g \sim 0.64$ eV) NTFETs and NWFETs is expected to be higher than that of Si ($E_g \sim 1.12$ eV) or GaAs ($E_g \sim 1.39$ eV) if same device dimensions are used (Fig. 10). Further, as the silicon thickness is reduced below 7 nm, the quantum confinement effects become dominant [32] and lead to a considerable discretization of the energy bands. This restricts the tunneling to occur between the first sub bands of the conduction band and valence band leading to an effective increase in the band gap [35]–[37]. The band gap increases to 1.341 eV when the silicon thickness is reduced to 5 nm [37]. Therefore, the L-BTBT and hence, the OFF-state current is expected to reduce significantly in the sub-5 nm regime where the quantum confinement effects are dominant.

The drain bias sensitivity of the L-BTBT in the NT and NWFETs has been compared in Fig. 11. While a V_{DS} of 0.5 V is insufficient to facilitate the band alignment for L-BTBT, a high V_{DS} (0.85 V) results in a larger drain induced barrier lowering (DIBL) and a consequent large drain induced barrier

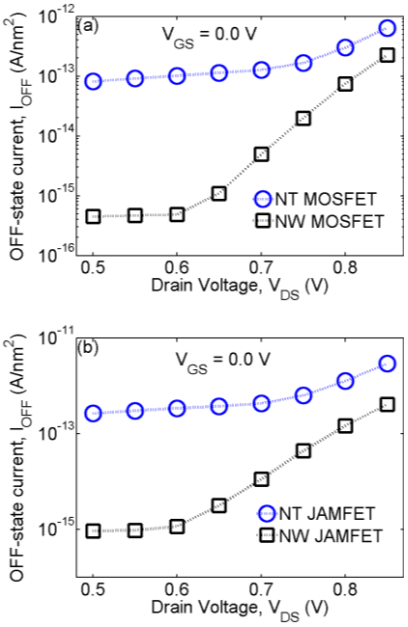

FIGURE 11. Variation of OFF-state current (I_{OFF}) of NT and NW (a) MOSFET and (b) JAMFET with the drain voltage (V_{DS}).

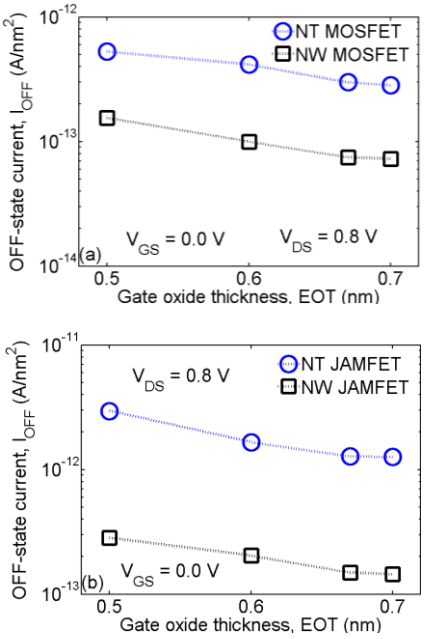

FIGURE 13. Variation of OFF-state current (I_{OFF}) of NT and NW (a) MOSFET and (b) JAMFET with the effective gate oxide thickness (EOT).

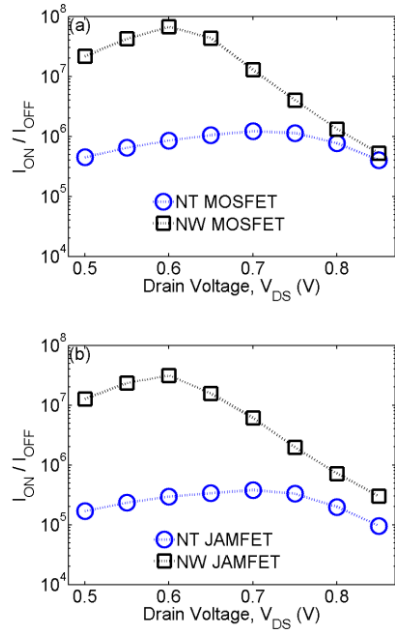

FIGURE 12. Variation of ON-state to OFF-state current current ratio (I_{ON}/I_{OFF}) of NT and NW (a) MOSFET and (b) JAMFET with the drain voltage (V_{DS}).

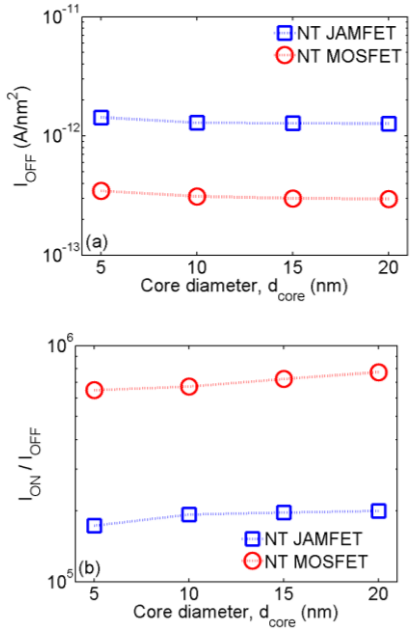

FIGURE 14. Variation of (a) OFF-state current (I_{OFF}) and (b) I_{ON}/I_{OFF} of NT MOSFET and JAMFET with the core diameter.

thinning (DIBT) [11] leading to a reduction in the tunneling width and a higher L-BTBT. Furthermore, a drain voltage of 0.7 V in NTFETs and 0.6 V in NWFETs is found to exhibit the maximum I_{ON}/I_{OFF} for the 8/7 nm technology node as shown in Fig. 12. It may be noted that the ON-state current has been extracted as the drain current at $V_{DS} = V_{GS} = V_{DD}$.

Since L-BTBT originates due to efficient gate control, it is also dependent on the effective oxide thickness (EOT). Fig. 13 compares the sensitivity of the OFF-state current on variation in the EOT of NT and NWFETs. The OFF-state current increases with a reduction in oxide thickness due to an enhanced gate control resulting in an increased L-BTBT.

Furthermore, the OFF-state current in NTFETs also increases somewhat with a reduction in the core diameter as shown in Fig. 14. A larger core diameter leads to a lower flux of electric-field lines into the silicon film and

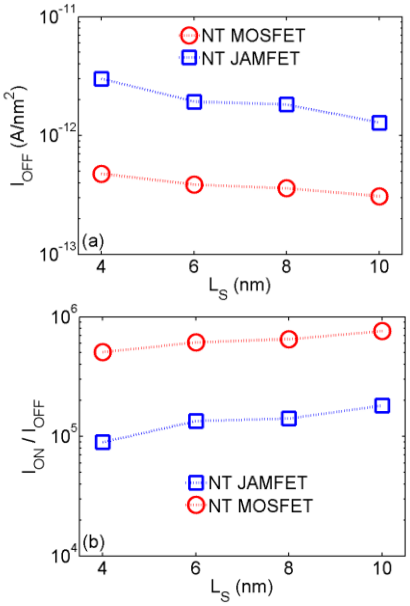

FIGURE 15. Variation of (a) OFF-state current (I_{OFF}) and (b) I_{ON}/I_{OFF} of NT MOSFET and JAMFET with the length of source/drain extension (L_S).

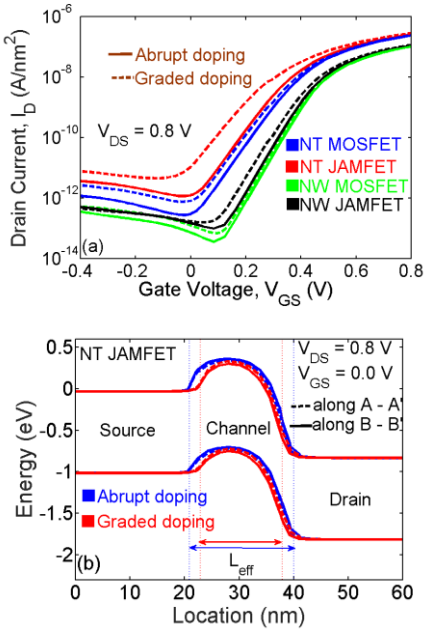

FIGURE 16. (a) Transfer characteristics of the NTFETs and NWFETs with an abrupt doping profile and with a graded doping profile (doping gradient = 1 nm/decade) and (b) Energy band profiles of the NT JAMFET with an abrupt doping profile and a graded doping profile.

therefore, results in a reduced electric-field [12]. A reduction in the electric field attenuates the band bending at the channel-drain interface and lowers the L-BTBT. However, an increase in the core diameter also enlarges the footprint of the NTFETs (which are inherently vertical). Therefore, the improvement in I_{ON}/I_{OFF} by increasing the core diameter can be traded-off with an increased footprint in NTFETs.

Since nanotube architecture is essentially a vertical structure, the scaling of the NTFETs is not limited by the length of the extension region. The core diameter, the silicon film thickness along with the gate electrode thickness dictates the footprint of the NTFETs and should be appropriately chosen. However, we have also analyzed the impact of the length of source/drain extension on the NTFETs as shown in Fig. 15. A shorter source/drain extension length leads to a higher electric field at the channel-drain interface resulting in a smaller tunneling width and therefore, a larger L-BTBT and a higher OFF-state current. Therefore, the source/drain extension length should be taken greater than 10 nm for optimum performance of NTFETs.

Furthermore, the L-BTBT changes with the doping profile and the abrupt doping profile considered in this work is not the realistic case. Therefore, to consider the realistic scenario, we have compared the transfer characteristics of the NTFETs and NWFETs with an abrupt doping profile and a graded doping profile at the source-channel and channel-drain interface with a doping gradient of 1 nm/decade [38], [39] as shown in Fig. 16. As can be observed from Fig. 16(a), the OFF-state current increases when a graded doping profile is used in both NTFETs and NWFETs. This can be understood from Fig. 16(b) and explained using the parasitic bipolar junction transistor (BJT) theory developed in [6]. The L-BTBT leads to the triggering of a parasitic BJT in the OFF-state in both NTFETs and NWFETs [6]. A graded doping profile renders a lower effective channel length as shown in Fig. 16(b) which essentially translates into an effective lowering of the base width of the parasitic BJT. Therefore, the gain of the parasitic BJT increases significantly. Although the tunneling width does not increase significantly when a graded doping profile is used, the increased gain of the parasitic BJT leads to a large amplification of the tunneling current (base current) and increases the drain current. A lower effective channel length also leads to an increased short channel effect and hence, a lower source to channel barrier height further increasing the OFF-state current. Therefore, although an abrupt doping profile is worst case scenario for L-BTBT, it may not be the worst case scenario for overall device performance. However, although the OFF-state current increases when a graded doping profile is used, the increment is not significant and the trends remain the same. Therefore, the conclusions pointed in this work are valid even when a graded doping profile is used.

Fig. 17 compares the normalized OFF-state current and ON-state to OFF-state current ratio (I_{ON}/I_{OFF}) of NTFETs and NWFETs with the ITRS target for the 8/7 nm technology node (OFF-state current = 10 pA/μm and ON-state to OFF-state current ratio of 5.74×10^6 [4], [30]). The drain current has been normalized per unit width by dividing it with the effective silicon film circumference, as done in [12], [22], and [23], which is $\pi(t_{Si})$ for the NWs and $\pi(d_{core} + t_{si})$ for the NTs. As can be observed from Fig. 17, although NWFETs and NTMOSFET satisfy the ITRS specifications of the

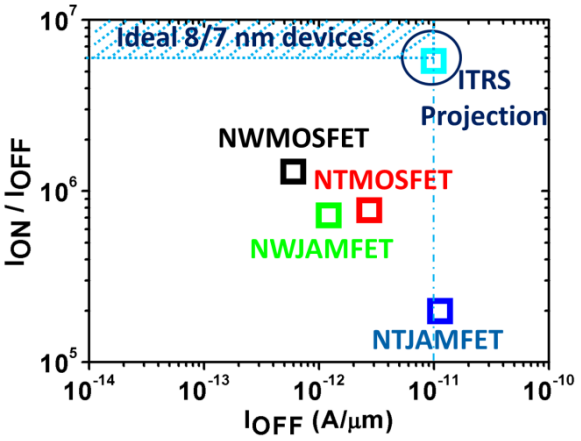

FIGURE 17. Comparison of the normalized OFF-state current (I_{OFF}) and ON-state to OFF-state current ratio (I_{ON}/I_{OFF}) of NTFETs and NWFETs with the ITRS target for the 8/7 nm technology node.

OFF-state current, all the NT and NW FET configurations fail to satisfy the ON-state to OFF-state current ratio requirement for the 8/7 nm node.

IV. CONCLUSIONS

In this work, we have performed a comparative analysis of L-BTBT GIDL in the NT and NWFETs. Our results clearly indicate that scaling the channel length and oxide thickness along with the supply voltage following a constant field scaling law does not mitigate the L-BTBT and it continues to degrade the performance of both NWFETs and NTFETs even at the 8/7-nm technology node. Moreover, the core gate induces an additional L-BTBT in the adjacent silicon film and increases the OFF-state current in NTFETs compared with the NWFETs. Therefore, the NTFETs exhibit a degraded performance in the sub-10 nm regime due to a larger L-BTBT. Therefore, the enhanced gate control offered by the nanotube architecture is detrimental from L-BTBT GIDL perspective and inhibits the scaling of NTFETs. In addition, we also demonstrate that compared with the NWFETs, although the total gate capacitance increases by nearly two times in NTFETs owing to the core gate, its dynamic performance is improved due to the increased drive current due to the NT architecture. Furthermore, we show that there exists a trade-off between the reduction in L-BTBT due to the use of (a) high-κ spacer and the intrinsic delay and (b) larger core diameter and device footprint. Therefore, these parameters must be chosen wisely while designing NTFETs. Although we have considered an abrupt doping profile to take into account the worst case scenario for L-BTBT and not considered direct source-to-drain tunneling (DSDT) due to the limitation of the commercial simulators to include intra-band tunneling, a full quantum simulation based study including the practical source/drain doping profiles, the impact of gate-drain overlap/underlap on L-BTBT and intra-band tunneling for evaluating the direct source-to-drain tunneling (DSDT) current for $L_g \leq 10$ nm could provide further new insights.

REFERENCES

[1] S. Saurabh and M. J. Kumar, *Fundamentals of Tunnel Field-Effect Transistors*. Boca Raton, FL, USA: CRC Press, Oct. 2016.

[2] M. K. Mamidala, R. Vishnoi, and P. Pandey, *Tunnel Field-Effect Transistors (TFET): Modelling and Simulation*. West Sussex, U.K.: Wiley, Nov. 2016.

[3] K. J. Kuhn, "Considerations for ultimate CMOS scaling," *IEEE Trans. Electron Devices*, vol. 59, no. 7, pp. 1813–1828, Jul. 2012.

[4] J. Fan, M. Li, X. Xu, Y. Yang, H. Xuan, and R. Huang, "Insight into gate-induced drain leakage in silicon nanowire transistors," *IEEE Trans. Electron Devices*, vol. 62, no. 1, pp. 213–219, Jan. 2015.

[5] J. Hur *et al.*, "Comprehensive analysis of gate-induced drain leakage in vertically stacked nanowire FETs: Inversion-mode versus junctionless mode," *IEEE Electron Device Lett.*, vol. 37, no. 5, pp. 541–544, May 2016.

[6] S. Sahay and M. J. Kumar, "Physical insights into the nature of gate-induced drain leakage in ultrashort channel nanowire FETs," *IEEE Trans. Electron Devices*, vol. 64, no. 6, pp. 2604–2610, Jun. 2017.

[7] S. Sahay and M. J. Kumar, "A novel gate-stack-engineered nanowire FET for scaling to the sub-10-nm regime," *IEEE Trans. Electron Devices*, vol. 63, no. 12, pp. 5055–5059, Dec. 2016.

[8] S. Sahay and M. J. Kumar, "Spacer design guidelines for nanowire FETs from gate-induced drain leakage perspective," *IEEE Trans. Electron Devices*, vol. 64, no. 7, pp. 3007–3015, Jul. 2017.

[9] S. Sahay and M. J. Kumar, "Insight into lateral band-to-band-tunneling in nanowire junctionless FETs," *IEEE Trans. Electron Devices*, vol. 63, no. 10, pp. 4138–4142, Oct. 2016.

[10] S. Sahay and M. J. Kumar, "Controlling L-BTBT and volume depletion in nanowire JLFETs using core–shell architecture," *IEEE Trans. Electron Devices*, vol. 63, no. 9, pp. 3790–3794, Sep. 2016.

[11] S. Sahay and M. J. Kumar, "Diameter dependence of leakage current in nanowire junctionless field effect transistors," *IEEE Trans. Electron Devices*, vol. 64, no. 3, pp. 1330–1335, Mar. 2017.

[12] S. Sahay and M. J. Kumar, "Nanotube junctionless FET: Proposal, design, and investigation," *IEEE Trans. Electron Devices*, vol. 64, no. 4, pp. 1851–1856, Apr. 2017.

[13] V. Nathan and N. C. Das, "Gate-induced drain leakage current in MOS devices," *IEEE Trans. Electron Devices*, vol. 40, no. 10, pp. 1888–1890, Oct. 1993.

[14] T. Hoffmann *et al.*, "GIDL (gate-induced drain leakage) and parasitic Schottky barrier leakage elimination in aggressively scaled HfO_2/TiN FinFET devices," in *IEDM Tech. Dig.*, 2005, pp. 725–729.

[15] J.-P. Colinge *et al.*, "Nanowire transistors without junctions," *Nature Nanotechnol.*, vol. 5, no. 3, pp. 225–229, Mar. 2010.

[16] S. Sahay and M. J. Kumar, "Realizing efficient volume depletion in SOI junctionless FETs," *IEEE J. Electron Devices Soc.*, vol. 4, no. 3, pp. 110–115, May 2016.

[17] M. J. Kumar and S. Sahay, "Controlling BTBT-induced parasitic BJT action in junctionless FETs using a hybrid channel," *IEEE Trans. Electron Devices*, vol. 63, no. 8, pp. 3350–3353, Aug. 2016.

[18] S. Sahay and M. J. Kumar, "Symmetric operation in an extended back gate JLFET for scaling to the 5-nm regime considering quantum confinement effects," *IEEE Trans. Electron Devices*, vol. 64, no. 1, pp. 21–27, Jan. 2017.

[19] C.-W. Lee *et al.*, "Performance estimation of junctionless multigate transistors," *Solid-State Electron.*, vol. 54, no. 2, pp. 97–103, Feb. 2010.

[20] T. K. Kim *et al.*, "First demonstration of junctionless accumulation-mode bulk FinFETs with robust junction isolation," *IEEE Electron Device Lett.*, vol. 34, no. 12, pp. 1479–1481, Dec. 2013.

[21] V. Thirunavukkarasu, Y.-R. Jhan, Y.-B. Liu, and Y.-C. Wu, "Performance of inversion, accumulation, and junctionless mode n-type and p-type bulk silicon FinFETs with 3-nm gate length," *IEEE Electron Device Lett.*, vol. 36, no. 7, pp. 645–647, Jul. 2015.

[22] H. M. Fahad, C. E. Smith, J. P. Rojas, and M. M. Hussain, "Silicon nanotube field effect transistor with core–shell gate stacks for enhanced high-performance operation and area scaling benefits," *Nano Lett.*, vol. 11, no. 10, pp. 4393–4399, Oct. 2011.

[23] H. M. Fahad and M. M. Hussain, "Are nanotube architectures more advantageous than nanowire architectures for field effect transistors?" *Sci. Rep.*, vol. 2, no. 2, Jun. 2012, Art. no. 475.

[24] D. Tekleab, H. H. Tran, J. W. Sleight, and D. Chidambarrao, "Silicon nanotube MOSFET," U.S. Patent 0 217 468, Aug. 30, 2012.

[25] D. Tekleab, "Device performance of silicon nanotube field effect transistor," *IEEE Electron Device Lett.*, vol. 35, no. 5, pp. 506–508, May 2014.

[26] A. N. Hanna, H. M. Fahad, and M. M. Hussain, "InAs/Si hetero-junction nanotube tunnel transistors," *Sci. Rep.*, vol. 9, Apr. 2015, Art. no. 9843.

[27] H. M. Fahad and M. M. Hussain, "High-performance silicon nanotube tunneling FET for ultralow-power logic applications," *IEEE Trans. Electron Devices*, vol. 60, no. 3, pp. 1034–1039, Mar. 2013.
[28] A. N. Hanna and M. M. Hussain, "Si/Ge hetero-structure nanotube tunnel field effect transistor," *J. Appl. Phys.*, vol. 117, no. 1, pp. 014310-1–014310-7, Jan. 2015.
[29] S. Soleimani-Amiri, A. Gholizadeh, S. Rajabali, Z. Sanaee, and S. Mohajerzadeh, "Formation of Si nanorods and hollow nano-structures using high precision plasma-treated nanosphere lithography," *RSC Adv.*, vol. 4, pp. 12701–12709, Feb. 2014.
[30] (2012). *International Technology Roadmap for Semiconductors*. [Online]. Available: http://public.itrs.net
[31] *Sentaurus Device User Guide*, Synopsys, Inc., Mountain View, CA, USA, 2010.
[32] J. Colinge, J. C. Alderman, W. Xiong, and C. R. Cleavelin, "Quantum-mechanical effects in trigate SOI MOSFETs," *IEEE Trans. Electron Devices*, vol. 53, no. 5, pp. 1131–1136, May 2006.
[33] S. Gundapaneni, M. Bajaj, R. K. Pandey, K. V. R. Murali, S. Ganguly, and A. Kottantharayil, "Effect of band-to-band tunneling on junctionless transistors," *IEEE Trans. Electron Devices*, vol. 59, no. 4, pp. 1023–1029, Apr. 2012.
[34] M. H. Na, E. J. Nowak, W. Haensch, and J. Cai, "The effective drive current in CMOS inverters," in *IEDM Tech. Dig.*, Dec. 2002, pp. 121–124.
[35] J. L. Padilla, F. Gámiz, and A. Godoy, "A simple approach to quantum confinement in tunneling field-effect transistors," *IEEE Electron Device Lett.*, vol. 33, no. 10, pp. 1342–1344, Oct. 2012.
[36] W. G. Vandenberghe, B. Sorée, W. Magnus, G. Groeseneken, and M. V. Fischetti, "Impact of field-induced quantum confinement in tunneling field-effect devices," *Appl. Phys. Lett.*, vol. 98, no. 14, pp. 143503-1–143503-3, Apr. 2011.
[37] D. D. D. Ma, C. S. Lee, F. C. K. Au, S. Y. Tong, and S. T. Lee, "Small-diameter silicon nanowire surfaces," *Science*, vol. 299, no. 5614, pp. 1874–1877, Mar. 2003.
[38] J.-S. Yoon, T. Rim, J. Kim, K. Kim, C.-K. Baek, and Y.-H. Jeong, "Statistical variability study of random dopant fluctuation on gate-all-around inversion-mode silicon nanowire field-effect transistors," *Appl. Phys. Lett.*, vol. 106, no. 10, pp. 103507-1–103507-5, Mar. 2015.
[39] J.-S. Yoon, K. Kim, T. Rim, and C.-K. Baek, "Variability study of Si nanowire FETs with different junction gradients," *AIP Adv.*, vol. 6, no. 1, pp. 015318-1–015318-7, Jan. 2016.

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