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A Modified Topology of Two-Switch Buck-Boost Converter

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ABSTRACT Two-switch buck–boost (TSBB) is one of the non-isolated dc-to-dc converters that can change its mode from among buck, boost, and buck–boost modes. Changing its mode is possible by controlling gate signals. This paper presents a novel modified topology of TSBB converter. Even if the proposed converter has the same number of components as a conventional TSBB converter, the proposed converter has fewer conduction components and switching semiconductors than a conventional TSBB. This results in reduced power loss. Moreover, source terminals of metal–oxide–semiconductor field-effect transistor in the proposed converter are directly connected to ground. This configuration has an advantage in selecting gate driver integrated circuit (IC), since the IC does not necessarily need to provide high-side gate signals. A printed circuit board was designed to evaluate the improvement of the proposed converter.

INDEX TERMS Boost converter, buck converter, buck-boost converter, conduction losses, non-isolated DC-to-DC converter, MOSFET source terminal, switching losses.

I. INTRODUCTION

Over the past few years, the concepts of renewable energy generation, the direct current (DC) micro grid, high voltage direct current (HVDC), and the connection between an energy storage system (ESS) and a DC line have been suggested as alternatives for existing power stations and alternating current (AC) lines [1], [2]. A DC-to-DC converter plays an essential role in a DC micro grid, and for an ESS and renewable power generating systems, such as wind power, tide power, and photovoltaic and geothermal power stations [3]. A renewable power generating system is more effective when an ESS is added to compensate for, or absorb, fluctuations in power. If the power generating system cannot keep up with load power consumption, the ESS compensates for the shortage, whereas if the system overproduces power that cannot be fully consumed by the load, the ESS stores the remainder [4]. This combined power generation and ESS system is connected to an AC line or a DC micro grid. Therefore, controlling the DC source to DC load becomes a more important issue. In particular, efficient, stable, and less noisy power transfer should be achieved even if diverse input and output conditions exist. There are three basic converters: buck, boost and buck-boost. Each single-switch buck, boost and buck-boost converter has unique advantages corresponding to input and load conditions of its own. A buck converter is basically a step-down converter and is relatively stable. A boost converter is step-up converter but has right-half-plane zero (RHPZ), and is thus rather unstable when the converter operates in continuous conduction mode (CCM). A buck-boost converter can satisfy either step-up or step-down needs, but has higher voltage stresses on semiconductors than buck and boost converters and also has RHPZ [5]. In this respect, the existing two-switch buck-boost (TSBB) converter has its own advantages, compared with single-switch buck-boost converters. A single-switch buck-boost converter diagram and a conventional two-switch buck-boost converter circuit diagram are presented in Fig. 1 and Fig. 2, respectively. The TSBB converter can switch to buck, boost or buck-boost mode to optimize the control strategy and its efficiency, while only two semiconductors are required to constitute the topology [6], [7]. A single-switch buck-boost converter, however, only operates in buck-boost mode. The TSBB converter puts lower voltage stress on semiconductors. As seen in Fig. 2, switch S_1 and diode D_1, and switch S_2 and diode D_2 are clamped to V_{in} and V_o, but in a single-switch buck-boost converter, semiconductors S_1 and D_1 have to endure $V_{in}+V_o$ voltages. However, the conventional TSBB converter has larger power losses than a single-switch buck

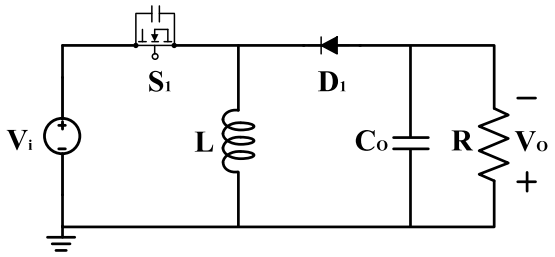


FIGURE 1. Circuit diagram of the single switch buck-boost converter.

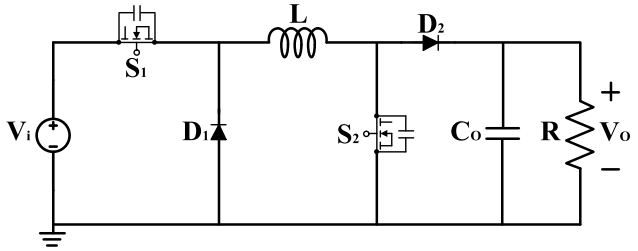


FIGURE 2. Circuit diagram of the conventional TSBB converter.

boost converter because of the additional semiconductors (one diode and one switch). In this paper, a new topology for a two-switch buck-boost converter is presented to decrease power losses of conventional TSBB, as shown in Fig. 3.

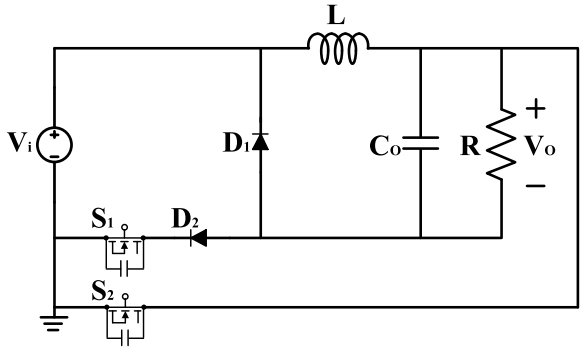


FIGURE 3. Circuit diagram of the proposed converter.

This paper is arranged as follows. At Section I, the reason for why modified version of TSBB topology is needed was suggested. Section II discusses operational principles of the conventional and the proposed converters in each mode. Analysis of reduced switching and conduction losses are discussed in Section III. Section IV explains the benefit of connection between the source of MOSFET and ground. Section V includes design and analysis of the proposed converter. Experimental results are presented in Section VI. Finally, the conclusions are given in Section VII.

II. OPERATION METHOD

A. CONVENTIONAL TSBB CONVERTER

Fig. 2 shows the conventional TSBB converter topology. The converter consists of an inductor, two switches, and two diodes. It can be simply derived from series connection of a basic buck converter and boost converter. It can change mode by controlling the gate signals of S_1 and S_2. Table 1 presents a control scheme to determine the converter's modes. For example, if S_2 is off and S_1 is switching as indicated in Table 1, the circuit acts as a buck converter.

TABLE 1. Control scheme of the conventional TSBB converter.

Mode	Control scheme
Buck	S_1: switching S_2: off
Boost	S_1: on S_2: switching
Buck-Boost	S_1: switching (simultaneously with S_2) S_2: switching (simultaneously with S_1)

B. PROPOSED CONVERTER

Fig. 3 suggests new buck boost converter to overcome power loss problems in the existing TSBB converter. The proposed converter can alternate from among three different basic DC-to-DC regulation modes: buck, boost and buck-boost. Table 2 presents a control scheme to determine the converter's mode. There are only two current paths that inductor current flows through. One leads to the load, and the other to S_2. Therefore, the average inductor current is dependent on d_2, the duty cycle of S_2. The average inductor current is equal to $I_O/(1-d_2)$, where I_O is load current [7]. Fig. 4 illustrates the current path of the proposed converter corresponding to each mode. The current path of each mode follows basic buck, boost and buck-boost converter principles. For example, when S_1 is on and S_2 is off in buck mode, which indicates subinterval t_0 to t_1 as marked in Fig. 4(a), inductor current begins to build up. Next, S_1 and S_2 are off, which points subinterval t_1 to t_0', then inductor current starts to descend and conducts via diode D_1, not input source V_I as shown in Fig. 4(a).

TABLE 2. Control scheme of the proposed converter.

Mode	Control scheme
Buck	S_1: switching S_2: off
Boost	S_1: on S_2: switching
Buck-Boost	S_1: off S_2: switching

An unusual switch on/off operation method is applied in boost mode. It is shown in Fig. 4(b). As seen in Table 2, S_1 is turned on continuously. This means that voltage between source and ground maintains the turn-on voltage of the gate. S_2 is also turned on during this interval. Then, there are two possible current paths. One candidate is the line between

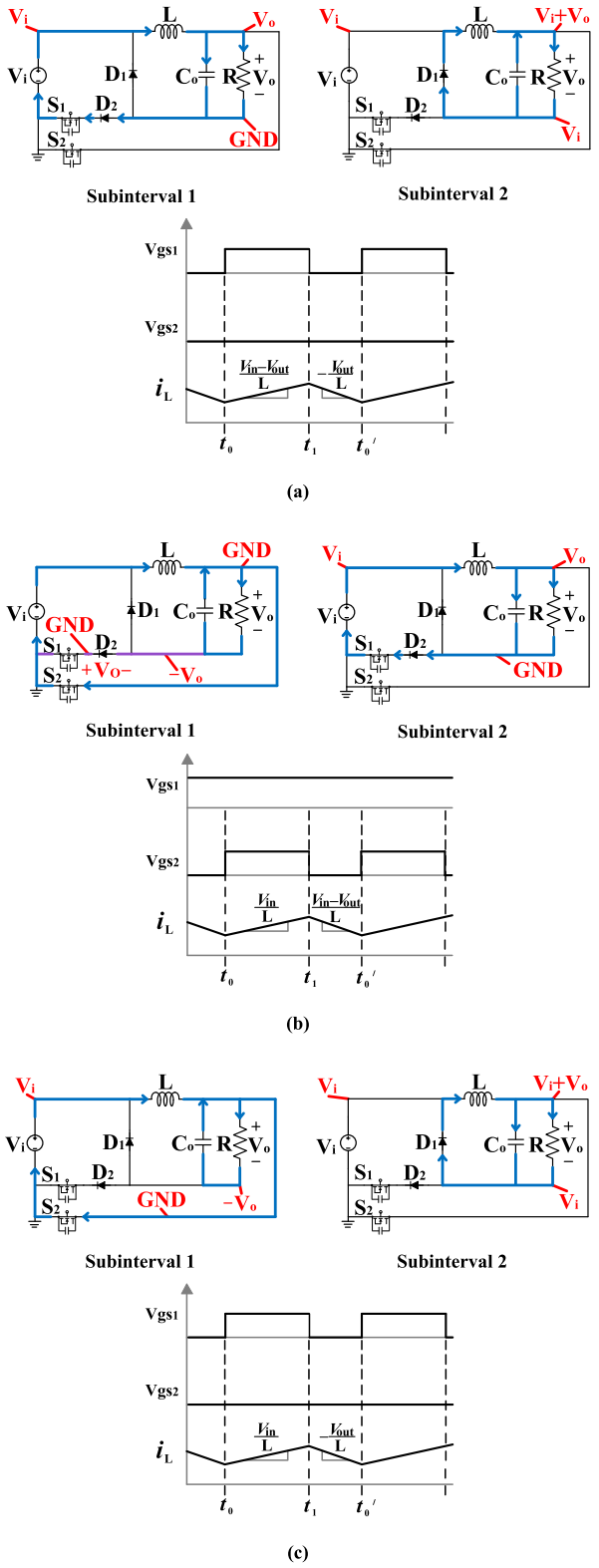


FIGURE 4. Current paths and inductor current wave of the proposed converter: (a) buck mode, (b) boost mode, and (c) buck-boost mode.

L and S_2. The other is the line through load D_2 and S_1. However, current only flows through the former. Since S_2 is turned on, the ground node extends to before the load. As a result, diode D_2 is reverse-biased, and current cannot be conducted via the purple line. Inductor current is built up during this time, and decreases during t_1 to t_0'. Further discussion will be offered in Section III in terms of boost mode operation in the proposed converter. Consequently, the converter operates normally with the above-mentioned gate control scheme.

III. ANALYSIS ON VOLTAGE STRESSES, CONDUCTION LOSSES AND SWITCHING LOSSES

The conventional TSBB has advantages, compared with the single-switch buck-boost converter, as discussed in Section I. However, a TSBB converter has additional semiconductors. These cause more power dissipation. In this paper and the experiments, MOSFETs are used for a switching device. Power loss in MOSFETs and diodes can be divided into conduction loss and switching loss. Switching losses are generated by the current and voltage during the transient phase from the on-state to the off-state, or vice versa. On the other hand, conduction losses occur while currents flow through semiconductors. Total losses in the MOSFET, P_M, are separated with

$$P_M = P_{cM} + P_{cBD} + P_{swM} + P_{swBD}, \tag{1}$$

where P_{cM} is conduction loss of the MOSFET itself, P_{cBD} is conduction loss of the body diode, P_{swM} is switching loss of the MOSFET itself, and P_{swBD} is switching loss of the body diode. Total power losses of the diode, P_D, are separated with

$$P_D = P_{cD} + P_{swD}, \tag{2}$$

where P_{cD} is conduction loss of the diode, and P_{swD} is switching loss of the diode [8].

Therefore, since the conventional TSBB converter has two more semiconductors, the sum of conduction and switching losses generated become larger than in a single-switch buck-boost converter. If the number of conduction and switching semiconductors decreases, the total loss in a converter diminishes. Viewed in this light, a new topology was suggested in Section II to attain higher efficiency by reducing the number of conduction and switching semiconductors. However, the voltage stresses across the semiconductors must be carefully considered, since the voltage stresses are one factor causing power losses in the semiconductors. The voltage stresses of the conventional and the proposed converter are listed in Table 3. In Table 3, C_S indicates an equivalent parallel capacitor when switches are in the off-state. It is usually designated C_{oss}. C_D is the equivalent parallel capacitor when the diodes are in the off-state [9]. C_S and C_D are needed to identify semiconductor voltage stresses. One can make the observation that S_1 and D_2 are connected sequentially in Fig. 4. Therefore, when S_1 and D_2 are off, voltages across S_1 and D_2 are divided by a capacitance voltage division rule. In the buck-boost mode, either larger voltage of V_{in} or V_{out} is the maximum voltage stress across S_1 and D_2.

Table 4 lists conduction and switching semiconductors of the conventional TSBB and the proposed converter in each

TABLE 3. Voltage stresses on semiconductors: (a) the conventional TSBB converter and (b) the proposed converter.

Operation mode	S1	S2	D1	D2
buck mode	V_{in}	V_{out}	V_{in}	-
boost mode	-	V_{out}	V_{in}	V_{out}
buck-boost mode	V_{in}	V_{out}	V_{in}	V_{out}

(a)

Operation mode	S1	S2	D1	D2
buck mode	$\frac{C_{D2}}{C_{S1}+C_{D2}}V_{in}$	$V_{in}+V_{out}$	V_{in}	$\frac{C_{S1}}{C_{S1}+C_{D2}}V_{in}$
boost mode	$\frac{C_{D2}}{C_{S1}+C_{D2}}V_{out}$	V_{out}	$V_{in}+V_{out}$	$\frac{C_{S1}}{C_{S1}+C_{D2}}V_{out}$
buck-boost mode	$\frac{C_{D2}}{C_{S1}+C_{D2}}V_{in}$ OR $\frac{C_{D2}}{C_{S1}+C_{D2}}V_{out}$	$V_{in}+V_{out}$	$V_{in}+V_{out}$	$\frac{C_{S1}}{C_{S1}+C_{D2}}V_{in}$ OR $\frac{C_{S1}}{C_{S1}+C_{D2}}V_{out}$

(b)

TABLE 4. Conduction and switching components of the conventional TSBB and the proposed converter: (a) conduction components and (b) switching components.

Operation mode	Subinterval	Conventional TSBB converter	Proposed converter
buck mode	Subinterval 1	S_1, D_2	S_1, D_2
	Subinterval 2	D_1, D_2	D_1
boost mode	Subinterval 1	S_1, S_2	S_2
	Subinterval 2	S_1, D_2	S_1, D_2
buck-boost mode	Subinterval 1	S_1, S_2	S_2
	Subinterval 2	D_1, D_2	D_1

(a)

Operation mode	Conventional TSBB converter	Proposed buck-boost converter
buck mode	S_1, D_1	S_1, D_1, D_2
boost mode	S_2, D_2	S_2, D_2
buck-boost mode	S_1, S_2, D_1, D_2	S_2, D_1

(b)

mode. If a semiconductor conducts subinterval 1 and does not conduct subinterval 2, the semiconductor is switching components.

When a MOSFET is on, on-state equivalent resistance R_{dson} is a relevant factor. The body diode is presumed to be off when the MOSFET is off.

$$v_{ds}(i_{ds}) = R_{dson}(i_{ds}) \times i_{ds}, \tag{3}$$

$$P_{cM}(i_{ds}) = R_{dson}(i_{ds}) \times I^2_{ds,rms}, \tag{4}$$

$R_{dson}(i_{ds})$ means R_{dson} is a function of i_{ds}, the conduction current through drains to the source. $R_{dson}(i_{ds})$ can be found in each MOSFET datasheet, and it is described in graph form [8]. On the other hand, when a diode is on, the voltages across the diode can be modelled with forward drop voltage v_{Df} and on-state resistance R_{Don}.

$$v_D(i_D) = v_{Df} + R_{Don} \times i_D, \tag{5}$$

$$P_{cD}(i_D) = v_{Df} \times I_{D,avg} + R_{Don} \times I^2_{D,rms}, \tag{6}$$

where, i_D is current flowing through a diode.

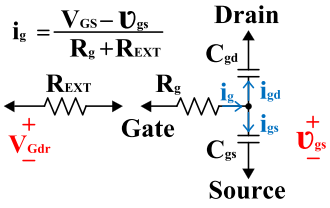


FIGURE 5. An equivalent gate circuit of a MOSFET and an external gate resistor.

Parameters in terms of switching losses in MOSFETs and diodes are more various than those of conduction losses. Fig. 5 draws a typical equivalent gate circuit of a MOSFET and an external gate resistor included in the gate drive circuit [10]. Fig. 6 describes the relationship between gate-source voltage, gate current, drain-source voltage and drain-source current when a MOSFET changes its state from off to on [10], [11]. When gate drive voltage V_{dr} is applied to a gate terminal, gate-source voltage v_{gs} starts to rise at t_1. When v_{gs} reaches threshold voltage, $V_{GS,th}$, drain-source current i_{ds} begins to go up until v_{gs} becomes the gate plateau voltage, $V_{GS,pl}$ ($t_1 \leq t \leq t_2$). v_{gs} is constant, when passing by the Miller plateau, and finally, the gate is fully on when v_{gs} has the same value as V_{dr}, and v_{ds} is equal to $R_{dson} \times i_{ds}$ at t_3. The same principles are applied for turn-off [8]. Fig. 6 shows that switching losses in MOSFETs can be divided into

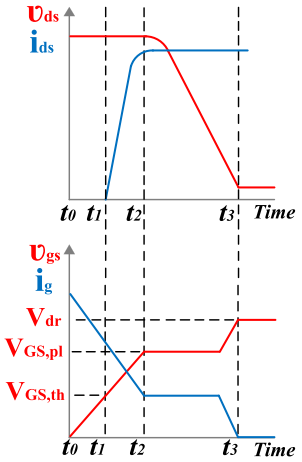


FIGURE 6. Turn-on transient of the MOSFET.

two factors. One is a function of v_{ds} and i_{ds}. This power loss occurs during t_1 to t_3. The other takes place due to V_{dr} and i_g, called gate-drive losses ($t_0 \leq t \leq t_3$). Therefore, $P_{DS,off}$ and $P_{GS,off}$ are obtained with the same formula in (8) and (9). P_{DS} is approximately proportional to v_{ds} and i_{ds} [8]. P_{GS} is formulated with a nonlinear function of v_{ds}, when V_{dr} is fixed, due to the nonlinear relationship between

$$P_{swM} = P_{DS} + P_{GS} = P_{DS,on} + P_{DS,off} + P_{GS,on} + P_{GS,off}, \quad (7)$$

$$P_{DS,on}(i_{ds}, v_{ds}) = \frac{1}{T_{sw}} \int_{t_1}^{t_3} i_{ds} \times v_{ds} dt, \quad (8)$$

$$P_{GS,on}(i_g, V_{dr}) = \frac{1}{T_{sw}} \int_{t_0}^{t_3} i_g \times V_{dr} dt \frac{V_{dr}}{T_{sw}} \int_{t_0}^{t_3} i_g dt, \quad (9)$$

v_{ds} and C_{iss}, where $C_{iss} = C_{gs} + C_{gd}$. C_{gs} is equivalent capacitance between gate and source. C_{gd} is equivalent capacitance between gate and drain. i_g is needed to charge or discharge C_{gs} and C_{gd} in Fig. 5. P_{GS} is much smaller than P_{DS} in ordinary situations. Since charges Q_{gs} and Q_{gd} are nano-scale, according to MOSFET data sheets generally, gate current i_g is very small.

Reverse recovery is the main cause of diode turn-off losses, $P_{swD,off}$. But diode turn-on losses are negligible. Therefore,

$$P_{swD} = P_{swD,on} + P_{swD,off} \approx P_{swD,off}, \quad (10)$$

Power losses of the proposed converter are compared to those of the conventional converter as demonstrated in the following three cases.

A. IN BUCK MODE

Table 4 gives information about which semiconductors conduct and which semiconductors generate switching losses. An assumption is needed whereby the ripple of the inductor current is sufficiently small. This assumption means the converters will operate only in CCM. Thus, by neglecting the current ripple, all conduction losses of semiconductors become functions of $I_{L,avg}$, where $I_{L,avg}$ is average inductor current. First, the sum of total conduction losses in the conventional TSBB converter is

$$P_{c,TSBB} = P_{cS1} + P_{cD2,1} + P_{cD1} + P_{cD2,2} \approx P_{cS1} + 2P_{cD2} + P_{cD1}, \quad (11)$$

The last approximation is reasonable under the above-mentioned assumption. In the proposed converter, the sum of total conduction losses is

$$P_{c,prop} = P_{cS1} + P_{cD2} + P_{cD1}, \quad (12)$$

Switching losses are unlike conduction losses. Switching losses are functions of their voltage stresses. Voltage stresses on the semiconductors are organized in Table 3. The sums of the switching losses in the conventional TSBB and the proposed converter are

$$P_{sw,TSBB} = P_{swS1}(V_{in}) + P_{swD1}(V_{in}), \quad (13)$$

$$P_{sw,prop} = P_{swS1}(\frac{C_{D2}}{C_{S1} + C_{D2}} V_{in}) + P_{swD1}(V_{in}) + P_{swD2}(\frac{C_{S1}}{C_{S1} + C_{D2}} V_{in}), \quad (14)$$

By comparing (11) to (12) and (13) to (14), one can reach the conclusion that the proposed converter has one less conduction component and one more switching component. However, in (14), the sum of $P_{swS1}(\frac{C_{D2}}{C_{S1}+C_{D2}} V_{in})$ and $P_{swD2}(\frac{C_{S1}}{C_{S1}+C_{D2}} V_{in})$ is not always larger than $P_{swS1}(V_{in})$. Since P_{swS} is approximately linear with voltages across the drain to the source, $P_{swS1}(\frac{C_{D2}}{C_{S1}+C_{D2}} V_{in})$ is smaller than $P_{swS1}(V_{in})$. Power losses due to reverse recovery are the main portion of P_{swD}. Therefore, though the proposed converter has one more switching component, if reverse recovery is not dominant, $P_{sw,prop}$ would be less than $P_{sw,TSBB}$. Consequently, the relative efficiency of the proposed converter over the TSBB converter in buck mode depends on properties that are given by data sheets and operation conditions.

B. IN BOOST MODE

By using the same principles, conduction and switching losses can be arranged in boost mode.

$$P_{c,TSBB} = P_{cS1,1} + P_{cS2} + P_{cS1,2} + P_{cD2} \approx 2P_{cS1} + P_{cS2} + P_{cD2}, \quad (15)$$

$$P_{c,prop} = P_{cS2} + P_{cS1} + P_{cD2}, \quad (16)$$

$$P_{sw,TSBB} = P_{swS2}(V_{out}) + P_{swD2}(V_{out}), \quad (17)$$

$$P_{sw,prop} = P_{swS2}(V_{out}) + P_{swD2}(\frac{C_{S1}}{C_{S1} + C_{D2}} V_{out}), \quad (18)$$

One conduction semiconductor, S_1, is less in $P_{c,prop}$. In addition, switching losses also diminish due to voltage stresses across D_2. However, the proposed converter operates with a special gate on-off strategy. In the ordinary method, S_1 and S_2 switch alternatively. On the other hand, in the proposed, converter S_1 maintains the on-state during either subinterval 1 or subinterval 2. Even if S_1 keeps the on-state, currents cannot flow through S_1 due to reverse voltage across D_2, and thus, the converter works without problem. Under this strategy, power losses occur in S_1. But this draws attention to power losses caused by leakage currents of Q_{gs}. To maintain v_{gs} to V_{dr} as shown in Fig. 6, C_{gs} holds charge Q_{gs} in Fig. 5. But leakage currents arise, and thus, the gate drive circuit has to replenish charges as much as leakage currents via current path i_g. Power losses occur by $V_{dr} \times i_g$. However, i_g is negligible, since Q_{gs} are dozens or less [nC]. Consequently, improvement by maintaining S_1 in the on-state is much greater than gate-drive losses.

As a result, the proposed converter is more efficient than the conventional TSBB converter owing to the number of conduction semiconductors, less voltage stress on the MOSFET, and the special switching method in boost mode.

C. IN BUCK-BOOST MODE

The same logic is valid in buck-boost mode. Conduction and switching losses are

$$P_{c,TSBB} = P_{cS1} + P_{cS2} + P_{cD1} + P_{cD2}, \quad (19)$$

$$P_{c,prop} = P_{cS2} + P_{cD1}, \quad (20)$$

$$P_{sw,TSBB} = P_{swS1}(V_{in}) + P_{swS2}(V_{out}) + P_{swD1}(V_{in}) + P_{swD2}(V_{out}), \quad (21)$$

$$P_{sw,prop} = P_{swS2}(V_{in} + V_{out}) + P_{swD1}(V_{in} + V_{out}), \quad (22)$$

By observing (19) and (20), the proposed converter has two fewer conduction semiconductors than the TSBB. Though the number of switching components in (22) is less than in (21), voltage stresses on S_2 and D_1 are the same as the sum of voltage stresses across switches and diodes in the conventional TSBB. Therefore, switching power losses depend on the condition. As a result, if switching losses of (21) and (22) are not dominant, the proposed converter that has two fewer semiconductors is more efficient.

Analysis of cases A, B, and C indicates that the proposed converter achieves improvement with regard to power losses by semiconductors. In case A (buck) and C (buck-boost), although switching losses depend on working conditions, the proposed converter operates with fewer conduction components. In case B (boost), the proposed converter is superior when it comes to either conduction losses or switching losses.

IV. CONNECTION BETWEEN SOURCE TERMINAL AND GROUND

The novel converter also provides another advantage regarding the design gate driver IC, since the proposed converter has a configuration where both source terminals of MOSFETs are connected to ground directly, as shown in Fig. 3. If the source terminal of a MOSFET is connected to floating voltage, the gate driver IC must support high-side gate control. Generally, there are several types of IC that can handle a high-side gate. For example, the bootstrap type and the isolated type are such ICs. The bootstrap type generally requires additional diodes and capacitors outside the IC, whereas the isolated type generally has a cost impact. The opto-coupler in this IC is relatively expensive. Bandwidth is also limited due to characteristics of the opto-coupler [12]. In this regard, the configuration where both source terminals of the MOSFETs are directly connected to ground provides benefits, since the circuit does not need to suffer from the above-mentioned disadvantages. Therefore, the proposed converter has wider options when selecting an IC. On the other hand, in a conventional TSBB, the source terminal of S_1 is connected to a floating voltage node, as shown in Fig. 2.

TABLE 5. The designed components for each converter and core parameters.

Components	TSBB converter	Proposed converter
Switch	RCX510N25 (V_{DS}=250 V, I_D=51 A, R_{dson}=48 mΩ)	
Diode	RF2001T3D (V_{RM}=350 V, I_O=20 A, V_F=1.3 V)	
Capacitor	100YXG820MEFC18X40/820μF	
Inductor	CH270125/250μH	

V. DESIGN AND ANALYSIS OF THE PROPOSED CONVERTER

For simple discussion, each component (switch, diode, capacitor, and inductor) is selected identically for both the TSBB

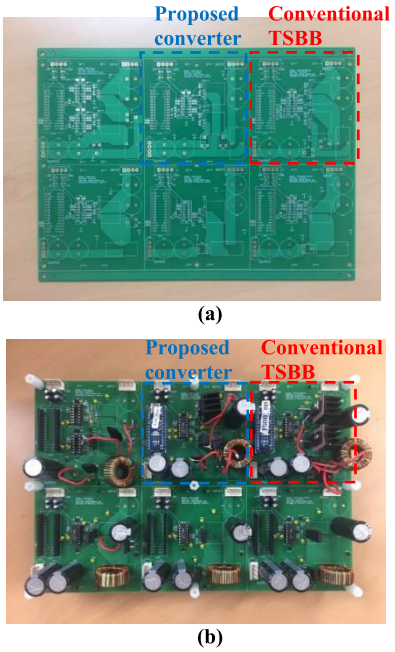


FIGURE 7. Pictures of the PCB: (a) bare PCB and (b) assembled PCB.

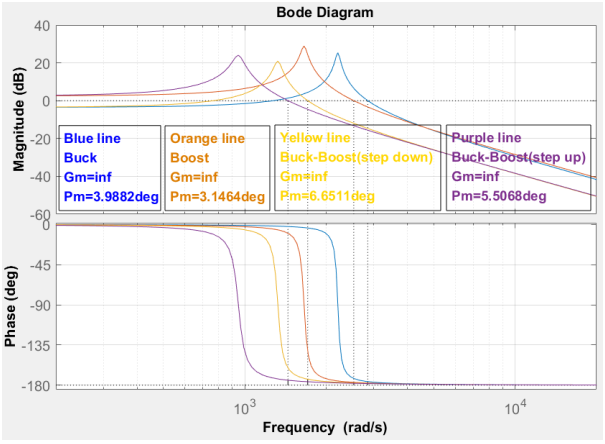


FIGURE 8. Open loop gains G_{vg} (s) of the proposed converter in buck, boost and buck-boost mode.

and the proposed converter, as shown in Table 5. To validate the effectiveness of each converter, a prototype was fabricated on a printed circuit board (PCB). Pictures of the PCB are in Fig. 7. Specifications were determined with input voltage $V_{in} = 36V$ or 72V, output voltage $V_{out} = 48V$, output power $P_{out} = 150W$, and switching frequency $f_s = 100$ kHz. Buck and step-down buck-boost mode convert input voltage of 72V to output voltage of 48V. Boost and step-up buck-boost mode change 36V to 48V. To analyze each converter's efficiency over various output voltage ranges, voltage stress and current stress margins were designed 20% larger than stresses at maximum load. Core parameters are also presented in Table 5.

With these parameters, open loop analysis is possible. Operational principles applied to each converter are the same, following buck, boost and buck-boost CCM operation. Open loop gain $G_{vg}(s)$ and its bode plot were obtained by using MATLAB, as shown in Fig. 8.

TABLE 6. Experimental voltage stresses on semiconductors: (a) the conventional TSBB converter and (b) the proposed converter.

Operation mode	S1	S2	D1	D2
buck mode	72	48	71	0
boost mode	0	47	34	45
buck-boost mode (step down)	72	48	71	46
buck-boost mode (step up)	36	44	34	43

(a)

Operation mode	S1	S2	D1	D2
buck mode	72	120	70	0
boost mode	0	47	81	46
buck-boost mode (step down)	78	120	117	95
buck-boost mode (step up)	45	81	79	73

(b)

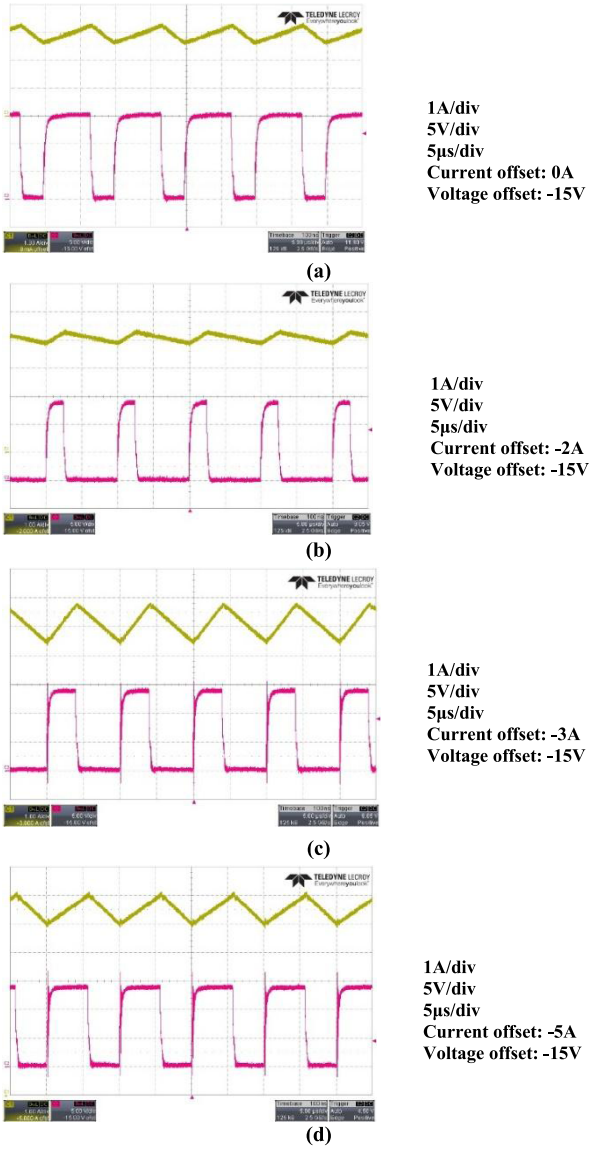


FIGURE 9. Inductor current and gate PWM wave form of the proposed converter in each mode: (a) buck, (b) boost, (c) step-down buck-boost, and (d) step-up buck-boost.

VI. EXPERIMENTAL RESULTS

Fig. 9 shows the experimental inductor current waveform and gate pulse width modulation(PWM) waveform of each mode from the proposed converter. Voltage stresses of each semiconductor are organized in Table 6. Voltage stresses on the proposed converter are larger than the TSBB converter. This problem can be dealt with via delay time of the gate PWM signal [7]. The measured efficiencies of the conventional and the proposed converter according to load are shown in Fig. 10. Full load current is 3.125A at 48V output voltage. Load condition was controlled by electronic load to change the load current from 10% to 100%. In buck and buck-boost modes, the measured efficacy of the proposed converter improved, compared to that of the TSBB converter. In buck mode, the proposed converter has efficiencies over 95%, but the TSBB is less than 95%.In buck-boost mode, both converters show less efficiency due to inductor current i_L. i_L is much higher in buck-boost mode than in buck and boost modes, which can be confirmed in Figs. 9 (c) and (d). This high i_L generates larger conduction and switching losses. Thus, efficiency becomes lower in buck-boost mode. The TSBB converter operates with efficiencies less than 90%, except for one point at 50% of the load, whereas the proposed converter provides efficiency over 90%, up to 91% at the 40% to 100% load range. On the other hand, in boost mode, the measured efficiency was almost the same as that of the conventional TSBB converter. Consequently, the proposed converter works efficiently in terms of efficiency, but has a voltage stress problem.

TABLE 7. Measured efficiency of the proposed and the TSBB converters.

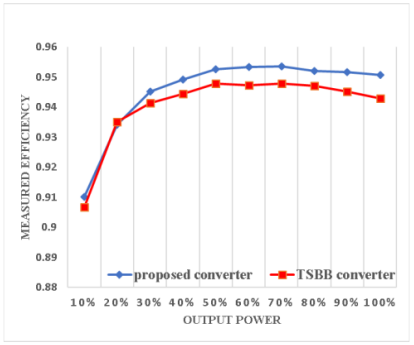
Condition	Mode	Input voltage	Measured efficiency (P_{out}/P_{in})		Comparative efficiency
		[V	Proposed converter(A)	Conventional TSBB converter(B)	A/B
duty ratio 0.25 output current 0.5A	buck mode	10	0.6714	0.5538	1.2123
		20	0.8370	0.7481	1.1188
		30	0.8500	0.8098	1.0497
		40	0.8732	0.8418	1.0373
		50	0.8639	0.8609	1.0095
		60	0.8568	0.8735	0.9809
		70	0.8676	0.8814	0.9843
		80	0.8627	0.8883	0.9712
	boost mode	10	0.8957	0.9074	0.9871
		15	0.9242	0.9223	1.0021
		20	0.9319	0.9172	0.9943
		25	0.9307	0.9401	0.9897
		30	0.9345	0.9430	0.9909
		35	0.9385	0.9446	0.9935
		40	0.9375	0.9493	0.9876
	buck-boost mode	10	0.7500	0.5722	1.3407
		20	0.8324	0.7541	1.1039
		30	0.8625	0.8143	1.0692
		40	0.8671	0.8440	1.0274
		50	0.8688	0.8526	1.0189
		60	0.8559	0.8574	0.9983
		70	0.8540	0.8687	0.9831
		80	0.8420	0.8708	0.9669

Condition	Mode	Input voltage	Measured efficiency (P_{out}/P_{in})		Comparative efficiency
		[V]	Proposed converter (A)	Conventional TSBB converter(B)	A/B
duty ratio 0.5 output current 1.25A	buck mode	10	0.7908	0.7308	1.0821
		20	0.8869	0.8569	1.0350
		30	0.9138	0.8944	1.0217
		40	0.9279	0.9126	1.0167
		50	0.9303	0.9207	1.0105
		60	0.9324	0.9268	1.0061
		70	0.9361	0.9329	1.0035
		80	0.9373	0.9379	0.9994
	boost mode	10	0.8700	0.8631	1.0079
		15	0.9060	0.9026	1.0037
		20	0.9209	0.9200	1.0009
		25	0.9299	0.9298	1.0004
		30	0.9349	0.9364	0.9984
	buck-boo st mode	10	0.8129	0.7271	1.1180
		20	0.8787	0.8459	1.0388
		30	0.8978	0.8800	1.0202
		40	0.9080	0.8958	1.0070
		50	0.8999	0.9032	0.9963
		60	0.8978	0.9065	0.9903

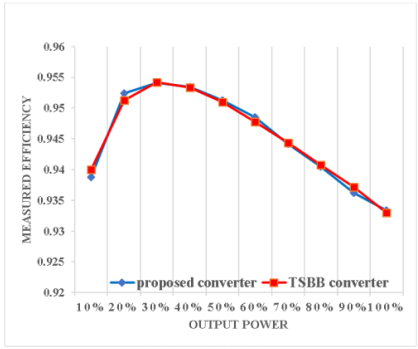
Condition	Mode	Input voltage	Measured efficiency (P_{out}/P_{in})		Comparative efficiency
		[V]	Proposed converter (A)	Conventional TSBB converter(B)	A/B
duty ratio 0.75 output current 1.25A	buck mode	10	0.8500	0.8313	1.0226
		20	0.9198	0.9057	1.0156
		30	0.9388	0.9329	1.0063
		40	0.9490	0.9426	1.0067
		50	0.9513	0.9485	1.0030
		60	0.9544	0.9536	1.0008
		70	0.9510	0.9562	1.0008
		80	0.9576	0.9532	0.9983
	boost mode	10	0.6207	0.5171	1.2003
		15	0.7289	0.6550	1.1128
		20	0.7834	0.7417	1.0561
		25	0.8133	0.7478	1.0875
		30	0.8325	0.7637	1.0901
	buck-boo st mode	10	0.7543	0.6707	1.1246
		20	0.7790	0.7093	1.0982
		30	0.7945	0.7400	1.0737
		40	0.8094	0.8076	1.0023
		50	0.8141	0.8235	0.9886

Table 7 shows the data that compare efficiencies under various load and input conditions. This implies the proposed converter reduces power dissipation more than the TSBB converter.

In particular, it is clear that the proposed converter is more efficient in low power ranges. In high power ranges, both converters reach full performance, and the difference is less than 1%.



(a)



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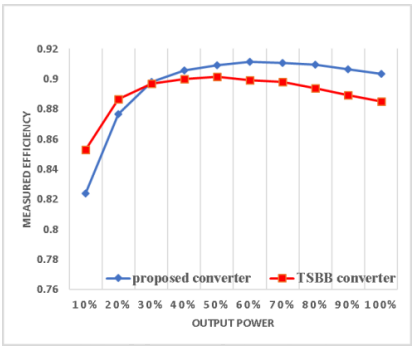
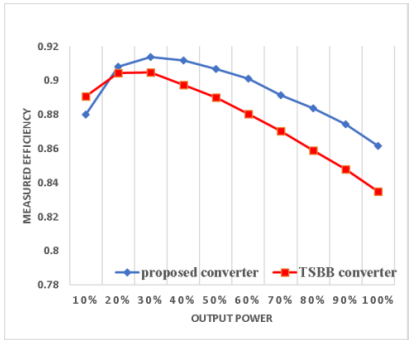


(c)



(d)

FIGURE 10. Measured efficiency at $V_{out} = 48V$, $f_{sw} = 100kHz$ according to load current. In (a) and (c), $V_{in} = 72V$ due to step-down. In (b) and (d), $V_{in} = 36V$ due to step-up. (a) buck mode. (b) boost mode. (c) buck-boost mode (step-down). (d) buck-boost mode (step-up).

VII. CONCLUSION

In this paper, a novel buck-boost DC-to-DC converter with two switches is introduced. The proposed converter has fewer

conduction and switching components than a conventional TSBB converter. Therefore, the overall tendency regarding the proposed converter's efficiency is higher than that of the conventional TSBB converter. Moreover, the proposed converter has another advantage in that the source terminals for both the switches are directly connected to ground. This gives a circuit designer a broader selection range for the gate driver IC. However, voltage stresses on semiconductors become larger, which is the trade-off relationship between efficiency and voltage stress.

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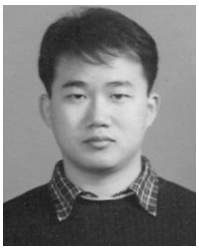

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