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A CMOS K-Band 6-bit Attenuator With Low Phase Imbalance for Phased Array Applications

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ABSTRACT A 6-bit digital-controlled attenuator with low phase imbalance for a K-band phased array system is presented in this paper. To decrease the insertion phase difference, the proposed design adopts a phase correction capacitor in the shunt branch of the conventional switched T/Pi structure. The capacitor and the parallel resistor compose a phase compensation network to correct the insertion phase error. The attenuator is designed and fabricated in 0.18 μm CMOS process. From 19 to 21 GHz, the insertion loss is 7.2–8 dB. The rms phase imbalance is less than 3.8° over 19–21 GHz. The attenuator has a maximum attenuation range of 32 dB with 0.5-dB step (64 states). The core cell chip size is 1.32 mm × 0.34 mm excluding pads.

INDEX TERMS Attenuator, CMOS, phase imbalance.

I. INTRODUCTION

In modern wireless communication system, variable gain amplifiers (VGA) and attenuators are extensively utilized as amplitude control circuits [1]–[5]. As attenuators possess better performance on linearity and power consumption compared with VGA, variable attenuators are more suitably adopted in the transceivers of phased-array systems to attain precise and broad amplitude control in different paths. Also, as the absence of digital-to-analog converters in the control units, digital step attenuators are used prior to VGA and the analog attenuator to reduce control complexity [3]. For averting tracking error and complex phase and amplitude calibration in phased array, attenuators need to maintain constant transmission phase while controlling the amplitude [4].

The distributed attenuators and switched T/Pi attenuators are mostly used topologies in the current design, shown in Fig. 1. The distributed topology usually employs the half or quarter-wavelength transmission lines and transistors as varistors to achieve relative attenuation. And it has low insertion loss because of the lack of switches between the series transmission lines, but covers very large chip area [5]. The T/Pi topology uses RF switches to transform the signal path between the series bypass and the resistive network for attenuation. It has compact chip size, however, its' performance is significantly influenced by the parasitic effects of the switches, especially the insertion phase [4], [6], [7]. As the constant phase change is requisite for phased array system [4], the method to reduce the insertion phase imbalance is necessary. Therefore, this paper proposes a 6-bit attenuator with low phase imbalance for a K-band phased array system.

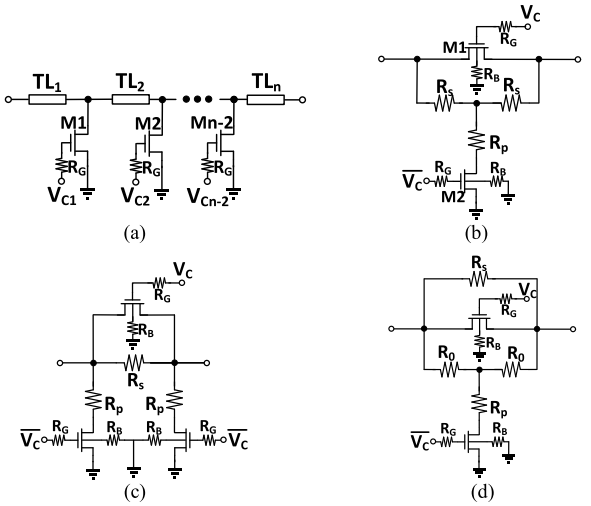

FIGURE 1. Topologies of traditional attenuator: (a) Distributed attenuator. (b) Switched T type. (c) Switched Pi type. (d) Switched bridge-T type.

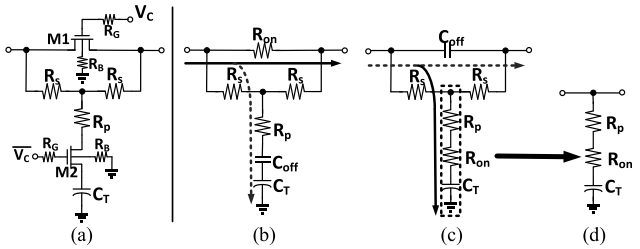

FIGURE 2. (a) T type attenuator with tail capacitor, and its' equivalent circuits at: (b) the reference state and (c) the attenuation state. (d) The equivalent circuits of the phase correction branch at the attenuation state.

II. CIRCUIT DESIGN

A. PROPOSED STRUCTURE

As shown in Fig. 2(a), a tail capacitor is added to the shunt branch of the traditional T attenuator. The body and series inductance parasitic is neglected in the simplified equivalent circuits. When switch M1 is on and M2 off, the attenuator works at the reference state. The signal passes through the series path, as shown in Fig. 2(b). When switch M1 is off and M2 on, it works at the attenuation state. The signal flows to the ground from the shunt attenuation branch, as shown in Fig. 2(c). The tail capacitor is introduced as a phase correction device in the attenuation branch. Thus, the correction network can affect the performance of the attenuation state. The phase correction branch at the attenuation state can be simplified to a T-type topology as shown in Fig. 2(d). The equation of transmission phase θ of this network can be derived as:

$$\theta = \tan^{-1} \frac{-C_T Z_0}{\omega(2C_T^2(R_p+R_{on})^2+C_T^2(R_p+R_{on})Z_0)+2/\omega}, \quad (1)$$

where ω is the operating frequency. For simplicity, all parameters but the operating frequency ω are treated as the constant. Therefore,

$$\theta = \tan^{-1} \frac{-A}{B \cdot \omega + 2/\omega}, \quad (2)$$

where

$$A = C_T Z_0$$

and

$$B = 2C_T^2(R_p + R_{on})^2 + C_T^2(R_p + R_{on})Z_0. \quad (3)$$

Therefore, θ is ploted in Fig. 3(a). The slope of θ alters from negative to positive value at certain critical frequency, where the slope is zero. This phenomenon can be used to correct the transmission phase error.

Fig. 3(b) exhibits the simulation results of the transmission phase of the phase correction branch in Fig. 2(d). The phase declines to a minimum value, where the slope is zero, and then rises with the frequency increasing, which verifies the mathematical functional image of (2), in Fig. 3(a).

In Fig. 3(c), the T-type attenuator's transmission phases of reference and attenuation states are simulated with various

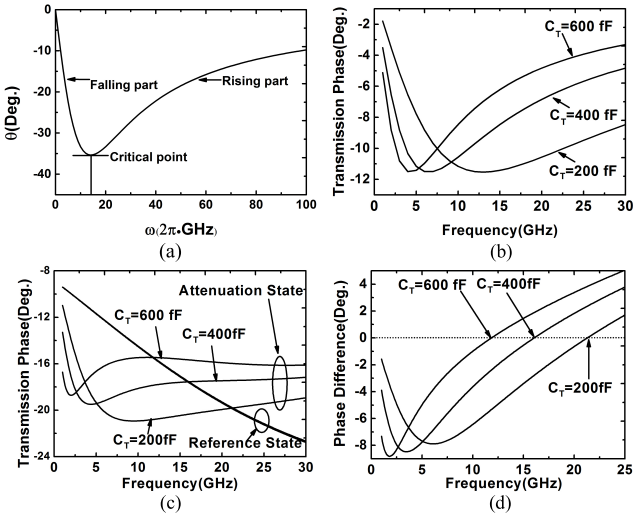

FIGURE 3. (a) The mathematical functional image of (2). The simulation results of the transmission phase of (b) the phase correction branch, and (c) the T type attenuator with tail capacitor. (d) The phase difference of reference and attenuation states with various C_T value.

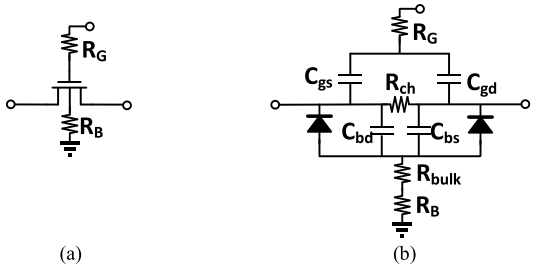

FIGURE 4. (a) The nMOS switch in the proposed attenuator (b) The equivalent circuit of the nMOS switch.

tail capacitor value (swept from 200 fF to 600 fF). The phases of attenuation states have the same variation trend with those of the phase correction branch in Fig. 3(b). It is obvious that the capacitance variation influences the attenuation state significantly, whereas it has less effect on the reference state. With the capacitance variation, the attenuation-state transmission phase intersects with the reference-state transmission phase at different frequencies with the zero phase difference. According to controlling the tail capacitor value, low phase imbalance within a particular frequency band can be achieved, as shown in Fig. 3(d).

Furthermore, as the insertion loss of the reference state is mainly introduced by the series switch, a large resistor R_B is added to the body terminal of the switch to enhance the insertion loss performance, as shown in Fig. 4 (a). The equivalent circuit of the switch is shown in Fig. 4. (b). When the bulk parasitic resistor R_{bulk} is small, the RF signal has access to the ground due to the capacity coupling effect caused by the parasitic capacitors of the reverse biased diodes and the parasitic capacitors of source/drain and the body. However, the added R_B is a considerable impedance for RF signal, so that it can prevent the signal from leaking to the

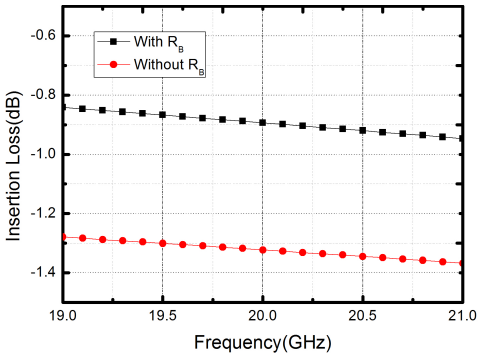

FIGURE 5. The insertion loss of the switches with and without the large resistor R_B.

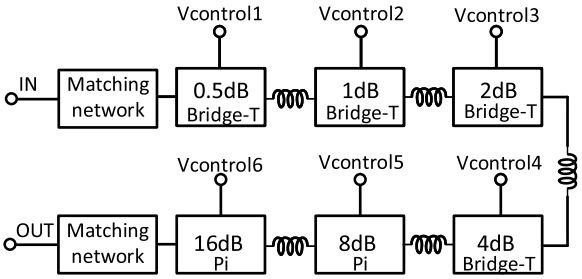

FIGURE 6. The system topology of the proposed 6-bit attenuator.

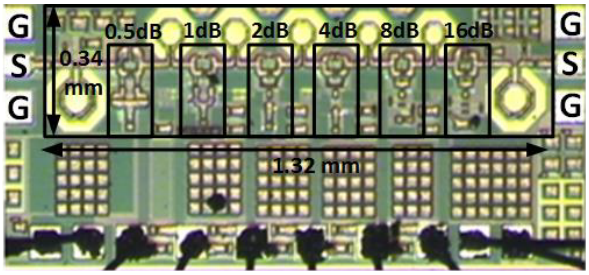

FIGURE 7. Micrograph of the proposed 6-bit switched Pi/T attenuator.

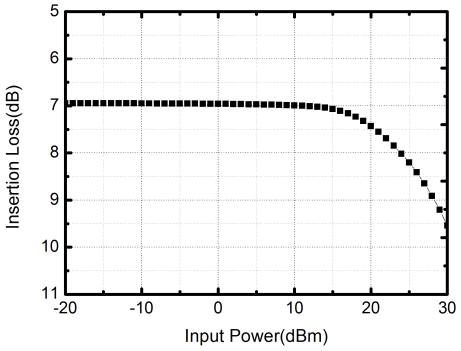

FIGURE 8. Simulated insertion loss of different the input power at 20 GHz.

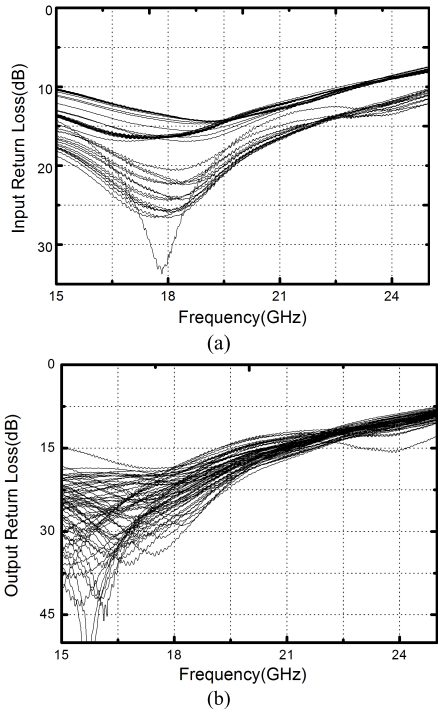

FIGURE 9. Measured (a) input return loss and (b) output return loss.

ground. In the simulation, the switch with the large resistor R_B of over 5000 ohm has better insertion loss than the switch without R_B by approximate 0.4dB, as shown in Fig. 5.

The proposed tail capacitor and switch can also be employed in Pi and bridge-T type attenuators to compose a phase correction network. They have the same operation principal to realize low phase imbalance as the analyzed T-type attenuator.

B. IMPLEMENTATION AND MEASUREMENT

A 6-bit digital attenuator has been designed using the Pi and bridge-T structures with the "tail capacitor."

Fig. 6 shows the ordering of the six attenuation bits of 0.5, 1, 2, 4, 8, and16 dB. The bridge-T type attenuators are used to realize 0.5, 1, 2, 4 dB attenuation, and Pi type attenuators are used to achieve 8, 16 dB attenuation. Inductors inserted between the attenuation units are used as the matching networks to connect the every single bit. The 6-bit attenuator has been integrated in the TSMC 180-nm process. From the chip photograph shown in Fig. 7, the attenuator core cell covers an area of 1320um × 340 um (0.45 mm^2) excluding the pads.

In simulation, the input P_{1dB} is better than 23 dBm, as shown in Fig. 8. In measurement, Fig. 9 shows the input and output return loss respectively, both of which are better than 10 dB from 19 to 21 GHz. In the input and output matching design, conventional LC networks are utilized to match the 50-ohm input and output impedance. There are totally 64 states including the reference state and the largest measured attenuation range is 32 dB. Fig. 10 shows the 63 relative attenuation states, which is calculated as the difference of the measured insertion loss of 63 attenuation states and the reference state. As shown in Fig. 11, the measured insertion loss of the attenuator is between 7.2 to 8 dB over

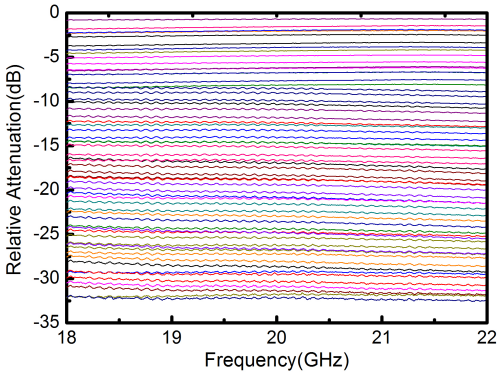

FIGURE 10. Measured relative attenuation.

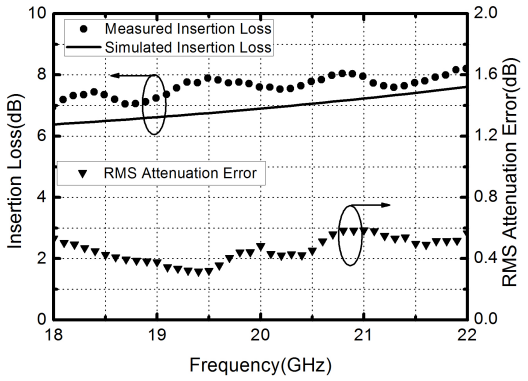

FIGURE 11. Simulated and measured insertion loss, and rms attenuation error.

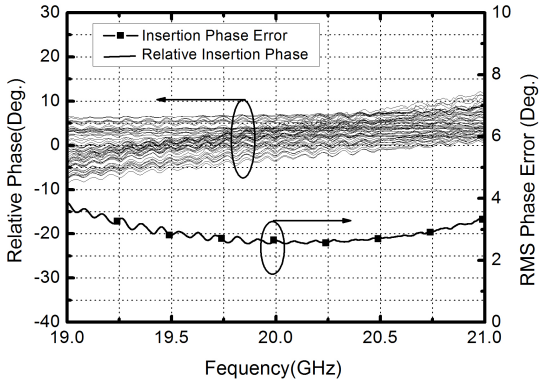

FIGURE 12. Measured relative insertion phase and calculated rms phase error.

19-21 GHz, higher than the simulated 6.4-7.6dB. This is caused by the lower quality factor of the matching inductors than the simulation. The maximum rms amplitude error is 0.6 dB from 19 to 21 GHz. As shown in Fig. 12, the relative insertion phase is between $-8°$ to $12°$ and the rms phase imbalance is below $3.8°$ over 19-21 GHz.

Table I compares the performance of the proposed digital attenuator with the state-of-art CMOS attenuators. Compared with the distributed attenuators in [4] and the switched T/Pi attenuators in [9], the proposed attenuator has

TABLE 1. Comparison of CMOS/Bicmos digital attenuators.

Ref.	[4]	[9]	[5]	[6]	This work
Freq.(GHz)	10-50	36-52	DC-14	6-12.5	19-21
Process	0.12-um BiCMOS	0.18-um BiCMOS	0.18-um CMOS	0.25-um SiGe BiCMOS	0.18-um CMOS
Structure	Distributed	Switched T/Pi	Switched T/Pi	Switched T/Pi	Switched T/Pi
Chip Area(mm^2)	0.75x0.2(0.15)	0.6x0.36 (0.22)	1.25x0.4 (0.5)	0.29	1.3x0.34 (0.45)
Number of states	11	8	64	64	64
Atten. range(dB)	11 (N/A)	7 (3-bit)	31.5 (6-bit)	16.5 (6-bit)	32 (6-bit)
Return loss (dB)	>9	>9.7	>10	>12.7	>12
Insertion loss(dB)	<3	<5.9	<10	<12.7	<8
Average IL of each bit	N/A	<1.96	<1.67	<2.1	<1.3
Rms phase error(deg.)	<3	<6.7	<4.2	<3.5	<3.8

The Chip area excludes RF and DC pads.

larger attenuation range and more attenuation states, and it maintains low phase imbalance even if it's more difficult to realize this with dynamic range increasing. Apparently, it has worse overall insertion loss because of consisting more attenuation units, however, the average insertion loss of each attenuation bit is still competitive. The switched T/Pi attenuators in [5] and [6] utilized similar principle to decrease the phase imbalance. Compared with them, the proposed attenuator possesses better insertion loss due to less inductors and in the series path. And with the limitation of the resonance effect, the phase compensation structures in [5] and [6] may not function properly over a higher frequency, about over 14 GHz. The proposed attenuator without frequency limitation is able to work at 19-21 GHz with low phase imbalance of rms phase error less than $3.8°$.

III. CONCLUSION

A 6-bit digital attenuator with low phase imbalance for a K-band phased array system is presented in this letter. In this design, a tail capacitor is inserted into the attenuation branch of the traditional Pi, T and bridge-T type attenuation units to form a phase correction network with the parallel resister. With the help of this technique, the transmission phase error of the attenuation state can be corrected, thus leading to a low phase imbalance. In measurement, the attenuator achieves a phase imbalance less than $3.8°$ (rms) and amplitude error less than 0.6 dB over 19-21 GHz. It has a maximum amplitude control range of 32dB with the approximate 0.5-dB step. Compared with other works using CMOS process, it has a larger range and more attenuation states and lower phase imbalance over a relatively higher frequency band.

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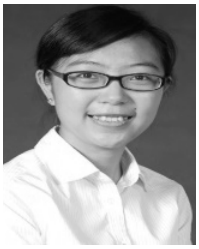

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