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DC Offset Rejection Improvement in Single-Phase SOGI-PLL Algorithms: Methods Review and Experimental Evaluation

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ABSTRACT DC offset in the input of phase-locked loops (PLLs) is a challenging problem since it will result in fundamental frequency oscillations in the estimated phase and frequency. In this paper, a comprehensive analysis and performance evaluation of several advanced second-order generalized integrator (SOGI)-based PLL methods in enhancing the dc offset rejection capability for single-phase grid-connected power converters is presented. These methods include the cascade SOGI, modified SOGI, $\alpha\beta$-frame delayed signal cancellation (DSC), complex coefficient filter, in-loop dq-frame DSC, notch filter, and moving average filter-based SOGI-PLL. Main characteristics and design aspects of these methods are presented. Main performance indexes, such as the setting time, frequency or phase errors are defined and these methods are systematically compared under various scenarios with both numerical and experimental results.

INDEX TERMS Phase-locked loop, dc offset, single phase grid-connected converter, filter.

I. INTRODUCTION

Phase-locked loop (PLL) is essential in the synchronization and closed-loop control of single-phase grid-connected systems (SPGCS), such as fuel cells, batteries, photovoltaic, and wind system [1]–[3]. The accurate detection of the frequency and phase angle by PLLs affects the power quality and reliability of SPGCS [4].

DC offset in the input of PLLs is a challenging problem since it will result in fundamental frequency oscillations in the estimated phase and frequency [5]–[9]. The dc offset is produced from difference sources, such as the offset of voltage sensors, A/D conversion, mismatches among semiconductor devices, and grid faults [10]. It will result in the dc injection problem in SPGCS since the PLL unit vector is usually used to generate the current reference in SPGCS. Thus, dc offsets are generated in the inverter voltage due to the offset error in the unit vector, which possibly violates the standard IEEE 1547-2003 [11] and IEC61727 [12]. To meet the two standards, the dc injection from SPGCS must be controlled within 0.5% and 1% of the rated output current, respectively.

To address this issue, several methods have been proposed in order to improve the dc offset rejection capability. In [13], the impact of dc offsets on the conventional synchronous reference frame (SRF) PLL is analyzed quantitatively by using a linear small-signal state-space model. The inherent relationship of SRF-PLL bandwidth with the dc offset variation is specified. With the increase of dc offset in the input, the bandwidth of the proposed algorithm must be accordingly reduced, which affects the dynamic performance.

In [14], a two-phase generator with a closed loop control is inserted in the SRF PLL to reject the dc offset. Firstly, the difference between the input and the extracted α-axis component is obtained, then, it passes through an integrator and the output, corresponding to the input dc component, will finally be subtracted from the input.

In [15], a dc offset error compensation algorithm is proposed by controlling the synchronous d-axis voltage to be zero. Firstly, the dc offset error is estimated from an integrator, then, a PI controller are tuned to remove the dc offset error in a closed loop manner. This method is effective for both steady state and transients. Furthermore, no additional hardware is required and the computational burden is low.

In [16], a dc-immune PLL is proposed to reject the dc offset error in the SRF PLL. The basic principle is to subtract the $\alpha\beta$-axis components from their delayed version. Then, a frequency adaptive matrix transform is conducted to adjust the phase and amplitude of the fundamental component. It shows good dynamic response. However, the cotangent function is used and the computation burden is increased.

In [17], a frequency-fixed cascaded generalized integrator (CGI) PLL is proposed to reject the input dc offset. The α-axis output of the first SOGI block is the input of the second SOGI block. The $\alpha\beta$-axis outputs of the second SOGI block are fed to the embedded SRF-PLL. However, the bandwidth of SRF-PLL affect the dynamic response and harmonic attenuation capability.

In [18], an improved SOGI PLL is proposed by including the third integrator in the SOGI-QSG with its output to cancel the input dc component. It can improve the performance without adding the complexity. However, in practical implementation, the fundamental frequency and phase sequence of input signals must be provided, which limit its application.

In [19], a comparison of some less discussed three-phase PLL algorithms in dc-offset rejection performance is presented with numerical results. However, considering the application features of single-phase grid-connected power converters and state-of-the-art SOGI based PLL algorithms proposed in recent years, a deep analysis and performance evaluation of most widely used and advanced SOGI based PLL algorithms to enhance the dc offset rejection capability is of great importance. Furthermore, no just limited by the dc-offset rejection capability, a comprehensive performance evaluation for complicated scenarios is conducted, combined with phase-angle jump and harmonics conditions. Thus, the comparison results drawn in this paper for single-phase application shows more value for practical industry application. This paper is organized as follows. Firstly the basic SOGI PLL method is reviewed and its limitation for dc offset rejection is illustrated. Then, several advanced algorithms for SPGCS are presented, including design guideline, digital implement and performance evaluation. Finally, the evaluation results for various scenarios are provided with both numerical and experimental results.

II. CONVENTIONAL SOGI-PLL

Fig.1 shows the schematic diagram of single-phase SOGI-PLL, where v represents the input grid voltage, $\hat{\omega}$ is the estimated frequency and $\hat{\theta}$ is the estimated phase angle, respectively. Since the PLL is sensitive to the grid voltage amplitude variation, the amplitude of the PI controller input v_q is normalized. Furthermore, the estimated frequency $\hat{\omega}$ is fed back to update the value of ω, which makes SOGI-PLL frequency adaptive [20]. The transfer functions of the SOGI base quadrature signal generator (QSG) with respect to the input can be expressed as

$$H_d(s) = \frac{v'}{v}(s) = \frac{k\omega s}{s^2 + k\omega s + \omega^2} \tag{1}$$

$$H_q(s) = \frac{qv'}{v}(s) = \frac{k\omega^2}{s^2 + k\omega s + \omega^2} \tag{2}$$

where ω represents the resonant frequency, usually $2\pi 50$ rad, and k is the damping coefficient. $H_d(s)$ is a band-pass filter, which is independent of the resonant frequency ω and can be exclusively set by k. $H_q(s)$ is a low-pass filter with 90 degree phase shift with respect to v' at resonant frequency ω. Select

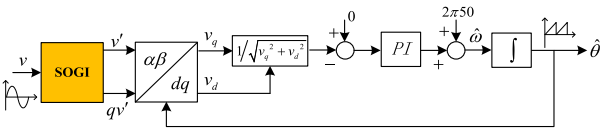


FIGURE 1. Schematic diagram of single-phase SOGI-PLL.

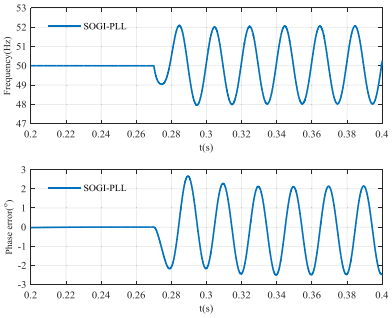


FIGURE 2. Response of SOGI-PLL under input dc offset condition.

$k = 1.414$ can achieve a satisfactory compromise between the disturbance rejection and the response speed.

The open-loop transfer function of SOGI-PLL with PI control can be expressed by

$$G_{ol}(s) = (k_p + \frac{k_i}{s})\frac{1}{s} = \frac{(k_p s + k_i)}{s^2} \tag{3}$$

where k_P is proportion gain, k_i represents integral gain. Then, the closed loop transfer function can be expressed by

$$G_{cl}(s) = \frac{G_{ol}(s)}{1 + G_{ol}(s)} = \frac{(k_p s + k_i)}{s^2 + k_p s + k_i} \tag{4}$$

Equation (4) is a typical second order system, where

$$\begin{cases} k_p = 2\varsigma\omega_n \\ k_i = \omega_n^2 \end{cases} \tag{5}$$

With general symmetrical design optimum method [21], [22], the parameters can be determined as

$$\begin{cases} \zeta = 0.707 \\ \omega_n = 2\pi 10 \end{cases} \tag{6}$$

As indicated in (2), $H_q(s)$ is a low-pass filter with 90 degree phase shift with respect to v' at resonant frequency ω. Furthermore, the dc component gain of qv' with respect to v is dependent on k. Thus, the dc offset in the input signal will affect both the quadrature signal qv' and the following PLL operation in the form of low-frequency oscillations, which will result in the fundamental disturbance in q-axis component of PD following the *Park* transform.

Fig.2 illustrates the frequency response of SOGI PLL under the 0.1pu dc offset condition. At 0.27s, 0.1pu dc offset is added in the input, which results in significant oscillations in the estimated frequency and phase. Specifically, the estimated fundamental oscillatory of estimated frequency is 4 Hz and the phase error is up to 5°.

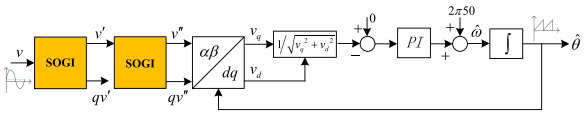


FIGURE 3. Schematic diagram of the cascade SOGI-PLL.

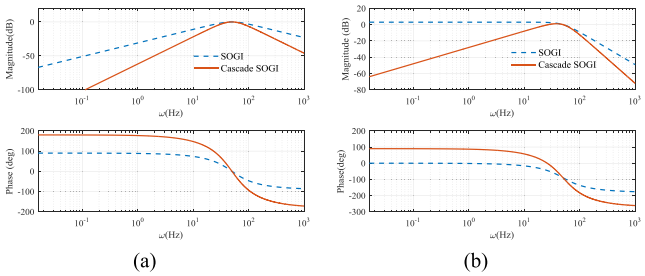


FIGURE 4. (a) Frequency response of $H_{d''}(s)$; (b) Frequency response of $H_{q''}(s)$.

III. ADVANCED SOGI-PLL ALGORITHMS

In this section, several advanced SOGI-PLL algorithms for dc offset rejection improvement are discussed. Basically these PLLs can be regarded as a conventional SRF-PLL with structure modification, or inclusion of some kinds of filters, either inside the SRF-PLL control loop or before its input.

A. CASCADE SOGI PLL

This algorithm is originated from the fact that v' in SOGI-PLL shows remarkable rejection for dc component although qv' generated by SOGI is sensitive to the input dc offset. Thus, two cascaded SOGIs, as shown in Fig .3, can eliminate the dc offset [23], [24].

The two in-quadrature output signals, v'' and qv'', can be defined by the following transfer functions:

$$H_{d''}(s) = \frac{v''}{v}(s) = \frac{k\omega s}{s^2 + k\omega s + \omega^2}\frac{k\omega s}{s^2 + k\omega s + \omega^2} \quad (7)$$

$$H_{q''}(s) = \frac{qv''}{v}(s) = \frac{k\omega s}{s^2 + k\omega s + \omega^2}\frac{k\omega^2}{s^2 + k\omega s + \omega^2} \quad (8)$$

Considering both requirements of disturbance rejection capability and dynamic response speed, k is finally selected as 1.414. Fig. 4 illustrates the frequency response plots. It shows that both $H_{d''}(s)$ and $H_{q''}(s)$ offers better attenuation than that of conventional SOGI, either below or above the resonant frequency. Furthermore, qv'' always hold 90 degree phase shift with v'' at resonant frequency.

Fig. 5 shows the frequency response of cascade SOGI under dc offset condition. It shows that the inputs for the *Park* transform block, v'' and qv'', are clean and quadrature although v contains dc offset. The qv'' is insensitive with dc offset although qv' is sensitive. Another important feature of this structure is that the dc term in the input v can be estimated by v-v'', as illustrated in Fig. 5 (b).

B. MODIFIED SOGI PLL

The basic structure of this algorithm is shown in Fig.6 [25]. The dc offset is estimated by a third integrator with a gain of

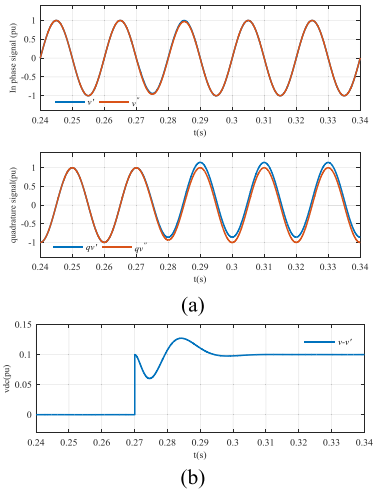


FIGURE 5. (a) Performance of the cascade SOGI under input dc offset condition; (b) DC term estimation.

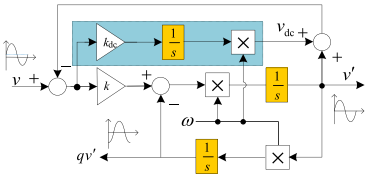


FIGURE 6. Modified SOGI.

$k_{\rm dc}\omega$, and then subtracted from the input in order to improve dc offset rejection ability.

The transfer functions of modified SOGI are:

$$\frac{v'}{v}(s) = \frac{k_{\rm dc}\omega s^2}{s^3 + (k + k_{\rm dc})\omega s^2 + \omega^2 s + k\omega^3} \quad (9)$$

$$\frac{qv'}{v}(s) = \frac{k_{\rm dc}\omega^2 s}{s^3 + (k + k_{\rm dc})\omega s^2 + \omega^2 s + k\omega^3} \quad (10)$$

$$\frac{v_{\rm dc}}{v}(s) = \frac{k_{\rm dc}\omega(s^2 + \omega^2)}{s^3 + (k + k_{\rm dc})\omega s^2 + \omega^2 s + k\omega^3} \quad (11)$$

where $v_{\rm dc}$ is estimated dc term, $k_{\rm dc}$ is a gain in dc offset estimate channel. The parameters are optimized as: $k = 1.414$ and $k_{\rm dc} = 0.4$. Fig. 7 illustrated the frequency responses of the modified SOGI. It shows that v_{dc}/v has the characteristic of low-pass filter. Fig.7 (b) shows the response of $v_{\rm dc}$ under the condition of 0.1pu dc offset in v. It shows that this algorithm can accurately estimate the dc offset and the settling time is 0.03s.

C. αβDSC SOGI PLL

The $\alpha\beta$-frame Delayed Signal Cancellation ($\alpha\beta$DSC) is a vector filter in the stationary frame, which is an effective way to detect fundamental sequence from harmonics. This operator is defined in the time domain as [26]

$$\alpha\beta{\rm DSC}_n(t) = \frac{1}{2}[v_{\alpha\beta}(t) + e^{j\frac{2\pi}{n}} v_{\alpha\beta}(t - T/n)] \quad (12)$$

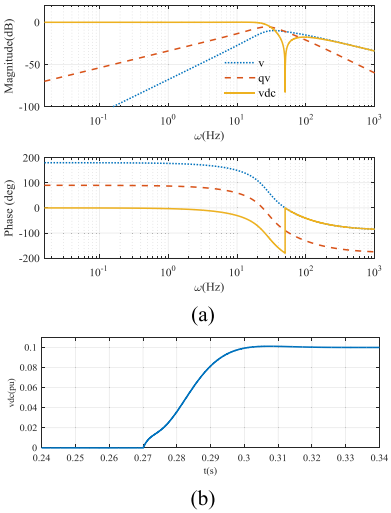


FIGURE 7. (a) Frequency response of v_{dc}/v; (b) Dc offset estimation of v_{dc}.

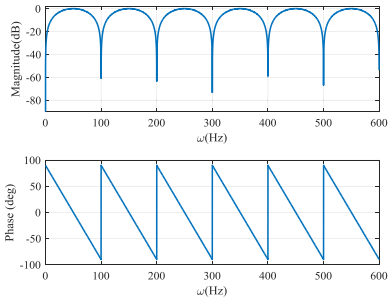


FIGURE 8. Frequency response of $\alpha\beta$DSC$_2$.

where $v_{\alpha\beta}(t)$ is the current voltage vector,$e^{j\frac{2\pi}{n}}$ is the rotate factor,$v_{\alpha\beta}(t-T/n)$ is the delayed voltage vector with T/n.

The magnitude and phase response of the $\alpha\beta$DSC$_n$ can be derived as

$$\alpha\beta\text{DSC}_n(j\omega) = \left|\cos(\frac{\omega T}{2n} - \frac{\pi}{n})\right| \angle -(\frac{\omega T}{2n} - \frac{\pi}{n}) \quad (13)$$

With different n, $\alpha\beta$DSC$_n$ has different attenuation for certain sets of harmonic sequences. The frequency response of $\alpha\beta$DSC$_2$ is shown in Fig.8. It can be observed that the even order harmonics are removed, meanwhile, the dc term can also be totally eliminated.

Fig. 9 shows the schematic diagram of the $\alpha\beta$DSC SOGI-PLL, where the $\alpha\beta$DSC$_2$ is cascaded with SOGI to filter out the dc term of qv'.

The time domain expression of (12) can be rewritten as

$$\alpha\beta\text{DSC}_n = \frac{1}{2}\{\begin{bmatrix} v_\alpha(t) \\ v_\beta(t) \end{bmatrix} + \begin{bmatrix} \cos(2\pi/n) & -\sin(2\pi/n) \\ \sin(2\pi/n) & \cos(2\pi/n) \end{bmatrix} \times \begin{bmatrix} v_\alpha(t-T/n) \\ v_\beta(t-T/n) \end{bmatrix}\} \quad (14)$$

In digital implementation, the T/n delay can be accomplished by n buffers of input. With parameters optimized as:

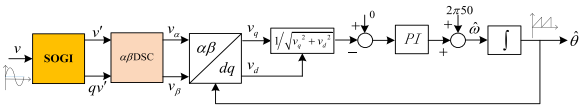


FIGURE 9. Schematic diagram of the $\alpha\beta$DSC SOGI-PLL.

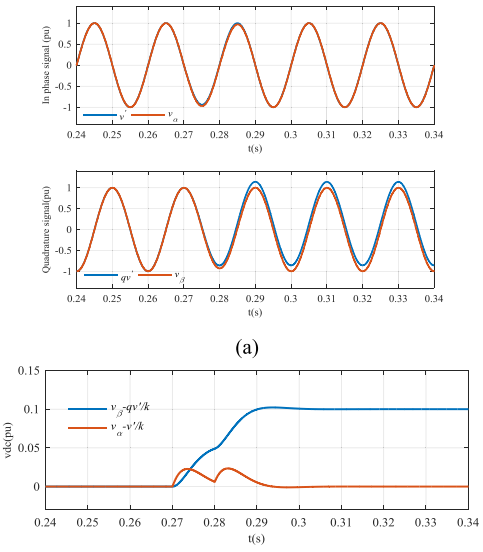


FIGURE 10. (a) Performance of the $\alpha\beta$DSC$_2$ under input dc offset condition; (b) DC term estimation.

$T_s = 0.0001$s, $n = 2$, $T/n = 100$, (14) can be expressed as

$$\alpha\beta\text{DSC}_n = \frac{1}{2}\{\begin{bmatrix} v_\alpha(k) \\ v_\beta(k) \end{bmatrix} + \begin{bmatrix} 1 & 0 \\ 0 & 1 \end{bmatrix} \begin{bmatrix} v_\alpha(k-100) \\ v_\beta(k-100) \end{bmatrix}\} \quad (15)$$

Fig. 10 illustrates the performance of the $\alpha\beta$DSC$_2$ under 0.1pu input dc offset condition. It shows that the influence of dc offset can be eliminated totally.

D. COMPLEX COEFFICIENT FILTER BASED PLL

Complex Coefficient Filter (CCF) is expressed as

$$G_{CCF}(s) = \frac{\omega_p}{s - j\omega + \omega_p} \quad (16)$$

where ω_p is the cutoff frequency, and ω is the offset frequency.

CCF is a band-pass filter with polarity selectivity and Fig. 11 illustrates the frequency response with $\omega = 2\pi \cdot 50$rad/s. It shows that the gain is unity at the positive offset frequency components, while it can attenuate the negative offset frequency components and other harmonic components [27]. Furthermore, the amplitude attenuation depends on the cutoff frequency ω_p. As ω_p decreased, the pass band for positive offset frequency components becomes narrow while the amplitude attenuation becomes more obvious for other frequency components. The detailed implementation of CCF is illustrated in Fig. 12.

Note that the cross couple feedback between two outputs is utilized to calculate the negative offset frequency components. The CCF needs to be implemented by multiplication,

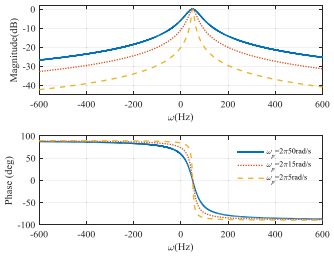


FIGURE 11. Frequency response of CCF.

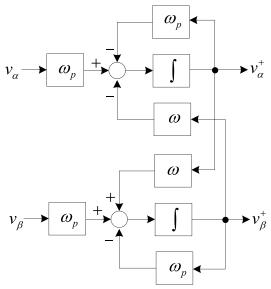


FIGURE 12. Implementation of CCF.

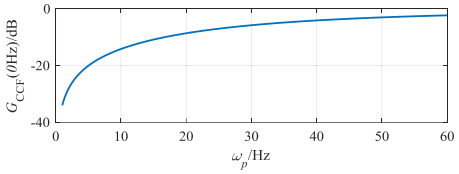


FIGURE 13. Dc term attenuation as function of ω_p.

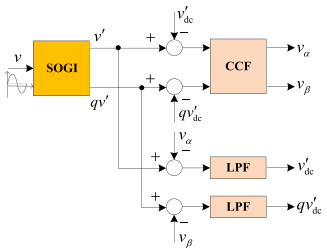


FIGURE 14. CCF based PLL.

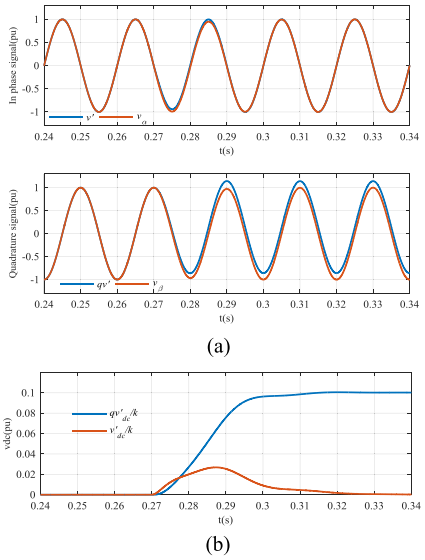
sum and integrator operation. Thus, compared with other algorithm, the computation burden of CCF is relatively high.

Fig.13 shows the dc term attenuation as function of ω_p. It shows that the attenuation of CCF for dc term is not zero, thus, CCF cannot separate the fundamental positive sequence accurately under dc offset input condition. To address this drawback, a cross feed forward decouple structure is used and shown in Fig. 14.

The LPF is expressed as

$$\mathrm{LPF}(s) = \frac{\omega_c}{s + \omega_c} \tag{17}$$

where ω_c is the cutoff frequency. Considering the response speed, this parameter is selected as: $\omega_c = 2\pi \cdot 15\mathrm{rad/s}$. With



(a)

(b)

FIGURE 15. (a) Offset evaluation with CCF under input dc offset condition; (b) DC term estimation.

this algorithm, the dc term can be expressed as

$$v_{\mathrm{dc}} = \frac{qv''}{k} \tag{18}$$

where k is the damping coefficient.

Fig. 15 shows the frequency response under dc offset condition. It shows that the output is immune with dc offset and the dynamic process takes over 1.5 fundamental cycles. Furthermore, this algorithm can achieve good performance under input harmonics condition.

E. DQ-FRAME DSC BASED PLL

The basic principle of this algorithm is that the sinusoidal waveform shows half-wave symmetric, thus, a harmonic can be cancelled by the sum of current value and one-half cycle delayed value. The Delayed Signal Cancellation (DSC_n) is expressed as

$$\mathrm{DSC}_n[x(t)] = \frac{1}{2}[x(t) + x(t - T/n)] \tag{19}$$

where n is the delay factor, T is the fundamental period. The transfer function can be expressed by

$$dq\mathrm{DSC}_n(j\omega) = \frac{1}{2}(1 + e^{-\frac{T}{n}s}) \tag{20}$$

Fig. 16 illustrates the frequency response of $dq\mathrm{DSC}_2$, which shows that $dq\mathrm{DSC}_2$ can remove all odd order harmonics and leave even order harmonics and dc term [28], [29].

The digital implementation of DSC_n can be written as

$$\mathrm{DSC}_n[x(k)] = \frac{1}{2}[x(k) + x(k - N')] \tag{21}$$

where N' is an integer rounded to the nearest integer of $T/T_s n$, $x(k)$ is the current sample of $x(t)$, $x(k - N')$ is the N' delayed sample of $x(t)$, T_s is the sample time.

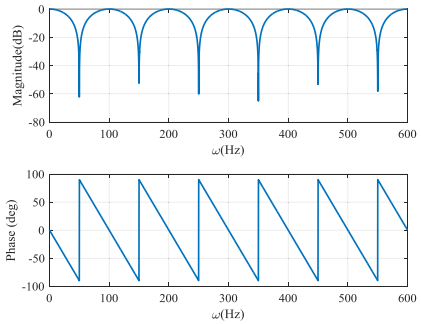


FIGURE 16. Frequency response of $dq\text{DSC}_2$.

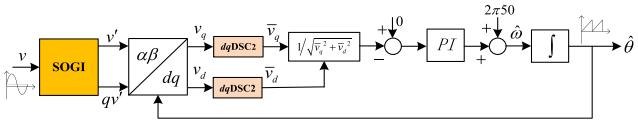


FIGURE 17. Schematic diagram of the $dq\text{DSC}_2$ SOGI-PLL.

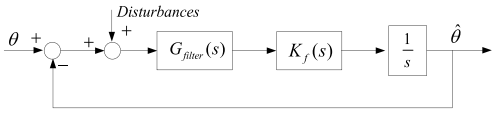


FIGURE 18. Small signal model for the $dq\text{DSC}_2$ SOGI-PLL.

With this algorithm, the input dc offset is transformed to the fundamental disturbance in q-axis component. Thus, $dq\text{DSC}_2$ is applied in loop of SOGI-PLL to remove this fundamental disturbance, as show in Fig. 17. Since it's the in-loop filter, which inevitably introduces time delay in PLL, a PI control is required to optimize the dynamics [21]. Fig. 18 shows the small signal model of this algorithm.

The transfer function of the in loop filter can be approximated as

$$G_{filter}(s) = \frac{1}{T_{filter}s + 1} \tag{22}$$

Then, the open-loop transfer function be given by

$$H_{ol}(s) = (k_p + \frac{k_i}{s})G_{filter}(s)\frac{1}{s} = \frac{1/T_{filter} \cdot (k_p s + k_i)}{s^2(s + 1/T_{filter})} \tag{23}$$

It can be expressed by a typical second order system, where

$$\begin{cases} \omega_c = \omega_p/b \\ k_p = \omega_c \\ k_i = \omega_c^2/b \end{cases} \tag{24}$$

b is a design constant which affects transient response and stability margin. Thus,

$$\begin{cases} \omega_c = 1/T_{filter}b \\ k_p = 1/T_{filter}b \\ k_i = 1/T_{filter}^2 b^3 \end{cases} \tag{25}$$

With general symmetrical optimum method, b can be set to 2.4 according to the tradeoff between the rapid response and stability [21], [29]. For $dq\text{DSC}_2$, the time constant is T/4.

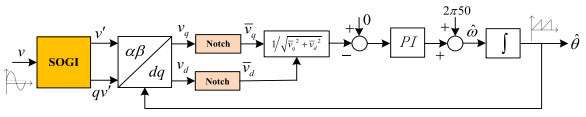


FIGURE 19. Schematic diagram of the NF SOGI-PLL.

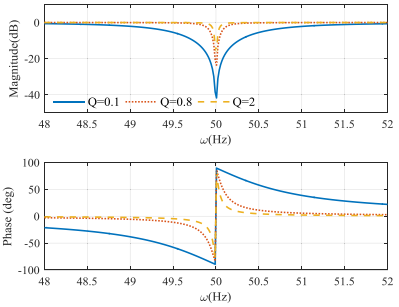


FIGURE 20. Frequency response of Notch Filter.

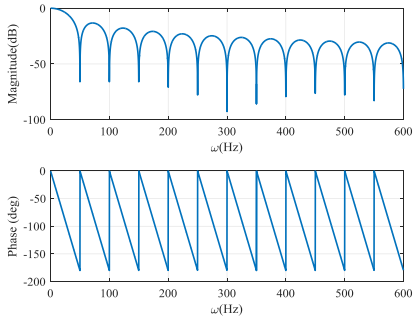


FIGURE 21. Frequency response of MAF.

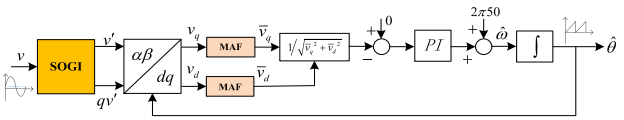


FIGURE 22. Schematic diagram of the dqMAF SOGI-PLL.

The LF are set with $k_p = 83.3333$, $k_i = 2893.519$ according to (25).

F. NOTCH FILTER BASED PLL

Fig. 19 shows the schematic diagram of notch filter (*NF*) based SOGI-PLL, where *NF* is arranged in loop of SRF-PLL to cancel the fundamental harmonic of PD effectively under input dc offset condition.

The transfer function of NF is given as [30]

$$N(s) = \frac{s^2 + \omega_z^2}{s^2 + s\omega_z/Q + \omega_z^2} \tag{26}$$

where ω_z is the notch frequency, Q is the damping ratio. Fig. 20 illustrates the frequency response of $N(s)$ with different value of Q with $\omega_z = 2\pi 50$. It shows that $N(s)$ provides considerable attenuation in a narrow band around the notch frequency. In discrete implementation, by using the Tustin method, the (26) can be expressed by

$$N(z) = N(s)|_{s=\frac{2}{T_s}\frac{z-1}{z+1}} = \frac{(\frac{2}{T_s}\frac{z-1}{z+1})^2 + \omega_z^2}{(\frac{2}{T_s}\frac{z-1}{z+1})^2 + (\frac{2}{T_s}\frac{z-1}{z+1})\omega_z/Q + \omega_z^2} \tag{27}$$

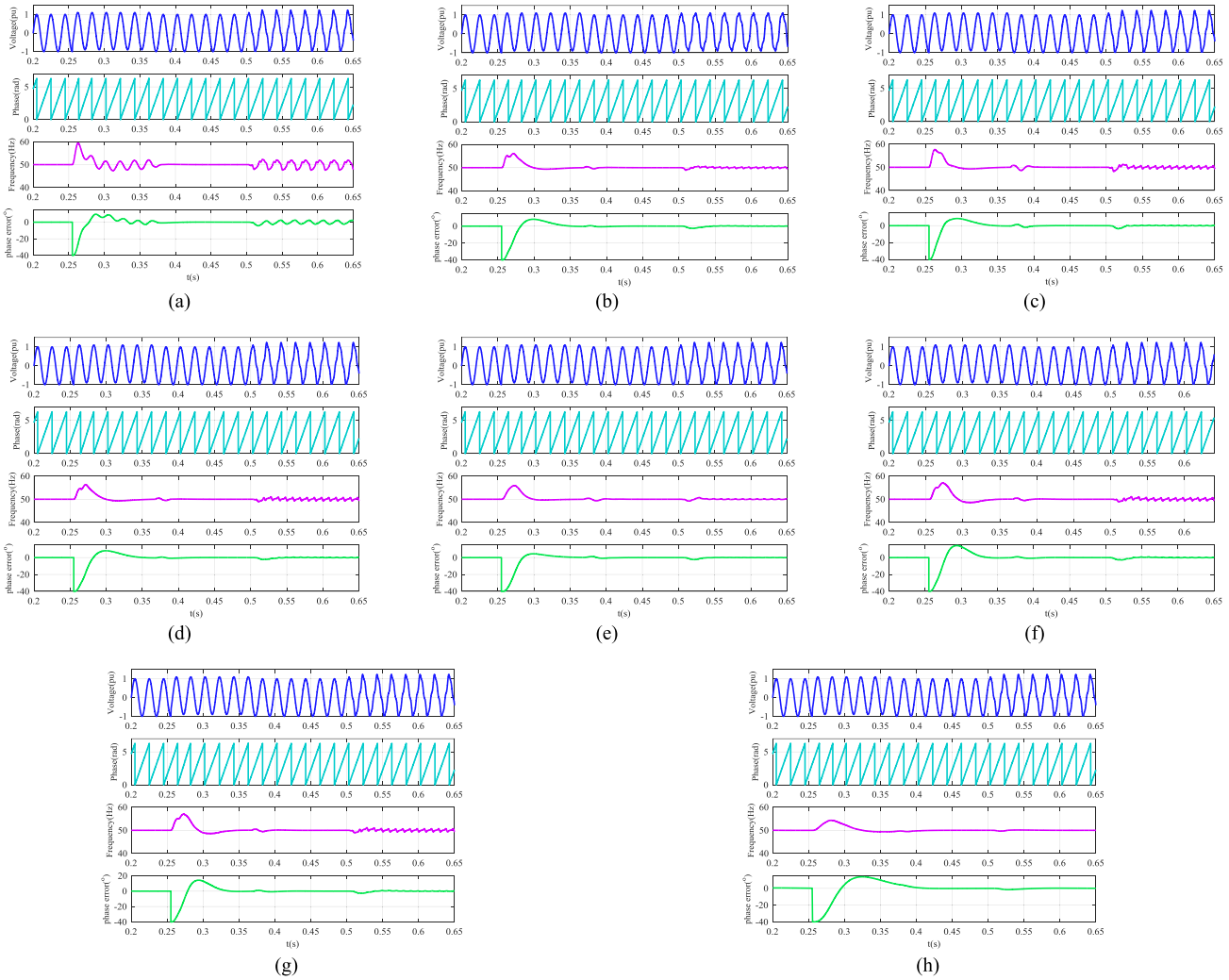


FIGURE 23. Numerical results: (a) Conventional SOGI-PLL, (b) Cascade SOGI-PLL, (c) Modified SOGI-PLL, (d) $\alpha\beta$DSC$_2$ SOGI-PLL, (e) CCF SOGI-PLL, (f) dqDSC$_2$ SOGI-PLL, (g) NF SOGI-PLL, and (h) dqMAF SOGI-PLL.

The parameters are selected as: $T_s = 0.0001$s, $Q = 0.8$, then

$$N(z) = \frac{1.0002 - 1.9995z^{-1} + 1.0002z^{-2}}{1.0199 - 1.9995z^{-1} + 0.9806z^{-2}} \tag{28}$$

This algorithm requires 5 multiplications, 4 additions and 5 buffers. NF can be approximated by a first order low pass filter with time constant $1/\omega_z Q$ [18]. According to (25), the LF parameters can be optimized as: $k_p = 104.1667$, $k_i = 4521.1227$.

G. MOVING AVERAGE FILTER BASED PLL

Moving Average Filter (MAF) is expressed as

$$\bar{x}(t) = \frac{1}{T_w} \int_{t-T_w}^{t} x(\tau) d\tau \tag{29}$$

where T_w is the filter window length, $x(t)$ is the signal to be filtered, and $\bar{x}(t)$ is the output. The transfer function can be given by

$$G_{MAF}(s) = \frac{\bar{x}(s)}{x(s)} = \frac{1 - e^{-T_w s}}{T_w s} \tag{30}$$

The Bode plot of (30) with $T_w = 0.02$s is shown in Fig. 21. It shows that MAF is a low-pass filter with multi-point notch attenuation at frequencies n/T_w ($n = 1, 2, 3 \ldots$) and can block these disturbances with unity gain for dc component [31].

In practical application, digital implementation of MAF can be derived as

$$\bar{x}(k) = \frac{1}{N} \sum_{i=0}^{N-1} x(k - i) \tag{31}$$

where x(k) is the current sample of x(t), $\bar{x}(k)$ is the digital output and the sample time is T_s. It can be conveniently implemented with the circular buffer in digital form and the computational burden is very low.

Fig. 22 shows the schematic diagram of the dqMAF SOGI-PLL. With time windows of 0.02s, this algorithm can filter

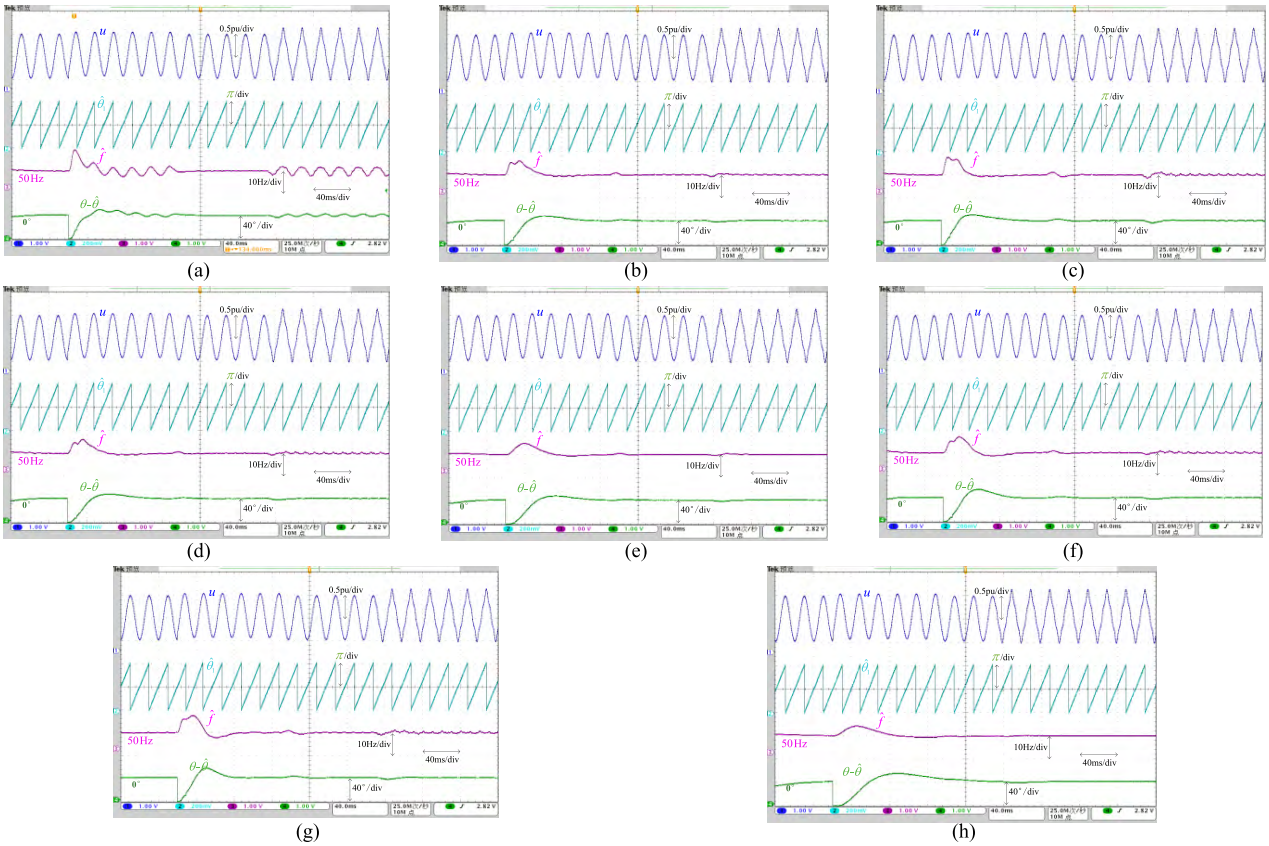


FIGURE 24. Experimental results: (a) Conventional SOGI-PLL, (b) Cascade SOGI-PLL, (c) Modified SOGI-PLL, (d) $\alpha\beta$DSC$_2$ SOGI-PLL, (e) CCF SOGI-PLL, (f) dqDSC$_2$ SOGI-PLL, (g) NF SOGI-PLL, and (h) dqMAF SOGI-PLL.

out all multiple fundamental disturbance and leave only dc term in dq-frame as the phase error information. For the time constant of MAF is T/2, the LF parameters of dqMAF SOGI-PLL can be tuned as: $k_p = 41.6667$, $k_i = 723.3796$.

IV. NUMERICAL AND EXPERIMENTAL RESULTS

In this section, eight SOGI-PLL algorithms are evaluated with both numerical and experimental results under the scenario of input dc offset combined with either phase-angle jump or harmonics condition in order to comprehensively evaluate the performance of these algorithms. Specifically, the dc offset steps up to 0.1pu with respect to fundamental amplitude at 0.255s. At the same time, it occurs with +40 degree input voltage phase angle jump. At 0.368s, both dc offset and phase angle return to nominal. At 0.503s, the dc offset steps up to 0.1pu as well as distorted by 3th and 5th harmonic with amplitude of 0.1pu.

Both numerical and experimental results are provided. The simulation model was implemented in Matlab/Simulink. An experimental platform was set up with floating point digital signal processor TMS320F28377S to implement different algorithms. The on-chip 12 bits AD module captures the input as voltage signal. The sample frequency is 10 KHz, and each PLL algorithm was executed in an interrupt routine.

The numerical and experimental results are shown in Fig. 23 and Fig. 24, respectively. Each result presents four graphics from top to bottom, including input voltage (u), estimated phase angle ($\hat{\theta}$), estimated frequency ($\hat{f}$), and phase error ($\theta - \hat{\theta}$).

For both the simulation and experiments, the PI parameters for each algorithm are tuned to achieve wide bandwidth considering both requirement of good dc offset rejection and fast dynamic speed. The delay caused by SOGI and prefiltering operation in the stationary reference frame is neglected. The simulation and experimental results with the conventional SOGI-PLL are illustrated in Fig. 23 (a) and Fig. 24 (a), which show significant steady-state ripple error in the estimated frequency and phase under this scenario.

Compared to conventional SOGI-PLL, all seven advanced algorithms track the frequency and phase with zero-steady state error under this scenario, as depicted by the transient process in numerical and experimental profiles. In order to quantitatively evaluation the performance of these algorithms, main performance indexes such as the setting time, frequency or phase errors are used. The phase settle time is measured by the time between the estimated phase reaches and remains within 1 degree of its steady-state values. Table I summarizes the performance comparison of the total eight SOGI-PLL algorithms under this scenario. The comparison

TABLE 1. Results summary for the eight SOGI PLL Algorithms.

	SOGI-PLL	Cascade SOGI-PLL	Midified SOGI-PLL	$\alpha\beta$DSC SOGI-PLL	CCF-based SOGI-PLL	dqDSC$_2$ SOGI-PLL	NF SOGI-PLL	MAF SOGI-PLL
Dc offset with Phase-angle jump 40°								
Phase settling-time* (ms, simulated)	---	84.3	79.6	84.7	83.0	75.0	143.1	149.7
Peak Phase error(°, simulated)	9.55	8.13	8.47	8.11	4.49	14.22	15.66	13.73
Peak Frequency error(Hz, simulated)	9.41	6.05	7.65	6.29	5.88	7.01	7.88	4.32
Dc offset with Phase angle jump 40°								
Phase settling-time** (ms, tested)	---	85.8	81.8	86.4	86.5	78.0	143.2	150.8
Peak Phase error(°, tested)	11.87	8.75	9.11	8.13	5.10	15.50	16.39	14.10
Peak Frequency error(Hz, tested)	9.53	6.41	7.96	6.25	4.02	6.92	8.06	4.53
Dc offset with harmonic								
Peak-to-peak Frequency error(Hz, simulated)	4.34	0.69	1.45	1.51	0.27	1.40	1.43	0
Peak-to-peak Phase error (°, simulated)	4.8	0.27	0.55	0.57	0.14	0.14	0.54	0
Dc offset with harmonic								
Peak-to-peak Frequency error(Hz, tested)	4.06	0.93	1.42	1.59	0.32	1.10	1.60	0
Peak-to-peak Phase error (°, tested)	5.63	0.44	0.67	0.62	0.22	0.30	0.44	0
DC offset estimation	---	Yes	Yes	Yes	Yes	No	No	No
Computation Burden	---	Low	Low	Moderate	High	Very Low	Very Low	Very Low

*in ±1°, ** in 0°.

of dc offset estimation capability, harmonic immunity, and computation burden is also illustrated. According to the comparison results, dqDSC2 show best dynamic response speed, followed by modified SOGI-PLL; MAF SOGI-PLL show highest harmonic immunity, followed by CCF-based SOGI-PLL and Cascade SOGI-PLL; besides, cascade SOGI-PLL, modified SOGI-PLL, $\alpha\beta$DSC, and CCF-based SOGI-PLL can estimate the dc offset component.

V. CONCLUSION

This paper presents a detailed investigation for dc-offset rejection capability of several advanced SOGI-PLL algorithms in single-phase system. By using the conventional SOGI PLL algorithm, the existence of dc offset in the PLL input results in fundamental frequency oscillatory errors in the estimated phase and frequency.

Thus, in order to meet the international grid standards, advanced algorithms must be proposed in order to improve the dc offset rejection capability. Specifically, in this paper, seven advanced SOGI based PLL methods are comprehensively evaluated, including the cascade SOGI, modified SOGI, $\alpha\beta$-frame delayed signal cancellation (DSC), complex coefficient filter, in-loop dq-frame DSC, notch filter, and moving average filter based PLL. Generally, these algorithms can be classified into three categories:

(1) QSG modification algorithms: with some kind of QSG structure change to realize QSG with better dc offset rejection and tune the output signals of QSG as ideal sinusoidal and quadrature. Both cascade SOGI and modified SOGI belong to this type. These two methods also show good harmonic filter capability with well-tuned parameter k.

(2) Fundamental-component separation algorithms: without changing the structure of QSG, $\alpha\beta$DSC and CCF-based technique separate the fundamental sequence of SOGI output in $\alpha\beta$-frame, meanwhile eliminate the dc term. The input signals fed to later *Park* transform are clean and sinusoidal. The research shows that the CCF based cross feed forward decouple structure offering excellent filter capability at the cost of more computer resource.

(3) Filter in-loop based algorithms: it employs a filter in loop of PLL without considering specific input signals fed to SRF-PLL. This kind of filter can pass the dc term that corresponds phase error information, and reject the fundamental disturbance corresponding to the input dc offset simultaneously. dq-frame DSC, notch filter and MAF belong to this category. All in-loop filter technique introduces the additional time delay, furthermore, the LFs need to be tuned carefully with respect to their time constant. Based on the open loop transfer function, the general symmetrical optimum tune method exhibits satisfied performance. The drawback of this technique is that the dc offset cannot be obtained directly.

The effectiveness of these methods was confirmed by using both the numerical and experiment results. Overall, these algorithms show merits for practical application for power converters. In the dc-offset rejection performance comparison, other important factors such as the dynamic response, harmonic immunity, dc-offset estimation capability, and computation burden are also considered. The performance comparison of the eight SOGI-PLL algorithms under different scenarios is summarized in Table I, which show that dqDSC$_2$ show best dynamic response speed, followed by modified SOGI-PLL; MAF SOGI-PLL show highest harmonic immunity, followed by CCF-based SOGI-PLL and Cascade SOGI-PLL; besides, cascade SOGI-PLL, modified SOGI-PLL, $\alpha\beta$DSC, and CCF-based SOGI-PLL can estimate the dc offset component. Regarding the computation burden, the filter in-loop based algorithms show obvious advantage.

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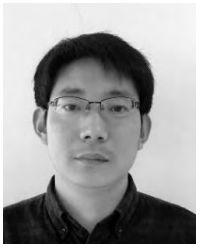

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