IEEE Access
Multidisciplinary | Rapid Review | Open Access Journal

SPECIAL SECTION ON POWER QUALITY AND HARMONICS ISSUES OF FUTURE AND SMART GRIDS

Received May 19, 2017, accepted June 18, 2017, date of publication June 23, 2017, date of current version July 17, 2017.

Digital Object Identifier 10.1109/ACCESS.2017.2719055

A Hidden Block in a Grid Connected Active Front End System: Modelling, Control and Stability Analysis

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This work was supported by the Australian Research Council's Future Fellowship Program under Grant FT150100042.

ABSTRACT An LCL filter utilized in an active front end (AFE) converter can generate significant resonance, which can affect quality and stability of the system. Thus, a proper active or passive damping technique and/or a suitable controller is required to be designed for the converter. The duty cycle constraint—though inevitable in practical inverter systems—is often ignored in most of the existing literature. The effects of measurement noise on filter control system performance must be considered and evaluated under different conditions. Finally, almost all inverter control systems are implemented digitally using microcontrollers. Consequently, the effects of sampling on control system stability and performance should be evaluated as well. Thus, this paper presents stability analysis of an AFE converter-based filter design with a complete practical system configuration, including saturation and sampling blocks and measurement noises. Mathematical analysis and simulations have been carried out to validate the proposed method.

INDEX TERMS LCL filters, duty-cycle saturation, control system design and analysis.

I. INTRODUCTION

In the development of modern society, saving energy and providing sustainable clean electricity are major factors in order to become more independent of oil and fossil fuel based energy resources. Greenhouse gas emission concern has been a new driving force to utilize more distributed generation energy sources such as grid connected solar inverters and wind turbines. Penetration of renewable energy systems based-power electronics has been increased in many countries including Australia. The main drawbacks of power electronics systems are low frequency (below 2 kHz) and/or high frequency (above 2 kHz) harmonic emissions [3]–[5]. Harmonics have short and long term effects on grids, grid connected equipment and communication signaling. These harmonic issues reduce quality, reliability and efficiency of electricity networks. New demands for efficient and reliable power electronics-based loads and renewable energy sources have promoted power electronic applications extensively in industrial, commercial and residential sectors as follows [1], [2].

- Penetration of grid connected renewable energy sources in low and medium voltage distribution networks is expected to increase threefold from 2009 to 2035. Global Trends in Renewable Energy Investment 2015, highlights a record $119 billion in new investment in renewable energy in China and Japan.
- Electric motors consume more than 40% of global electrical energy. The energy consumption of the motor is reduced from a full power to a partial power using power electronics drives for the same performance.
- The trend toward a clean transportation brings electric cars in residential sectors as well. The end-use energy efficiency of these applications plays a key role in reducing CO_2 emissions.

There are a number of different converter topologies utilized in different power electronics applications. However, for bidirectional power flow, the front side converter should be based on an inverter with active switches. An Active Front End (AFE) converter – single or three phase system - is a bidirectional power flow converter with a high quality, sinusoidal line current waveform suitable for many applications such as renewable energy system, motor drives and battery chargers. The system has active power switches such as IGBTs or MOSFETs which are controlled based on a Pulse Width

Modulation (PWM) technique. In order to control the switching frequency ripple, a front side filter is required which can be *L*, *LC*, *LCL* or *LCLL* type [6]–[8]. The *LCL* filter is a common filter as it can reduce current ripple arising mainly due to high frequency switching and clean the line current at the grid side. However, due to resonant issues of the LCL filter, which can affect the stability of the converter, a proper damping method is required.

There are many research publications addressing a single loop current feedback either from the grid or the inverter side. For both cases, the grid impedance variation and the inverter parameters have a big impact on the stability and the robustness of the system. In order to improve the performance of the system, Active Damping method has been proposed based on additional control loop feedbacks [9] such as the capacitor current feedback [10], [11], [15], the capacitor voltage feedback [12]–[14] or multivariable feedback methods [13], [14]. Although these methods are very promising and can stabilize the system, additional high quality and precision sensors are required which can increase the cost and the complexity of the system. State estimation approaches have been proposed to observe the capacitor current or voltage but the control systems can be highly sensitive to even slight variations in state estimates [12], [16]. The resonant frequency of the LCL filter and digital sampling have big impacts on the stability of the system. In [14] it is shown that the grid-side current is essential with a low resonant frequency region while an active damping is not required for a high frequency resonant region.

Several controller design approaches have been proposed [17]–[20] for grid connected inverter with the LCL filter. In [18]–[20], a step-by-step controller design is analysed based on active damping to suppress resonance generated by the LCL filter while a Proportional-Integrator (PI) or Proportional-Resonant (PR) compensator is utilized in order to reduce the steady state error [21]–[23].

In a real case design, the losses in the *LCL* filter and the power quality of the grid such as low order harmonics should be considered for the overall design of the control system. In [13], a filter design has been considered based on the feedback and the feedforward of the grid current using two degrees of PID controller – independent action of PI and D terms.

Stability analysis of the AFE system and developing a proper controller is one of the challenging issues of the AFE converter. The main design issue and constraint is related to the transfer function of the filter and its parameters. In particular, the controller design approach is very challenging due to close locations of the system poles to the origin and on the imaginary axes. One of the solutions to damp the resonance of the filter is to use an appropriate filter which does not need any sensors. However, the solution suffers from a lack of robustness, narrow bandwidth and higher complexity. The filter should be designed to control the high frequency dynamics of the system while a proper current controller can stabilize the low frequency dynamics of the system. In the filter design approach, the gain and the phase margins are increased in order to improve the stability and robustness of the system.

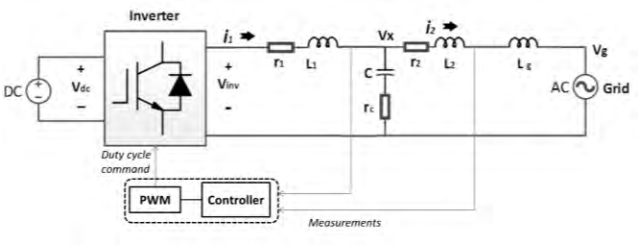

FIGURE 1. A single phase grid connected Active Front End converter.

In practice, a power electronic system is usually designed based on a digital control system in which a Digital Signal Processing (DSP) controller is programmed as the main part of the whole control system. Digital implementation of controllers involves use of a sampler/zero order hold. Therefore, effect of sampling needs to be modelled in the control model of the system. In order to properly analyse a power electronics system, the effects of sample-hold and PWM function should be considered as well. During each switching cycle, the measured current and/or voltage values are kept constant based on a sample-hold system and these values are normally updated at the middle or at the end of the switching cycle. In [10], [14], and [24], the effects of the sampling and the PWM system have been considered for an active damping method with the capacitor current loop. The ratio of the resonant to sampling frequency can affect the robustness and the stability of the converter. In [11], [24], and [25], the stability issues of an *LCL* type inverter is analysed with a high variation of grid impedance in discrete-time domain.

In all literature, a saturation block in the PWM module has not been modelled and its effects on the stability of the system has not been considered. In this paper, a comprehensive analysis of a grid connected AFE has been considered taking into account a saturation block - as a non-linear block - affecting the stability of the system. The effects of noise and sampling units have also been considered for control analysis of the system. Stability advantages of the passive damping method have been discussed with respect to other control approaches.

II. SYSTEM MODELLING AND PROBLEM FORMULATION

Figure 1 shows a circuit diagram of a single phase grid connected inverter with an *LCL* filter. The transfer function of the system can be extracted based on the system parameters and state variables of i_1, v_C and i_2. The system parameters are described in Table I. The voltage across the capacitor leg, v_x, is derived as below.

$$v_x = (1 + sr_C C)v_c \tag{1}$$

where v_C is the voltage across the capacitor. The current through the first inductor, i_1 can be extracted based on the inverter voltage v_{inv} and v_x.

$$v_{inv} - v_x = (r_1 + sL_1)i_1 \tag{2}$$

TABLE 1. Filter parameters.

PARAMETER	DESCRIPTION	VALUE
V_{dc}	*DC link voltage*	500 V
r_1	*Internal resistance of the inductor L1*	0.1 Ω
r_2	*Internal resistance of the inductor L2*	0.1 Ω
r_C*	*A resistor in series with the capacitor*	0.1 - 6 Ω
L_1	*The first inductor at the inverter side, L_1*	0.5 mH
L_2	*The second inductor at the grid side, L_2*	0.19 mH
C	*The capacitor in the LCL filter, C*	50 μF
L_g	*The grid inductor*	100 μ H

* r_C= 6 Ω (passive damping); r_C= 0.1 Ω - 0.6 Ω (without passive damping)

The current at the grid side, i_2 is given as below where v_g is the grid voltage.

$$v_x - v_g = (r_2 + sL_2 + sL_g)i_2 \tag{3}$$

Using (1)-(3), the line current can be found in terms of the inverter and grid voltages.

$$i_2 = \frac{Z_c}{K_1}v_{inv} - \frac{K_2}{K_1}v_g \tag{4}$$

where

$$\begin{cases} K_1 = Z_1Z_c + Z_2Z_c + sCZ_1Z_2 \\ K_2 = Z_c + sCZ_1 \\ Z_c = (1 + sr_CC) \\ Z_1 = (r_1 + sL_1) \\ Z_2 = (r_2 + sL_2 + sL_g) \end{cases}$$

By defining:

$$G_{LCL}(s) = \frac{I_2(s)}{d(s)} = \frac{V_{dc}Z_c}{K_1}, \tag{5}$$

the transfer function of the system can be expressed in terms of the filter and the inverter parameters as below (without L_g):

In (6), L_g can be easily include by replacing L_2 with $(L_2 + L_g)$. The grid-side current i_2 is chosen as the targeted variable whose response and value are to be regulated. From $G_{LCL}(s)$ it is clear that the inverter *LCL* filter model is a linear time invariant (LTI) model and represents a 'Type 0' system - it has no integrator. When the *LCL* filter is considered as a loss-less system, then all resistors r_1, r_C and r_2 are zero and $G_{LCL}(s)$ is simplified based on (6) as follows:

$$G_{LCL}(s) = \frac{1}{CL_1(L_2 + L_g)s^3 + (L_1 + L_2 + L_g)s} \tag{7}$$

From (7) it is clear that with the resistors r_1, r_2 and r_C set as 0 Ω the system Type changes to Type 1 (one integrator). Type 1 systems are difficult to stabilize and, therefore, are generally not employed in practice. Furthermore, for stability analysis of the system, Routh's criterion should be satisfied while there is no s^2 term in the denominator of the transfer function. Thus, the open loop transfer function of the system has one pole at zero and two poles on the imaginary axes, which shows a marginally stable system.

On the other hand, adding resistors in the filter to increase the damping factor of the system can affect the efficiency of the system. A promising solution is to add only a resistor in series with the capacitor as the major high frequency current circulates through the capacitor while the fundamental high power current at 50 Hz or 60 Hz passes through the inductors, L_1 and L_2. However, when the switching frequency of the inverter is low, the resonant frequency of the *LCL* filter is shifted to a lower frequency range as well. Hence the capacitance value is determined based on the reactive power through the capacitor at 50 Hz as well as the resonant frequency of the filter based on:

$$f_{res} = \sqrt{\frac{L_1 + L_2 + L_g}{CL_1(L_2 + L_g)}} \times \frac{1}{2 * \pi} \tag{8}$$

Consequently, in this paper, the values of the resistors are given in Table I and r_c is changed from 0.1-6 Ω to analyse the stability issues of the converter.

Figure 2 represents the block diagram representation of the *LCL* filter control system based on the LTI system model (6). The overall control problem considered in this paper is to design a compensator $G_C(s)$ to track the grid-side current i_2 as per a predefined desired reference $i_{2,ref}$. This control objective is to be achieved through an appropriate adjustment of the duty cycle. Three key practical factors are considered, namely, duty cycle constraints, robustness of the control system to noise and effects of digital implementation of control systems. The duty cycle commands generated by $G_C(s)$ are subject to hard constraints due to the switched nature of modern power electronic inverters. Consequently, in practical inverter systems commanded duty cycle is clipped for values beyond -1 and $+1$. This phenomenon is represented by the saturation block in Figure 2. Nevertheless, for the time-domain simulations included in this paper, the saturation phenomenon is captured through the use of a high-fidelity inverter model including PWM that is used for controller validations (as shown in Figure 1). The duty cycle constraint, though inevitable in practical inverter systems, is often ignored in most of the existing literature on *LCL* filter control system design methods. The effects of measurement noise and electromagnetic interference on filter control system performance must be considered and evaluated. Finally, almost all inverter control systems are implemented digitally using microcontrollers. Consequently, the effects of sampling on control system stability and performance must be evaluated.

$$G_{LCL}(s) = \frac{V_{dc}(1 + sCr_C)}{CL_1L_2s^3 + C(L_1r_C + L_1r_2 + L_2r_1 + L_2r_C)s^2 + (L_1 + L_2 + C(r_1r_C + r_1r_2 + r_2r_C))s + (r_1 + r_2)} \tag{6}$$

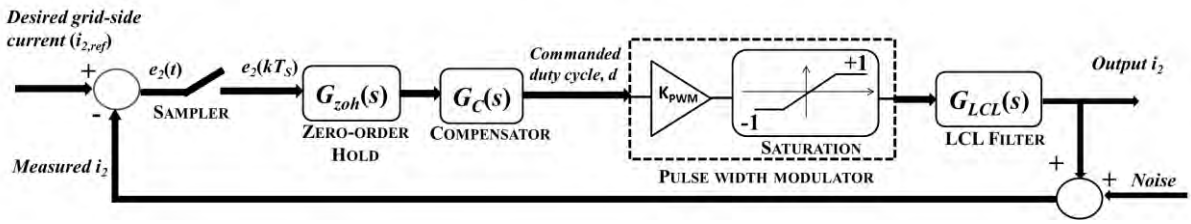

FIGURE 2. Block diagram representation of *LCL* filter closed loop control system.

III. A SYSTEMATIC APPROACH TO FILTER CONTROL SYSTEM DEVELOPMENT AND ANALYSIS

The design of filter control systems is perhaps the key to the overall operational performance of inverters and to achieve acceptable power quality level. The overall filter design involves two (often conflicting) requirements. On one hand, the filter design configuration is to be chosen to maximise the efficiency of the system through the choice of smallest possible resistors. On the other hand, control system stability and performance guarantees must be ascertained keeping in view practical considerations such as duty cycle saturation and measurement noise. The objective of the control systems is to establish the best possible trade-off between the two requirements while ensuring certain predefined filter performance specifications are met.

Throughout this section, the terms controller and compensator are used synonymously. Given the system open-loop transfer function $G_{LCL}(s)$ there are two possible approaches to develop filter control/compensator system. One approach is to choose sufficiently large resistor(s) to obtain a *passively damped* filter configuration. With passively damped filter configuration the task of control system development gets substantially simplified. An alternative approach is to choose the compensator structure and filter design parameters so as to minimise the resistor sizes while ensuring acceptable closed loop performance. Table I lists the values of the parameters used in $G_{LCL}(s)$. In the ensuing analysis, the value of r_C is varied to evaluate and discuss the effect of the choice of r_C on control system's achievable performance. Specifically, r_C value is varied because the value of r_C has a greater influence on filter's susceptibility to resonance as the high frequency currents mainly circulates through the capacitor. A range of successively lower r_C (between 0.1 Ω – 0.6 Ω) values are considered to evaluate and discuss the challenges associated with control system development with low values of r_C. In addition, analysis is also performed with r_C chosen as 6 Ω to represent a passively damped *LCL* filter configuration.

The aim of this section is to demonstrate a systematic guided approach to *LCL* filter control system development, highlight practical challenges that are often not considered in literature but have a significant effect on filter stability and performance, and in doing so limit trial and error approach to overall filter design. The aim here is also to demonstrate and highlight the significance of collectively considering all practical aspects of control system development. First, a procedure to design a compensator to address the effects of duty cycle saturation and noise is presented and discussed. Then, the practical validity of the design is evaluated for sampled data control implementation based on first-order sample-hold system.

A. COMPENSATOR DEVELOPMENT WITHOUT PASSIVE DAMPING

1) ANALYSIS OF FILTER SYSTEM WITH PROPORTIONAL-ONLY COMPENSATOR, WITHOUT MEASUREMENT NOISE AND DUTY CYCLE SATURATION

The performance specifications can be described in time domain, including overshoot, settling time, and in frequency domain in terms of relative stability margins and bandwidth.

- Time domain specifications include low or negligible overshoot, fast settling time and negligible steady state error.
- Frequency domain specifications include sufficiently high gain (GM) and phase margins (PM) and large bandwidth.

The precise numerical values of performance specifications vary on a case-by-case basis and depend on the nature of application where an inverter is to be used. Some example numerical values are discussed in the sequel. Our objective is to design a compensator $G_C(s)$ to meet the performance requirements. Simultaneously, the effect of successively lower resistor values is to be considered and discussed to establish practical guidelines for the choice of resistors.

Let us consider *LCL* filter configuration as *without passive damping* by setting $r_C = 0.6\ \Omega$. First, let us analyse the $G_{LCL}(s)$ without the effects of duty cycle saturation and sampling. Such designs, without explicit consideration of sampling, are common in digital control and are commonly referred to as *emulation* of continuous design. Such designs are likely to be successful if the sampling frequency is sufficiently high (this point is illustrated later in this paper in section 3.6). Similarly, systems with saturation are often designed in this way and in the second step an anti-windup compensator is added. The existing practical inverters already have anti-windup feature included as a part of their control systems (implemented by resetting the integrator at the end of each switching cycle). Nevertheless, the duty cycle saturation issue arises due to inverter PWM control. Therefore,

saturation issue can arise regardless of the type of controller used and cannot be addressed through an integrator anti-windup compensator. The compensator $G_C(s)$ is chosen as a basic proportional constant gain. The analysis is performed by using the root locus and Bode plot techniques. The corresponding plots are shown in Figure 3. The plots were obtained using MATLAB.

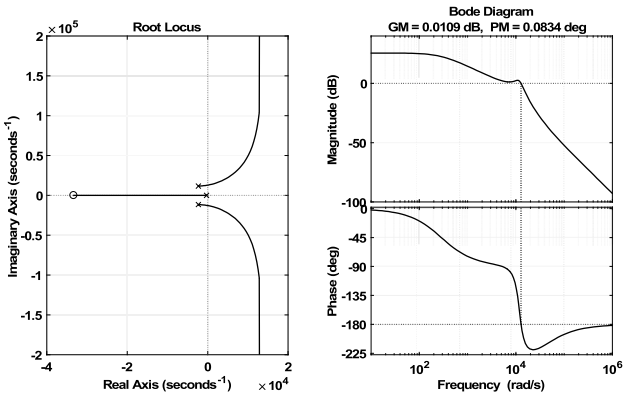

FIGURE 3. (a) Root locus of $G_{LCL}(s)$; (b) Bode plot of $G_C(s) \times G_{LCL}(s)$ with $G_C(s) = 0.00764$.

It may be noted that root locus trajectories show how the closed loop pole locations change with changes in system gain (with proportional-only compensator, $G_C(s)$ itself is the constant gain parameter that is adjusted). Using the root locus plot, the closed loop poles corresponding to a specific gain value can be determined. On the other hand, Bode plots show the relative stability margins in terms of GM and PM. That is, how much gain can be increased and/ or phase delayed before the closed-loop system becomes unstable. For stability with inherent robustness, both GM and PM should be positive with sufficiently large values.

G_{LCL}(s) root locus plot in Figure 3 shows that successive increases in gain successively moves the closed loop poles closer to the imaginary axis and eventually cross over to the right half s-plane resulting in closed loop instability. Using Figure 3 and MATLAB tools it is found that the gain can be increased up to only around 0.00764, further increases in gain result in closed loop poles in the right half s-plane. Increase in gain is essential to reduce the steady state error, however, with the gain of 0.00764 the corresponding peak overshoot is found to reach nearly 38% and settling time of around 132 s. Figure 3 also shows the Bode plot of $G_C(s) \times G_{LCL}(s)$ with $G_C(s) = 0.00764$. The corresponding GM and PM are close to zero implying poor relative stability. Consequently, with proportional-only compensator range of gain adjustment is severely limited, increasing gain does not deliver acceptable time domain performance and the associated relative stability margins gradually diminish with increasing gain.

2) EFFECT OF DUTY CYCLE SATURATION

In practical power electronic systems, duty cycle commanded by $G_C(s)$ is constrained to take values between -1 and $+1$. Any value outside this range is clipped. Consequently, there is a saturation block (with limits -1 and $+1$) between $G_C(s)$ and G_{LCL}(s) (ref. Figure 2). Presence of saturation makes the otherwise LTI filter system nonlinear. The classical frequency domain approaches such as root locus and Bode plots are applicable to LTI systems only. These methods do not explicitly take into account nonlinearities in the feedback loop. This is a major limitation of classical frequency domain design methods because they do not allow saturation to be explicitly considered during the design stage.

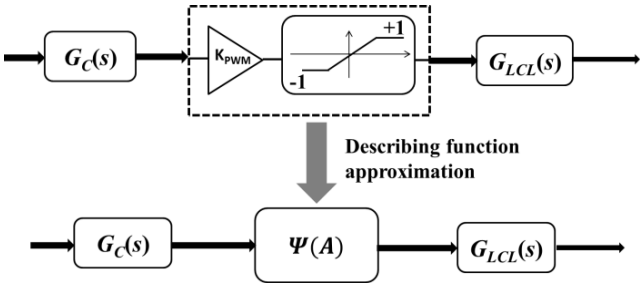

FIGURE 4. Describing function approximation of the saturation nonlinearity for prediction of limit cycles.

Although saturation cannot be considered in the design stage, its effect on stability and existence of limit cycles can be estimated through an approximation of saturation nonlinearity (Figure 4). This approach is called the *Describing Function method*. This section presents a brief overview of this approach (full details can be found in [26]). In subsequent section, describing function methods is used to evaluate the effect of saturation on stability and existence of limit cycles on compensator designs.

Let A denotes the amplitude of the periodic duty cycle signal that appears at the input of saturation function. Let the describing function approximation of the saturation nonlinearity be denoted as $\Psi(A)$. For saturation nonlinearity, $\Psi(A)$ is given as follows (for full details see [26, p. 285]):

$$\psi(A) = \begin{cases} 1, & \text{if } 0 \le A \le 1 \\ \frac{2}{\pi}\left[sin^{-1}\left(\frac{1}{A}\right) + \frac{1}{A}\sqrt{1-\left(\frac{1}{A}\right)^2}\right], & \text{if } A > 1 \end{cases} \tag{9}$$

Note that $\psi(A) \le 1, \forall A$.

Using Figure 4, the stability condition for the *LCL* filter closed loop system is governed by the following equations:

$$G_C(j\omega) \times \Psi(A) \times G_{LCL}(j\omega) + 1 = 0 \tag{10}$$

Therefore, the expression for predicting the stability properties (existence of limit cycles) in presence of saturation nonlinearity is

$$G_C(j\omega) \times G_{LCL}(j\omega) = -\frac{1}{\Psi(A)} \tag{11}$$

Condition (11) is used to evaluate the stability properties of the compensators $G_C(s)$ in presence of saturation nonlinearity. Stability condition (11) implies that the closed loop system remains stable if the Nyquist plot of $G_C\,(j\omega) \times G_{LCL}\,(j\omega)$ and the plot of $-1/\Psi(A)$ do not intersect. Intersection of the Nyquist plots of $G_C\,(s) \times G_{LCL}\,(j\omega)$ and $-1/\Psi(A)$ implies existence of limit cycles. For a given choice of compensator $G_C\,(j\omega)$ and the value of the amplitude A at which the sustained oscillations (limit cycles) occur can be estimated from the point of intersection of $G_C\,(j\omega) \times G_{LCL}\,(j\omega)$ and $-1/\Psi(A)$.

3) MEASUREMENT NOISE

Sensor measurements are often deteriorated due to noise and switching effects of power converters. Any measurement noise (n) present in i_2 measurements will be fed to the compensator through e_2:

$$\begin{aligned} e_2 &= i_{2,ref} - i_{2,measured} \\ &= i_{2,ref} - \left(i_{2,actual} + n\right) = \tilde{e_2} - n \end{aligned} \tag{12}$$

where $\tilde{e_2} = i_{2,ref} - i_{2,actual}$. Consequently, the duty cycle command (d) generated by $G_C(s)$ in response to e_2 that appears at its input is influenced by the measurement noise:

$$d(s) = G_C(s) \times (\tilde{e_2} - n) \tag{13}$$

From (13), it is clear that the effect of n is governed by the structure of compensator $G_C(s)$. Noise is of particular concern if $G_C(s)$ contains derivative control action. With derivative control action $d(s)$ relies on $K_d \frac{de}{dt}$ (with gain $K_d > 0$) and, therefore, on $K_d \frac{dn}{dt}$. Since, derivative control action is not physically realisable the usual practice is to use its digital approximation as per the following equation:

$$K_d \frac{dn}{dt} \approx K_d \frac{(n_k - n_{k-1})}{T_S} \tag{14}$$

where T_S represents the sampling period and n_k represents the noise value at the k^{th} sampling instant. From (14) it is clear that rapid sample by sample variations in noise coupled with high sampling frequency (low T_S) severely affect $d(s)$ values and, therefore, the overall control stability and performance. This phenomenon is validated in the subsequent sections to demonstrate the effect of noise on the achievable stability and performance of $G_C(s)$ designs.

4) EFFECT OF r_C VARIATION

Figure 5 shows the root locus and Bode plots of $G_{LCL}(s)$ with resistor values of $0.1\ \Omega - 0.6\ \Omega$. For comparison plots corresponding to passive damping (with $r_C = 6\ \Omega$) are also included. Root locus plots show that as r_C is successively reduced the $G_{LCL}(s)$ poles correspondingly move closer to the imaginary axis. As a results, reduction in r_C results in gradual reduction in the range of proportional gain adjustment before the trajectories cross to the right half s-plane. For example, for $r_C = 0.1\ \Omega$ the gain can be increased up to only 0.00157. With this gain the corresponding steady state error, overshoot

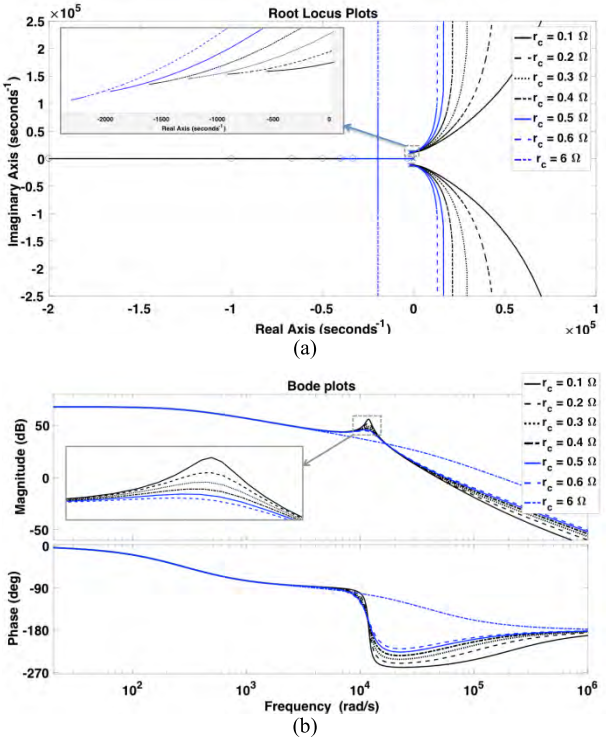

FIGURE 5. Root locus and Bode plots of $G_{LCL}(s)$ with different r_C values (insets show the zoomed-in views).

and settling time are found to be 21%, 11% and 22 seconds, respectively. This indicates that although increasing the gain up to 0.00157 ensures nominal stability (closed loop poles in the left half plane), the closed loop performance remains poor. Furthermore, close proximity to the imaginary axis on the root locus implies near zero GM and PM and, thus, negligible relative stability. Consequently, with successive reduction in r_C value, mere gain adjustment becomes *even* less promising and relative stability significantly worsens. From the Bode plots shown in Figure 5, it is seen that the resonant peak becomes more prominent with reduction in r_C value. Consequently, lower the r_C value greater is *LCL* filter's susceptibility to resonance.

When compared with passive damping, it is clear that the *LCL* filter with $r_C = 6\ \Omega$ remains stable for all gain values as the root locus trajectories completely lie in the left half *s*-plane. Furthermore, as expected the Bode plot does not display a resonant peak confirming that with passive damping the *LCL* filter is immune to resonance.

Table II summarizes the time domain performance indicators for successively lower r_C values. It is clear that as r_C is reduced the closed loop performance becomes exceedingly worse in terms of every time domain performance indicator. Steady state error is inversely proportional to gain, therefore, increase in gain improves the steady state error performance. On the other hand, reduction in gain improves damping factor and settling time because settling time is inversely proportional to damping factor (ζ) and undamped natural frequency

TABLE 2. Time-domain performance indicators.

r_C (Ω)	Maximum gain before instability	Steady state error at max. gain (%)	Overshoot (%)	Settling time (s)
0.6	0.0076479	5	38.2	132
0.5	0.0061744	6.1	33.2	87.4
0.4	0.004872	7.6	28.2	71
0.3	0.003695	10	22.7	43.3
0.2	0.002605	13.3	17.3	31.1
0.1	0.001575	20.3	11.6	22.4

(ω_n) (settling time $= 4/\zeta\omega_n$). Consequently, reduction in gain improves damping factor and settling time, however, comes at the expense of serious deterioration in steady state error. For example, with $r_C = 0.6\Omega$a reduction in gain to obtain a critically damped response entails steady state error of nearly 45%. This further confirms that mere gain adjustment is insufficient to meet design specifications of low steady state error, fast response and improved relative stability regardless of the choice of r_C values. In order to meet the performance specifications, ω_n needs to be increased while keeping ζ at desired value (to reduce settling time) without compromising steady state error. In order to achieve this, an appropriate compensator must be designed. This discussion is presented in the next section.

B. COMPENSATOR DESIGN FOR LCL FILTERS WITHOUT PASSIVE DAMPING

In the last section it is concluded that mere gain adjustment (proportional-only controller) is insufficient to meet the design requirements. Therefore, this section explores the design of alternative compensator design approaches.

The natural transition from proportional-only controller is to design a proportional-integral (PI) controller, which involves an integral action to eliminate the steady state error. Since the open loop $G_{LCL}(s)$ system is a Type 0 system, theoretically a PI (lag) and PD (lead) compensators can be designed to achieve the desired performance. A well-tuned PI controller theoretically has the potential to improve steady state performance while mostly conserving the transient response. However, the PI controller tends to result in a large overshoot. More importantly, in this particular application inclusion of an integrator in the compensator design pushes the root locus trajectories further in the right half s-plane, which makes the closed loop system further susceptible to instability. On the other hand, if a lead compensator is included in addition to a lag compensator (to obtain a PID controller) then theoretically the overall response including steady state error, settling time and overshoot can be improved. However, due to the presence of an integrator, even with any best tuned PID compensator the marginal stability cannot be improved in this application. This is due to the fact that the inclusion of integral action bends the root-locus trajectories towards the right half of s-plane. This limits the achievable performance by restricting the freedom to adjust gain without causing instability and deterioration in relative stability margins.

1) INCLUDING ZEROS IN COMPENSATOR DESIGN

To improve the steady state performance (low settling time, steady state error without compromising the damping ratio) and relative stability margins, let us consider the proposition of adding a compensating complex zero pair somewhere in the left half of s-plane. The key effect of additional compensating zeros will be that the complex branches will be bent away from the imaginary axis. As a result, all branches of root locus will significantly move to the left half s-plane which will provide greater flexibility in the choice of gain without causing instability.

a: CONSIDERATIONS FOR POSITIONING ZEROS FOR STABILITY

Let p_1, p_2 and p_3 represent the poles of $G_{LCL}(s)$ and z represents the zero. Accordingly, $G_{LCL}(s)$ can be expressed in the pole-zero form as follows:

$$G_{LCL}(s) = \frac{K\,(s+z)}{(s+p_1)\,(s+p_2)\,(s+p_3)} \tag{15}$$

For the nominal system data given in Table I,

$$K = 3\times10^9, z = 3.33\times10^4,$$
$$p_{1,2} = (-0.23 \pm j1.16)\times10^4, p_3 = -286.$$

Let a pair of complex conjugate zeros at $s = -z_{1,2} = -(x \pm jy)$ be added to $G_{LCL}(s)$ such that the new transfer function takes the following form

$$\frac{K\,(s+z)}{(s+p_1)\,(s+p_2)\,(s+p_3)}\times K_z\left(\frac{s}{z_1}+1\right)\left(\frac{s}{z_2}+1\right) = \frac{K\,(s+z)}{(s+p_1)\,(s+p_2)\,(s+p_3)}\times K_z\left(\frac{s^2}{|z_1|^2}+s\left(\frac{2\times x}{|z_1|^2}\right)+1\right) \tag{16}$$

where K_z represents the compensator gain. Using (15) and (16), the difference between the uncompensated and the compensated (with an added pair of zeros at $z_{1,2}$) responses are governed by the following terms:

$$K_z\frac{s^2}{|z_1|^2}\left(\frac{K\,(s+z)}{(s+p_1)\,(s+p_2)\,(s+p_3)}\right) + K_z s\frac{2\times x}{|z_1|^2}\left(\frac{K\,(s+z)}{(s+p_1)\,(s+p_2)\,(s+p_3)}\right) \tag{17}$$

From the above equation it is clear that the positioning of $z_{1,2}$ affects the transient response of the compensated system. In particular, as $z_{1,2}$ is moved from infinity to zero along the negative real axis, $z_{1,2}$ eventually becomes dominant and will contribute to overshoot. The smaller the value of real part of $z_{1,2}$ the larger is the overshoot and the larger the settling time. Consequently, the zeros should be positioned deep in the left half s-plane (larger than the $G_{LCL}(s)$ poles and zeros) so that their effect on the transient response is negligible.

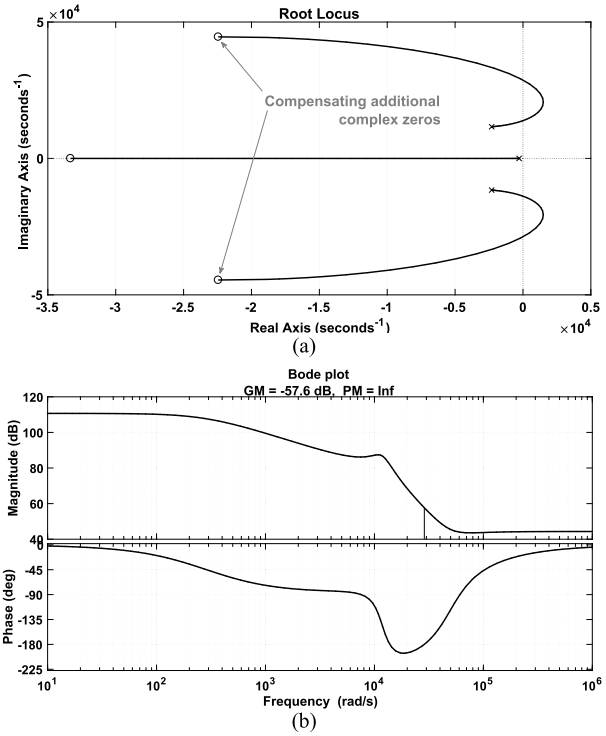

FIGURE 6. **(a) Root-locus of $G_{LCL}(s)$ compensated with zeros placed at $-22491 \pm j44531$; (b) Bode plot of $G_C(s) \times G_{LCL}(s)$ with $G_C(s)$ as per (18).**

b: COMPENSATOR DESIGN WITH COMPENSATING ZEROS

Let us consider the nominal filter system $G_{LCL}(s)$ described as per equation (6) and Table I. Let a complex conjugate zero pair is added at $-z_{1,2} = -22491 \pm j44531$ to the system to pull the root locus trajectories to the left half of s-plane. Clearly, the chosen zeros are positioned much deeper in the left half of s-plane than the $G_{LCL}(s)$ poles. The resulting root locus, obtained using MATLAB, is shown in Figure 6a. Using the root-locus given in Figure 6a let the closed loop pole locations are chosen as $p_{1,2} = (-2.24 \pm j4.4) \times 10^4$ and $p_3 = -2.72 \times 10^4$. The corresponding compensator is given as

$$G_C(s) = 5.49 \times 10^{-8} \left(s^2 + 4.49 \times 10^4 s + 2.49 \times 10^9 \right) \quad (18)$$

Consequently, $G_C(s)$ as per (18) ensures absolute stability because the closed-loop poles are located in the left half of s-plane.

With $G_C(s)$ as per (18), the Bode plot of $G_C(s) \times G_{LCL}(s)$ is given in Figure 6a. Although the compensator chosen from Figure 6a root locus ensures negative closed-loop poles and, therefore, stability of $G_C(s) \times G_{LCL}(s)$, the system lacks relative stability properties attributed to negative GM (Figure 6b). This is coupled with the fact that the root-locus partially crosses the right half s-plane and, consequently, the gain cannot be arbitrarily chosen without compromising the closed loop stability. The negative gain margin in this instant indicates that instability can be caused if the gain is attenuated. For example, the presence of a saturation block between $G_C(s)$ and $G_{LCL}(s)$ can act as a source of gain attenuation and, therefore, can compromise the system stability.

Now let us evaluate the performance of $G_C(s)$ as per (18) through time domain simulations. Let the control objective is to accurately track the grid-side current i_2 while ensuring that the performance specifications are met. Figure 7 shows the time response for step changes in grid current reference $i_{2,\text{ref}}$. Figure 7a shows the grid current i_2 response. For simulation, the grid current reference $i_{2,\text{ref}}$ undergoes step changes at 0.05 s (from 200A to 400A) and again at 0.1 s (from 400A to 40A). It is clear that the developed controller is proficient in delivering adequate tracking response despite sharp step changes in the reference. Figure 7b shows the corresponding duty cycle response that delivers the tracking accuracy. It can be seen that the commanded duty cycle undergoes large and sharp transients at the instants of step changes in $i_{2,\text{ref}}$ so as to apply adequate V_{dc} voltage to achieve the tracking performance.

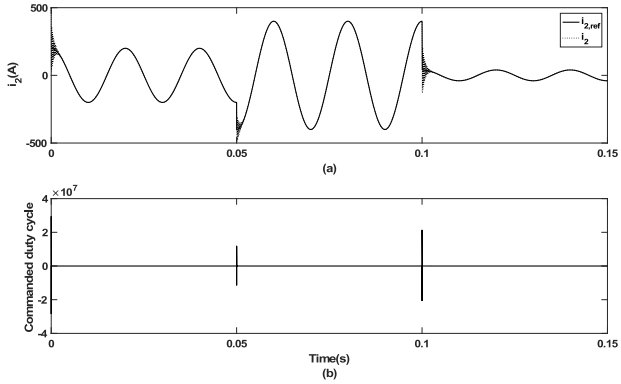

FIGURE 7. **Tracking response using (18) and without duty cycle saturation.**

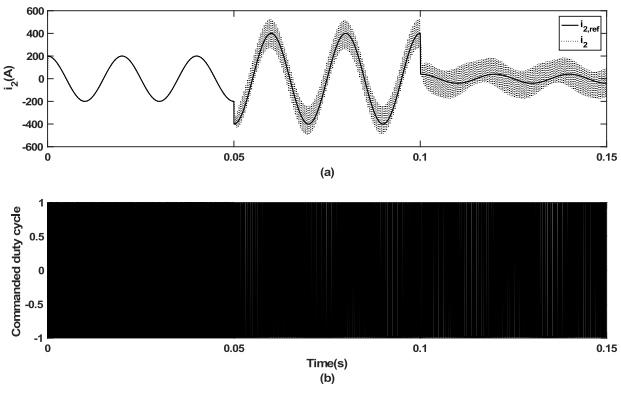

FIGURE 8. **Tracking response using (18) and with duty cycle saturation.**

In practical inverter systems the duty cycle is constrained to take values between -1 and $+1$. Therefore, commanded duty cycle response as per Figure 7b is practically unrealisable and will be clipped for values beyond -1 and $+1$. Figure 8 shows the response of the system with the same $G_C(s)$ as defined by (18) but with the duty cycle saturation block included

with saturation limits of -1 and $+1$. It is clear that upon step change in $i_{2,\text{ref}}$ the commanded and actual duty cycles (and, therefore, the applied V_{dc}) differ. In particular, the saturation block acts as a nonlinear block such as a source of gain attenuation. Although the designed compensator is stable but the negative gain margin makes this compensator susceptible to instability in the event of reduction/attenuation in gain caused by the duty cycle saturation. This is evident in Figure 8a which shows that following step changes in $i_{2,\text{ref}}$ the actual i_2 response becomes oscillatory.

Most existing literature on filter control design completely ignore the existence of duty cycle saturation phenomenon. As demonstrated through Figures 7 and 8, duty cycle saturation is unavoidable when $i_{2,\text{ref}}$ is subject to sudden and large changes. Therefore, any controller design with lack of consideration to duty cycle saturation is susceptible to instability and oscillations when implemented on practical inverters. It may further be noted that classical frequency domain based controller design methods are exclusively applicable to LTI systems, while the presence of saturation makes the otherwise LTI system a nonlinear system.

c: DESCRIBING FUNCTION ANALYSIS FOR LIMIT CYCLE PREDICTION

Figure 9 shows the describing function analysis (verification of condition (11)) with $G_C(s)$ as per (18). Figure 9b shows that Nyquist plots of $G_C\,(s) \times G_{LCL}\,(s)$ and $-1/\Psi(A)$ intersect. This indicates that the compensator without adequate stability margins is susceptible to limit cycles (oscillations). The point of intersection gives $-1/\Psi\,(A_0) \approx -120$. Therefore, using (9) the describing function method predicts the duty cycle amplitude at which sustained oscillations occur as approximately $A_0 = 200$. Figure 9c shows the zoomed-in view of Figure 7b that corresponds to the commanded duty cycle generated by $G_C(s)$ as per (18) without saturation. It is clear that describing function approximation is able to analytically verify the findings observed in simulations.

2) ADJUSTMENTS IN THE POSITIONING OF ZEROS TO ACCOUNT FOR THE DUTY CYCLE SATURATION CONSTRAINTS

As discussed in the previous section, adequate relative stability margins (GM and PM) are essential to ensure system stability in the face of unmodelled practical factors such as the duty cycle saturation. Accordingly, it is essential that zero locations be chosen in such a way to ensure that the root locus completely lies in the left half s-plane so that the gain can be arbitrarily chosen without compromising margins for stability. Besides saturation, another caveat concerning the controller design lies in the proper use of the Bode plot method. Since, the phase plot in this case is non-monotonic at frequencies before and after 180ř, direct reliance on GM and PM from Bode plots can lead to false stability guarantees [27]. This is particularly the case if the system gain is likely to be attenuated due to the presence of unmodelled factors such as duty cycle saturation.

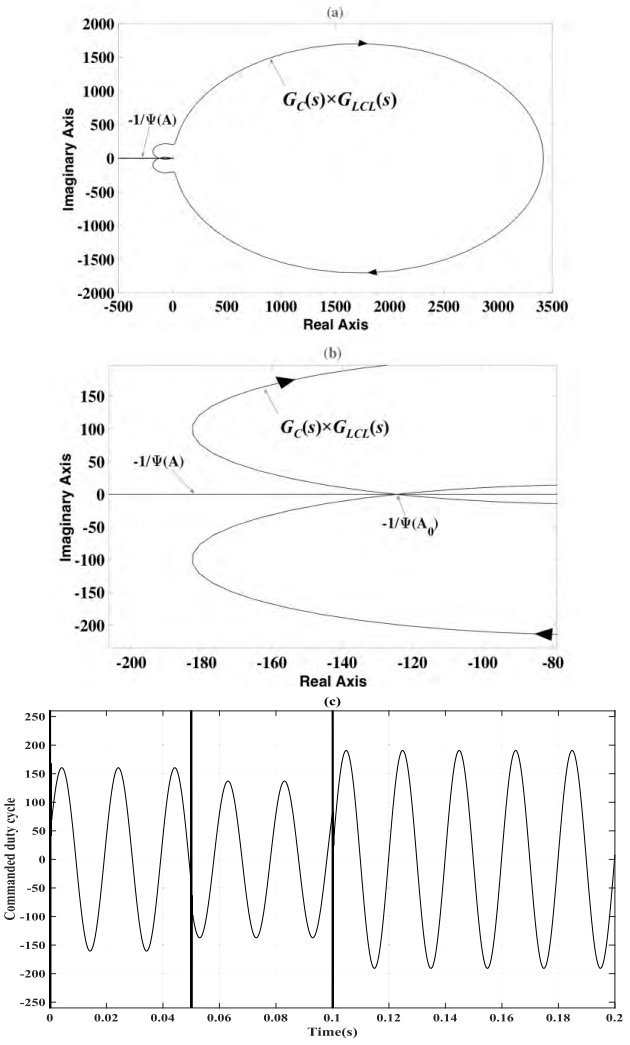

FIGURE 9. Describing function analysis with $G_C(s)$ as per (18). (a) Nyquist plots of $G_C\,(s) \times G_{LCL}\,(s)$ and $-1/\Psi(A)$; (b) zoomed-in view to show the point of intersection of $G_C\,(s) \times G_{LCL}\,(s)$ and $-1/\Psi(A)$; (c) zoomed-in view of the commanded duty cycle as per Figure 7b.

One way to overcome these issues is to place zeros in such a way that infinite GM and PM are obtained. Figure 10 shows an example of positioning zeros resulting in infinite GM and PM. Figure 10a shows the modified design for the same system as Figure 6 with zeros re-positioned such that the trajectories completely lie in the left half s-plane. This design allows any arbitrary choice of gain without transgressing into the right half plane and compromising closed loop stability. The corresponding Bode plot in Figure 10b confirms that infinite GM and PM are obtained. This design eliminates the problem of both negative gain margin as well as non-monotonicity of the phase margin plot which otherwise may render Bode analysis inadequate for the compensator design.

Using Figure 10, let the new compensator is selected as

$$G_C(s) = 1.39\times10^{-7}\left(s^2 + 7.517\times10^4 s + 1.607\times10^9\right) \quad (19)$$

The corresponding i_2 tracking responses, without and with duty cycle saturation active, are given in Figure 11.

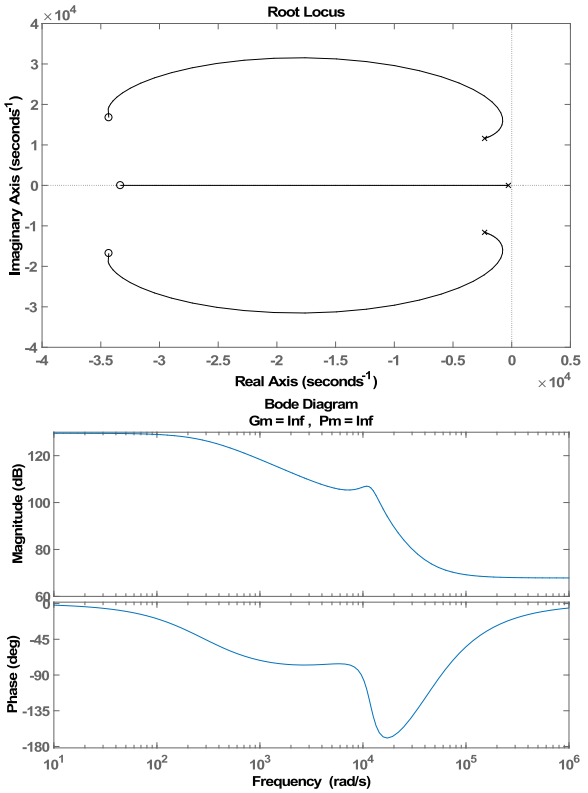

FIGURE 10. Re-positioning of complex zeros to obtain infinite GM and PM.

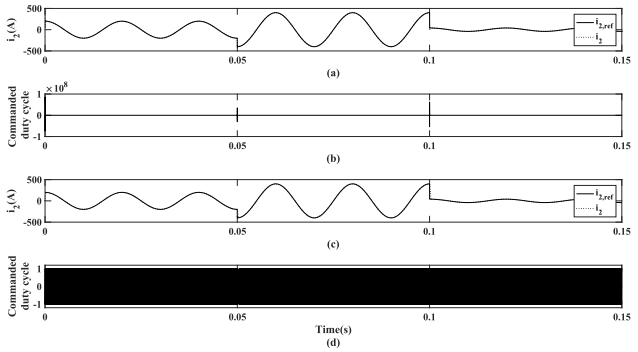

FIGURE 11. Response with $G_C(s)$ as per (19) characterised with sufficient stability margins (for $r_C = 0.6\ \Omega$): (a)-(b) without duty cycle saturation; (c)-(d) with duty cycle saturation.

Figures 11 (a) and (c) show the response of i_2 tracking without and with saturation. It can be seen that with adequate relative stability margins the responses are almost identical. With adequate relative stability margins the controller is able to withstand duty cycle saturation. It may be noted that saturation compromises the closed loop performance as guaranteed through the root locus and Bode design, nonetheless, this can be significantly mitigated through the choice of sufficiently large gain as seen in Figure 11.

Although the compensator design demonstrated through Figures 10 and 11 is for $r_C = 0.6\ \Omega$, similar compensators

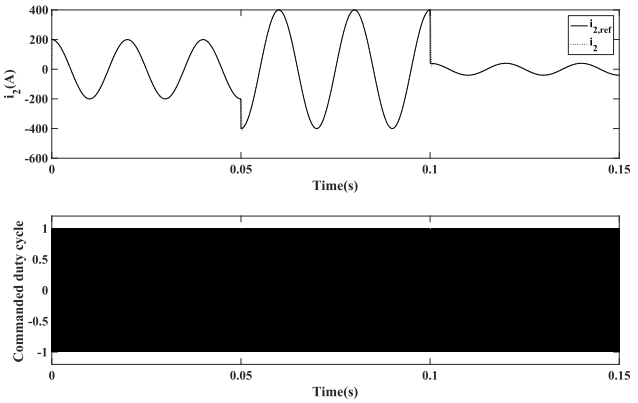

FIGURE 12. With duty cycle saturation response with compensator characterized with sufficient stability margins (for $r_C = 0.1\ \Omega$).

TABLE 3. Sample compensators ($G_c(s)$) for successively reduced r_C values that deliver infinite GM and PM.

r_C (Ω)	Compensator (with compensating complex zeros)
0.6	$K_{0.6} \times (s^2 + 7.517 \times 10^4 s + 1.607 \times 10^9)$
0.5	$K_{0.5} \times (s^2 + 7.77 \times 10^4 s + 1.704 \times 10^9)$
0.4	$K_{0.4} \times (s^2 + 6.043 \times 10^4 s + 1.035 \times 10^9)$
0.3	$K_{0.3} \times (s^2 + 4.201 \times 10^4 s + 6.478 \times 10^9)$
0.2	$K_{0.2} \times (s^2 + 3.608 \times 10^4 s + 4.213 \times 10^9)$
0.1	$K_{0.1} \times (s^2 + 1.817 \times 10^4 s + 2.349 \times 10^9)$

can be designed for any non-zero values of r_C to achieve infinite GM and PM margins. Table III presents sample expressions for the compensator $G_C(s)$ for successively reduced r_C values that deliver infinite GM and PM. It may be noted that in Table III all gain K's can be assigned any arbitrarily large gain value. Figure 12 shows the response for filter with r_C set at 0.1 Ω with duty cycle saturation active. When compared with the time domain response characteristics for $r_C = 0.1\ \Omega$ given in Table II (for proportional-only controller), it is clear with new compensator as per Table III the tracking response is significantly improved.

a: DESCRIBING FUNCTION ANALYSIS FOR LIMIT CYCLE PREDICTION

Figure 13 repeats the describing function analysis (verification of condition (11)) with $G_C(s)$ as per (19). In this case, the Nyquist plots of $G_C(s) \times G_{LCL}(s)$ and $-1/\Psi(A)$ do not intersect. This implies system stability with $G_C(s)$ as per (19). This analytically confirms that adequate GM and PM are required to ensure filter stability in presence of duty cycle constraints and saturation.

C. EFFECT OF NOISE ON DERIVATIVE CONTROL ACTION

The compensator developed in the previous section through the addition of zeros is inherently characterised with derivative control actions. As demonstrated in the previous section, such a control is capable to delivering acceptable performance under any noise free conditions even in the presence of duty cycle saturation. However, in practice presence of sensor noise is inevitable. Furthermore, the inverter filter is vulnerable to high frequency noise propagating from the AC

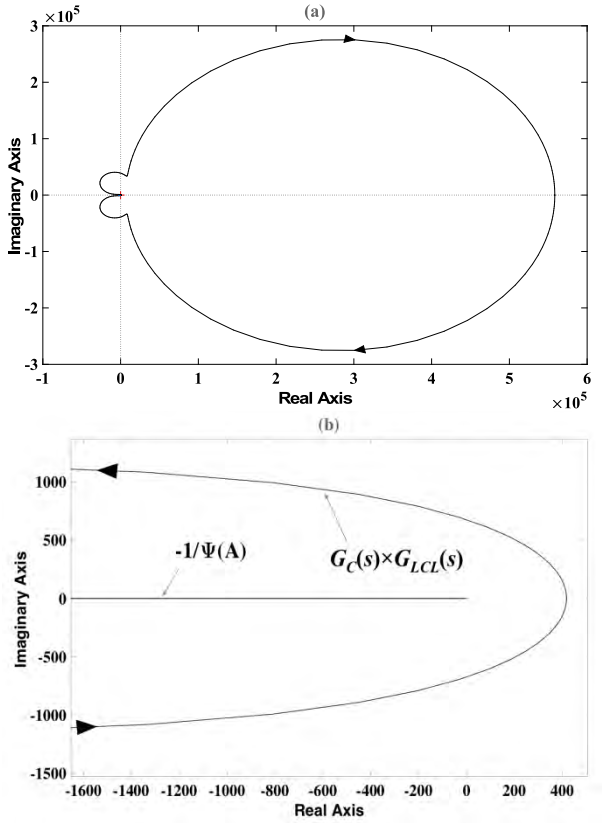

FIGURE 13. Describing function analysis with $G_C(s)$ as per (19). (a) Nyquist plots of $G_C(s) \times G_{LCL}(s)$ and $-1/\Psi(A)$; (b) zoomed-in view to show no intersection occurs between $G_C(s) \times G_{LCL}(s)$ and $-1/\Psi(A)$.

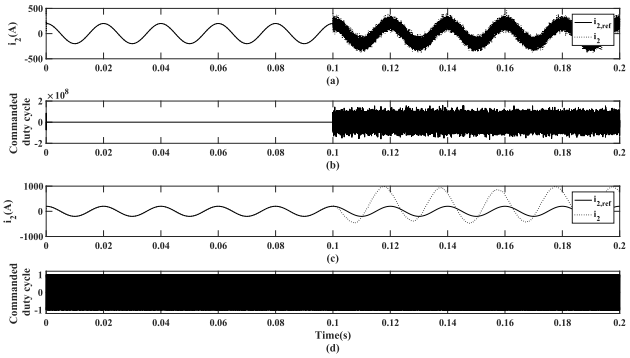

FIGURE 14. (a)-(b) without saturation; (c)-(d) with saturation. $i_{2,\text{ref}}$ set at 200A throughout, noise activated at $t = 0.1$s.

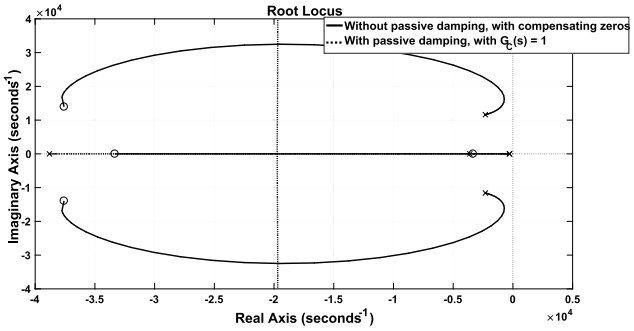

FIGURE 15. Root locus of uncompensated $G_{LCL}(s)$ with passive damping ($r_C = 6\ \Omega$).

grid-side. Consequently, the filter and the compensator are exposed to unmodelled noise effects. As discussed through (12)-(14), the derivative control actions are well known to result in significantly deteriorated performance even in the presence of random noise with relatively low peak power. This is because the derivative control action responds to the rapid changes in the error signal and, therefore, any fluctuations at the input of the derivative control gets amplified due to combined effect of derivative of rapid transients and high gain (as per (14)). Use of high gain is proposed for the compensator proposed in section 3.2 (obtained through the placement of additional compensating zeros) to obtained better transient performance. Figure 14 demonstrates the response when a moderate sensor noise is injected as the sensor noise at 0.1 seconds. It is clear that in presence of noise the tracking response gets significantly deteriorated regardless of the consideration of the saturation block. In practice, sensor measurements should be passed through an appropriate filter (e.g. Kalman filter) to mitigate the effects of noise.

D. COMPENSATOR DEVELOPMENT WITH PASSIVE DAMPING

One way to avoid the use of derivative control action and simplify the task of control system development is at the filter parameter selection level, whereby a large value of r_C is selected to obtain a *passively damped* filter configuration.

1) ANALYSIS WITH A PROPORTIONAL-ONLY CONTROLLER AND PASSIVE DAMPING WITHOUT MEASUREMENT NOISE AND DUTY CYCLE SATURATION

Figures 15 and 16 show the root locus and Bode plot of $G_C(s) \times G_{LCL}(s)$ with passive damping and $G_C(s) = 1$. Passive damping is achieved by selecting $r_C = 6\ \Omega$. For comparison plots for without passive damping (with $G_C(s)$ as per (19)) are also included. From Figure 15 it is clear that the root locus trajectories are entirely in the left half s-plane. This enables choice of any gain to design a proportional controller. Figure 16 shows that adequate relative stability margins are achieved even with a very straightforward choice of a compensator.

2) EFFECT OF DUTY CYCLE SATURATION

Having chosen$G_C(s) = 1$, the next task is to evaluate its time domain performance and the effect of duty cycle saturation without measurement noise. Figures 17(a)-(b) display the tracking performance without consideration of duty cycle saturation between -1 and $+1$. $i_{2,ref}$ is step changed at $t = 0.05s$ (from peak values of 200A to 400A) and again at $t = 0.1s$ (from peak values of 400A to 40A). Figure 17a shows that the proportional controller is capable of delivering acceptable

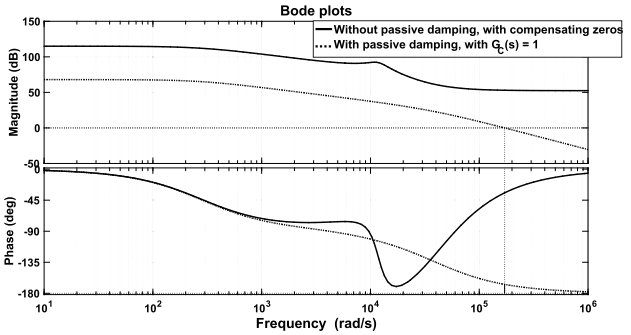

FIGURE 16. Bode plot of $G_C(s) \times G_{LCL}(s)$ with $r_C = 6\ \Omega$ and $G_C(s) = 1$ (chosen as a basic proportional controller).

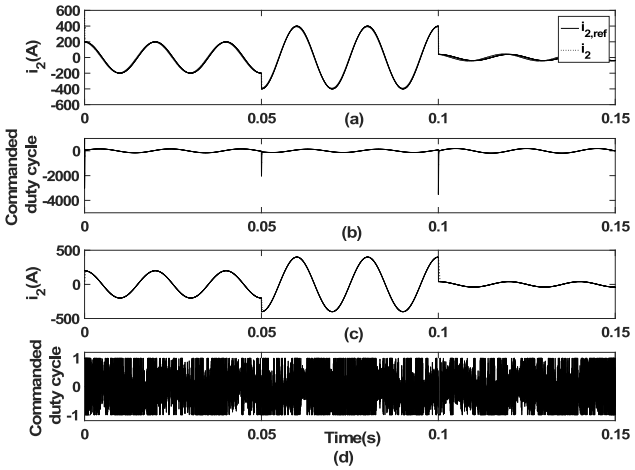

FIGURE 17. Responses with passive damping ($r_C = 6\ \Omega$) and basic proportional controller ($G_C(s) = 1$): (a)-(b) without duty cycle saturation; (c)-(d) with duty cycle saturation.

tracking performance. Figure 17b shows the corresponding commanded duty cycle to achieve the tracking performance of Figure 17a. It is clear that the commanded duty cycle violates the duty cycle constraints at the instant of step changes in $i_{2,ref}$. Figure 17c-d demonstrate the tracking performance of the same compensator with duty cycle saturation considered. It is clear that acceptable tracking performance is achieved even with duty cycle saturation. This can be attributed to infinite GM, which ensures control system stability even when the filter is subject to gain alterations caused by duty cycle saturation.

3) EFFECT OF DUTY CYCLE SATURATION AND MEASUREMENT NOISE

Figure 18 shows the tracking performance with $G_C(s) = 1$ in presence of duty cycle saturation and measurement noise. For simulations, $i_{2,ref}$ is step changed at $t = 0.05s$ followed by injection of noise $t = 0.1s$. To generate the noise signal, Simulink's bandlimited white noise block is used with the power of 0.01 and sampling time of 1μs.

It is clear from Figure 18 that with passively damped *LCL* filter, even a basic proportional controller (unity feedback)

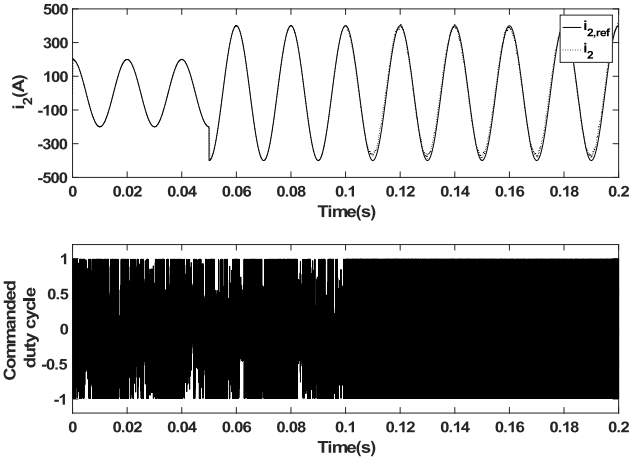

FIGURE 18. Response of passively damped LCL filter ($r_C = 6\ \Omega$) and a proportional controller ($G_C(s) = 1$) with duty cycle saturation and measurement noise activated at $t = 0.1s$.

is sufficient to deliver acceptable closed loop performance despite presence of unmodelled factors such as duty cycle saturation and measurement noise. Consequently, it can be concluded that passive damping significantly alleviates the task of compensator design and is less vulnerable to stability and performance challenges arising due to noise and duty cycle saturation. Nevertheless, due to efficiency loss reduction considerations it is highly desirable to reduce the r_C value to as low as possible without compromising closed loop performance which entails complex control system development. The inverter filter designer is faced with two conflicting choices, one is to use passive filter design, which simplifies the task of control system development, but results in higher losses and, therefore, lower efficiency. The second choice is to reduce r_C as low as possible and use compensator involving good stability margins through the use of derivative control actions but with increased susceptibility to noise and grid disturbances.

E. EFFECTS OF SAMPLED DATA CONTROL

The analysis so far assumes that the overall control system is completely in continuous-time. Nonetheless, most power electronic controllers are implemented digitally as sampled data control systems through the use of microcontrollers. Typical sampled data control architecture is shown in Figure 19. The error signal at the input terminals of controller block $G_C(s)$ is sampled at a chosen sampling period (T_S) and passed through a filtering mechanism to hold/freeze the sampled value for the duration of T_S. Zero-order hold (zoh) is the most common and simplest hold circuit which holds the value of the last received k^{th} sample between two consecutive samples kT_S and $(k+1)T_S$.

Since, the sample and hold incorporates a time-delay in the control loop the choice of T_S is critical in ascertaining the closed loop stability properties of the sampled data control loop. In order to evaluate the effect of sample and hold on

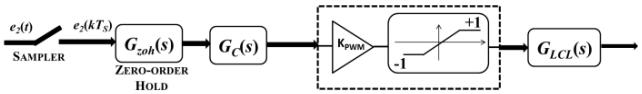

FIGURE 19. Sampled data control architecture including sampler and zero-order hold (S/H).

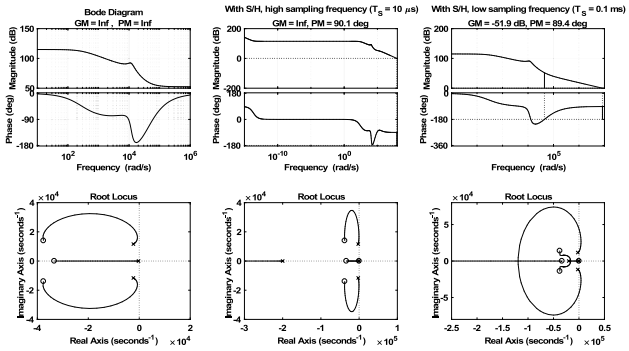

FIGURE 20. Analysis of without and with S/H ($r_C = 0.1\ \Omega$ and $G_C(s)$ as per (19)).

the closed loop stability the zoh transfer function needs to be considered. The transfer function for the zoh block can be derived as (see for [28] full derivation)

$$G_{zoh}(s) = \frac{1 - e^{-sT_S}}{sT_S} \tag{20}$$

Therefore, to analyse the effect of sampled data control system $G_{zoh}(s)$ must be taken into account along with $G_C(s) \times G_{LCL}(s)$. In order to focus on the effect of T_S on stability the saturation block is not considered in this section.

For analysis and design using classical techniques, an approximation of (20) is often used. Since (20) appears as a time-delay element in the closed loop, it can be approximated using a first-order *Padé* approximation obtained as follows:

$$e^{-sT_S} \approx \frac{1 - \frac{s}{2/T_S}}{1 + \frac{s}{2/T_S}} \underset{in(20)}{\overset{Substituting}{\Longrightarrow}} G_{zoh}(s) \approx \frac{\Delta_S}{s + \Delta_S}; \quad \Delta_S = \frac{2}{T_S} \tag{21}$$

Using (21) it can be concluded that the inclusion of sample and hold incorporates an additional open loop pole whose location is governed by the choice of T_S. Smaller the value of T_S (higher the sampling frequency) deeper the pole corresponding to sample and hold will be in the left half s-plane. Therefore, high sampling frequency is desirable so that the effect of sampling is minimal on the closed loop stability and dynamic performance. However, high sampling frequencies are limited due to hardware limits. In particular, in inverter PWM control the sampling frequency is limited from few MHz to as low as 10 kHz.

Figures 20 and 21 summarise the effect of S/H on LCL filters without and with passive damping respectively. High

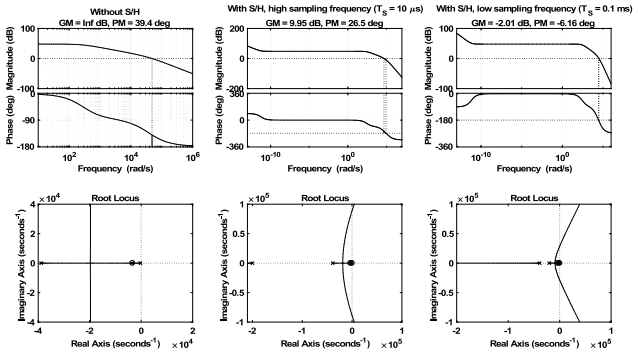

FIGURE 21. Analysis of without and with S/H ($r_C = 6\ \Omega$ (passive damping) and $G_C(s) = 0.1$).

sampling frequency ($T_S = 10\ \mu$s) and low sampling frequency ($T_S = 0.1$ ms) scenarios are considered to evaluate the effect of reducing sampling frequency. In particular, in Figure 20 $r_C = 0.6\ \Omega$ is used and $G_C(s)$ is taken as per (19). For high sampling frequency (e.g. corresponding to $T_S = 10\ \mu$s) the pole due to $G_{zoh}(s)$ is far inside the left half s-plane and, therefore, has minimal effect of filter dynamic properties. Furthermore, the stability margins remain high although there is some reduction in PM with respect to without S/H. On the other hand, as the sampling frequency is reduced (e.g. 10 kHz, $T_S = 0.1$ ms) the pole corresponding to $G_{zoh}(s)$ is very close to $G_{LCL}(s)$ poles and, therefore, influence the filter dynamics. It can be seen that low sampling frequency pushes the root locus trajectories partially to the right half s-plane. This reduces the flexibility in gain adjustment and makes the system susceptible to instability as the gain is increased. This is supported by Bode plot which shows the gain margin as negative indicating susceptibility to oscillations.

Figure 21 is obtained with $r_c = 6\ \Omega$ (passive damping) and a simple proportional controller, $G_C(s) = 0.1$. Inclusion of the pole corresponding to S/H bends the root locus trajectories to the right half s-plane. Lower the sampling frequency greater is the bending and, consequently, lower is the range of proportional gain adjustment without crossing to right half s-plane. Although reduced gain can ascertain stability even with low sampling frequency, the corresponding time domain performance will be compromised. Therefore, even with passive damping, to account for the deterioration in performance due to S/H a simple proportional controller is unlikely to be sufficient. Thus, a hybrid controller can be utilized based on a similar controller design approach and a suitable r_c resistor as a passive damping. This can improve the stability and robustness of a grid connected inverter in a practical application.

IV. CONCLUSION

This paper considers the problem of *LCL* filter design and control in modern power electronic inverters. An overview of *LCL* filter modelling is presented followed by a detailed discussion on a systematic approach to control system

development. Various practical considerations including duty cycle saturation, noise and sampled data control implementation are collectively considered. Passive damping method is also considered for comparison with the filter design approach (with very small resistors). Based on the analysis, some of the key noteworthy observations are as follows:

- The biggest purpose of this paper is to emphasise that during the filter control development all practical aspects of control system design, namely, (a) duty cycle saturation, (b) robustness to noise and (c) effects of S/H, must be collectively taken into account. As demonstrated in this paper, controller designs which consider these aspects in isolation are susceptible to being of limited practical utility.
- If the LCL filter is without significant resistors (passive damping), then the filter control system must be sufficiently sophisticated to ensure closed loop stability and performance. Basic proportional or conventional proportional-integral controllers are found to be inadequate. Inclusion of complex zeros for compensator design is found to be essential to pull the root locus trajectories to the left half s-plane. Nevertheless, compensator designed through the placement of complex zeros is highly susceptible to noise. This is because the associated derivative control action amplifies the noise levels resulting in deterioration in stability and performance. Therefore, additional noise filtering is essential that will entail additional cost.
- It is found that duty cycle saturation has a profound effect on the stability and performance of the grid connected inverter. Duty cycle saturation, though unavoidable in inverter applications, is often ignored in literature due to the inability of classical control design methods to explicitly take duty cycle saturation into account. It is found that duty cycle saturation can make the system unstable unless sufficiently large stability margins are ensured during the compensator design stage.
- Finally, the design sampled data control considerations are paramount especially when the inverters switching and sampling frequencies are in kHz range. Even a well-developed compensator may fail or yield unexpectedly poor performance in practical implementation due to the time-delay effects of sample and hold.

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