IEEE Access
Multidisciplinary | Rapid Review | Open Access Journal

Received March 10, 2017, accepted April 3, 2017, date of publication April 19, 2017, date of current version June 28, 2017.

Digital Object Identifier 10.1109/ACCESS.2017.2692765

Analysis and Design of Inductorless Wideband Low-Noise Amplifier With Noise Cancellation Technique

YIMING YU[1], KAI KANG[1], (Member, IEEE), YIMING FAN[2], CHENXI ZHAO[1], (Member, IEEE), HUIHUA LIU[1], YUNQIU WU[1], (Member, IEEE), YONG-LING BAN[1], (Member, IEEE), AND WEN-YAN YIN[3], (Fellow, IEEE)

[1]School of Electronic Engineering, University of Electronic Science and Technology of China, Chengdu 611731, China
[2]Department of Electrical and Computer Engineering, The Ohio State University, Columbus, OH 43221, USA
[3]College of Information Science and Electronic Engineering, Zhejiang University, Hangzhou 310027, China

Corresponding author: Kai Kang (kangkai@uestc.edu.cn)

This work was supported in part by the National Science Fund of China under Grant 61331006 and Grant 61422104, in part by the National Science and Technology Major Project of the Ministry of Science and Technology of China under Grant 2016ZX03001015-004, and in part by the National High Technology Research and Development Program of China under Grant 2015AA01A704 and Grant 2015AA7124068B.

ABSTRACT This paper deals with the fabrication of an inductorless wideband low-noise amplifier (LNA). The LNA includes two branches in parallel: a common-source (CS) path and a common-gate (CG) path. The CS path is responsible for providing enough power gain, while the CG path is used to achieve the input impedance matching. To eliminate the noise contribution of the CG path, the noise cancellation technique is applied. Therefore, the overall noise figure (NF) is improved. The phase mismatch between the two paths is also quantitatively analyzed to investigate its effect on gain and NF. The analytical results agree well with the simulation results. The LNA has been fabricated by a commercial 0.18-μm CMOS process. The measurement results show that the LNA has achieved a maximum gain of 14.5 dB with 1.7-GHz 3-dB gain bandwidth and a minimum NF of 3 dB. The tested input 1-dB gain compression point ($IP_{1\ dB}$) is -10.4 dBm at 1 GHz and the input third-order intercept point is 0.25 dBm. With 1.8-V supply, the LNA draws only 6-mA dc current.

INDEX TERMS Low-noise amplifier, inductorless, noise cancellation, phase mismatch, noise figure, CMOS, RFIC.

I. INTRODUCTION

The rapid development of wireless communication systems and wireless sensors for Internet of Things (IoT) has led to enormous increase in the demand for wideband low noise blocks, characterized by compactness of chip and low power consumption [1], [2]. To meet these requirements, inductorless structures for RF circuits have been widely studied in recent years in both academic and industrial fields.

Compared with the traditional RF circuits, having on-chip inductive devices, the inductorless RF circuits occupy much smaller chip area [3], [4]; however, the latter suffer from relatively high NF and low linearity. As a result, the devices, such as MOSFETs, resistors, etc., which are used to replace inductive devices, contribute high noise power, besides causing supply-voltage headroom issue. In [5], an inductorless LNA, with a tunable active shunt-feedback technique, has been presented [see Fig. 1 (a)]. It draws power consumption of 0.4 mW and occupies 0.0052 mm^2 chip area. But this comes at the expense of poor NF and IIP3, which are only 4.9 dB and -10 dBm, respectively. Belmas *et al.* [3] designed an inductorless Gm-boosted LNA [Fig. 1 (b)], which has lower power consumption and high voltage gain. However, the linearity of the circuit is limited and the IIP3 is only -13 dBm. Bruccoleri *et al.* [6] developed a resistive feedback noise cancellation technique for inductorless wideband LNAs design. With a feedforward path, it cancels thermal noise and distortions of the main transistors to achieve good NF and linearity. But the LNA consumes 35-mW dc power [6]. Based on CG-CS topology, as shown in Fig. 1 (c), several novel noise cancellation LNAs are also proposed to achieve low NF in [7]–[9]. However, they suffer from high power consumption or poor linearity.

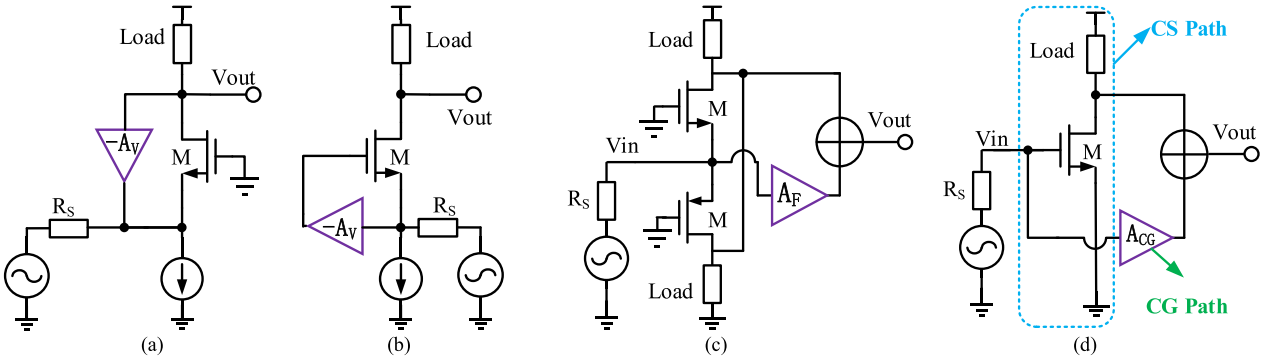


FIGURE 1. (a) Shunt-feedback LNA [5]. (b) Generic Gm-boost CG LNA [3]. (c) Simplified structure of noise cancellation LNA [7]. (d) The proposed LNA.

Chen and Liu [10] propose two gain-enhanced noise cancellation structures, they reduce the power consumption and increase the bandwidth. However, their gains are low, which are only 10.5 dB and 10.7 dB.

In this paper, the design and analysis of a CMOS low-noise amplifier, using a noise cancellation technique, are presented. The LNA proposed here includes a CG path and a CS path [see Fig. 1(d)]. To balance the gain, linearity and the power consumption, the CS path is used to provide enough power gain, while the CG path is applied to achieve the input impedance matching. The noise cancelling method is adopted to minimize the noise contribution of the CG path. Meanwhile, with the help of the active low-noise CG path, the gain and the overall NF are also further improved when compared with the CS path. It has been observed that the CG path has little effect on the linearity of the proposed LNA. Therefore, the bias voltage of the devices in the CG path is optimized to minimize its power consumption. The poles that the two paths of the noise cancellation LNAs go through introduce a phase mismatch between the two paths. This mismatch adversely impacts the noise cancellation and gain [11]. Therefore, its effect on gain and NF is also quantitatively analyzed in this paper.

The remainder of the paper is organized as follows: Section II presents the basic idea and systemic analysis of the proposed LNA; Section III presents the design and analysis of the circuit with considering the phase mismatch; Section IV presents the implementation and measurement results; Section V summarizes the conclusions drawn from this study.

II. BASIC IDEA AND SYSTEMIC ANALYSIS

A. BASIC IDEA

In inductorless LNAs, the CG amplifier suffers from more serious voltage and gain headroom issues than in the CS topology [see Fig. 2 (a)], because a current source or other is required for the CG amplifier to isolate RF signal flow into ground [see Fig. 2 (b)]. Therefore, the CS amplifier is adopted to design the primary gain path in this design. As shown in Fig. 2 (a), the CS amplifier needs additional devices to achieve input impedance matching, but passive

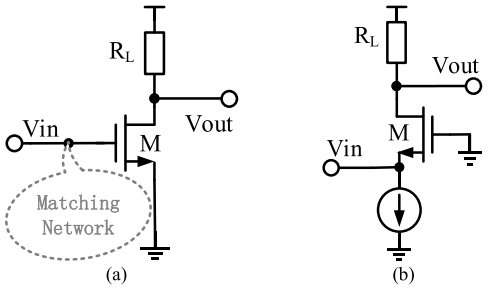


FIGURE 2. (a) Simplified common-source (CS) amplifier. (b) Simplified common-gate (CG) amplifier.

resistors or active devices will severely deteriorate the NF. Therefore, a 50-Ω input matching network without noise or with low noise contribution is required to achieve good noise performance for the inductorless LNAs based on the CS topology [12]. The CG topology is applied to provide the input matching, due to its natural advantage of adjusting input impedance. To minimize its noise contribution, a noise cancellation technique has been used for the CG amplifier. Thus, a low-noise inductorless matching network can be achieved for the CS amplifier.

B. SYSTEMIC ANALYSIS

For systemic analysis, the proposed structure is considered as two behavioral amplifiers that represent the two paths [see Fig. 3]. Using an adder, the output signals of the two paths can be aggregated. The total voltage gain (A_V^T) is equal to

$$A_V^T = A_V^{CS} + A_V^{CG}. \tag{1}$$

A_V^{CS} and A_V^{CG} are the gains of the CS and CG paths, respectively.

The noise factor of the CS amplifier can be calculated thus:

$$F_{CS} = 1 + \overline{v_{CS,n}^2} / \left(\overline{v_{S,n}^2} \left(A_V^{CS} \right)^2 \right), \tag{2}$$

where $\overline{v_{S,n}^2}$ and $\overline{v_{CS,n}^2}$ represent the noise power caused by the source resistance and the CS amplifier, respectively. When the CG path is noiseless, the total output noise ($\overline{v_{O,n}^2}$) is generated by the source resistance (Rs) and the CS amplifier.

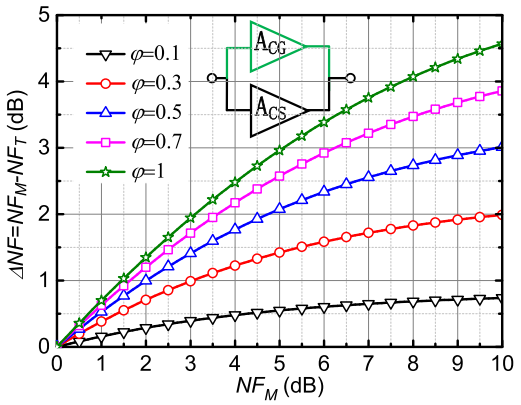


FIGURE 3. The NF improvement of the CS amplifier with the noiseless CG path compared with that of the CS amplifier.

Because the circuit's gain increases to A_V^T with the CG path, the noise power ($\overline{v_{O,n}^2}$) at the output node is amplified as:

$$\overline{v_{O,n}^2} = \overline{v_{S,n}^2}\left(A_V^T\right)^2 + \overline{v_{CS,n}^2}. \tag{3}$$

Based on (3), the overall noise factor is calculated thus:

$$F_T = \frac{\overline{v_{O,n}^2}}{\overline{v_{S,n}^2}\left(A_V^T\right)^2} = 1 + \frac{\overline{v_{CS,n}^2}}{\overline{v_{S,n}^2}}\frac{1}{(A_V^{CS} + A_V^{CG})^2}. \tag{4}$$

Compared with F_{CS}, F_T has significantly decreased, and the ratio between F_T and F_{CS} can be derived thus:

$$\frac{F_T - 1}{F_{CS} - 1} = \frac{1}{(1+\varphi)^2}, \tag{5}$$

where $\varphi = A_V^{CG}/A_V^{CS}$. From (5), it can be inferred that the CG path not only provides the input impedance matching, but also reduces the NF, and that the reduction of the NF is related to φ. Fig. 3 shows the relationship of the NF reduction ($\Delta NF = log_{10}F_{CS} - log_{10}F_T$) versus NF_{CS} ($NF_{CS} = log_{10}F_{CS}$) and φ. From this figure, it can be seen that the bigger φ, the larger would be ΔNF. ΔNF also increases with increase in the NF of the CS path. This indicates that noiseless or low-noise active matching network is very useful for the inductorless LNAs in achieving good noise performance, whose primary gain amplifiers suffer from high NF.

III. DESIGN AND ANALYSIS OF THE PROPOSED LNA

A. DESIGN OF THE PROPOSED LNA

1) CS PATH

As shown in Fig. 4, the CS path is realized by a two-stage CS amplifier. The first stage comprises a transistor M_1 and a resistor R_1. The second stage, consisting of M_2 and M_3, functions as the output stage. To drive 50-Ω load of measurement equipment, the size of M_3 has been so optimized as to achieve nearly 20 mS g_{m3}. The small signal model is shown in Fig. 5. Ignoring the parasitic capacitors (C_{gs}, C_{gd}, *etc.*) of the transistors and assuming the input impedance (Z_{in}) is matched

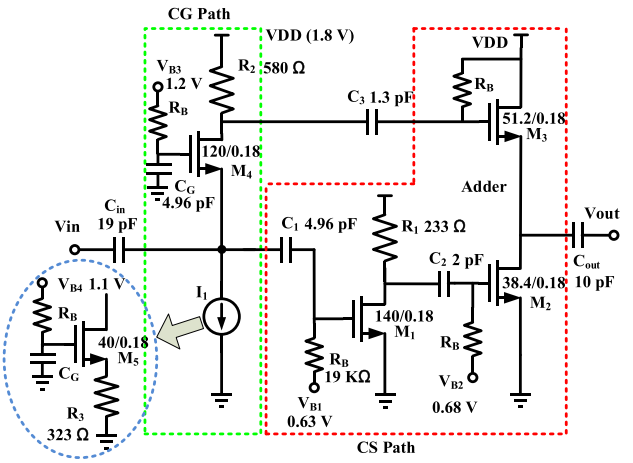


FIGURE 4. The schematic of the low noise amplifier, based on the noise cancellation technique (note: the unit of transistor size is μm).

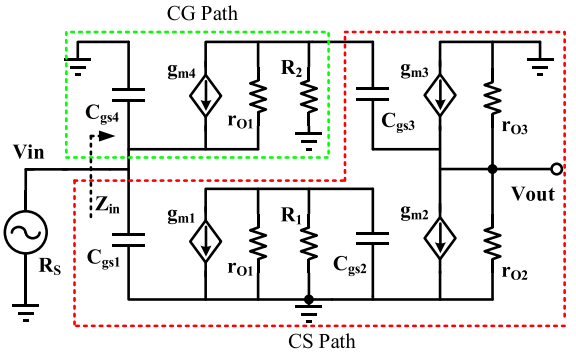


FIGURE 5. Equivalent small signal model of the proposed LNA.

with R_S, the CS path's voltage gain is given by

$$A_V^{CS} \approx \frac{1}{2}g_{m1}R_1\frac{g_{m2}}{g_{m3}}, \tag{6}$$

g_{mi} denotes the transconductance of transistor M_i.

2) CG PATH

As depicted in Fig. 4, the CG amplifier which consists of M_4, R_2, and a dc current source I_1 is adopted to design the CG path for achieving the input impedance matching. The input impedance of the circuit is dominated mainly by the transconductance of M_4 (g_{m4}). Hence, g_{m4} of around 20 mS has been chosen to match with R_S. According to the small signal model shown in Fig. 5, the voltage gain of the CG path with the adder is deduced thus:

$$A_V^{CG} \approx \frac{1}{2}g_{m4}\beta R_2. \tag{7}$$

β is the signal transfer function from the gate of M_3 to the source of M_3 and is given by

$$\beta = \frac{g_{m3}(r_{O2}\|r_{O3})}{1 + g_{m3}(r_{O2}\|r_{O3})}, \tag{8}$$

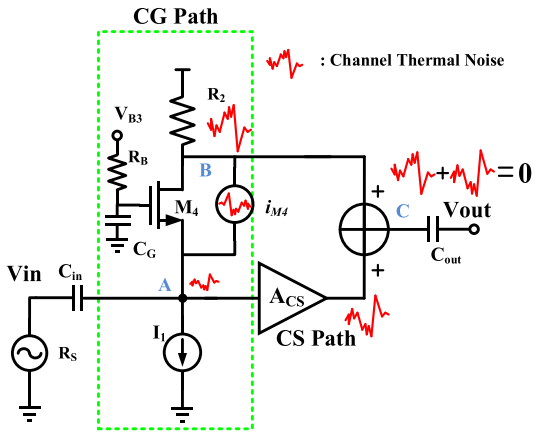


FIGURE 6. The principle of channel noise cancellation for M_4.

where r_{Oi} means the drain output impedance of transistor M_i. In fact, $g_{m3}(r_{O2}\|r_{O3}) \gg 1$ for the used CMOS technology and β is approximately equal to 1.

Unlike the input matching networks associated with inductors or transmission lines, the active devices generate lots of noise power. Therefore, a noise cancellation scheme is implemented to reduce the noise of M_4 ($\overline{i_{M4}^2}$) which is the foremost noise generator in the CG path. As illustrated in Fig. 6, $\overline{i_{M4}^2}$ causes two instantaneous voltage responses, one each at nodes A and B, with opposite signs, as shown below:

$$v_{A,M4} = i_{M4}(Z_{in}\|R_S) \approx i_{M4}\frac{1}{2g_{m4}}, \tag{9}$$

$$v_{B,M4} = -i_{M4}\,(1 - g_{m4}R_s/2)\,R_2. \tag{10}$$

The noise voltage at node A ($v_{A,M4}$) is amplified by the CS path. At the output node C, the noise voltage transferred by $v_{A,M4}$ is given by

$$v_{A,M4}^o = 2A_V^{CS}v_{A,M4} = i_{M4}A_V^{CS}/g_{m4}. \tag{11}$$

Considering the phase mismatch between the CG and CS paths ($\Delta\theta$), the output noise voltage transferred by $v_{B,M4}$ is revised thus:

$$v_{B,M4}^o = \beta v_{B,M4}e^{j\Delta\theta} = -i_{M4}\left(1 - \frac{g_{m4}R_s}{2}\right)\beta R_2 e^{j\Delta\theta}. \tag{12}$$

At the output node C, the total noise voltage generated by M_4 is calculated thus:

$$\begin{aligned} v_{C,M4} &= v_{A,M4}^o + v_{B,M4}^o \\ &= i_{M4}[\frac{A_V^{CS}}{g_{m4}} - \left(1 - \frac{g_{m4}R_s}{2}\right)\beta R_2 e^{j\Delta\theta}]. \end{aligned} \tag{13}$$

To minimize the noise contribution of M_4, the circuit needs to be satisfied thus:

$$\left(1 - \frac{g_{m4}R_s}{2}\right)\beta R_2\cos(\Delta\theta) = \frac{1}{g_{m4}}A_V^{CS}. \tag{14}$$

As already mentioned, $g_{m4} = 1/R_S$. Substituting (14) for (7), the relationship between A_V^{CS} and A_V^{CG} for the optimal noise cancelation is obtained by

$$\left|A_V^{CG}\right| = \frac{1}{\cos(\Delta\theta)}\left|A_V^{CS}\right|. \tag{15}$$

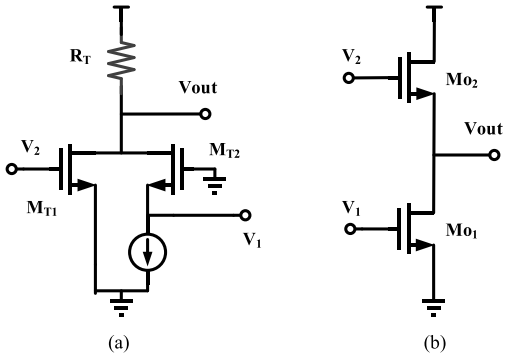


FIGURE 7. Adders: (a) Type I with two shunt current branches; (b) Type II with one current branch.

3) ADDER

Two types of adders can be applied to aggregate the signals and the noises of the two paths, as shown in Fig. 7. Type I adder has two shunt current branches with one common load, while Type II adder has one current branch. Therefore, Type I adder has more freedom to control the ratio of the voltage gains between the two active paths by independently adjusting the transconductances of M_{T1} and M_{T2}. However, this entails more power consumption. Since Type II adder has fewer devices, its noise performance in ordinary cases is better than that of Type I. In addition, the noise of M_{O2} can be degraded by M_{O1} in Type II [12]. Hence, Type II has been chosen to realize the adder in this design. As depicted in Fig. 4, Type II adder reuses the second stage of the CS amplifier.

With the adder, the CS and CG paths have been aggregated. Considering the phase mismatch between the two paths, the overall voltage gain is revised as:

$$A_V^T = A_V^{CS} + A_V^{CG}(\Delta\theta) = \frac{1}{2}\left(g_{m1}R_1\frac{g_{m2}}{g_{m3}} + g_{m4}\beta R_2 e^{j\Delta\theta}\right). \tag{16}$$

To achieve optimally cancel the noise power of M_4, the ratio of A_V^{CS} and A_V^{CS} (φ) can be calculated thus:

$$\varphi = A_V^{CG}/A_V^{CS} = 1 + j\tan(\Delta\theta). \tag{17}$$

B. NOISE FIGURE WITH PHASE MISMATCH

To inspect the NF, a simplified schematic with noise sources has been built, as shown in Fig. 8. The expressions of MOS transistors' and resistors' thermal noises are given by [13], as shown below:

$$\overline{i_{Mi}^2} = 4kT(\gamma_i/\alpha_i)g_{mi}\Delta f, \tag{18}$$

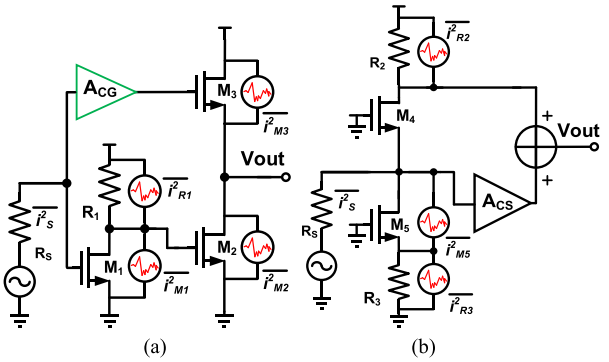


FIGURE 8. Simplified circuit of the proposed LNA with noise sources. (a) The CS amplifier, (b) the CG amplifier.

$$\overline{i_{Ri}^2} = 4kTR_i^{-1}\Delta f, \tag{19}$$

where γ_i is the coefficient of the channel thermal noise of M_i, $\alpha_i = g_{mi}/g_{d0i}$, and g_{d0i} is the zero-bias drain conductance of M_i. As shown in Fig. 8 (a), the noise factor of the CS path is derived as:

$$F_{CS} \approx 1 + \frac{1/R_1 + g_{m1}(\gamma/\alpha)}{g_{m1}^2 R_S} + \frac{(g_{m2} + g_{m3})(\gamma/\alpha)}{g_{m1}^2 g_{m2}^2 R_1^2 R_S}. \tag{20}$$

Thanks to the noise cancellation technique, the noise power of M_4 is minimized at the output terminal, because of which the CG amplifier has low noise contribution to the overall NF. Substituting (17) into (5), the ideal overall noise factor ($F_{T,I}$), without considering the noise contribution of the CG path, can be derived as thus:

$$F_{T,I} = \frac{3}{4 + \tan^2(\Delta\theta)} + \frac{1}{4 + \tan^2(\Delta\theta)} F_{CS}. \tag{21}$$

In (21), the improvement of the noise factor is mainly due to the enhancement in the overall gain with the CG path. However, the noise power of M_4 cannot be completely cancelled, because of the phase mismatch. Besides, the devices, including R_2, M_5, and R_3 in the CG amplifier, will also contribute some noise to the whole circuit. According to Fig. 8 (b), the noise factor contributed by M_4, M_5, R_2, and R_3 can be obtained thus:

$$\begin{aligned}\Delta F_{CG} \approx{}& \frac{\tan^2(\Delta\theta)}{4 + \tan^2(\Delta\theta)} \frac{(\gamma/\alpha)}{g_{m4} R_S} + \frac{1/\cos^2(\Delta\theta)}{4 + \tan^2(\Delta\theta)} \frac{1/R_2}{g_{m4}^2 R_S} \\ &+ \left(\frac{\gamma}{\alpha}\right) g_{m5} R_S \left[\frac{1/g_{m5}}{1/g_{m5} + R_3}\right]^2 \\ &+ \frac{g_{m5}^2 \left(\frac{1}{g_{m5}} \| R_3\right)^2 R_S}{R_3}.\end{aligned} \tag{22}$$

In this design, g_{m5} and R_3 have been carefully optimized by SPECTRE simulation to minimize their noise contribution, which are about 10 mS and 323 Ω, respectively. Considering the phase mismatch, the overall noise factor $F_{T,F}$ of the LNA can be calculated follows:

$$F_{T,F} = F_{T,I} + \Delta F_{CG}. \tag{23}$$

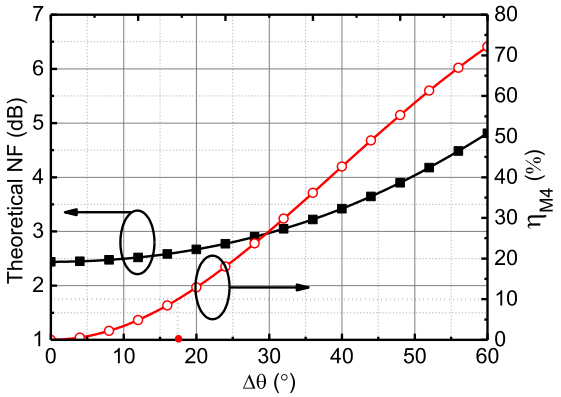


FIGURE 9. Theoretical NF and η_{M4} versus the phase mismatch ($\Delta\theta$) between the two paths ($\gamma = 2.5$, $\alpha = 0.8$) [14].

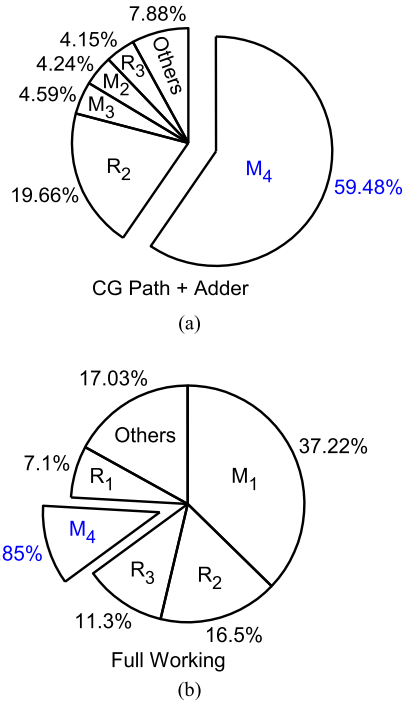


FIGURE 10. The simulated noise contribution summary in the single CG path mode at 1.5 GHz (CG path with adder working); (b) simulated noise contribution summary of the LNA in full working mode at 1.5 GHz.

From (23) and Fig. 9, it can be seen that the overall NF (NF $= 10\log_{10} F_{T,F}$) increases with increase in $\Delta\theta$. To quantitatively investigate the influence of $\Delta\theta$, the noise contribution percentage of M_4 (η_{M4}) is defined thus:

$$\eta_{M4}(\Delta\theta) = \frac{\tan^2(\Delta\theta)}{4 + \tan^2(\Delta\theta)} \frac{(\gamma/\alpha)}{g_{m4} R_S} / \left(F_{T,F} - 1\right). \tag{24}$$

According to Fig. 9, η_{M4} is less than 10% when $\Delta\theta < 17.5°$, but it rapidly increases with further increase in $\Delta\theta$. Based on (24) and Fig. 9, it can be generalized that the phase mismatch between the two paths has serious effect on the implementation of noise cancellation.

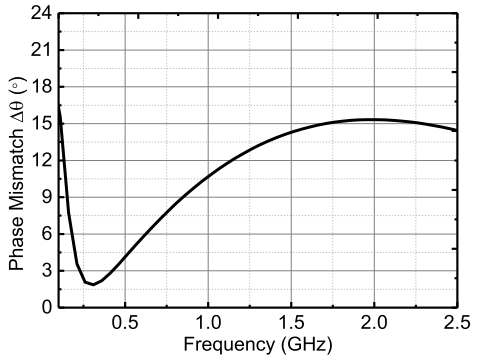


FIGURE 11. Simulated phase mismatch ($\Delta\theta$) between the CS and CG paths.

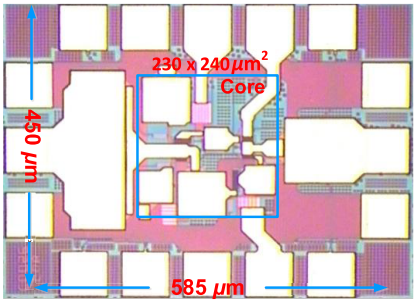


FIGURE 12. Chip micrograph of the LNA.

C. NOISE SIMULATION AND VERIFICATION

To evaluate the performance of noise cancellation technique in this design, the summary of the noise contributions of the devices has been obtained by post-layout simulation, which is presented in Fig. 10. In the CG amplifier with the adder, M_4 contributes nearly 60% noise power at 1.5 GHz [see Fig. 10 (b)], which is about three times that of the second biggest noise contributor R_2. After turning on the CS path ($V_{B1} = 630$ mV), the percentage of M_4's noise contribution to the whole circuit has decreased to 10.85% at 1.5 GHz, which is much smaller than that of R_2 [see Fig. 10 (b)]. Therefore, it can be inferred that the noise cancellation technique cancels most of M_4's noise power.

Even so, M_4 still contributes nearly 10.85% noise power to the whole circuit. To verify whether the noise contribution of M_4 is caused by the phase mismatch or not, $\Delta\theta$ has been obtained by the post-layout simulation, whose outcome is shown in Fig. 11. $\Delta\theta$ ranges from 2° to 15.5° at 0.1∼2.5 GHz, whereas it is 14.3° at 1.5 GHz. According to Fig. 9, the theoretical noise contribution of M_4 (η_{M4}) is about 6.8% when $\Delta\theta$ is 14.3°. It is close to the simulated value (10.85%). It can therefore be inferred that the noise contribution of M_4 is caused mainly by $\Delta\theta$ (vide the analysis in Part B of Section III). Three probable reasons can be cited to explain why the theoretical value of η_{M4} is less than the simulated one. The first reason is that, in this design, the voltage gain ratio of the CS and CG paths (φ) deviates a little from the normal. The second one is that the noise analysis considers only the channel thermal noise, ignoring other noises, like flicker noise, parasitic resistance noises etc. The third one is the empirical values of γ and α, which are 2.5 and 0.8 [14]. These values may not be accurate enough for the CMOS technology used. However, it may be stated that, in general, the analysis of the phase mismatch reliably estimates the performance of noise cancellation LNAs.

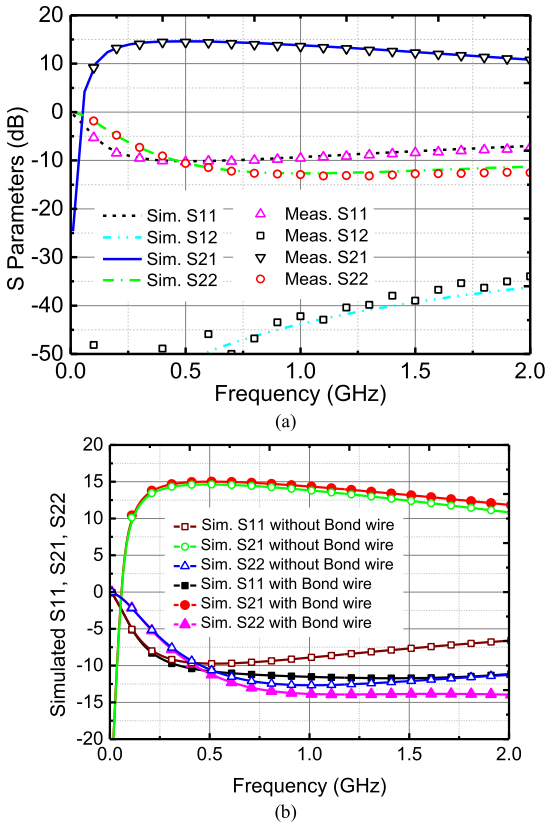


FIGURE 13. (a) On-chip Measured (symbol) and post-simulation (line) S parameters of the proposed LNA. (b) Post-layout simulated S_{11}, S_{21}, S_{22} with and without bond wires.

IV. IMPLEMENTATION AND MEASUREMENT

The proposed inductorless wideband LNA has been designed and fabricated following commercial 0.18-μm CMOS technology. In this design, small inter-stage dc-isolation capacitors have been used to obtain a compact chip size at the expense of the bandwidth and the gain. The two-stage CS path consumes 4.8 mA dc current under 1.8-V supply. The dc current of the CG path is only 1.2 mA with the same supply voltage. The chip micrograph is shown in Fig. 12. It occupies an area of 585 × 450 μm^2, while the core of the circuit, with passive inter-stage capacitors, is only 230 × 240 μm^2 in area.

As shown in Fig. 12, the chip has been mounted on a printed circuit board (PCB). The S-parameters of the LNA have been measured using Agilent Vector Network Analyzer N5247A. The NF has been measured with Agilent Noise Figure Analyzer N8975A and Agilent Noise Source 346C.

The measured two-port S parameters, shown in Fig. 13 (a), agree well with the simulation results. The measured maximum gain is 14.5 dB. A 3-dB gain bandwidth of 1.7 GHz

TABLE 1. Performance summary and comparison.

	Technology	Technique	$BW_{3\text{-}dB}$ (GHz)	NF (dB)	Peak Gain (dB)	IIP3 (dBm)	P_{DC} (mW) (VDD)	S_{11} (dB)	Size (mm^2)	*NO. of Inductor*	*FoM*
TMTT'10 [15]	0.18-μm CMOS	Dual Negative Feedback	1.05~3.05	2.57#	16.9 V	-0.7	12.6 (1.8 V)	<-11*	0.073	4O	12 V
TMTT'12 [16]	0.13-μm CMOS	Feedback	0.1 ~ 2.0	3.8#	7.6	0.5	3 (1.2 V)	<-10*	0.075	0	6.9
TMTT'16 [5]	0.13-μm CMOS	Tunable Active Shunt-Feedback	0.1~2.2	4.9~6	12.3	-11.5~-9.5	0.4 (1 V)	<-9	0.0052	0	8.9V
JSSC'07 [17]	0.13-μm CMOS	Noise Canceling	1.2-11.9	4.5~5.1	9.7	-6.2	29 1.8 V	<-11*	0.59&	5	-9
JSSC'08 [7]	65-nm CMOS	Noise Canceling	0.2~5.2	<3.5	15.6V	>0	21 (1.2 V)	<-10	0.009	0	13
TCAS Ⅰ' 10 [11]	0.13-μm CMOS	Noise Canceling	0.2~3.8	2.8~3.4	19 V	-4.2	5.7 (1 V)	<-9	0.025	0	22 V
MWCL'14 [18]	0.18-μm CMOS	Shunt feedback	0~1.4	3.0#	16.4	-13.3	12.8 (1.2 V)	<-10	0.038	0	-9.2
IMS'13 [21]	0.18-μm CMOS	Dual Feedback	DC~5	2.76#	13.9	-14	10.4	<-10	0.45&	2	-5.9
This Work	**0.18-μm CMOS**	Noise Canceling	**0.1~1.8**	**3.0~3.8**	**14.5**	**0.25**	**10.8 (1.8 V)**	**<-7.8**	**0.055**	**0**	**9.5**

* Estimated from the curves; # Min. NF; & Including pads; V Voltage gain de-embedded output buffer; O off-chip indcutors; S Simulated result.

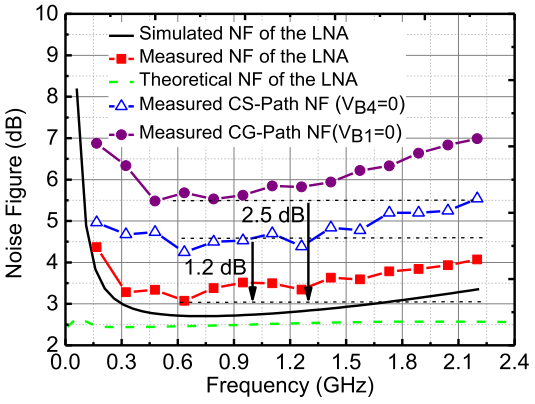


FIGURE 14. Simulated and measured NF. The NFs of the CS and CG paths are measured by setting $V_{B4} = 0$ and $V_{B1} = 0$, respectively.

from 100 MHz to 1.8 GHz has been achieved. In the operating bandwidth, the S_{11} and S_{22} are smaller than -7.8 dB and -9 dB, respectively. The parasitic capacitors of M_1 and M_4 degrade the input return loss and the output return loss. However, they can be neutralized by bond wires in application. As shown in Fig. 13 (b), the post-layout simulated S_{11} and S_{22} with the bond wires are smaller than -10 dB in the whole 3-dB gain bandwidth.

Fig. 14 shows the measured NF of the LNA, which varies from 3.0 dB at 630 MHz to 3.8 dB at 1.8 GHz. Considering the simulated $\Delta\theta$ [see Fig. 11], the theoretical NF is calculated by (23), and is found to be close to simulated NF [see Fig. 14]. The measured NF has increased by about 0.4 dB, as compared to the simulated one. This is possibly because of the deviation of measurement and the lack of precise PDK noise model. According to Fig. 14, the measured NF in the full working mode has decreased by about 1.2 dB, as compared to that of the single CS-path mode at 0.63 GHz ($V_{B4} = 0$). The NF of the CG path has also been tested by turning off the CS path ($V_{B1} = 0$ V), as shown in Fig. 14. Compared with the single CG-path mode, the measured NF of the full working mode also has decreased by about 2.5 dB in the operating frequency band. This indicates that the noise power of M_4 has been effectively eliminated by the noise cancellation technique. They match with the theoretical analysis results, presented Sections II and III.

The IP_{1dB} has been tested to examine the linearity of the LNA. As shown in Fig. 15, the IP_{1dB} of -10.4 dBm has been achieved at 1 GHz. Compared with the single CG-path mode, the IP_{1dB} of the full working mode has increased by about 9 dBm.

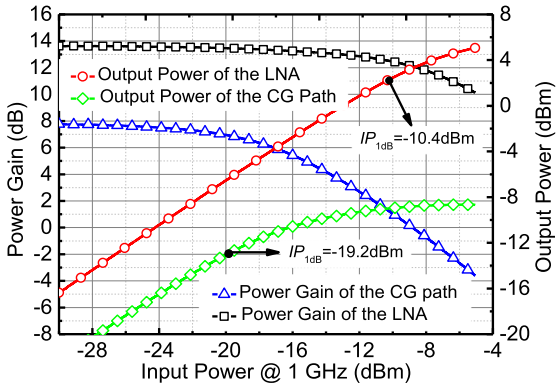


FIGURE 15. Measured LNA's IP_{1dB} and the CG path's input IP_{1dB} ($V_{B1} = 0$ V).

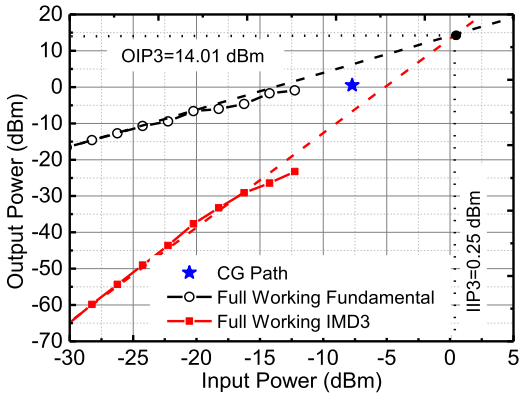


FIGURE 16. Measured third-order intercept points of LNA; the IIP3 of the single CG path mode is −7.72 dBm.

The IIP3 of the proposed LNA has also been measured. The two tone frequencies for the measurement are 1 GHz and 1.01 GHz. As presented in Fig. 6, the IIP3 is 0.25 dBm. The IIP3 of the single CG-path mode has been tested and is found to be −7.72 dBm. It is much lower than that of the full working mode.

According to the measurement results shown in Figs. 15 & 16, both the overall IP_{1dB} and IIP3 of the LNA are much better than the ones obtained by turning off the CS path. Therefore, it can be inferred that the CG path has little influence to the overall linearity and it can be implemented with drawing low dc power consumption. Moreover, the high-order distortions in the CS path can be cancelled to some extent with the CG path. The linearity of the proposed LNA is further improved because of the noise cancellation technique [8], [19], [20].

The chip performance is summarized and compared with that of the state-of-art LNAs, presented in Table 1. According to [5], the figure-of-merit (*FoM*) is defined by

$$FoM = 20\log_{10}\left(\frac{IIP3[mW]G_{av.}[lin]Bandwidth[GHz]}{P_{DC}[mW](F_{av.}[lin]-1)}\right), \tag{25}$$

where $G_{av.}$ and $F_{av.}$ denote the average power gain and the average noise factor of LNAs, respectively.

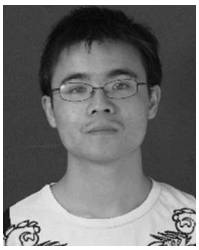
V. CONCLUSION

This paper presents the design and fabrication of a wide-band inductorless LNA with the noise cancellation technique. It comprises a CS path and a CG path. The CS path is applied to provide enough gain for the LNA. The CG path, with the noise cancellation technique, is designed to achieve low noise input impedance matching. Because of the low noise CG path, not only the LNA's gain has increased, but also the overall NF and linearity have improved, and that too by consuming low dc power. The phase mismatch between the CS and CG paths has also been analyzed, particularly its effect on the NF. The results of theoretical analysis have been validated by the simulation results. The measurement results show that the circuit achieves a maximum gain of 14.5 dB with a bandwidth of 1.7 GHz. The tested NF is 3.0∼3.8 dB across 3-dB gain bandwidth. Compared with the single CS- and CG-path modes, the measured overall NF has improved by 1.2 dB and 2.5 dB, respectively. The tested IP_{1dB} and IIP3 of the LNA are −10.4 dBm and 0.25 dBm, respectively.

REFERENCES

[1] J. Kim and J. Silva-Martinez, "Low-power, low-cost CMOS direct-conversion receiver front-end for multistandard applications," *IEEE J. Solid-State Circuits*, vol. 48, no. 9, pp. 2090–2103, Sep. 2013.
[2] M.-T. Lai and H.-W. Tsao, "Ultra-low-power cascaded CMOS LNA with positive feedback and bias optimization," *IEEE Trans. Microw. Theory Techn.*, vol. 61, no. 5, pp. 1934–1945, May 2013.
[3] F. Belmas, F. Hameau, and J.-M. Fournier, "A low power inductorless LNA with double G_m enhancement in 130 nm CMOS," *IEEE J. Solid-State Circuits*, vol. 47, no. 5, pp. 1094–1103, May 2012.
[4] E. A. Sobhy, A. A. Helmy, S. Hoyos, K. Entesari, E. Sanchez-Sinencio, "A 2.8-mW sub-2-dB noise-figure inductorless wideband CMOS LNA employing multiple feedback," *IEEE Trans. Microw. Theory Techn.*, vol. 59, no. 12, pp. 3154–3161, Dec. 2011.
[5] M. Parvizi, K. Allidina, and M. N. El-Gamal, "An ultra-low-power wide-band inductorless CMOS LNA with tunable active shunt-feedback," *IEEE Trans. Microw. Theory Techn.*, vol. 64, no. 6, pp. 1843–1853, Jun. 2016.
[6] F. Bruccoleri, E. A. M. Klumperink, and B. Nauta, "Wide-band CMOS low-noise amplifier exploiting thermal noise canceling," *IEEE J. Solid-State Circuits*, vol. 39, no. 2, pp. 275–282, Feb. 2004.
[7] W.-H. Chen, G. Liu, B. Zdravko, and M. A. Niknejad, "A highly linear broadband CMOS LNA employing noise and distortion cancellation," *IEEE J. Solid-State Circuits*, vol. 43, no. 5, pp. 1164–1176, May 2008.
[8] S. C. Blaakmeer, E. A. M. Klumperink, D. M. W. Leenaerts, and B. Nauta, "Wideband balun-LNA with simultaneous output balancing, noise-canceling and distortion-canceling," *IEEE J. Solid-State Circuits*, vol. 43, no. 6, pp. 1341–1350, Jun. 2008.
[9] J. Shim, T. Yang, and J. Jeong, "Design of low power CMOS ultra wide band low noise amplifier using noise canceling technique," *Microelectron. J.*, vol. 44, no. 9, pp. 821–826, Sep. 2013.
[10] K.-H. Chen and S.-I. Liu, "Inductorless wideband CMOS low-noise amplifiers using noise-canceling technique," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 59, no. 2, pp. 305–314, Feb. 2012.
[11] H. Wang, L. Zhang, and Z. Yu, "A wideband inductorless LNA with local feedback and noise cancelling for low-power low-voltage applications," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 57, no. 8, pp. 1993–2005, Aug. 2010.
[12] B. Razavi, "Low-noise amplifier," in *RF Microelectronics*, 2nd ed. Beijing, China: Publishing House of Electronics Industry, 2012, pp. 263–266.
[13] T. H. Lee, "Noise," in *The Design of CMOS Radio-Frequency Integrated Circuits*, 2nd ed. Beijing, China: Publishing House of Electronics Industry, 2012, pp. 259–262.
[14] B. Razavi, "Noise," in *Design of Analog CMOS Integrated Circuits*. Beijing, China: China Machine Press, 2013, pp. 212–213.

[15] J. Kim, S. Hoyos, and J. Silva-Martinez, "Wideband common-gate CMOS LNA employing dual negative feedback with simultaneous noise, gain, and bandwidth optimization," *IEEE Trans. Microw. Theory Techn.*, vol. 58, no. 9, pp. 2340–2351, Sep. 2010.
[16] J. Kim and J. Silva-Martinez, "Wideband inductorless balun-LNA employing feedback for low-power low-voltage applications," *IEEE Trans. Microw. Theory Techn.*, vol. 60, no. 9, pp. 2833–2842, Sep. 2012.
[17] C. Liao and S. Liu, "A broadband noise-canceling CMOS LNA for 3.1–10.6-GHz UWB receivers," *IEEE J. Solid-State Circuits*, vol. 42, no. 2, pp. 329–339, Feb. 2007.
[18] J. Y.-C. Liu, J.-S. Chen, C. Hsia, P.-Y. Yin, and C.-W. Lu, "A wideband inductorless single-to-differential LNA in 0.18μm CMOS technology for digital TV receivers," *IEEE Microw. Wireless Compon. Lett.*, vol. 24, no. 7, pp. 472–474, Jul. 2014.
[19] A. L. T. Costa, H. Klimach, and S. Bampi, "A 2-decades wideband low-noise amplifier with high gain and ESD protection," in *Proc. 28th Symp. Integr. Circuits Syst. Design (SBCCI)*, Sep. 2015, pp. 1–6.
[20] S. Arshad, R. Ramzan, K. Muhammad, and Q. Wahab, "A sub-10 mW, noise cancelling, wideband LNA for UWB applications," *Int. J. Electron. Commun.*, vol. 69, pp. 109–118, Sep. 2015.
[21] H.-T. Chou, S.-W. Chen, and H.-K. Chiou, "A low-power wideband dual-feedback LNA exploiting the gate-inductive bandwidth/gain-enhancement technique," in *IEEE MTT-S Int. Microw. Symp. Dig.*, Jun. 2013, pp. 1–3.



YIMING YU was born in Zhejiang, China. He received the B.S. degree in electronic engineering from the University of Electronic Science and Technology of China, Chengdu, China, in 2012, where he is currently pursuing the Ph.D. degree.

His research interests include modeling of on-chip devices, CMOS RF, and mm-Wave integrated circuits and phased array transceiver design.

KAI KANG (M'17) received the B.Eng. degree in electrical engineering from Northwestern Polytechnical University, China, in 2002, and the joint Ph.D. degree from the National University of Singapore, Singapore, and the Ecole Supérieure D'électricité, France, in 2008.

From 2006 to 2010, he was a Senior Research Engineer with the Institute of Microelectronics, A*STAR, Singapore. Since 2011, he has been with the University of Electronic Science and Technology of China, where he is currently a Professor and the Associate Dean of the School of Electronic Engineering. His research interests are RF and mm-Wave integrated circuits design and modeling of on-chip devices.

YIMING FAN received the B.S. degree in electronic engineering from the University of Electronic Science and Technology of China, Chengdu, China, in 2016. He is currently pursuing the M.S. degree with The Ohio State University.

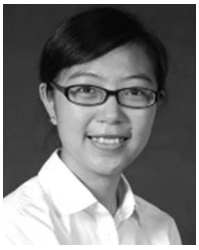
His research interests include modeling of devices, CMOS analog circuits, and RF wireless transceiver design.

CHENXI ZHAO (M'17) received the B.S. and M.S. degrees from the University of Electronic Science and Technology of China, Chengdu, China, in 2004 and 2007, respectively, and the Ph.D. degree from the Pohang University of Science and Technology, Pohang, South Korea, in 2014, all in electrical engineering.

Since 2014, he has been a Lecturer with the School of Electronic Engineering, University of Electronic Science and Technology of China. His research interests include RF CMOS device modeling, CMOS RF transceivers, and power amplifier design for millimeter wave application.

HUIHUA LIU received the B.S. degree in electrical and mechanical engineering from the China University of Petroleum, Beijing, China, in 1999, and the M.S degree in electrical engineering from the University of Electronic Science and Technology of China (UESTC), Chengdu, China, in 2006, where he is currently pursuing the Ph.D. degree with the School of Microelectronics and Solid-State Electronics.

His research interests include digital IC design, high-speed clock and data recovery, and A/D and D/A converters.



YUNQIU WU (M'11) received the B.S. and Ph.D. degrees from the University of Electronic Science and Technology of China (UESTC), Chengdu, China, in 2004 and 2009, respectively.

She was with the Technical University of Denmark, Kongens Lyngby, Denmark, from 2012 to 2013. She is currently with UESTC as an Associate Professor. Her current research interests include characterizing the microwave parameters of materials and IC device de-embedding and modeling.

YONG-LING BAN (M'14) received the B.S. degree in mathematics from Shandong University, China, in 2000, the M.S. degree in electromagnetics from Peking University, China, in 2003, and the Ph.D. degree in microwave engineering from the University of Electronic Science and Technology of China (UESTC), Chengdu, China, in 2006.

Since 2010, he has been an Associate Professor of Microwave Engineering with UESTC. His research interests include multiband small antennas and MIMO antennas for 4G/5G terminal devices, and smart antennas for wireless AP.

WEN-YAN YIN (M'99–SM'01–F'13) received the M.Sc. degree in electromagnetic field and microwave technique from Xidian University, Xi'an, China, in 1989, and the Ph.D. degree in electrical engineering from Xi'an Jiaotong University, Xi'an, in 1994.

He has been with the National University of Singapore, Singapore, since 1998. He joined the Center for Optical and Electromagnetic Research, Zhejiang University, Hangzhou, China, as a Qiu Shi Professor, in 2009.