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Harmonic Emissions of Three-Phase Diode Rectifiers in Distribution Networks

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ABSTRACT Harmonic emissions have been changed in distribution networks, with respect to frequency range and magnitude, due to the penetration of modern power electronics systems. Two new frequency ranges 2–9 and 9–150 kHz have been identified as new disturbing frequency ranges affecting distribution networks. This paper presents the effects of grid-connected three-phase systems with different front-end topologies: conventional, small dc-link capacitor, and electronic inductor. A power converter with a small dc-link capacitor can create a resonant frequency with the line impedance below and above 1 kHz depending on the grid configurations. The resonant effects depend on many factors, such as load power levels, filter types, and the number of parallel drives. These issues can affect the grid current harmonics and power quality of the distribution networks. Analyses and simulations have been carried out for three different topologies and the results have been verified by experimental test at system level. Current harmonic emissions have been considered for 0–2, 2–9, and 9–150 kHz frequency ranges.

INDEX TERMS Harmonic mitigation techniques, power quality, DC-link capacitor, distribution networks, resonant frequency, 2–9 kHz.

I. INTRODUCTION

Three phase power converters with low cost diode rectifiers are still widely used in motor drive systems to regulate motor speed in different residential, commercial and industrial applications [1], [2]. The diode rectifiers can achieve lower power losses, but may significantly increase current harmonics due to their non-linear effects. The current harmonics may result in low power quality, resonances, and finally stability issues of the distribution networks. Therefore, a number of harmonic mitigation techniques have been developed for different applications such as passive filters [3], multi-pulse transformer based rectifiers [4], [5] and active harmonic filtering techniques [6], [7]. These harmonic mitigation solutions can increase the overall system cost and volume or complicate the entire control system but are required due to international regulations.

In many power electronics applications, a three-phase diode rectifier with a large electrolytic DC-link capacitor and a DC choke (or AC choke) is preferred due to cost-effectiveness, simplicity, and reliability advantages as it is illustrated in Fig. 1(a) [8]. However, the electrolytic DC-link capacitor is bulky and expensive with a limited lifetime [9], [10]. The sizing of the DC-link capacitors has become important due to more stringent power density requirements [11]. In the recent years, three-phase diode rectifiers with Small DC-Link Capacitors (SDLC) – normally less than 100 μF – have been getting more attention by power electronics and drive manufactures due to longer lifetime and reduced line current harmonics emission [12], [13]. It has been addressed in the literature that the distortion of the line current can be reduced when the DC-link capacitor is reduced in size [12]–[15]. This can be advantageous because current harmonics lead to an increase in power loss [16], [17], grid instability [16] and interference with communication signals [18]. As analyzed in [12]–[15], the capability of the SDLC drive to reduce harmonics has only been considered at a single unit and not at a system level when many drives are connected and operated in parallel as shown in Fig. 1(b). In [19] and [20] analyses have been carried out for a sufficient numbers of SDLC drives connected in parallel at the Point of Common Coupling (PCC). As the small capacitor cannot store high levels of energy, its filtering capabilities are

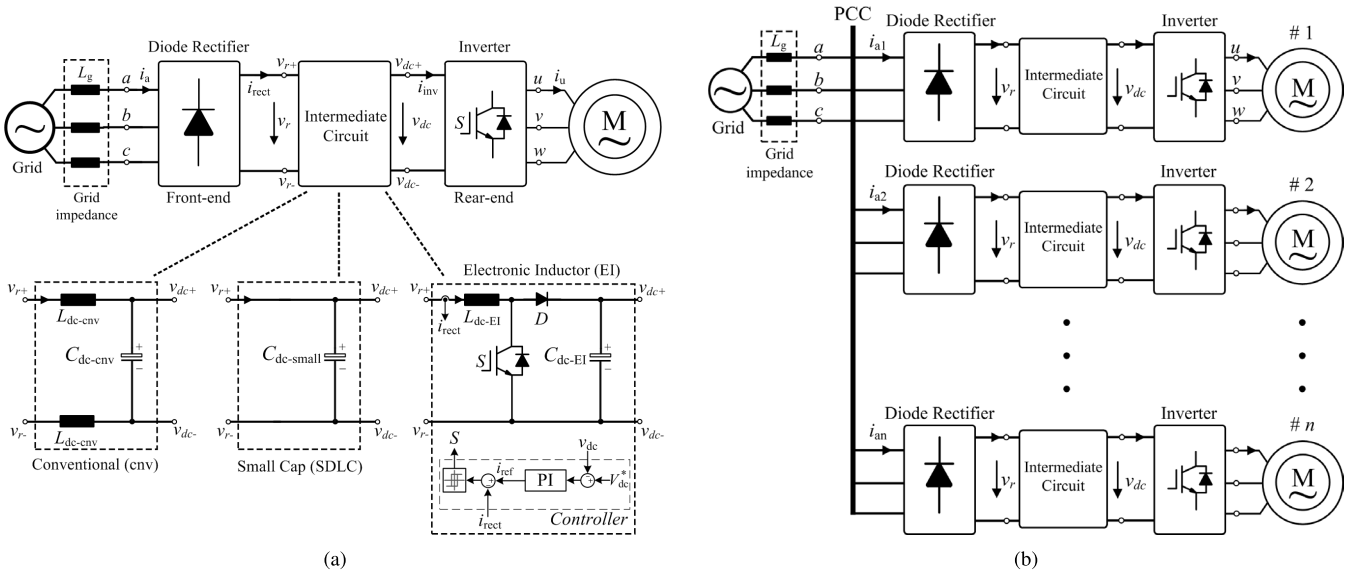

FIGURE 1. Block diagram of (a) Single motor drive system with different DC-side filter solutions, (b) Multi-drive configuration.

reduced and voltage oscillations appear at the DC-link side. The DC voltage fluctuation is one of the drawbacks of this topology [14]. Control and modulation techniques [15] have been proposed for a motor drive system with a SDLC in order to improve quality of the output current and also the voltage waveforms.

Besides the continuous efforts toward employing and utilizing the industrial motor drives based on the line commutated front-end diode rectifiers with AC and/or DC passive chokes (in conventional and SDLC drives), substantial interests are also devoted to suitable cost-effective active methods which can be combined with the existing motor drives. Meanwhile, employing an Electronic Inductor (EI) placed at the DC-link stage can emulate an active front-end along with the diode rectifier, as it is shown in Fig. 1(a). The main idea behind using EI is to replace the bulky DC-link inductor with a relatively small inductor incorporated with a DC-DC converter to behave like an ideal infinite inductor, which can significantly improve the drives input current quality. An acceptable compromise between the DC-link inductor size and the switching frequency of the converter will determine the operating mode of the EI [21]. Moreover, applying a multi-pulse pattern modulation technique on the DC-DC converter results in a selective harmonic mitigation of the drive's input current [22], [23]. This issue will be more valuable at multi-drive applications, where implementing a suitable modulation scheme with respect to the number of drives will enhance the grid power quality at the PCC.

Increasing the use of distributed energy sources and modern power converter technologies such as Active Front End (AFE) converters in distribution networks causes harmonic emissions over the frequency range of 2–9 kHz, which has become an important power quality issue [24], [25]. Thus, there is a serious action supported by international standardization organizations to consider compatibility level for this new frequency range of 2–9 kHz [24], [26]. Although, this is a very important area, there are very limited information available about the distortion and measurement techniques in this frequency range. In recent years few articles have been published, which mainly cover the distortion and emissions of different equipment in this frequency range [25], [27].

Three-phase diode rectifiers are still commonly utilized in many applications such as adjustable speed drive systems, which may be one of the major sources of harmonic emission in the distribution networks. Therefore, in this paper, the harmonic distortion generated by three different topologies utilized in the three-phase diode rectifier based systems have been analyzed and compared for 0–9 kHz frequency range. This paper elaborates mathematical expressions and modelings of multi-drive systems with respect to their power quality and resonant frequency issues and the analyses have been verified by several tests.

This paper is structured as follows. Section II describes the frequency ranges of harmonic emissions and their importance. Comprehensive mathematical harmonic analysis of grid connected drives are presented in Section III. Section IV is dedicated to experimental results in order to demonstrate the effectiveness of the developed analysis. Finally, conclusions are drawn in Section V.

II. FREQUENCY RANGES OF HARMONIC EMISSIONS

Power electronics system is a key technology for distribution networks, which can transfer electrical power from renewable energy sources to grids or generate regulated frequency and/or voltage for different loads such as variable speed drives and battery chargers. New demands for a) cost and size reduction, b) performance and quality improvement and

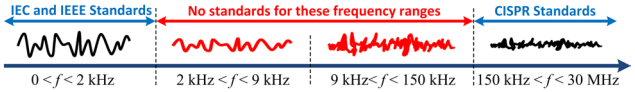

FIGURE 2. Different frequency ranges of harmonic emission classified by IEC for distribution networks.

c) flexibility on power management have promoted power electronics applications extensively in industrial, commercial and residential sectors such as in transportation, utility and home appliances in the recent years.

Main drawbacks of power electronic systems are low (below 2 kHz) and/or high (above 2 kHz) frequency harmonics emissions. The utilization of power electronics systems has been increased significantly in many applications such as motor drive systems, roof-top solar inverters and compact fluorescent lamps, which can inject high-frequency and high-energy harmonics within the frequency range of 2–150 kHz in the distribution networks.

Conventional power electronics products have affected the quality of power networks due to significant injection of low order harmonics (mainly below 2 kHz). Power Factor Correction (PFC) circuits have been proposed for single-phase power electronic products in order to improve line current quality and power factor. The line current of a single-phase converter with a PFC system has very low current distortion below 2 kHz but can inject harmonics at high frequencies. This technology cannot be used in a three-phase power electronics systems to completely eliminate the most important low order harmonics - the 5th and the 7th orders - but it can mitigate the harmonics below a certain level defined by standards such as IEC61000-3-2 or IEC61000-3-12 [28].

Harmonics have short and long term effects on grids, and also on grid connected electronics and power electronics equipment such as malfunction, failure and losses. These issues reduce the reliability, lifetime and efficiency of the electricity networks. As shown in Fig. 2, there are no general regulations and compatibility levels for harmonics within the frequency range of 2–150 kHz to protect all electricity networks and grid connected equipment. The International Electro-technical Commission (IEC), Technical Committee 77A (TC 77A) – the world leading authority to prepare technical documents for international standards – has requested international experts to define standardization for harmonics within the frequency range of 2–150 kHz [29]. The new challenging issues of future grids are related to this new frequency range and they are classified as: 1) generation of high-frequency harmonics, 2) creation of new resonance frequencies and 3) strong harmonic interactions between different types of power electronic systems. Hence the utility companies, renewable energy and power electronics manufactures have been facing new challenges to solve these harmonic issues and define proper harmonics standards and regulations for grid connected electronics and power electronics equipment.

The fundamental principles, which led to the harmonic standards can be noted as:

a) Avoid system and load damage as well as disruption due to high harmonic levels
b) Reduced losses to an acceptable level
c) A proper and an economical mitigation solution for both manufacturers and utility companies

According to the existing IEC regulations, there are two main frequency ranges for which equipment require to comply with harmonic emission limits: 0–2 kHz and above 150 kHz. Currently, there is not any general regulation to cover all products within the frequency range of 2–150 kHz. Due to increasing a number of grid connected high-frequency power electronics converters such as motor drive systems, solar inverters and single-phase converters with PFC systems, different disturbances have been reported in distribution networks [27]. Thus, the following frequency ranges cover almost all frequency ranges: noitemsep

- 0–2 kHz (*Low-frequency harmonic*)
- 2–9 kHz
- 9–150 kHz
- 150 kHz–30 MHz (*Conducted emission*)
- Above 30 MHz (*Radiated emission*)

III. HARMONIC ANALYSIS OF GRID CONNECTED DRIVES

As mentioned above, a motor drive system with a Small DC-link Capacitor (SDLC) has some advantages compared to a conventional motor drive system with a large DC-link capacitor and inductor [20]. From a design point of view, the conventional drives have a large size DC or AC choke in order to reduce the line current harmonics emissions as well as a large DC capacitor to control and reduce DC-link voltage fluctuation. These DC-link components increase the cost of the conventional drives compared to the SDLC drives. However, a comprehensive analysis is required to investigate the power quality of a distribution network with different penetrations of power electronics systems like the SDLC systems.

As shown in Fig. 3, one of the main problems of SDLC motor drives is the resonant frequency generated by the DC-link capacitor and the line inductance (L_g). The line inductance of a low-voltage distribution network is mainly defined by the size and the type of the step-down transformer and feeders. Thus, the resonant frequency of the system depends on the grid parameters and its configuration – line impedance value and a number of nonlinear loads – and the drives parameters. The resonant frequency may appear at any frequency from 150 Hz to 3 kHz in a typical low-voltage distribution network [19], [28]. The main focus of this paper is to analyze two power quality issues of a low-voltage distribution network with grid connected three-phase motor drive systems based on Fig. 1(b):

a) The resonance effect due to the DC-link capacitor of a drive
b) Line current harmonics emissions affecting the power quality of a grid at PCC

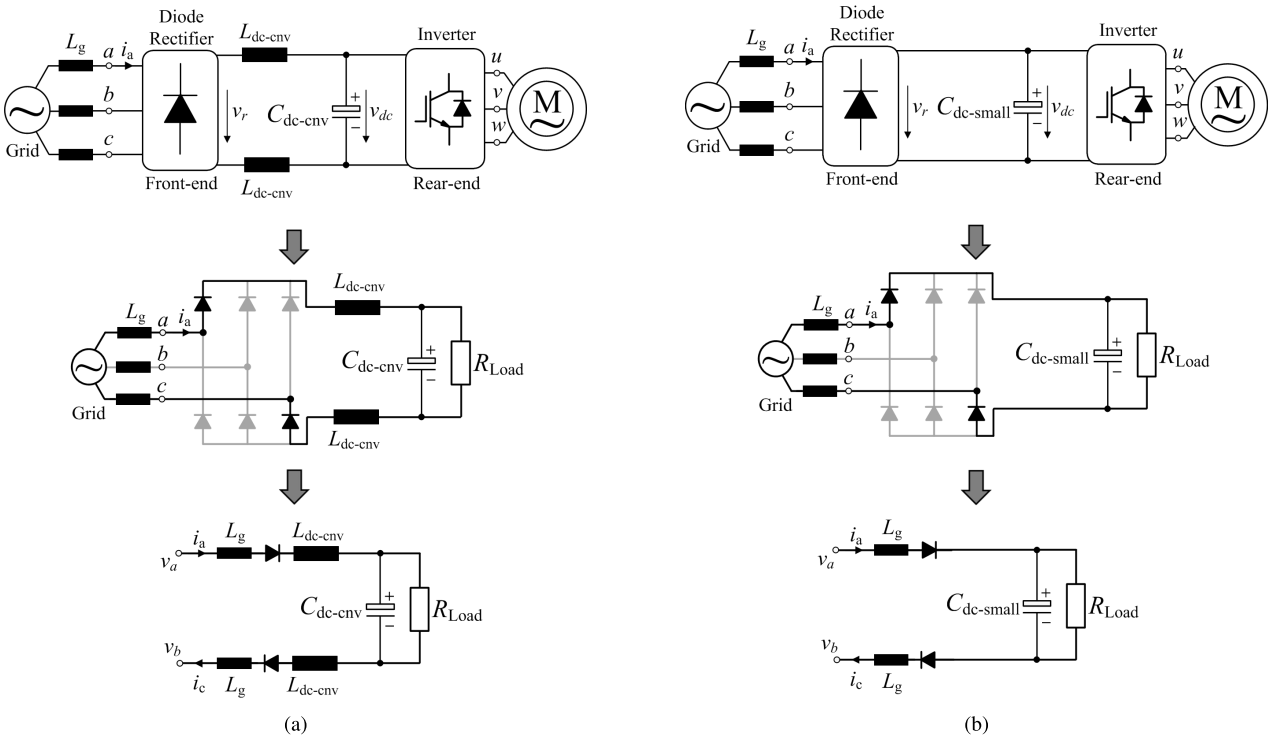

FIGURE 3. A block diagram of a motor drive system and equivalent impedance model for (a) Conventional drive, (b) SDLC drive.

It is important to emphasize that the main goal of this research work is to highlight power quality issues of three-phase diode rectifiers with different front-end topologies and configurations. It has been reported by many authors that SDLC motor drives have DC-link voltage stability issues. Different active and passive damping methods including different modulation techniques have been addressed to reduce the DC-link voltage fluctuation and the resonance due to the small capacitance in the DC link [30]–[32]. Therefore, the main focus of this paper is not on the motor control side of the motor drive. On the other hand, it is assumed that the SDLC motor drive operates properly at the load side while its line current and DC-link effects will be analyzed at the grid side.

In the following sections, three-phase diode rectifiers with a) Conventional (CNV), b) SDLC and c) Electronic Inductor (EI) connected to motor drives are analyzed at a unit (single drive) and at a system level (multi-drives) with different configurations and load profiles. The harmonic analyses have been considered for two frequency ranges: 0–2 and 2–9 kHz.

A. HARMONIC ANALYSIS OF A DRIVE AT A UNIT LEVEL

1) RESONANT EFFECT AND LINE CURRENT HARMONIC EMISSIONS FOR 0–2 kHz FREQUENCY RANGE

In this analysis it is assumed that only one drive is connected to an ideal voltage source – a non-distorted three-phase balanced system – as shown in Fig. 3. The total line inductance of each phase is assumed as L_g and nonlinear effects of other loads connected to the same PCC are not considered. The main focus of this section is to analyze the resonant effect of the DC-link capacitor with the line impedance and consequently the line current harmonic emissions generated by the drive.

Fig. 3(a) shows the equivalent impedances of the systems with the conventional drive during each conduction period of the three-phase diode rectifier. At any instant of time, two input voltage sources are connected to the DC-link of the drive through two diodes. Thus the whole system can be modeled as an RLC circuit where $2L_g$ is the grid inductance during the conduction period of the diode rectifier, C_{dc-cnv} is the DC-link capacitor, L_{dc-cnv} is the inductor of each positive and negative DC-link branch and R_{Load} is an equivalent resistor to model the load power. Therefore, the impedance of the system seen from the grid side is calculated for the conventional drive and the result is given in equation (1):

$$Z_{in} = \frac{1 - 2\omega^2(L_g + L_{dc-cnv})C_{dc-cnv} + j\omega\dfrac{2(L_g + L_{dc-cnv})}{R_{Load}}}{j\omega C_{dc-cnv} + \dfrac{1}{R_{Load}}} \tag{1}$$

where the resonant frequency (f_o) and the damping factor (ξ) of the single conventional drive system are defined as follows:

$$\left.\begin{aligned} f_o &= \frac{1}{2\pi\sqrt{2(L_g + L_{dc-cnv})C_{dc-cnv}}} \\ \xi &= \frac{1}{2R_{Load}}\sqrt{\frac{2(L_g + L_{dc-cnv})}{C_{dc-cnv}}} \end{aligned}\right\} \tag{2}$$

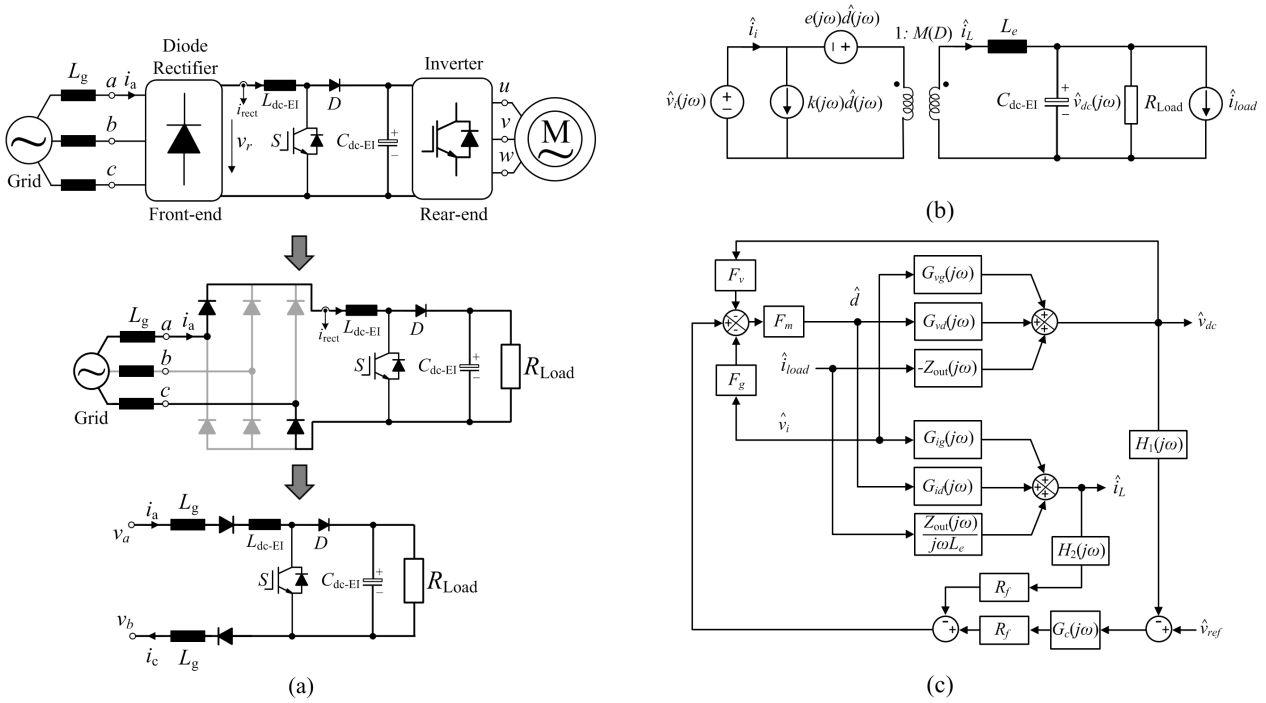

FIGURE 4. (a) Simplified model of the EI drive, (b) Small-signal model of the converter under CCM operation, (c) Mathematical model of the converter operating in a current mode control.

TABLE 1. System Parameters

	General Parameters			Conventional Drive		SDLC Drive	EI Drive			
Symbol	v_{abc}	f_g	L_g	L_{dc-cnv}	C_{dc-cnv}	$C_{dc-small}$	L_{dc-EI}	C_{dc-EI}	V_{dc}	k_p, k_i
Parameter	Grid phase voltage	Grid frequency	Grid impedance	DC-link inductor	DC-link capacitor	Small DC-link capacitor	DC-link inductor	DC-link capacitor	Output voltage	PI parameters
Value	230 V_{rms}	50 Hz	128 μH	1.25 mH	500 μF	30 μF	2 mH	500 μF	700 V_{dc}	1.5, 0.05

At the resonant frequency (f_o), the impedance value is decreased in magnitude and the damping factor (ξ) depends on the load power and the converter parameters.

In order to compare the system characteristic of the conventional drive with the SDLC drive, the same analysis has been carried out and the results are given in equations (3) and (4) based on the equivalent impedances of the system illustrated in Fig. 3(b).

$$Z_{in} = \frac{1 - 2\omega^2 L_g C_{dc-small} + j\omega \dfrac{2L_g}{R_{Load}}}{j\omega C_{dc-small} + \dfrac{1}{R_{Load}}} \tag{3}$$

$$\left.\begin{aligned} f_o &= \frac{1}{2\pi\sqrt{2L_g C_{dc-small}}} \\ \xi &= \frac{1}{2R_{Load}}\sqrt{\frac{2L_g}{C_{dc-small}}} \end{aligned}\right\} \tag{4}$$

In this case, the DC-link capacitor is reduced in size, $C_{dc-small}$ and there is no DC-link inductor. Thus, it is expected that the resonant frequency (f_o) and the damping factor (ξ) of the impedance are changed significantly. For example, following Table 1, a conventional drive with $C_{dc-cnv} = 500\ \mu$F and $L_{dc-cnv} = 1.25$ mH connected to a grid with $L_g = 128\ \mu$H has a resonance frequency of 136 Hz, while a drive with SDLC, $C_{dc-small} = 30\ \mu$F has a resonance frequency of 1816 Hz.

The EI topology has a very high impedance due to the current control of the DC link. However, as it is shown in Fig. 4(a), its input impedance seen from the diode rectifier side needs to be calculated. The closed-loop input impedance of the boost converter based on its small-signal model (Fig. 4(b)) is defined as given below:

$$Z_{in,CL}(j\omega) = \frac{\hat{v}_i(j\omega)}{\hat{i}_i(j\omega)}\Big|_{\hat{i}_{Load}(j\omega),\hat{v}_{ref}=0} \tag{5}$$

Taking into account the condition in (5), following equations are found from Fig. 4(c):

$$\left.\begin{aligned} \hat{d} &= F_m\left[-R_f H_1 G_c \hat{v}_{dc} - R_f H_2 \hat{i}_L - F_g \hat{v}_i - F_v \hat{v}_{dc}\right] \\ \hat{i}_L &= G_{id}\hat{d} + G_{ig}\hat{v}_i \\ \hat{v}_{dc} &= G_{vd}\hat{d} + G_{vg}\hat{v}_i \end{aligned}\right\} \tag{6}$$

TABLE 2. Boost Converter Model Parameters With Current Controlled Gains

$M(D)$	L_e	$e(j\omega)$	$k(j\omega)$	F_m	F_g	F_v
$\frac{V_{dc}}{V_i}=\frac{1}{(1-D)}$	$\frac{L_{dc-EI}+2L_g}{(1-D)^2}$	$V_{dc}(1-\frac{j\omega L_{dc-EI}}{(1-D)^2R_{Load}})$	$\frac{V_{dc}}{(1-D)^2R_{Load}}$	$\frac{-2\left(L_{dc-EI}+2L_g\right)}{T_sV_{dc}}$	$\frac{(1-D)T_s}{2\left(L_{dc-EI}+2L_g\right)}$	$-\frac{T_s}{2\left(L_{dc-EI}+2L_g\right)}$

Notably the current controller gains are given in Table 2. These parameters are calculated for the hysteresis current control [33], [34]. The relationship between the input current and the inductor current can be obtained from Fig. 4(b) as given below:

$$\hat{i}_i = k\left(j\omega\right)\hat{d} + M\left(D\right)\hat{i}_L \tag{7}$$

Using (6) and (7), the relationship between $\hat{v}_i$ and $\hat{i}_i$ yields in the closed-loop input impedance:

$$Z_{in,CL}\left(j\omega\right) = \frac{P\left(j\omega\right)}{k\left(j\omega\right)M\left(D\right)G_{id} + P\left(j\omega\right)M\left(D\right)G_{ig}} \tag{8}$$

where $P(j\omega)$ is obtained as:

$$P\left(j\omega\right) = -\frac{1 + F_mR_fH_2G_{id} + G_{vd}F_m\left(R_fH_1G_c + F_v\right)}{F_m\left[R_fH_2G_{ig} + F_g + G_{vg}\left(R_fH_1G_c + F_v\right)\right]} \tag{9}$$

here H_1, H_2 and R_f are the voltage and the current sensing transfer functions and gains, which depend on the utilized sensors. Moreover, G_{vd}, G_{vg}, G_{ig} and G_{id} are small-signal open-loop transfer functions, which are defined as (10) (at the bottom of this page) [33]–[35]. Notably, $G_c(j\omega)$ is the voltage controller, which is implemented based on a Proportional-Integral (PI) controller given by:

$$G_c\left(j\omega\right) = k_p + \frac{k_i}{j\omega} \tag{11}$$

As it can be seen from the simulation results shown in Fig. 5, the load profile has less effect on the harmonics emissions of the conventional drive due to the fact that the resonant frequency is placed close to the 3rd harmonic (150 Hz) with a narrow-band characteristic. Thus, other current harmonics around the resonant frequency are not affected significantly. Moreover, the SDLC drives may affect power quality

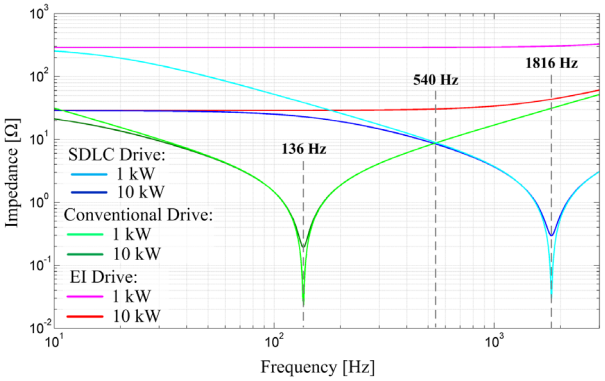

FIGURE 5. Impedance characteristics of conventional, SDLC and EI drives at two output power levels using the parameters given in Table 1.

of grids as other non-linear loads connected to the same PCC will be influenced by the resonant frequency. The electronic inductor is controlled to behave like an infinite inductor. In this respect, a very high damping factor can be achieved due to the high DC-link impedance.

In order to analyze the resonant effects in details, the three different topologies have been simulated based on a 10 kW drive and the results are shown in Fig. 6 and Fig. 7. When the SDLC drive operates at a high power, the impedance characteristic of the drive is improved at the resonant frequency due to a better damping factor. This means that the SDLC drive operating at high power may not inject significant current harmonics at its resonant frequency. As shown in Fig. 5, at 1 kW power level, the loop impedance of the SDLC drive is decreased significantly at the resonant frequency due to poor damping factor. Therefore, high current harmonic emission is expected for the drive at this power level.

$$\left.\begin{aligned}
G_{vd}\left(j\omega\right) &= \frac{\hat{v}_{dc}\left(j\omega\right)}{\hat{d}\left(j\omega\right)}\Big|_{\hat{v}_i(j\omega),\hat{i}_{Load}(j\omega)=0} = \frac{M\left(D\right)k\left(j\omega\right)}{1-\omega^2L_eC_{dc-EI}+\frac{j\omega L_e}{R_{Load}}}\\
G_{vg}\left(j\omega\right) &= \frac{\hat{v}_{dc}\left(j\omega\right)}{\hat{v}_i\left(j\omega\right)}\Big|_{\hat{d}(j\omega),\hat{i}_{Load}(j\omega)=0} = \frac{M\left(D\right)}{1-\omega^2L_eC_{dc-EI}+\frac{j\omega L_e}{R_{Load}}}\\
G_{ig}\left(j\omega\right) &= \frac{\hat{i}_L\left(j\omega\right)}{\hat{v}_i\left(j\omega\right)}\Big|_{\hat{d}(j\omega),\hat{i}_{Load}(j\omega)=0} = \frac{M\left(D\right)\left(\frac{1}{R_{Load}}+j\omega C_{dc-EI}\right)}{1-\omega^2L_eC_{dc-EI}+\frac{j\omega L_e}{R_{Load}}}\\
G_{id}\left(j\omega\right) &= \frac{\hat{i}_L\left(j\omega\right)}{\hat{d}\left(j\omega\right)}\Big|_{\hat{v}_i(j\omega),\hat{i}_{Load}(j\omega)=0} = \frac{M\left(D\right)k\left(j\omega\right)\left(\frac{1}{R_{Load}}+j\omega C_{dc-EI}\right)}{1-\omega^2L_eC_{dc-EI}+\frac{j\omega L_e}{R_{Load}}}
\end{aligned}\right\} \tag{10}$$

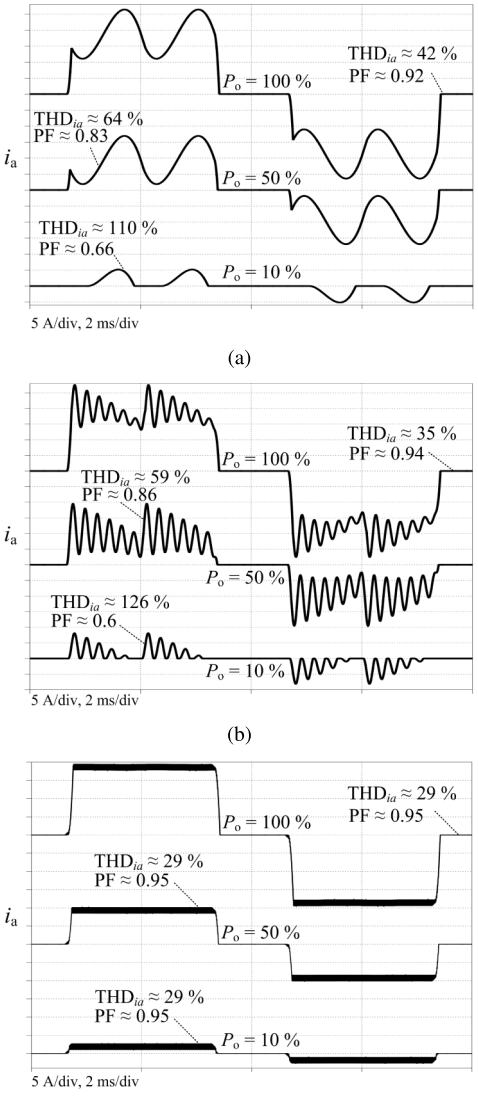

FIGURE 6. Simulated input current (i_a) waveforms of (a) Conventional drive, (b) SDLC drive, (c) EI drive systems, at different output power levels following system parameters in Table 1 (with rated output power of 10 kW).

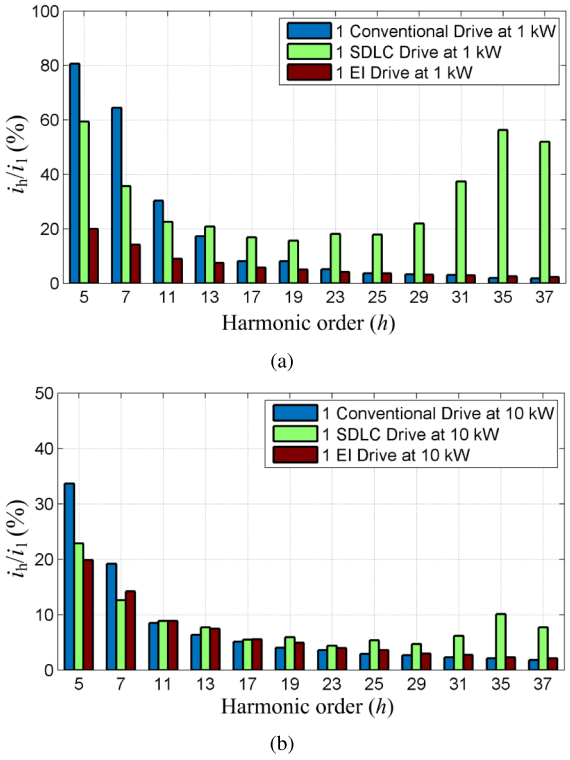

FIGURE 7. Harmonic emissions of conventional, SDLC and EI drives (a) at 1 kW, (b) at 10 kW.

According to the impedance models shown in Fig. 5, it is expected that the SDLC drive has a better harmonic performance (up to 540 Hz) at the system level compared to the conventional drive. This is due to the fact that the system impedance value is higher than the conventional drive for this frequency range. Therefore, other nonlinear loads connected to the same PCC do not resonate significantly with the SDLC drives.

As shown in Fig. 6(b), the SDLC drive generates high-frequency line current compared to the conventional drive. This is due to the resonant effects of the small DC-link capacitor with the line impedance. In fact, the DC-link current and the line current are influenced by a) the rectified voltage of the diode rectifier and b) the loop impedance of the system (grid impedance and DC-link capacitor). Thus, the current harmonics are generated at the resonant frequency of the system in which the loop impedance is decreased.

As shown in Fig. 6(c), the EI drives control the DC-link current to a constant value, proportional to the load power and hence the line current is almost a square-wave at different load power levels. The DC-link current (i_{rect}) is controlled in the Continuous Conduction Mode (CCM), and therefore the grid current will be a rectangular waveform. In order to avoid having the DC-link current in the Discontinuous Conduction Mode (DCM), the EI parameters (e.g., inductor size and switching frequency) should be designed in accordance to the partial load condition [21]. Notably, as the DC-link current is controlled based on the load power, the input current Total Harmonic Distortion (THD) and the Power Factor (PF) have become independent of the load profile.

The current harmonics generated by these three topologies have been analyzed based on time-domain simulations. As it is shown in Fig. 7, the electronic inductor is not influenced by the load profile and has lower line current harmonic emission for the frequency range of 0–2 kHz. Although the current harmonics (in percentage) generated by the conventional drive are higher in magnitude at 1 kW compare to 10 kW load power but the harmonic reductions have a same trend from the 5th order up to the 37th for both power levels. This is consistent with the impedance characteristic of the conventional drive as shown in Fig. 5. On the other hand, the SDLC drive has different current harmonic performances at both low and high power levels. This is due to the low damping performance of the SDLC drive at the low power operation, around its resonant frequency.

2) LINE CURRENT HARMONIC EMISSIONS FOR THE FREQUENCY RANGE OF 2–9 kHz

So far, the above three-phase drives have been analyzed with respect to the resonant issues and the line current harmonic emissions at the grid side for the frequency range of 0–2 kHz. As the DC-link sides of these drives are connected to a motor drive, hence the high-frequency harmonic emissions of the whole system need to be analyzed for the frequency range of 2 kHz and above.

As a result of Pulse Width Modulation (PWM) process, the rear-end inverter produces pulsating three-phase pole voltages $v_x(t)(x = u, v, w)$ and feeds AC motors such as an Induction Motor (IM) at the demanded voltage level, frequency and power. The switched voltage waveform is a periodic signal with respect to the reference and carrier signals, and its harmonic contents can hence be obtained by employing a double Fourier integral solution [36]. A general closed form solution of the output pulsating voltages can be expressed as (12), where it is composed of a DC offset value, baseband harmonics and carrier group harmonic,

$$\begin{aligned} v_x(t) = \frac{A_{00}}{2} + \sum_{n=1}^{\infty}[A_{0n}\cos(n[\omega_{mo}t - p\frac{2\pi}{3}]) \\ + B_{0n}\sin(n[\omega_{mo}t - p\frac{2\pi}{3}])] \\ + \sum_{m=1}^{\infty}\sum_{n=-\infty}^{\infty}[A_{mn}\cos(m\omega_c t + n[\omega_{mo}t - p\frac{2\pi}{3}]) \\ + B_{mn}\sin(m\omega_c t + n[\omega_{mo}t - p\frac{2\pi}{3}])] \end{aligned} \tag{12}$$

with m and n representing the carrier group and baseband group index, respectively. A_{0n}, B_{0n}, A_{mn}, and B_{mn} denote the harmonic coefficients, which should be obtained according to the associated modulation methods applied on the inverter. The fundamental and carrier angular frequencies are stated as ω_{mo} and ω_c. The parameter p will choose 0, 1 and -1 for the output phases u, v, and w.

Assuming that the inverter drives the IM as a balanced load, the frequency domain three-phase output current $I_x(\omega)(x = u, v, w)$ can be obtained as,

$$\begin{bmatrix} I_u(\omega) \\ I_v(\omega) \\ I_w(\omega) \end{bmatrix} = \frac{V_{dc}}{3Z(\omega)} \begin{bmatrix} 2 & -1 & -1 \\ -1 & 2 & -1 \\ -1 & -1 & 2 \end{bmatrix} \begin{bmatrix} S_u(\omega) \\ S_v(\omega) \\ S_w(\omega) \end{bmatrix} \tag{13}$$

with V_{dc} and Z_ω stating the DC value of the DC-link voltage and the frequency domain phase impedance of the IM, respectively. The well-known inverter switching functions are denoted as $S_x(\omega)(x = u, v, w)$ and they are given based on Fig. 3 for the conventional and SDLC drives as,

$$S_x(\omega) = \frac{V_x(\omega)}{V_{dc}}, \quad x \in \{u, v, w\} \tag{14}$$

Considering the inverter operates in a lossless condition, then the DC-link inverter side I_{inv} current in the frequency domain can be calculated by,

$$I_{inv}(\omega) = \sum_{x\in\{u,v,w\}} S_x(\omega) \otimes I_x(\omega) \tag{15}$$

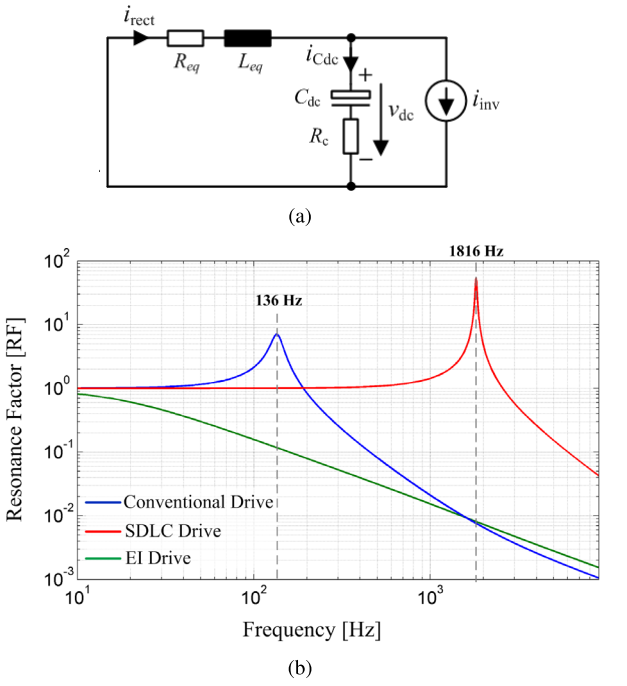

FIGURE 8. (a) DC-link equivalent circuit for motor drive. (b) DC-link resonance factor in the conventional, SDLC and EI drives.

Thus, the load current generated by PWM voltage is defined as a current source at the DC-link as it is shown in Fig. 8(a). The DC-link oscillations in (15) generated by the inverter operation are divided into two different currents. According to the circuit law $i_{inv} = i_{rect} - i_{Cdc}$, where i_{rect} and i_{Cdc} are the currents flowing out of the rectifier DC terminal and through the DC-link capacitor, respectively. The DC-link equivalent circuit of the drive system, as shown in Fig. 8(a), represents the current transfer from the inverter DC side to the rectifier DC side. The equivalent DC-link inductance L_{eq} and damping resistance R_{eq} for each conduction period of a three phase drive system are defined as,

$$L_{eq} = 2L_{dc} + 2L_g \tag{16}$$

$$R_{eq} = 2R_{dc} + 2R_g \tag{17}$$

where the grid inductance and resistance, and the DC-link choke resistance are denoted as L_g, R_g and R_{dc}, respectively. The DC-link current oscillation amplification, when passing from the inverter side to the rectifier side can then be determined by a Resonance Factor (RF), which is given as,

$$RF = \frac{I_{rect}}{I_{inv}} = \left|\frac{Z_C}{Z_C + Z_L}\right| \tag{18}$$

with $Z_c = R_c + 1/(j\omega C_{dc})$ and $Z_L = R_{eq} + j\omega L_{eq}$. In order to calculate the RF for the EI drive, the closed-loop response

needs to be found following Fig. 4 as:

$$RF = \left| \frac{\hat{i}_L(j\omega)}{\hat{i}_{Load}(j\omega)} \Big|_{\hat{v}_i(j\omega),\hat{v}_{ref}=0} \right| \tag{19}$$

Fig. 8(b) shows the resonance factors associated with the conventional, the SDLC and the EI drives, which are drawn using the parameters listed in Table 1 and Table 2. The motor drive load current has high-frequency ripple current based on the switching frequency of the inverter and motor parameters. The three-phase load currents are rectified through the switches of the inverter and the total current circulates through the DC-link and rectifier stages, encountered with the DC-link resonance factor. As can be observed from Fig. 8(b), the resonance amplification in the SDLC drive appears at a higher frequency compared to the conventional case. Consequently, the high-frequency oscillations inherited from the output side witness lower impedance at the DC link in the SDLC drives. This may generate more high-frequency oscillations and harmonics at the rectifier side. Thereafter, the multiplication of the rectifier current with the well-known six-pulse diode rectifier switching functions may result in high-frequency distortion in the drive input currents.

The high-frequency current harmonics of the EI drive has two harmonic sources. The first high-frequency current harmonic source is generated by the inverter, which is similar to the above analysis for the conventional and the SDLC drives. The second high-frequency current harmonic source is the switching effects of the EI inductor, which may generate high-frequency harmonics. The magnitude of the noise depends on many factors such as the switching frequency, inductor and capacitor sizes and control method of the EI system. This second harmonic source is an extra harmonic emission of the EI drives compared to the conventional and the SDLC drives. It is expected that the switching frequency of the EI is much higher than 9 kHz. Therefore, in the following section, the first high-frequency harmonic source – generated by the inverter and PWM voltage – is only considered for these drives with three different topologies and the second high-frequency current harmonic source of the EI drive is analyzed later, when test results of all drives are compared together.

Fig. 9 shows the input current frequency spectrum (between 2 and 9 kHz) of the conventional, the SDLC and EI drives, at the output frequency $f_{mo} = 40$ Hz, $f_{sw} = 5$ kHz and the load torque $T_L = 40$ Nm. From Fig. 9(a) it is evident that in the conventional drive case, the equivalent DC-link filter attenuates significantly the high-frequency oscillations, transferred from the inverter side to the rectifier side. Fig. 8(b) and Fig. 9(b) show that the SDLC drive with shifted resonant frequency to 1816 Hz, may allow high-frequency oscillations at the grid side due to high resonance factor (RF). The subject will be more critical if a lower switching frequency (e.g., 3 kHz) is selected for the inverter operation. Therefore, according to the simulation results, the SDLC drive has higher harmonic emission than the conventional and the EI drives.

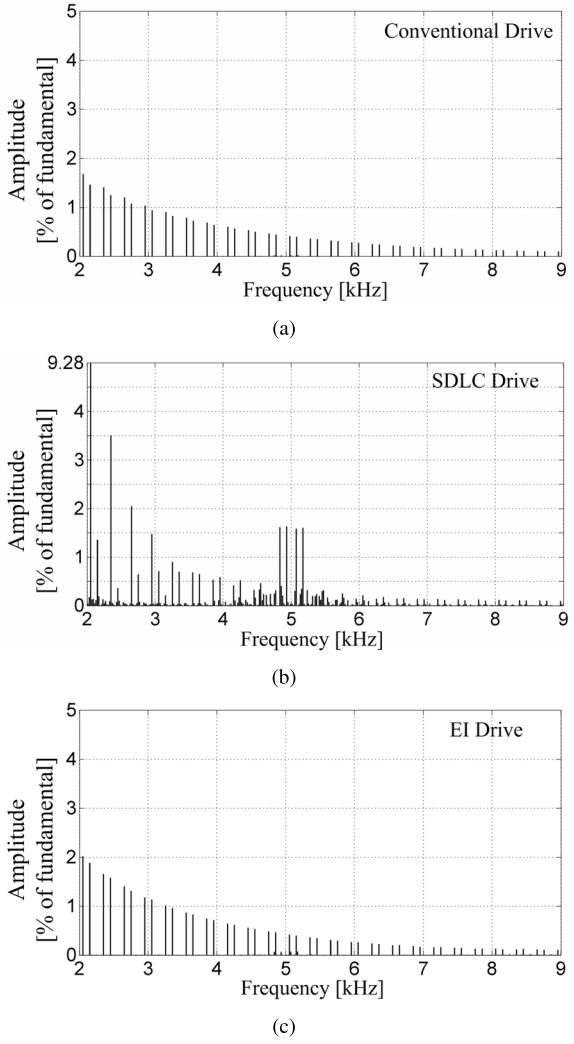

FIGURE 9. Input current harmonic emissions from 2–9 kHz in, (a) Conventional drive, (b) SDLC drive, (c) EI drive, when the motor operates at the output frequency of $f_{mo} = 40$ Hz, the switching frequency of $f_{sw} = 5$ kHz and the torque $T_L = 40$ Nm.

As the SDLC drive has a small DC-link capacitor compared to the conventional drives, the high-frequency noise emission depends on the grid impedance value as well. Hence, the high-frequency harmonic emission of the SDLC drive is not predictable at the system level due to different grid impedance of the weak and stiff grids.

B. HARMONIC ANALYSIS OF MULTI-DRIVES AT A SYSTEM LEVEL

In a typical distribution network system, a number of power electronics converters including motor drive systems may be connected to a low-voltage distribution network in a commercial or an industrial segment. In order to analyze harmonics and power quality issues of the motor drives topologies, first a SDLC motor drive connected to a low-voltage distribution system is considered. It is assumed that "n" numbers of SDLC drives are connected in parallel at a PCC as shown in Fig. 10. Interconnection impedances between the drives

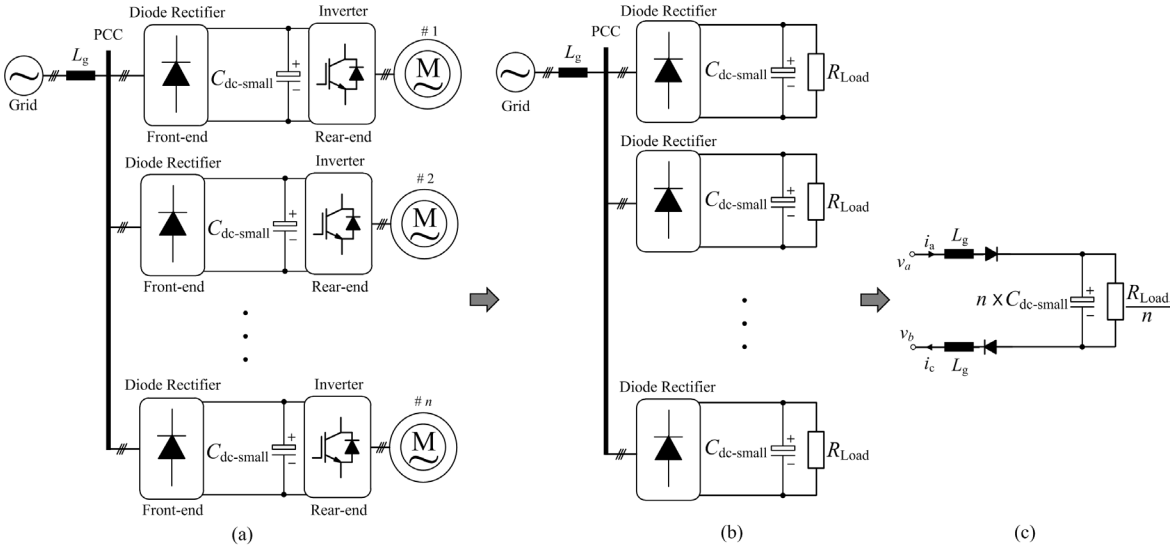

FIGURE 10. Block diagram of multi-drive configuration: (a) A low-voltage distribution network with "*n*" number of drives (b) Simplified model of the multi-drive system (c) An equivalent impedance model of the multi-drive system.

are assumed to be negligible and the low-voltage distribution transformer is defined as the major inductive impedance of the system at the grid side.

In order to simplify the configuration and analyze the multi-SDLC drives at a system level, the grid voltage is assumed to be an ideal voltage source – balanced with no distortion – and only the SDLC drives at a same power level are connected to the grid. Similar to the above analysis, the equivalent circuit of each drive (refer to Fig. 3) is considered for a multi-drive analysis and the system configuration is shown in Fig. 10. As the drives are connected in parallel, the equivalent impedance model of the whole system is shown in Fig. 10(c). The load power level of each drive is modeled as a resistor (R_{Load}) connected in parallel across the DC-link capacitor. Thus, the total load power and the DC-link capacitor of the multi-drive system are modeled as R_{Load}/n and $nC_{dc-small}$, respectively.

The impedance of the multi-drive system is calculated as follows:

$$Z_{in_s} = \frac{1 - 2\omega^2 L_g(nC_{dc-small}) + j\omega \dfrac{2L_g}{\left(\dfrac{R_{Load}}{n}\right)}}{j\omega(nC_{dc-small}) + \dfrac{1}{\left(\dfrac{R_{Load}}{n}\right)}} \tag{20}$$

At the system level, the resonant frequency is decreased when the number of the drives is increased. As given below, the resonant frequency (f_{o_s}) of the system with "n" drives is reduced by the factor of $1/\sqrt{n}$, while the damping factor (ξ_s) is increased by a factor of $\sqrt{n}$. This may affect specific harmonic orders at a new resonant frequency – depending on the grid impedance and the number of units. This harmonic issue is not considered at the unit level.

$$\left.\begin{aligned} f_{o_s} &= \frac{1}{2\pi\sqrt{2L_g C_{dc-small}}} \cdot \frac{1}{\sqrt{n}} \\ \xi_s &= \frac{1}{2R_{Load}}\sqrt{\frac{2L_g}{C_{dc-small}}} \cdot \sqrt{n} \end{aligned}\right\} \tag{21}$$

In order to analyze the current harmonics emissions and power quality issues of a multi-drive system based on system parameters mentioned in Table 1, the following cases have been defined:

a) The number of drives n =1, 5 and 10
b) $C_{dc-small} = 30\ \mu$F
c) $L_g = 128\ \mu$H. Each SDLC motor drive operates at 1 kW.

Fig. 11 shows the resonant frequencies of the SDLC drives, which are changed from 574 Hz to 1816 Hz. According to the simulation results, 10 SDLC drives have a lower resonant frequency (at 574 Hz) than the single SDLC drive (at 1816 Hz). This resonant effect – at the system level – is almost negligible for the conventional drives as the resonant frequency of the single unit is designed at 150 Hz. Thus, a resonant frequency of a multi-parallel conventional drives can be reduced below 150 Hz in which no significant harmonics are generated by power converters between 50 and 150 Hz.

In order to study the harmonic emissions of the multi drives at the system level and compare it with the single SDLC drive, additional time-domain simulations have been carried out and the results are shown in Fig. 12. It is also important to analyze and compare the damping factors of the SDLC drives at different output power levels. As shown in Fig. 12(a), a single SDLC motor drive is simulated in time domain at different power levels (1, 2, 3, 10, 20, 30 and 100 kW) and the

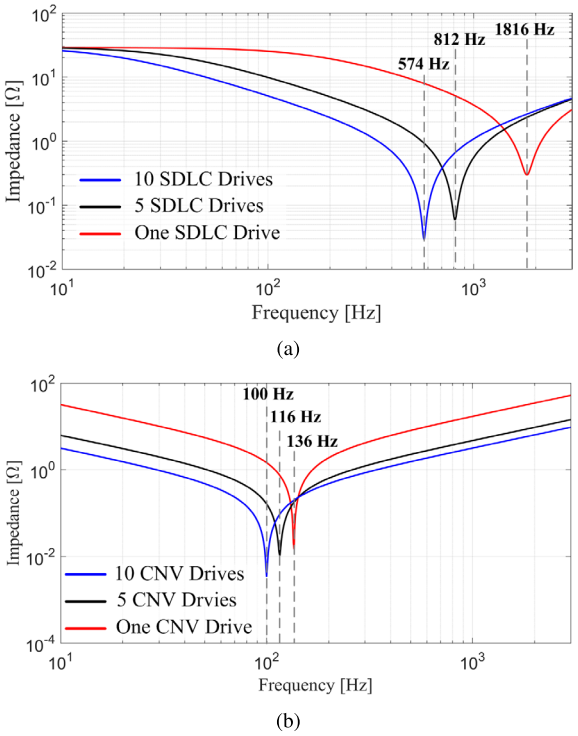

FIGURE 11. A comparison between the system input impedances of SDLC and conventional drives at total output power of 10 kW: (a) Single, five and ten SDLC drives, (b) Single, five and ten conventional drives.

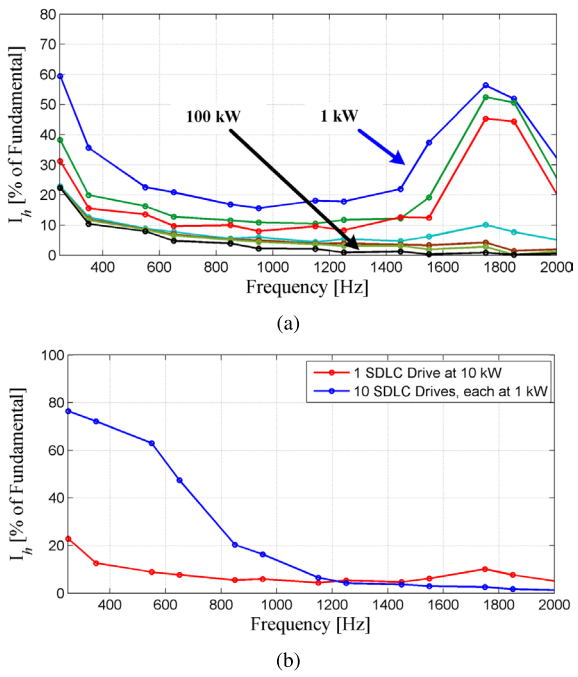

FIGURE 12. (a) Line current harmonics emissions of a single SDLC drive at different output power levels, (b) Line current harmonics emissions of a single and 10 SDLC drives, both at total power of 10 kW.

line current harmonics (0–2 kHz) have been extracted based on Fast Fourier Transform (FFT). When the power level is increased, the current harmonics emissions (in percentage)

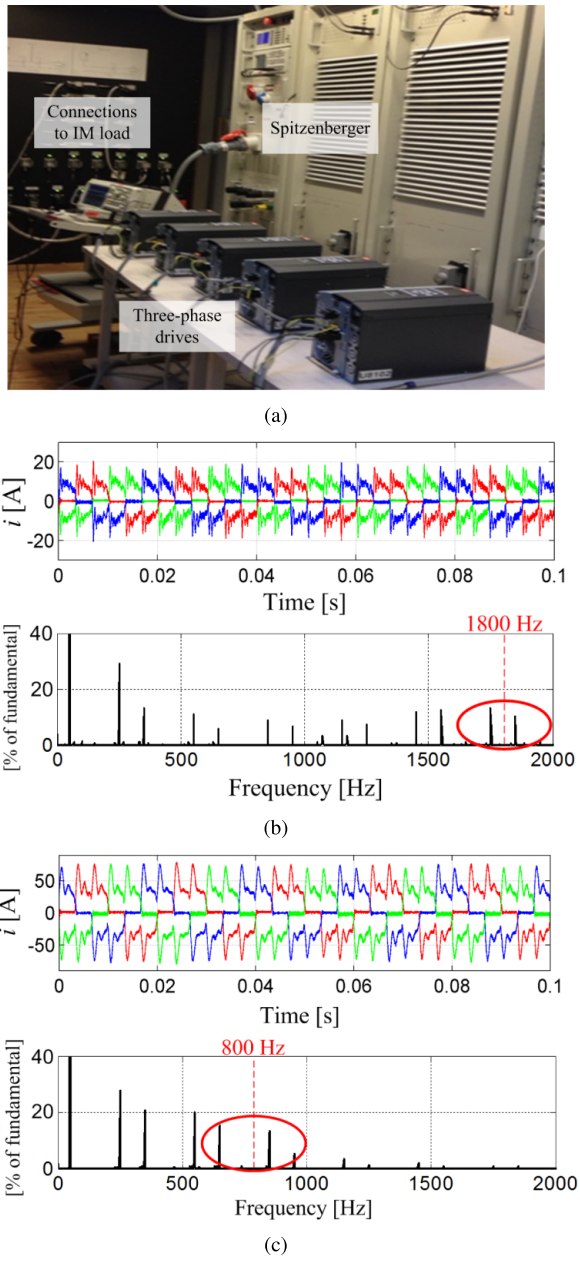

FIGURE 13. Test results, line currents in time and frequency domain (i_h/i_1); (a) Test setup for multi-drive systems, (b) Single SDLC Drive, (c) Five SDLC Drives.

are decreased around the resonant frequency due to better damping factors. Thus, the performance of the SDLC drive can be improved significantly at a full power level compared to a partial load power.

Fig. 12(b) shows the harmonic performances of two systems, a) a single SDLC drive at 10 kW with a resonant frequency at 1816 Hz and b) 10 SDLC drives each at 1 kW with a resonant frequency around 574 Hz. It is obvious that for the same total power of 10 kW, the performance of the multi drives are significantly affected at the system level due to shifting of the resonant frequency and poor damping.

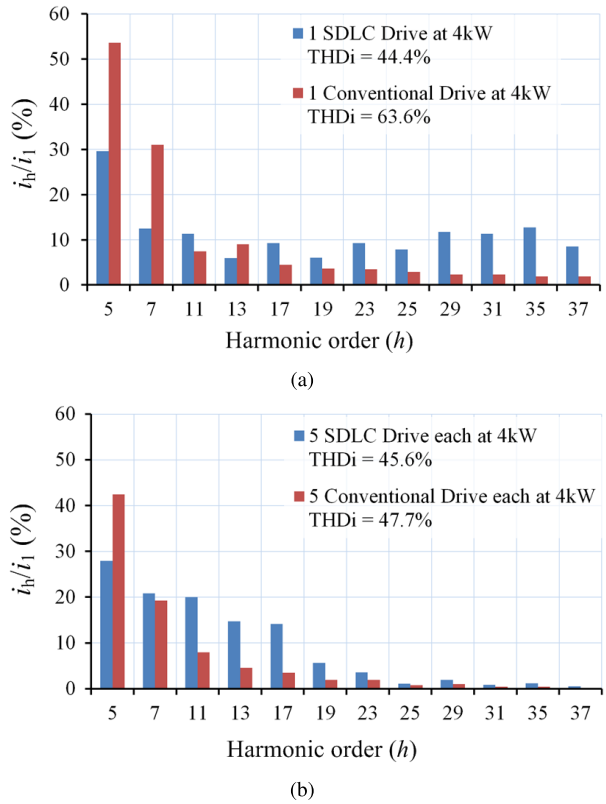

FIGURE 14. Comparative experimental results based on line input current harmonics in: (a) Single conventional and SDLC drives, (b) Five conventional and SDLC drives.

IV. TEST RESULTS

In order to validate the modeling and the simulation results, 7.5 kW three-phase SDLC motor drives have been developed with DC-link capacitor $C_{dc-small}$ =30 μF and without any DC-link choke. The SDLC drive has been compared with a conventional drive with L_{dc-cnv} = 1.25 mH and C_{dc-cnv} =500 μF. Two configurations (a single drive and five parallel drives) have been considered for tests and evaluations. The drives have been tested with a Spitzenberger grid simulator with a line inductance of 128 μH as shown in Fig. 13(a). The resonant frequencies of a single and five SDLC drives are 1816 Hz ($\sim$ the 35th and 37th harmonics) and 812 Hz ($\sim$ the 17th harmonic), respectively as shown in Fig. 11(a). As mentioned in the previous sections, the resonant frequencies of the conventional drives – a single drive or multi drives – are below 150 Hz, which do not affect current harmonics emissions of the system, when the number of drives is increased.

Fig. 13(b) shows the line current harmonics of the single SDLC drive at which its current harmonics have been affected around the resonant frequency (1816 Hz). When the number of the SDLC drives is increased to five units, the resonant frequency of the system is decreased from 1816 Hz down to 812 Hz. In fact, the same drives – each operating at the same load condition – have different harmonic performances at a system level (multi-drive) due to the shifting of the

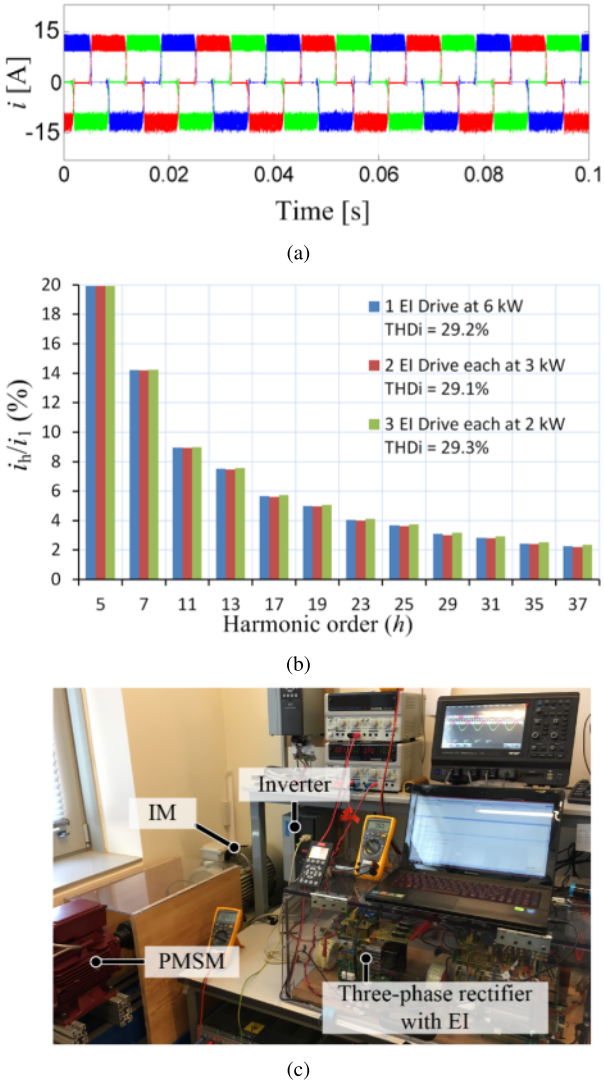

FIGURE 15. Experimental results; input currents of EI drive: (a) Single EI drive at 6 kW, (b) Comparative harmonic spectrum, (c) Test setup for EI drive.

resonant frequency. This has been verified by the system tests as shown in Fig. 13(c).

Several other tests have been carried out for the conventional drives – a single and five units – at the same power levels and the results have been analyzed and compared with the SDLC drives. Fig. 14(a) shows that the low order line current harmonics of the SDLC drive (the 5th and the 7th) are much lower than the conventional drive while the high order harmonics of the SDLC drive are higher in magnitude. Fig. 14(b) shows the effects of the resonant frequency on the line current harmonics. In fact, when the number of drives is increased, the line current harmonics and consequently the voltage harmonics will be affected accordingly.

As the EI drive has a controlled current source at the DC-link side, hence its line current is almost square wave based on the conduction angles of the three-phase diode rectifier. Therefore, at the system level, when few of them are connected in parallel, the current harmonics are not changed

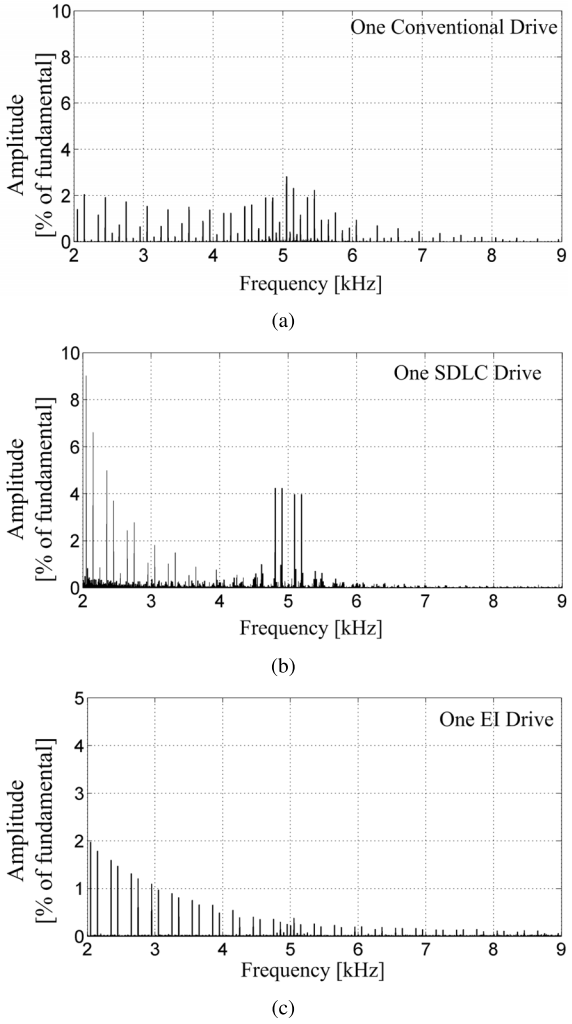

FIGURE 16. Experimental drives input current harmonic emissions between 2 and 9 kHz in, (a) One conventional drive, (b) One SDLC drive, (c) One EI drive.

in percentage. In Fig. 15, the test results show that the line current is almost square-wave and current harmonic magnitudes and THD_i values are not changed for few drives in parallel operating at the same total power.

Fig. 16 shows the test results of three different drives for the frequency range of 2–9 kHz based on the system parameters given in Table 1. These test results show that the SDLC drive cannot suppress high-frequency current harmonics generated by the load – inverter at the DC-link side – while the conventional drive has a better performance. However, the EI drive has the best harmonic performance for this frequency range as the EI generate a high impedance at the rectifier side and can buffer the inverter noise significantly. As discussed in the previous section, the EI circuit at the DC-link side generates ripple current and high-frequency noise, depending on its system parameters such as the inductor size and type and the switching frequency and transient times. Although the main focus of the paper is on the frequency range of 0–9 kHz, in order to clarify this issue, additional high-frequency tests have been performed for the EI drive for the frequency range

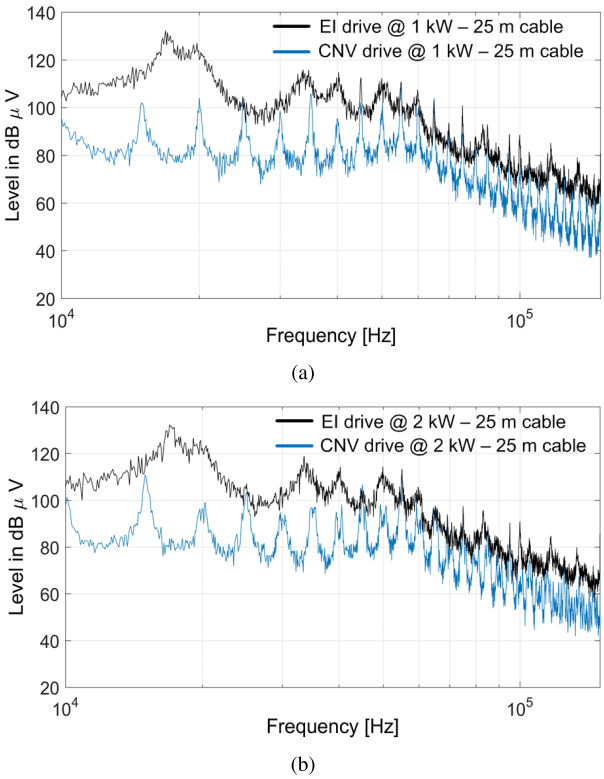

FIGURE 17. Test results: comparative noise emission spectrum (10–150 kHz) performed using a LISN network with the laboratory motor drive setup; a motor cable length of 25 m with the conventional and the EI-based drives at: (a) Output power of 1 kW, and (b) Output power of 2 kW.

of 10–150 kHz as shown in Fig. 17. It is obvious that high-frequency noise generated by a power electronics system may damage sensitive measuring devices like a harmonic receiver. Therefore, in order to reduce high-frequency noise level, an Electromagnetic Interference (EMI) filter has been placed at the input side of the converter in order to measure the high-frequency noise (above 9 kHz) generated by the EI drive.

Although, in all power electronics system an EMI filter is required to reduce conduced emission noise below a certain limit, hence it is not easy to compare high-frequency noise emission of all drives with one EMI filter. On the other hand, the EMI filter of a power converter needs to be optimized with respect to its configuration, topology, operating mode and application. In a motor drive system, common-mode and differential-mode noises are generated due to different couplings and PWM strategies. The electronic inductor generates mainly a differential mode noise however its high impedance at the DC-link side can affect the overall performance of the system including the EMI filter. Thus, Fig. 17 shows only the noise emission of the harmonics generated by the whole system and it is compared with the conventional drive with the same EMI filter.

V. CONCLUSION

In this paper, grid connected three-phase motor drive systems with different front-end topologies have been analyzed at a

unit and a system level. The analysis shows that the resonant frequencies of the single and the multi-drive systems are affected by the size of the DC-link components and the grid configuration. The resonant frequency of the SDLC drive is higher than the conventional and EI drives due to the small DC-link capacitor, which has a large impact on line current harmonics emissions and consequently on power quality of the system. One of the main factors which can control the power quality and current harmonics emissions is the damping factor of the system, which depends on the drive characteristics and operating mode. The simulations, analyses and test results show that the single and multi-SDLC drives operating at high power levels have a better harmonic performance at a broad range of frequency while at partial power their performances depend on the grid configuration, drive parameters and load profile. On the other hand, the conventional and the EI drives have consistent harmonic emissions for the frequency range of 0–2 kHz. Harmonic emissions of these three different drives have been analyzed and tested for the frequency range of 2–9 kHz and the results show that the SDLC drives have less capability to buffer high-frequency noise generated by the inverter at the motor side. EMI filter types and configurations including all capacitive couplings within a drive have a big impact on the circulating common-mode and differential-mode currents. Thus to improve the overall harmonic performances of the drives for the high-frequency range of 2–9 kHz and above, the whole system and layout need to be optimized with respect to all converter design factors and applications.

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