IEEE Access
Multidisciplinary | Rapid Review | Open Access Journal

Received November 2, 2016, accepted November 18, 2016, date of publication December 13, 2016, date of current version March 8, 2017.

Digital Object Identifier 10.1109/ACCESS.2016.2636128

Design and Analysis of Multiplier Using Approximate 15-4 Compressor

R. MARIMUTHU, (Member, IEEE), Y. ELSIE REZINOLD, AND P. S. MALLICK, (Senior Member, IEEE)
School of Electrical Engineering, VIT University, Vellore 632014, India
Corresponding author: P. S. Mallick (psmallick@vit.ac.in)

ABSTRACT This paper presents the design of approximate 15-4 compressor using 5-3 compressors as basic module. Four different types of approximate 5-3 compressors are used in a 15-4 compressor for less power consumption and high pass rate. We have analysed the results in all the cases. A 16 × 16 bit multiplier is simulated using the proposed 15-4 compressor. Simulation results show that the multipliers with proposed approximate compressors achieve significant improvement in power as compared to the multipliers with accurate 15-4 compressor. Pass rate of the proposed multipliers are high as compared to other existing approximate multipliers. Finally, the proposed multiplier is used in image processing applications, where the peak signal to noise ratio of the image is measured. Quality of the image is compared with an accurate multiplier and the obtained results show that our proposed multiplier performs better than existing approximate multiplier.

INDEX TERMS Approximate 5-3 compressor, approximate 15-4 compressor, multiplier, image processing, higher order compressor.

I. INTRODUCTION

Microprocessors and Digital Signal Processors (DSP) are playing a significant role to handle the complexity of digital signal. About 95% of the processors in the market are based on digital signal [1]. Digital signal processors take care of convolution, correlation and filtering of digital signal [2]. Multipliers, shifters and adders are mainly used to accomplish these tasks. Among the three modules, multiplier is the most complex one. Multipliers take more time and consume higher power than other two modules [3]. Multipliers have three phases - generation of partial products, reduction of partial products and final stage addition. Reduction of partial products take much time and power in the multiplier. Many techniques were proposed to reduce the critical path in the multiplier [4], [5]. Among them, the use of compressors in partial product reduction stage is the most popular. Compressors are basic circuits which are made of full adders or half adders to count the number of ''ones'' in the input. Several compressors are required in the partial product reduction stage. Various compressors such as 3-2, 4-2, 5-2 and 5-3 were proposed by researchers in the last 20 years [6]–[9]. These are useful only when the size of multiplier is small. 16 × 16, 32 × 32 bit multipliers require large size of compressors. High order compressors provide better results in terms of power and speed [10]–[12]. But it consumes more area than low order compressors.

All these techniques perform the exact computation and modules produce the correct result. Accuracy of the module/device is always 100% in exact computing. But exact computing has one major drawback. It is not possible to optimize all the parameters of the circuit in exact computing. However, exact computing is not essential for every application. There are some applications like image processing and multimedia can tolerate errors and provide meaningful results. Inexact (approximate) computing techniques have become popular because of its low complexity and less power consumption. Inexact computing produces reasonable result, even it has low accuracy. In approximate computing, the value of error rate (ER), error distance (ED) and normalized error distance (NED) play an important role to calculate the final output [13]. Error rate is given by a number of erroneous outputs over the total number of outputs. Error Distance is the arithmetic distance between an erroneous output and the correct one. Normalized Error Distance is the ratio of mean error distance over all inputs by maximum input of the circuit. Several approximation techniques were proposed for adders and multipliers [14]–[32]. From central point to the most significant bit (MSB) is called accurate and to the least significant bit (LSB) is called inaccurate part of adders which was discussed by Zhu *et al.* [14]. Inaccurate computing in MSB side causes large error. The normal addition rule is applied in accurate part whereas a special method of addition takes place

in inaccurate part. Output ''sum'' value is calculated normally when any one of the operand value of adder is ''0''. When both operands are ''1'', ''sum'' value can be fixed as ''1'' from that bit position to least significant bit. This technique is used to minimize the error distance of the adder.

Approximate XOR/XNOR adder for inexact computing is proposed by Yang *et al.* [15]. Both XOR and XNOR gates are required to calculate the output of the adder. Three different approximate methods were proposed. The output expression for ''sum'' and ''carry'' is approximated. Instead of using two XOR gates, only one XNOR gate has been utilized to calculate ''sum''. Similarly, one XOR, one OR and two AND gates are used for ''carry''. Low power imprecise adder were proposed by Jiang *et al.* [16] where they optimized transistor count, power consumption and power delay product (PDP) of the adder. Moreover, the number of incorrect outputs of the adder is also small. In [17] and [18], accuracy, error distance and various design parameters of approximate adders are analysed and compared.

Approximation methodologies were applied in generating the partial product phase [19]. A 2 × 2 bit approximate multiplier is designed by altering the one output combination. In this technique, multiplier produces ''7d'' when it multiplies ''11'' by ''11''. But the actual output of the multiplier is ''1001''. The probability of getting error in this multiplier is 0.0625. An error has been introduced in the partial product generation phase. Adder tree (reduction tree) of this multiplier is same as accurate multiplier.

Several other approximation techniques were proposed in the partial product reduction stage [20]–[27]. One need not consider the particular row of partial products when the value of multiplier bit is ''0'' also particular column value can be skipped when multiplicand bit is ''0''. This technique is called row and column bypassing [20], [21]. In [22], some of carry-save adders are skipped in both horizontal and vertical directions based on the number of zeros in the multiplier input. In [23], partial product tree is splitted into two parts. Accurate multiplier was used in MSB side of the multiplier. No multipliers was used in LSB side where approximation rule was applied.

In [24], ''n'' bit multiplier was implemented by two ''n/2'' bit sub-multipliers. Then, most significant ''n/2'' multiplier was implemented by two further ''n/4'' sub multipliers and least significant ''n/2'' multiplier was implemented by an approximate ''n/4'' multiplier. Then, all partial products are accumulated by a Wallace tree. Every proposed technique has its own merits and demerits. But in accuracy point of view, all techniques have high normalized error distance (NED) and a low pass rate. Pass rate of the multipliers discussed so far is almost 0%. The performance of the approximate multiplier is not only decided by the circuit metrics. It is also based on the error tolerance [28]. Getting low error and better circuit performance are always challenging.

Various inaccurate compressors were introduced in the reduction tree [29]–[33]. Compressors can handle large number of inputs than half and full adders. 4-2 compressor is widely used by various researchers which reduces the four partial products into two partial products. The probability of getting an error in approximate 4-2 compressor is 0.003 which is very minimum than any inaccurate adder circuit [29]. In [30], different approximate compressors are proposed and utilized in 16 × 16 bit Vedic multiplier. 4-2 compressor is further optimized to get the best power and lower delay with compromising accuracy [31]. Two designs of approximate 4-2 compressor are proposed in this paper. Design 2 of approximate 4-2 compressor is the best compressor in recent days. In [28], the performance of various multipliers was compared. It was found that, introducing compressors in the partial production tree gives the lowest error rate, minimum normalized error distance and decent circuit metrics. In this paper, we have proposed higher order compressor for 16 × 16 bit multiplier. Use of several approximate 4-2 compressors in large size multiplier causes large error. It is necessary to get a minimum error as well as decent circuit performance.

The paper is organized as follows. Designs of approximate 5-3 compressors are elaborated in section II. Design of 15-4 compressor using 5-3 compressor is described in section III. Section IV describes design of 16 × 16 multiplier. Result analysis is described in section V. Image processing application using proposed multiplier is given in section VI. Finally, the conclusion is presented.

II. DESIGNS OF APPROXIMATE 5-3 COMPRESSORS

In this section, four designs of a 5-3 approximate compressor are presented. 5-3 compressor has five primary inputs $(X_0, X_1, X_2, X_3, X_4)$ and three outputs (O_0, O_1, O_2). This compressor uses the counter property. Output of the compressor depends on number of ones present at input. This proposed compressor also called as 5-3 counter [11]. In this paper, we have called this module as a compressor because this module compresses five bits into three bits. We have chosen 5-3 compressor because it is a basic module for 15-4 compressor. Error rate and error distance of each design are considered.

A. DESIGN 1

In this design, initially output O_2 of 5-3 compressor is approximated. Logical AND between inputs X_3 and X_2 matches with accurate output O_2 of the conventional 5-3 compressor with an error rate of 18.75%. The following expressions show design 1 of 5-3 approximate compressor. Figure 1 shows the design1 of approximate 5-3 compressor.

$$O_2' = X_3 \bullet X_2 \tag{1}$$

$$\begin{aligned} O_2 = {} & (X_0 \bullet (\sim (X_0 \oplus X_1)) + X_2 \bullet (X_0 \oplus X_1) \\ & \bullet (X_3 \bullet (\sim (X_0 \oplus X_1 \oplus X_2 \oplus X_3)) \\ & + X_4 \bullet (X_0 \oplus X_1 \oplus X_2 \oplus X_3) \end{aligned} \tag{2}$$

$$\begin{aligned} O_1 = {} & (X_0 \bullet (\sim (X_0 \oplus X_1)) + (X_2 \bullet (X_0 \oplus X_1)) \\ & \oplus (X_3 \bullet (\sim (X_0 \oplus X_1 \oplus X_2 \oplus X_3))) \\ & + (X_4 \bullet (X_0 \oplus X_1 \oplus X_2 \oplus X_3 \oplus X_4))) \end{aligned} \tag{3}$$

$$O_0 = X_0 \oplus X_1 \oplus X_2 \oplus X_3 \oplus X_4 \tag{4}$$

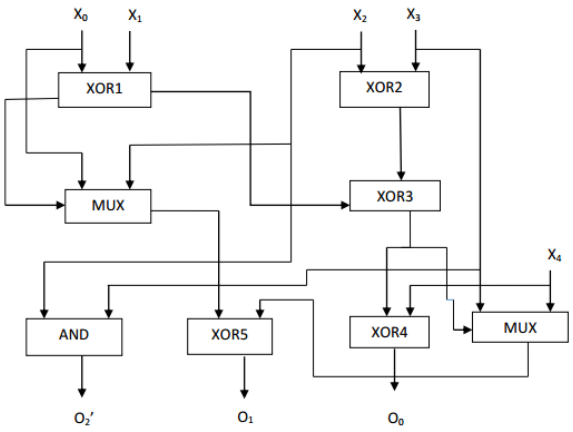


FIGURE 1. Approximate 5-3 compressor (Design 1).

O'_2 is the approximated output and O_2, O_1, O_0 are the accurate output of the 5-3 compressor. The approximated output matches with the accurate output for 26 inputs out of 32 inputs. Table 1 shows the error distance between approximate O'_2 and actual output O_2.

TABLE 1. Relationship between approximated (O'_2) and accurate output (O_2, O_1 and O_0).

X[4 : 0]	O'_2	O_2	O_1	O_0	Error Distance
0	0	0	0	0	0
1	0	0	0	1	0
2	0	0	0	1	0
3	0	0	1	0	0
4	0	0	0	1	0
5	0	0	1	0	0
6	0	0	1	0	0
7	0	0	1	1	0
8	0	0	0	1	0
9	0	0	1	0	0
10	0	0	1	0	0
11	0	0	1	1	0
12	1	0	1	0	4
13	1	0	1	1	4
14	1	0	1	1	4
15	1	1	0	0	0
16	0	0	0	1	0
17	0	0	1	0	0
18	0	0	1	0	0
19	0	0	1	1	0
20	0	0	1	0	0
21	0	0	1	1	0
22	0	0	1	1	0
23	0	1	0	0	-4
24	0	0	1	0	0
25	0	0	1	1	0
26	0	0	1	1	0
27	0	1	0	1	-4
28	1	0	1	1	4
29	1	1	0	1	0
30	1	1	0	1	0
31	1	1	0	1	0

In this design, only O_2 is approximated and O_1, O_0 are same as original expression. Here, O_2 and O_1 have weightages of 4 and 2; the weightage of O_0 is 1. In this design, the error distances for remaining 6 error cases are either 4 or -4. In order to get the minimum error distance, the output O_0 of 5-3 compressor is replaced by following expression.

$$\begin{aligned} O'_0 = {} & [(X_3 \bullet X_2 \bullet (\sim X_1) \bullet (\sim (X_0)) \\ & + ((\sim X_4) \bullet X_3 \bullet X_2 \bullet (X_1 \oplus X_0)) \\ & + (X_4 \bullet X_1 \bullet X_0 \bullet (X_2 \oplus X_3))]? \\ & \times (\sim (X_3 \bullet X_2)) : (X_4 \oplus X_3 \oplus X_2 \oplus X_1 \oplus X_0) \end{aligned} \quad (5)$$

Finally, O_1 is kept as original expression. O_2 replaced by O'_2 and O_0 is replaced by O'_0 to get the minimum error distance. Maximum error distance is 4 for only one input pattern (i.e input number 12) and in the remaining five cases; the error distance is either $+3$ or -3. Critical path of this design is higher than accurate design. This design has additional logic gates such as one MUX and one XOR in critical path when compare to accurate design.

TABLE 2. Error cases and distance of design 2.

X[4 : 0]	O'_2	O_2	O_1	O'_1	O'_0	Error Distance
9	0	0	1	0	0	-2
10	0	0	1	0	0	-2
12	0	0	1	0	0	-2
15	0	1	0	1	0	-2
16	0	0	0	1	1	2
19	1	0	1	0	1	2
21	1	0	1	0	1	2
22	1	0	1	0	1	2

B. DESIGN 2

In this design, O_2, O_1 are approximated and O_0 is kept as the same as original expression. Error distance of all the error cases is either -2 or $+2$. From the truth table, it can be noted that pass rate of O'_2 is 87.5% when O_2 alone is replaced with O'_2 in a 5-3 compressor. Similarly, pass rate of O'_1 is 75% when compared with the O_1 output of the 5-3 compressor. Expression for O'_2 and O'_1 are modified to get the minimum error distance. The overall pass rate of this design is 75%. The output of the compressor differs only in eight input cases. Table 2 shows all error cases and the error distance between actual and approximated outputs. In this design, the critical path is between input X_0 and output O_0. Four XOR gates are involved in the critical path. This design has least critical path than other proposed designs. Figure 2 shows the logic diagram of design 2 approximate 5-3 compressor.

$$\begin{aligned} O'_2 = {} & X_4 \bullet [X_0 \bullet (\sim (X_0 \oplus X_1)) \\ & + (X_2 \bullet (X_0 \oplus X_1))] \end{aligned} \quad (6)$$

$$\begin{aligned} O'_1 = {} & X_4 \oplus [X_0 \bullet (\sim (X_0 \oplus X_1)) \\ & + (X_2 \bullet (X_0 \oplus X_1))] \end{aligned} \quad (7)$$

C. DESIGN 3

In this design, only output O_1 is replaced by O'_1. Expression for O'_1 is given below. Remaining outputs of the compressor (O_0 and O_2) are kept same as original expression. The pass

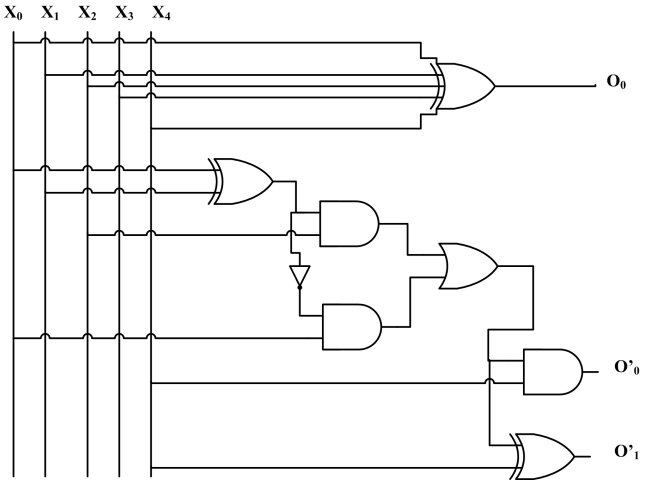


FIGURE 2. Logic diagram of design 2 approximate 5-3 compressor.

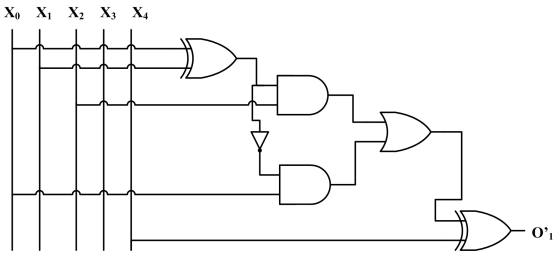


FIGURE 3. Logic diagram of output O'_1.

rate of the compressor is 75% and error distance is either +2 or −2. In this design, the critical path has three XOR, two AND, one OR and one inverter gates. Figure 3 shows the logic diagram of output O'_1 in design 3 approximate compressor.

$$O'_1 = X_4 \oplus [X_0 \bullet (\sim (X_0 \oplus X_1)) + (X_2 \bullet (X_0 \oplus X_1))] \quad (8)$$

D. DESIGN 4

In this design, output of O_1 expression is approximated (O'_1) and expressions for O_0 and O_2 are kept as an accurate. Expression for approximated O'_1 is given below.

$$O'_1 = X_2 \oplus X_3 \quad (9)$$

Only one X-OR gate is utilized to get approximated O'_1. The length of the critical path is same as design 3. This consumes the lesser area and power than the other proposed 5-3 compressor designs. But the pass rate of this compressor is 62.5% and the maximum error distance is either +2 or −2.

III. DESIGN OF 15-4 COMPRESSOR

This section describes the design of 15-4 compressor using approximate 5-3 compressors. The 15-4 compressor was proposed in [12] as shown in figure 4. This compressor has fifteen inputs (X0 - X14) and it produces four outputs (O0 - O3).

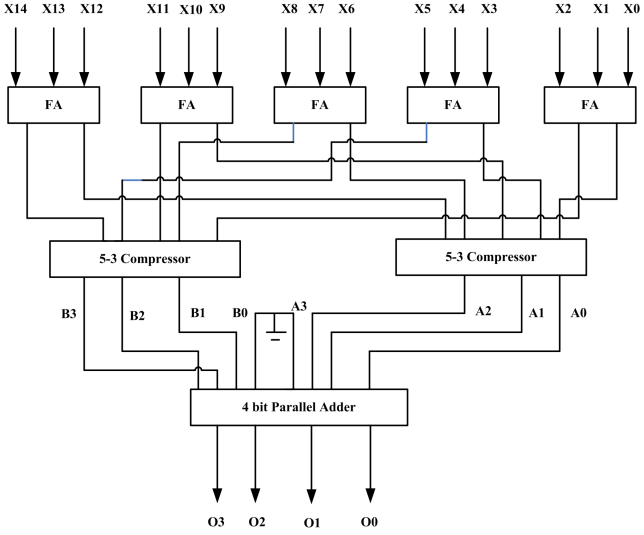


FIGURE 4. Design of accurate 15-4 compressor [12].

This compressor has five full adders at first stage, two 5-3 compressors in second stage and final stage has parallel adder. Each full adder receives three primary inputs and it generates "Sum" and "Carry". "Sum" of all full adders is given to the 5-3 compressor. Similarly, "Carry" of all full adders is given to another 5-3 compressor. Outputs of the 5-3 compressors are given to the parallel adder. Parallel adder is used to generate the final output. In approximate 15-4 compressor, instead of using accurate 5-3 compressors, we have used proposed approximate 5-3 compressors. Full adders and parallel adders are kept as original adders in proposed 15-4 compressor.

Four approximate designs of 15-4 compressor are proposed. 5-3 compressors are used in first three designs of approximate 15-4 compressor which uses the design 1, 2 and 3 of proposed approximate 5-3 compressor. Design 1 and design 4 of proposed approximate 5-3 compressor are used in design 4 of 15-4 compressor. Design 1 approximate 5-3 compressor is used to handle "carry" signals because output "carry" has more weightage than "sum". Moreover, a pass rate of design 1 compressor is higher than design 4. Design 4 approximate 5-3 compressor is used to handle sum signals.

IV. MULTIPLIER DESIGN

In this section, design of 16 × 16 multiplier is presented. Four approximate multipliers are designed using the proposed four 15-4 compressors. In addition to this, one accurate multiplier and four other approximate multipliers are considered. Approximate multipliers using the proposed approximate 15-4 compressors are compared with the accurate 16 × 16 multipliers with accurate 15-4 compressors and also with other multipliers designed using various other approximate compressors. Figure 5 shows the design of 16 × 16 bit multiplier using 15-4 compressor where, each dot represents

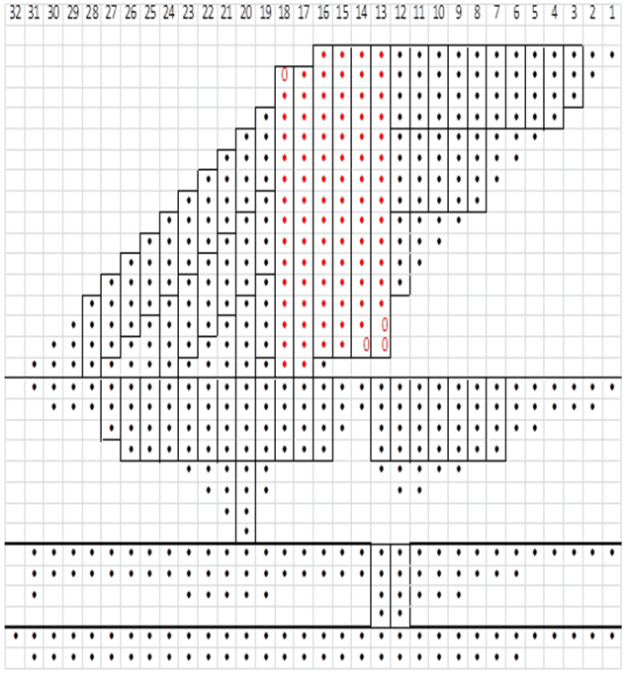


FIGURE 5. Design of 16 × 16 Multiplier using 15-4 compressor.

one partial product. Six 15-4 compressors are used to design one multiplier in the partial product reduction and finally four multipliers are designed.

In figure, rectangular boxes indicate the use of 15-4 and 4-2 compressor in the multiplier. 15-4 compressors are used in the multiplier from 13^{th} column onwards. Column number 13 of the multiplier has only thirteen partial products. Two zeros are added in that column to make use of the 15-4 compressor. Similarly, one "0" is added in 14^{th} column. Along with 15-4 compressors in the multiplier other accurate compressor like 4-2 and half, full adders are used for partial product reduction. Approximate compressors are used in 13^{th}, 14^{th} and 15^{th} column of multipliers. Use of approximate compressors in most significant part would produce a larger error rate. Design 1 of 15-4 approximate compressor is used in multiplier 1. Similarly, design 2, 3 and 4 of 15-4 approximate compressors are used in multiplier 2, 3 and 4 respectively. In accurate multiplier, all accurate 15-4 compressors are used along with accurate 3-2 and 4-2 compressors.

Accurate 4-2 compressors, half and full adders are used in second and third stage of partial product reduction tree. In final stage, parallel adders are used to compute the final result.

V. SIMULATION RESULTS AND DISCUSSION

Xilinx software is used to verify the functionality of our design. The Cadence RTL compiler is used to calculate the power, speed and area. All designs are compiled with 90 nm technology and a typical library of Cadence is used to get the results. We have also discussed about the results of 5-3, 15-4 compressors and multipliers in this section.

TABLE 3. Simulation results of 5-3 compressor.

5-3 Compressor	Area (μm^2)	Power (μW)	Time (ηs)	Pass rate of 5-3 compressor
Accurate [9]	42.33	3.52	0.94	100%
Design 1 (Proposed)	52.21	3.04	1.06	81.25%
Design 2 (Proposed)	42.33	2.29	0.88	75%
Design 3 (Proposed)	43.04	3.10	0.90	75%
Design 4 (Proposed)	40.92	2.29	0.91	62.5%

A. RESULTS OF 5-3 COMPRESSORS

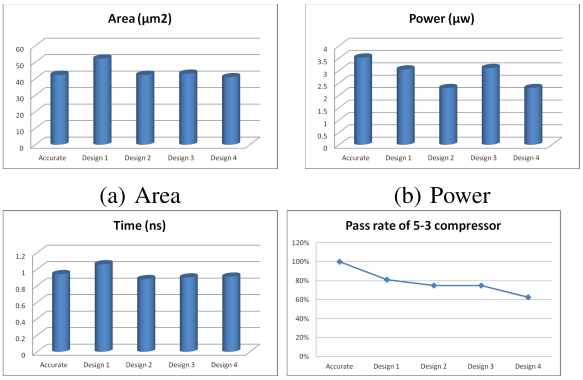
Simulation results of various 5-3 compressors are discussed here. Table 3 shows the pass rate and circuit metrics of 5-3 compressor. As expected, accurate 5-3 compressor has large delay and consumes more power than other designs. Design 1 of proposed 5-3 compressor consumes 13.63% less power than accurate, but it has 18.9% of area overhead and 11.4% more delay than accurate design because this design has a large number of gates and length of the critical path is also higher than accurate design. Power consumption of this design is considerably low because number of active cells in the critical path is lower than accurate design. The pass rate of this approximate compressor is high among other proposed designs.

Design 2 of proposed compressor provides a 34.9% power and 6.38% speed improvement than accurate design. In this design, we have approximated two outputs of the compressor. Moreover, the number of logic gates in the critical path is lower than accurate design. This leads to provide lower power consumption and high speed. Similarly, design 3 provides 11.9% power and 4.4% speed improvement than accurate design. Pass rate and error distance of design 2 and 3 are similar, except the number of outputs approximated.

Design 4 of 5-3 compressor provides 3.3% lesser area, 34.9% power and 3.19% speed improvement than accurate design. Design 3 and 4 produces the same speed. Power consumption of design 4 is better than design 3 because this design uses only one XOR gate to compute output (O_1). Pass rate of this design is low among other proposed designs. This improves the area and power. Figure 6 shows the results of 5-3 compressor in graphical form.

B. RESULTS OF 15-4 COMPRESSORS

This section describes the result of various 15-4 compressors. Table 4 shows the performance of 15-4 compressor and its error rate. Accurate compressor [12] is designed and compared with other approximate designs. Power consumption of design 1 is 3% better than accurate design. But area and delay of this design are larger than accurate design because 5-3 compressor used in 15-4 compressor is the design 1 of approximate 5-3 compressor. The error rate of this compressor is 35.4%. Figure 7 shows the performance of 15-4 compressor in graphical form.



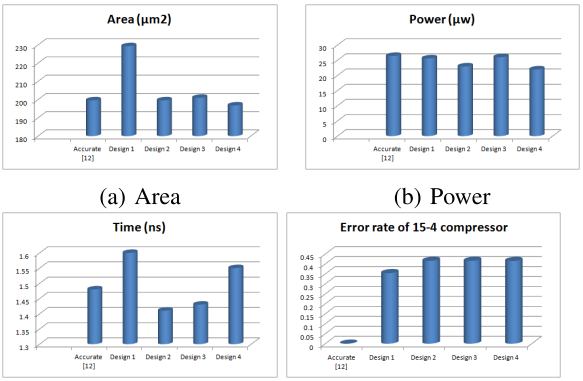
(a) Area (b) Power

(c) Time (d) Pass Rate

FIGURE 6. Graphical representation of 5-3 compressor results. (a) Area. (b) Power. (c) Time. (d) Pass rate.

TABLE 4. Result analysis of various 15-4 compressors.

15-4 Compressor type using	Area (μm^2)	Power (μW)	Time (ηs)	Error rate of 15-4 compressor
Accurate [12]	199.6	26.40	1.48	0
Design 1 (proposed)	229.3	25.59	1.60	35.4%
Design 2 (proposed)	199.6	22.94	1.41	41.57%
Design 3 (proposed)	201.0	26.0	1.43	41.57%
Design 4 (proposed)	196.8	21.95	1.55	41.5%



(a) Area (b) Power

(c) Time (d) Error Rate

FIGURE 7. Graphical representaion of 15-4 compressor results. (a) Area. (b) Power. (c) Time. (d) Error rate.

Design 2 provides the best results in terms of power consumption and speed. In this design, we have approximated two outputs of 5-3 compressor. Moreover, both expressions have common min-terms. This reduces the power consumption by 13% and speed increment by 4.74% than the accurate 15-4 compressor. But the overall error rate of design 2 and 3 compressor is 41.57%. In design 3, only O_1 is approximated in a 5-3 compressor. Speed and power improvement of this compressor is 4.75% and 1.5% respectively than accurate compressor.

Area optimization of design 4 is 1.4% and power gain is 17% than an accurate design with almost the same error rate of previous designs. In this design, 15-4 compressor uses design 1 and design 4 of 5-3 compressor. Design 4 of 5-3 compressor provides overall better performance. Design 1 of 5-3 compressor has the highest pass rate. The combination of two compressors gives better result than other proposed 15-4 compressors.

C. ANALYSIS OF 16 × 16 BIT MULTIPLIER

This section describes the performance analysis of various multipliers. Accurate multiplier using 4-2 compressor is designed and result of this multiplier is compared with other proposed multipliers. 10^6 random test vectors are applied to the multiplier and results are obtained. Table 5 shows the results of different 16 × 16 multipliers.

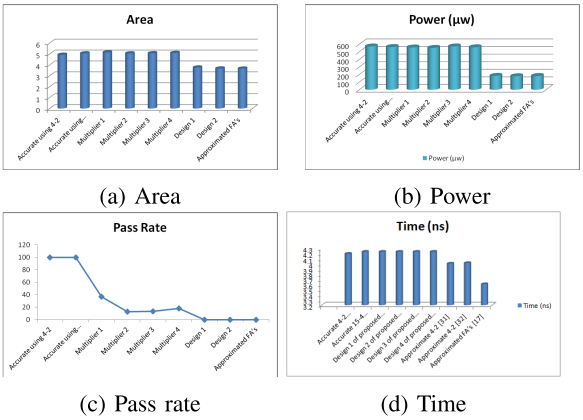
TABLE 5. Result analysis of different multipliers.

Multiplier Number	16 × 16 Multiplier using	Area (μm^2)	Power (μW)	Time (ηs)
1	Accurate 4-2 compressor [8]	4939.2	570.551	4.20
2	Accurate 15-4 compressor [12]	5066.2	563.20	4.24
3	Design 1 of proposed 15-4 compressor	5159.3	557.2	4.24
4	Design 2 of proposed 15-4 compressor	5066	551.92	4.24
5	Design 3 of proposed 15-4 compressor	5074	571.05	4.24
6	Design 4 of proposed 15-4 compressor	5104	560.2	4.24
7	Approximate 4-2 [31]	3764.3	182.87	4.01
8	Approximate 4-2 [32]	3671.2	178.11	4.02
9	Approximated FA's [17]	3662.02	181.28	3.61

Multiplier designed using accurate 15-4 compressor provides 1.3% less power and 2.5% area overhead than an accurate multiplier as calculated from table 5. Multiplier designed using 15-4 compressor has additional logic gates in critical path. This gives slightly more latency (around 1%) as compared to accurate multiplier designed using 4-2 compressor. Multiplier designed using 15-4 compressor has area overhead because the total number of gates in 15-4 compressor is higher. Power consumption is 2.3% less in multiplier designed using design 1 of proposed 15-4 compressor. But it has 4.2% area overhead. This multiplier has the largest area overhead. Similarly, multipliers using design 2 and design 3 of proposed 15-4 compressors take around 2.5% more area. Power reduction of multiplier using design 2 of proposed 15-4 compressor is 3.2%. But, power improvement of multiplier using design 3 of proposed 15-4 compressor is

same as accurate multiplier. 3.2% area overhead and 1.8% power improvement in multiplier using design 4 of proposed 15-4 compressor as calculated from table 5. Delay of multiplier designed using various proposed 15-4 compressors are same as multiplier designed using accurate 15-4 compressor because 15-4 compressors are used only in first stage of partial product reduction tree of the multiplier.

Multiplier designed using approximate 4-2 compressor and approximated full adders (FAs) provide the better result than other proposed multipliers. The multiplier using design 1 of approximate 4-2 compressor [31] provides 68% power reduction and 23.7% area improvement. Similarly, multiplier using design 2 of approximate 4-2 compressor [32] and multiplier using approximate full adders [17] provide 68.7% and 68.2% reduction in power respectively as calculated from table 5. Also, these multipliers occupy 25.6% and 25.85% lesser area than accurate design. Multipliers using approximated 4-2 compressor and approximated FAs have a lesser transistor count compared to accurate multipliers. This uses low power in multiplier design. Delay of multiplier designed using approximate 4-2 compressor [31], [32] is 5.4% less than multiplier designed using 15-4 compressor. Critical path of compressor used in this multiplier is optimized as compared to accurate 4-2 compressor. As expected, delay of multiplier designed using approximate FA's [17] is 14.8% lower than accurate 15-4 multiplier. Approximate adders are used in 4-2 compressor and it has least critical path among other 4-2 compressor. Figure 8 shows the performance of various multipliers in graphical form.



(a) Area (b) Power

(c) Pass rate (d) Time

FIGURE 8. Graphical representaion of 16 × 16 bit multiplier results. (a) Area. (b) Power. (c) Pass rate. (d) Time.

Error tolerance of multipliers using approximate 4-2 compressor and approximate FAs is not as good as proposed multipliers. Normalized error distances (NED) and pass rate are used to compare the multiplier performance. A pass rate of multipliers using approximated 4-2 compressor and approximated FAs are 0% and accurate multipliers are 100%. The pass rate of multipliers using design 1, 2, 3 and 4 of proposed 15-4 approximate compressor is 36.9%, 12.9%, 13.23% and 18.08% respectively. Similarly, average NED values of those

TABLE 6. Result analysis of different multipliers.

Multiplier Number	16 × 16 Multiplier using	Pass rate (%)	Average NED
1	Accurate 4-2 compressor [8]	100	0
2	Accurate 15-4 compressor [12]	100	0
3	Design 1 using proposed 15-4 compressor	36.9	3.91×10^{-5}
4	Design 2 using proposed 15-4 compressor	12.9	4.18×10^{-5}
5	Design 3 using proposed 15-4 compressor	13.23	4.26×10^{-5}
6	Design 4 using proposed 15-4 compressor	18.08	7.07×10^{-5}
7	Approximate 4-2 [31]	0	0.44
8	Approximate 4-2 [32]	0	0.02
9	Approximated FA's [17]	0	0.22

(a) (b)

FIGURE 9. Image representaion. (a) Original image. (b) Contrasted image.

multipliers are 3.91×10^{-5}, 4.18×10^{-5}, 4.26×10^{-5} and 7.07×10^{-5} respectively as calculated from table 6.

Average NED values of multipliers using approximate 4-2 compressors and approximated FAs are 0.44, 0.02 and 0.22 respectively. Inexact application prefers the multiplier with minimum average NED values. Approximated 4-2 compressors and approximated FAs based multipliers provide the excellent circuit performance than accurate multipliers with the limitations of pass rate and average NED values. Table 6 shows the pass rate and average NED values of various multipliers.

VI. APPLICATION: IMAGE PROCESSING

This section describes the application of our multipliers designed using approximate compressors. Image contrasting is done with the help of proposed multiplier. MATLAB is used to process the image. We have chosen one colour image from database. The size of our input image is 512 × 512. This image has RGB pixels. The total number of pixels in an input

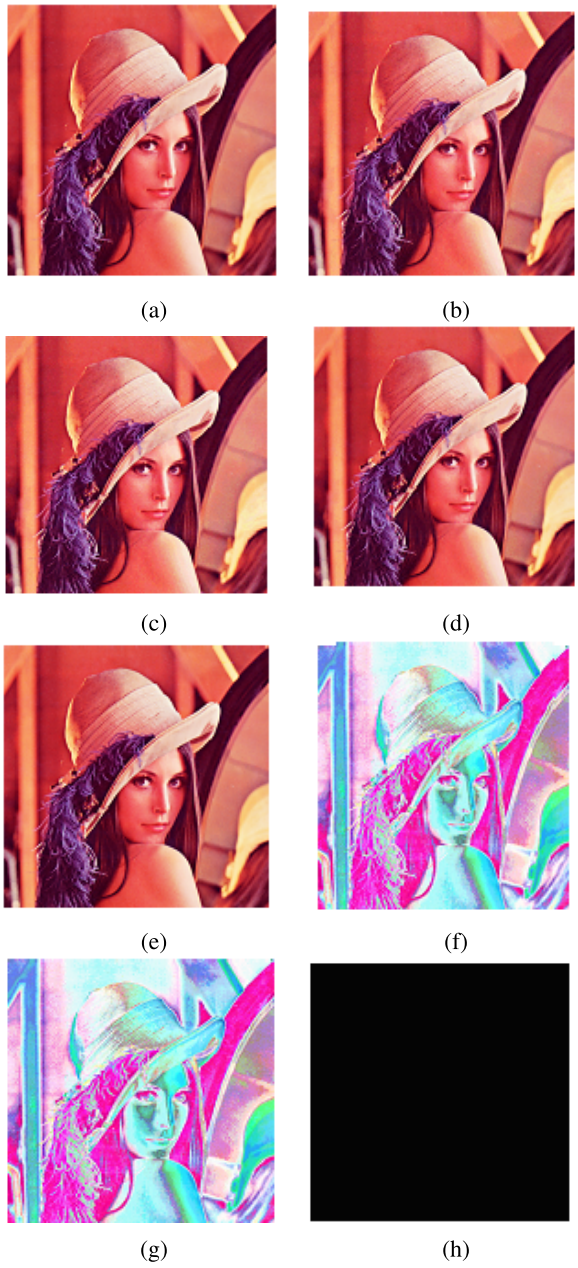


FIGURE 10. Image contrast results using various multipliers. (a) Multiplier 2. (b) Multiplier 3. (c) Multiplier 4. (d) Multiplier 5. (e) Multiplier 6. (f) Multiplier 7. (g) Multiplier 8. (h) Multiplier 9.

image is $512 \times 512 \times 3 = 786432$. The size of each pixel is 8 bits. Each pixel has the value in the range is 0-255. The size of our multipliers is 16×16 bit. It is necessary to convert the each pixel value into 16 bits. All input image pixel values are mapped from (0-255) to (0-65535). Image contrast is done with the help of following equations.

$$F = (InputImage \times \pi) \div 65535 \tag{10}$$

$$ContrastImage = (1 - \cos(F)) \div 2 \tag{11}$$

Pixel values of the input image are multiplied with Pi and scaled it to maximum possible value of the 16×16 bit multiplier. Proposed multipliers are used to multiply the input image pixel value with Pi. All outputs of processed pixels are recorded and multiplier outputs are converted back into 8 bit pixel. Finally, the cosine value of the processed pixels forms the contrast image. Figure 9 (a), 9 (b) show the input and contrast images respectively.

Figure 10 shows the contrast image of various multipliers. Quality of the image is measured based on peak signal to noise ratio (PSNR) value of the image. Peak signal noise ratio (PSNR) of the output image is computed based on mean squared error (MSE). The equations for MSE and PSNR are given in (12) and (13).

$$MSE = (1 \div mp) \times \left(\sum_{x=0}^{x-1} \sum_{y=0}^{y-1} [x(i,j) - y(i,j)]^2 \right) \tag{12}$$

$$PSNR = 10log_{10} \times \left(MAX_I^2 \div MSE \right) \tag{13}$$

In equation (12), m and p represent the image dimensions x(i,j) and y(i,j) which are the exact and obtained value of each pixel respectively. In equation (13), MAX_I represents the maximum value of the pixel. Table 7 shows the PSNR value of output images. The PSNR value of the multiplier designed using approximate 15-4 compressor is above 30 dB. This is sufficient for most of the image processing applications [34]. The image quality of the proposed multipliers using 15-4 compressors seems to be accurate image because of human perception. Normalized error distance of proposed multipliers is smaller than other recent approximate multipliers. Error distance of multiplier 7 and 8 is very high for any input combinations. This will give the low PSNR value of the image. The MSE value of multiplier 9 is very high than other multipliers. This provides the output image of the multiplier in dark colour.

TABLE 7. PSNR value of output image.

Approximate Multiplier Number	PSNR(dB)
3 (Proposed)	54.6
4 (Proposed)	34.5
5 (Proposed)	34.5
6 (Proposed)	32
7 [31]	8.3
8 [32]	8.3
9 [17]	5.6

VII. CONCLUSIONS

This paper presents the four designs of approximate 15-4 compressor. Approximate 16×16 bit multipliers are designed using those proposed 15-4 compressors. Approximate multipliers provide better performance than accurate multipliers with compromising of error rate. Moreover, we have achieved high pass rate and the normalized error distance value of multipliers designed using proposed

15-4 compressor is very small. Latency of the proposed multiplier is almost equal as compared to the accurate multipliers.

In order to validate our work, image contrast has been performed with the help of proposed multiplier. The quality of the processed image shows that our proposed multipliers are working fine. The PSNR value of other approximate multiplier is less than 10 dB, but our proposed multiplier provides greater than 30 dB, which is sufficient for most of the image processing applications. The proposed multipliers (3)-(6) are suitable for image processing applications whereas, multipliers (7)-(9) can be used where circuit performance is complex. Researchers can choose the multipliers based on their applications. Finally, our proposed multipliers consume low power and capable of giving the good result in terms of pass rate and error distance with the slight overhead of area as compared to other approximate multipliers. In future, researchers can work towards minimizing the area and pass rate of approximate multipliers.

REFERENCES

[1] D. Liu, *Embedded DSP Processor Design*, 1st ed. San Mateo, CA, USA: Morgan Kaufmann, 2008.

[2] K. K. Parhi, *VLSI Digital Signal Processing Systems: Design and Implementation*, 1st ed. Hoboken, NJ, USA: Wiley, 1999.

[3] Y. Kim, Y. Zhang, and P. Li, "An energy efficient approximate adder with carry skip for error resilient neuromorphic VLSI systems," in *Proc. Int. Conf. Comput.-Aided Design (ICCAD)*, Nov. 2013, pp. 130–137.

[4] A. Pishvaie, G. Jaberipur, and A. Jahanian, "Improved CMOS (4; 2) compressor designs for parallel multipliers," *Comput. Elect. Eng.*, vol. 38, no. 6, pp. 1703–1716, Nov. 2012.

[5] D. Baran, M. Aktan, and V. G. Oklobdzija, "Energy efficient implementation of parallel CMOS multipliers with improved compressors," in *Proc. ACM/IEEE Int. Symp. Low-Power Electron. Design (ISLPED)*, Aug. 2010, pp. 147–152.

[6] S. Veeramachaneni, K. M. Krishna, L. Avinash, S. R. Puppala, and M. B. Srinivas, "Novel architectures for high-speed and low-power 3-2, 4-2 and 5-2 compressors," in *Proc. Int. Conf. VLSI Design (VLSID)*, Jan. 2007, pp. 324–329.

[7] R. Menon and D. Radhakrishnan, "High performance 5 : 2 compressor architectures," *Proc. IEE-Circuits, Devices Syst.*, vol. 153, no. 5, pp. 447–452, Oct. 2006.

[8] A. Pishvaie, G. Jaberipur, and A. Jahanian, "High-performance CMOS (4:2) compressors," *Int. J. Electron.*, vol. 101, no. 11, pp. 1511–1525, Jan. 2014.

[9] O. Kwon, K. Nowka, and E. Swartzlander, Jr., "A 16-bit by 16-bit MAC design using fast 5:3 compressor cells," *J. VLSI Signal Process. Syst. Signal, Image Video Technol.*, vol. 31, no. 2, pp. 77–89, Jul. 2002.

[10] S. Mehrabi, R. F. Mirzaee, S. Zamanzadeh, K. Navi, and O. Hashemipour, "Design, analysis, and implementation of partial product reduction phase by using wide m:3 ($4 \leq m \leq 10$) compressors," *Int. J. High Perform. Syst. Archit.*, vol. 4, no. 4, pp. 231–241, Jan. 2013.

[11] A. Dandapat, S. Ghosal, P. Sarkar, and D. Mukhopadhyay, "A 1.2-ns 16×16 bit binary multiplier using high speed compressor," *Int. J. Elect. Electron. Eng.*, vol. 4, no. 3, pp. 234–239, 2010.

[12] R. Marimuthu, M. Pradeepkumar, D. Bansal, S. Balamurugan, and P. S. Mallick, "Design of high speed and low power 15-4 compressor," in *Proc. Int. Conf. Commun. Signal Process. (ICCSP)*, Apr. 2013, pp. 533–536.

[13] J. Liang, J. Han, and F. Lombardi, "New metrics for the reliability of approximate and probabilistic adders," *IEEE Trans. Comput.*, vol. 62, no. 9, pp. 1760–1771, Sep. 2013.

[14] N. Zhu, W. L. Goh, and K. S. Yeo, "An enhanced low-power high-speed adder for error-tolerant application," in *Proc. 12th Int. Symp. Integr. Circuits (ISIC)*, Nov. 2009, pp. 69–72.

[15] Z. Yang, A. Jain, J. Liang, J. Han, and F. Lombardi, "Approximate XOR/XNOR-based adders for inexact computing," in *Proc. IEEE Int. Conf. Nanotechnol. (IEEE-NANO)*, Aug. 2013, pp. 690–693.

[16] H. Jiang, J. Han, and F. Lombardi, "A comparative review and evaluation of approximate adders," in *Proc. ACM Great Lakes Symp. VLSI (GLSVLSI)*, May 2015, pp. 343–348.

[17] V. Gupta, D. Mohapatra, S. P. Park, A. Raghunathan, and K. Roy, "IMPACT: IMPrecise adders for low-power approximate computing," in *Proc. Int. Symp. Low Power Electron. Design (ISLPED)*, Aug. 2011, pp. 409–414.

[18] C. Liu, J. Han, and F. Lombardi, "A low-power, high-performance approximate multiplier with configurable partial error recovery," in *Proc. Int. Conf. Design Autom. Test Eur. (TEST)*, Mar. 2014, Art. no. 95.

[19] P. Kulkarni, P. Gupta, and M. D. Ercegovac, "Trading accuracy for power in a multiplier architecture," *J. Low Power Electron.*, vol. 7, no. 4, pp. 490–501, Dec. 2011.

[20] S. Balamurugan and P. S. Mallick, "Fixed-width multiplier circuits using column bypassing and decompositon logic techniques," *Int. J. Elect. Eng. Inform.*, vol. 7, no. 4, pp. 655–664, Dec. 2015.

[21] S. Balamurugan, S. Ghosh, Atul, S. Balakumaran, R. Marimuthu, and P. S. Mallick, "Design of low power fixed-width multiplier with row bypassing," *IEICE Electron. Exp.*, vol. 9, no. 20, p. 1568–1575, Oct. 2012.

[22] H. R. Mahdiani, A. Ahmadi, S. M. Fakhraie, and C. Lucas, "Bio-inspired imprecise computational blocks for efficient VLSI implementation of soft-computing applications," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 57, no. 4, pp. 850–862, Apr. 2010.

[23] K. Y. Kyaw, W. L. Goh, and K. S. Yeo, "Low-power high-speed multiplier for error-tolerant application," in *Proc. IEEE Int. Conf. Electron Devices Solid-State Circuits (EDSSC)*, Dec. 2010, pp. 1–4.

[24] K. Bhardwaj, P. S. Mane, and J. Henkel, "Power- and area-efficient approximate Wallace tree multiplier for error-resilient systems," in *Proc. 15th Int. Symp. Quality Electron. Design (ISQED)*, Mar. 2014, pp. 263–269.

[25] M. S. K. Lau, K.-V. Ling, and Y.-C. Chu, "Energy-aware probabilistic multiplier: Design and analysis," in *Proc. Int. Conf. Compil., Archit., Synth. Embedded Syst.*, Oct. 2009, pp. 281–290.

[26] R. Venkatesan, A. Agarwal, K. Roy, and A. Raghunathan, "MACACO: Modeling and analysis of circuits for approximate computing," in *Proc. Int. Conf. Compil., Archit., Synth. Embedded Syst. (ICCAD)*, Nov. 2011, pp. 667–673.

[27] F. Farshchi, M. S. Abrishami, and S. M. Fakhraie, "New approximate multiplier for low power digital signal processing," in *Proc. 17th Int. Symp. Comput. Archit. Digit. Syst. (CADS)*, Oct. 2013, pp. 25–30.

[28] H. Jiang, C. Liu, N. Maheshwari, F. Lombardi, and J. Han, "A comparative evaluation of approximate multipliers," in *Proc. Int. Symp. Nanosc. Archit. (NANOARCH)*, Jul. 2016, pp. 191–196.

[29] C.-H. Lin and I.-C. Lin, "High accuracy approximate multiplier with error correction," in *Proc. IEEE 31st Int. Conf. Comput. Design (ICCD)*, Oct. 2013, pp. 33–38.

[30] Y. Bansal and C. Madhu, "A novel high-speed approach for 16×16 vedic multiplication with compressor adders," *Comput. Elect. Eng.*, vol. 49, pp. 39–49, Jan. 2016.

[31] A. Momeni, J. Han, P. Montuschi, and F. Lombardi, "Design and analysis of approximate compressors for multiplication," *IEEE Trans. Comput.*, vol. 64, no. 4, pp. 984–994, Apr. 2015.

[32] N. Maheshwari, Z. Yang, J. Han, and F. Lombardi, "A design approach for compressor based approximate multipliers," in *Proc. 28th Int. Conf. VLSI Design (VLSID)*, Jan. 2015, pp. 209–214.

[33] J. Ma, K. L. Man, N. Zhang, S.-U. Guan, and T. T. Jeong, "High-speed area-efficient and power-aware multiplier design using approximate compressors along with bottom-up tree topology," in *Proc. Int. Soc. Opt. Photon. (ICMV)*, Mar. 2012, pp. 1–9.

[34] Z. Wang, A. C. Bovik, H. R. Sheikh, and E. P. Simoncelli, "Image quality assessment: From error visibility to structural similarity," *IEEE Trans. Image Process.*, vol. 13, no. 4, pp. 600–612, Apr. 2004.

R. MARIMUTHU received the bachelor's degree in electronics and instrumentation from Bharathiyar University, India, and the master's degree from Anna University, India. He is currently an Assistant professor (Sr.,) with the School of Electrical Engineering, VIT University, India. He has authored 20 scopus indexed papers in different journals and conferences. His current research area is low power VLSI, high speed architecture, and embedded systems.

Y. ELSIE REZINOLD is currently pursuing the bachelor's degree with the Department of Electronics and Instrumentation, VIT University, Vellore. His area of interests is low power VLSI design, computer architecture, and embedded systems.

P. S. MALLICK (SM'10) was the Dean of the School of Electrical Engineering, VIT University, India, from 2011 to 2015. He was the Technical Head of IAAB Electronics a Swedish Industry in Bangladesh. He led various research teams and developed Online Laboratory in Microelectronics, Monte Carlo Simulator of Compound Semiconductors, Nanostructured MIM Capacitor, and Low cost Electric Fencers. He is currently a Professor of Electronics Engineering and the Director of Office of the Ranking and Accreditation, VIT University. He has authored 72 research papers in different journals and conferences of international repute. His recent interest includes advancement of technical education through innovations. He is the past Chapter Chair and a present Chapter Adviser of the IEEE-EDS VIT of Region 10 Asia pacific. He was an enlisted Technical Innovator of India in 2007. He organized two major International Conferences ICAEE-2014 (jointly with KTH, Sweden) and CommV-2009 in VIT University. He is finding new materials and technology for future nanoscale electronics.