IEEE Access
practical innovations : open solutions

Received August 21, 2013, accepted January 29, 2014, date of publication February 5, 2014, date of current version February 18, 2014.

Digital Object Identifier 10.1109/ACCESS.2014.2304568

Compact MOSFET Modeling for Process Variability-Aware VLSI Circuit Design

SAMAR K. SAHA

S. K. Saha (samar@ieee.org)

Prospicient Devices, Milpitas, CA 95035, USA

ABSTRACT This paper presents a systematic methodology to develop compact MOSFET models for process variability-aware VLSI circuit design. Process variability in scaled CMOS technologies severely impacts the functionality, yield, and reliability of advanced integrated circuit devices, circuits, and systems. Therefore, variability-aware circuit design techniques are required for realistic assessment of the impact of random and systematic process variability in advanced VLSI circuit performance. However, variability-aware circuit design requires compact MOSFET variability models for computer analysis of the impact of process variability in VLSI circuit design. This paper describes a generalized methodology to determine the major set of device parameters sensitive to random and systematic process variability in nanoscale MOSFET devices, map each variability-sensitive device parameter to the corresponding compact model parameter of the target compact model, and generate statistical compact MOSFET models for variability-aware VLSI circuit design.

INDEX TERMS Process variability, local variations, global variations, variability modeling, mismatch modeling, BSIM4 MOSFET model, statistical compact modeling.

I. INTRODUCTION

With continued miniaturization of metal-oxide-semiconductor field-effect transistor (MOSFET) devices [1]–[6], performance variability induced by process variability has become a critical issue in the design of VLSI circuits using advanced complementary metal-oxide-semiconductor (CMOS) technologies. Process variability has severely impacted delay and power variability in VLSI devices, circuits, and chips, and this impact keeps increasing as MOSFET devices and CMOS technologies continue to scale down [7]–[11]. The increasing amount of within-die process variability on the yield of VLSI circuits, such as static random access memory (SRAM), has imposed an enormous challenge in the conventional VLSI design methodologies. Similarly, the chip mean variation due to across the chip systematic process variability, also, imposes serious challenge in the conventional VLSI circuit design methodologies. Because of process variability constraints, an advanced VLSI circuit optimized using the conventional design methodology is more susceptible to random performance fluctuations. Thus, new circuit design techniques to account for the impact of process variability in VLSI circuits have become essential [7]. Although it is desirable to mitigate the risk of process variability on device and circuit performance by innovative device architectures [12], [13], process control, and a combination of process and circuit design techniques, modeling process variability is critical for variability-aware circuit design [7]. Thus, compact model addressing the impact of process variability in scaled MOSFET devices is crucial for computer-aided design (CAD) and analysis of advanced VLSI circuits.

In order to generate compact variability model for process variability-aware circuit design, a major set of model parameters sensitive to process variation is determined [7]. Typically, a standard set of model parameters is used to generate compact model library for worst-case analysis of circuit performance [7]. However, for realistic process variability modeling, a large sample of production control electrical test (ET) data is collected from different wafers and wafer-lots over a period of time [14]–[16]. Then a set of process variability-sensitive model parameters is determined by principle component analysis (PCA) [14]. Though PCA is the most effective way to determine the process variability-sensitive device parameters, it is resource intensive and not suitable for concurrent next generation technology and product development. Similarly, a standard set of model parameters is inadequate for characterizing process variability in

2169-3536 © 2014 IEEE. Translations and content mining are permitted for academic research only.
Personal use is also permitted, but republication/redistribution requires IEEE permission.
See http://www.ieee.org/publications_standards/publications/rights/index.html for more information.

nanoscale MOSFET devices. Therefore, it is crucial to adopt an analytical approach to determine the process variability-sensitive critical model parameters for compact variability modeling. In this paper, we present a generalized methodology to determine the device parameters most sensitive to process variation and map each of these device parameters to the corresponding compact model parameters to build compact model library for variability-aware VLSI circuit analysis.

The objective of this paper is to present a systematic methodology to develop compact MOSFET model library for variability-aware VLSI circuit design. In order to achieve this goal, first of all, the paper reviews the critical sources of process variability in scaled MOSFET devices along with their impact on advanced VLSI device performance. Then a brief overview of different approaches to modeling process variability for VLSI circuit CAD is described. After reviewing the conventional process variability modeling approaches, the paper presents an analytical approach to generate compact model library for variability-aware circuit design. In this approach, first the major set of MOSFET device parameters sensitive to the local and global process variability is determined from the basic device theory. Then each process variability-sensitive device parameter is mapped to the corresponding compact model parameter of the target compact model (e.g. BSIM4 [17]). After parameter mapping, a simplified procedure is used to generate compact MOSFET model library for variability-aware VLSI circuit optimization.

II. SOURCES OF FRONT-END PROCESS VARIABILITY

Generally, the intrinsic sources of variability in VLSI device performance arise from random variability of wafer fabrication processing steps [7], [9]. Typically, the intrinsic process variability is grouped as stochastic and systematic. The stochastic group is defined as the local or intra-die process variability and the systematic component is defined as the global or inter-die process variability [7]–[11]. Local process variability causes parametric fluctuations or mismatch between identically designed devices within a die, whereas the global process variability causes die-to-die, wafer-to-wafer, or lot-to-lot systematic parametric fluctuations between identical devices [7]–[10]. Global variability causes a shift in the mean value of the sensitive design parameters, including the channel length (L), channel width (W), gate oxide thickness (T_{ox}), resistivity, doping concentration, and body effect [7]. The major sources of intrinsic process variability in advanced CMOS technologies include random discrete doping (RDD), line-edge roughness (LER), line-width roughness (LWR), and oxide thickness variation (OTV) as shown in Fig. 1 [7]–[10].

The detailed description of the major sources of front-end process variability in metal-oxide-semiconductor (MOS) devices and their impact on device performance is reported in [7] and is summarized in subsections $A-D$ below:

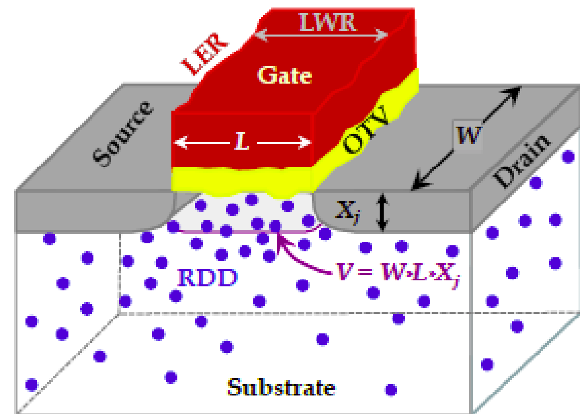

FIGURE 1. The critical sources of variability in CMOS devices; here L, W, and X_j are the channel length, channel width, and source/drain junction depth of MOSFET devices, respectively; and V is the volume of charge in the channel region.

A. RANDOM DISCRETE DOPING

In the channel region of an MOS device, RDD results from the discreteness of dopant atoms as shown in Fig. 1. In an MOS device, the channel region is doped with dopant atoms to control its threshold voltage (V_{th}). For a device with channel doping concentration N_{CH}, and source/drain (S/D) junction depth X_{j}, the total number of dopant atoms in the channel region is given by [7]:

$$N_{CHtotal} \cong N_{CH}(W.L.X_{\mathrm{j}}) \quad (1)$$

Equation 1 shows that the continuous scaling down of L, W, and X_{j} causes $N_{CHtotal}$ to decrease, despite the corresponding increase in the channel-doping concentration according to CMOS scaling guidelines [1]–[3]. Using Eq. (1) and data for advanced CMOS technology scaling from 'International Technology Roadmap for Semiconductors (ITRS)' [18], the estimated decrease in $N_{CHtotal}$ over the scaled technology nodes is shown in Fig. 2. Fig. 2 implies that

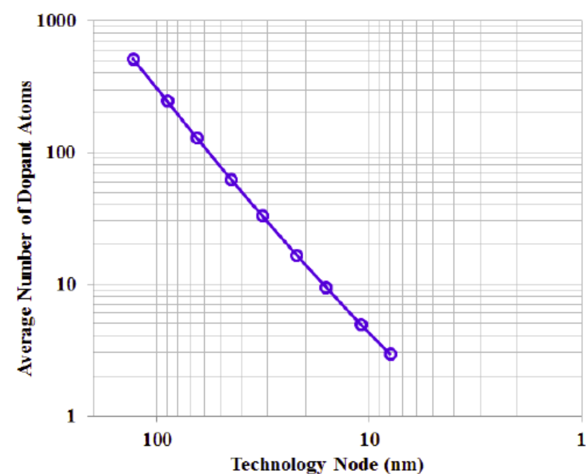

FIGURE 2. Estimated average channel doping concentration with scaling bulk-CMOS devices in the nanoscale regime; the calculation is performed following ITRS [18].

the number of dopants in a transistor channel is a discrete statistical quantity with probability to occupy any random location. Therefore, in an advanced CMOS technology, two identical transistors sitting side by side have different electrical characteristics because of the randomness in a few dopant atoms, resulting in intra-die device and circuit performance variability.

The major effects of RDD are significant variability in MOSFET threshold voltage V_{th}, variability in the overlap capacitance due to uncertainty in the position of S/D dopants under the gate, and variability in the effective S/D series resistance (R_{DS}). The impact of RDD-induced process variability on V_{th} mismatch between two identically designed within-die devices is given by [19], [20]:

$$\sigma V_{th,RDD} \cong C \cdot \left(\sqrt[4]{q^3 \varepsilon_{Si} \phi_B}\right) \frac{T_{ox}}{\varepsilon_{ox}} \left(\frac{\sqrt[4]{N_{CH}}}{\sqrt{W_{eff} L_{eff}}}\right) \quad (2)$$

where C is a number and is given by 0.8165 [19] or 0.7071 [20] with or without the dopant variation along the depth of the channel region, respectively; q is the electronic charge, ε_{Si} and ε_{ox} are the permittivity of silicon and silicon-dioxide (SiO_2), respectively; $\phi_B = 2k_B T \ln(N_{CH}/n_i)$ is the bulk potential of the channel region of MOSFETs with k_B, T, and n_i are the Boltzmann constant, absolute temperature, and intrinsic carrier concentration, respectively; and W_{eff} and L_{eff} represent the effective dimension of W and L, respectively. Since the device area ($W_{eff} L_{eff}$) decreases with each new technology generation, the net result of RDD is a significant increase in process variability for scaled CMOS technology as shown in Fig. 3. In fact, RDD is a major contributor to the mismatch (σV_{th}) in advanced MOSFETs [21]. As the device size scales down, $N_{CHtotal}$ decreases as shown in Fig. 2, resulting in a larger variation of dopant numbers, and significantly impacting V_{th} as shown in Fig. 3.

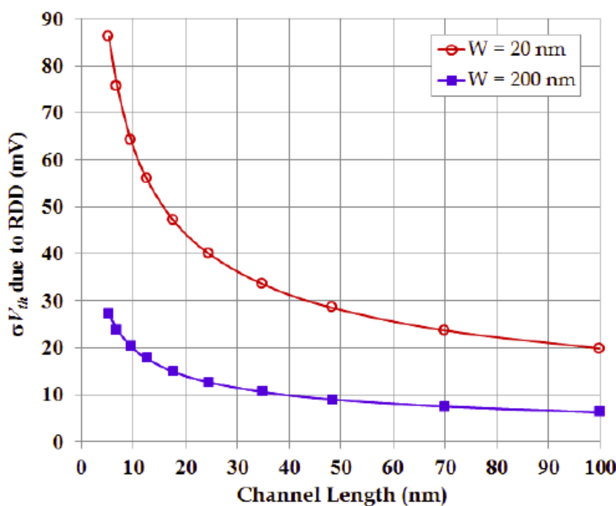

FIGURE 3. Estimated threshold voltage variation for a typical 20 nm bulk-CMOS technology as a function of device channel length for different channel width following ITRS [18] using Eq. (2); parameters used in Eq. (2) are $N_{CH} = 6 \times 10^{18}$ cm^{-3}; SiO_2 Equivalent Oxide Thickness (EOT) = 1.1 nm; and $C = 0.8165$.

B. LINE-EDGE ROUGHNESS

In CMOS technology, LER results from sub-wavelength lithography and etching process that causes variation in the critical dimension (CD) of the transistor feature size as shown in Fig. 1 [22]. The impact of LER includes variation in V_{th} and higher subthreshold current. LER-induced V_{th} mismatch depends on the variability in W_{eff} of MOSFETs and is given by [7], [22], and [23]:

$$\sigma V_{th,LER} \propto \frac{1}{\sqrt{W_{eff}}} < \sigma V_{th,RDD} \quad (3)$$

Thus, LER increases as VLSI technology scales down. In scaled MOSFET devices, LER has become a larger fraction of L and a major source of intrinsic statistical variation causing significant variability in VLSI device and circuit performance. The mismatch due to LER and RDD is statistically independent and can be modeled independently [7].

C. OXIDE THICKNESS VARIATION

In CMOS technologies, OTV is caused by atomic level interface roughness between silicon and gate dielectric and remote interface roughness between gate material and gate dielectric, hereafter referred to as the "surface roughness (SR)," as shown in Fig. 1. This SR causes fluctuations of the voltage drop across the oxide layer resulting in V_{th} variation [7], [24], [25]. In nanoscale MOSFETs, OTV is becoming more dominant as T_{ox} approaches to the length of a few silicon atoms and is comparable to the thickness of interface roughness.

In nano-MOSFET devices, OTV causes significant device parameter variability. In polysilicon gate MOSFETs, OTV introduces a gate current (I_g) variation. This I_g variation induces a voltage drop in the polysilicon gate and significantly changes V_{th}. In addition, the device transconductance, g_m changes significantly because of the reduction in the gate voltage V_{gs} due to the voltage drop in the polysilicon gate. In high-k gate dielectric and metal gate devices, OTV introduces significant mobility degradation [7].

D. OTHER SOURCES PROCESS VARIABILITY

Other sources of process variability include variation associated with polysilicon as well as metal gate granularity [26], [27]; variation in fixed charge [28], and defects and traps in gate dielectric [29]; variation associated with patterning proximity effects such as optical proximity correction [30]; variation associated with polish such as shallow-trench isolation [31] and gate [32]; variation associated with the strain such as in wafer-level biaxial strain [33], high-stress capping layers [34], and embedded silicon germanium (SiGe) [35]; and variation associated with implants and anneals due to implant tools, implant profiles, and millisecond annealing [36], [37].

Thus, from the above discussions, it is clear that the advanced CMOS process technologies introduce within-die random performance variability which causes severe variability in the performance of advanced VLSI circuits and systems.

Therefore, it is critical to accurately model process variability when predicting the performance of advanced VLSI circuits and systems.

III. CONVENTIONAL METHODOLOGIES FOR MOSFET VARIABILITY MODELING

In order to account for process variability in circuit performance, typically, corner models are used to set the lower and upper limits of process variation. These models are implemented in the process-design kit (PDK) to support process variability-aware VLSI circuit design.

A. WORST-CASE FIXED CORNER MODELS

In conventional circuit design technique, process variability is modeled by four worst-case corners—two for analog applications and two for digital [7]. The corner models for analog applications are generated from slow nMOS and slow pMOS (SS) to model the worst-case speed (WS), and from fast nMOS and fast pMOS (FF) to model the worst-case power (WP); whereas, the corner models for digital applications are generated from fast nMOS and slow pMOS (FS) to model the worst-case '1,' (WO) and from slow nMOS and fast pMOS (SF) to model the worst-case '0' (WZ). A standard set of model parameters (e.g. V_{th}) is used to account for process variability and model the worst-case corner performance of devices and circuits of the target CMOS technology [7].

In this modeling approach, the standard deviation (σ) limits are preset pessimistically to include any potential process variability over a wide range. The worst-case corner models are generated by offsetting the selected compact-model parameters, P of the typical (TT) compact model by $\pm dP = n\sigma$ to account for the window of process variability, where n is the number of σ for P so that $3 \leq n \leq 6$ is selected to set the fixed lower and upper limits, LL and UL, respectively of the worst-case models; and TT is the typical compact model extracted from the "golden die" of the "golden wafer" representing the centerline process technology [7]. For example, the corner models of a BSIM4 TT model parameter V_{TH0} is defined as $V_{\mathrm{TH}} = V_{\mathrm{TH0}} \pm dvth$ where $dvth$ is used to set the fixed LL and UL of the worst-case models.

In order to obtain the worst-case corner of drain current I_{ds}, we consider the basic I_{ds} expression in the ON state of large MOSFETs [38]:

$$I_{ds} \cong \left(\frac{W}{2L}\right) \mu_{eff} C_{ox} \left(V_{gs} - V_{th}\right)^2 ; 0 < \left(V_{gs} - V_{th}\right) \geq V_{ds} \quad (4)$$

where μ_{eff}, C_{ox}, and V_{ds} are the inversion carrier mobility, gate oxide capacitance, and drain to source voltage, respectively; and the remaining parameters have their usual meanings as defined earlier. Then, the UL is set by taking the appropriate maximum or minimum offset of the device parameters to maximize the value of I_{ds}. Thus, the UL of ION for nMOSFETs is given by:

$$IONN(UL) \cong \mu_{eff} \left(\frac{W + dW}{2(L - dL)}\right) \left(\frac{\varepsilon_{ox}}{T_{ox} - dT_{ox}}\right) \times \left(V_{gs} - (V_{th} - dV_{th})\right)^2 \quad (5)$$

In (5), W is increased by dW, L is reduced by dL, T_{ox} is reduced by dT_{ox}, and V_{th} is reduced by dV_{th} to achieve the UL of I_{ds} specification. Similarly, the LL for ION is set by:

$$IONN(LL) \cong \mu_{eff} \left(\frac{W - dW}{2(L + dL)}\right) \left(\frac{\varepsilon_{ox}}{T_{ox} + dT_{ox}}\right) \times \left(V_{gs} - (V_{th} + dV_{th})\right)^2 \quad (6)$$

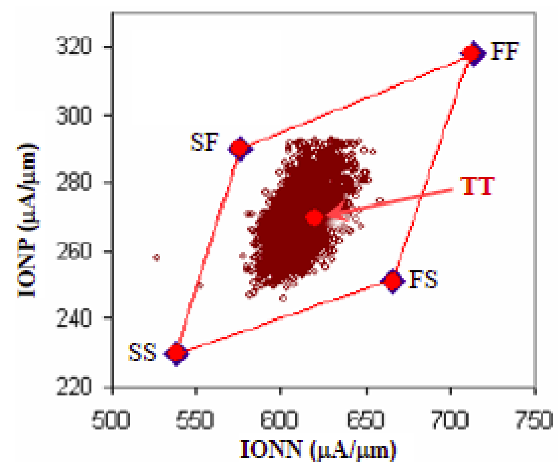

FIGURE 4. The distribution of measurement data along with the simulation data generated by fixed-corner models: nMOS ON current (IONN) versus pMOS ON current (IONP); (FF: fast nMOS and fast pMOS; FS: fast nMOS and slow pMOS; SF: slow nMOS and fast pMOS; SS: slow nMOS and slow pMOS) [7].

Fig. 4 shows ION-plots for both n/pMOSFETs obtained by fixed-corner models along with the distribution of ET data. It is observed from Fig. 4 that the simulation results obtained by fixed-corner models are too wide, so it could end up rejecting a valid design, causing yield loss. The major problems with the worst-case corner models are that in most cases the existing correlations between the device parameters are ignored and the models include pessimistic corner values. As a result, the models generate a large spread of data during circuit simulation [7].

The worst-case corner models offer designers capability to simulate the pass/fail results of a typical design and are usually pessimistic.

B. STATISTICAL CORNER MODELS

Unlike fixed corner models, the statistical corner models are generated using ET data from different die, wafers, and wafer lots collected over a certain period of time to represent realistic process variability of a target technology [14]–[16]. Some of the methodologies used to generate statistical corner models are briefly outlined below:

1) PERFORMANCE-AWARE MODELING (PAM)

In one approach, ET data are measured from a large number of sites of the target technology. And, for each site of ET data a compact model file is generated. Thus, a large number of compact model files, referred to as the "performance aware model (PAM)" cards are generated for any target technology [39], [40]. In this approach about 1000 PAM cards or model files are generated for realistic statistical analysis of circuit performance.

2) LOCATION DEPTH CORNER MODELING (LDCM)

In this modeling approach, ET data are used to determine the depth of the location of device parameters in the distribution for corner model generation, referred to as the "location depth corner modeling (LDCM)" [41]. In LDCM, the wafers corresponding to the extreme data points in the distribution are used to extract separate compact models. Thus, using LDCM, the number of model cards (<20) is significantly reduced in contrast to PAM. An enhanced LDCM (ELDCM) is used with proper guard banding to ensure design validation against future process shift from the baseline specifications [41].

3) STATISTICAL COMPACT MODELING

The statistical modeling approach, referred to as the "backward propagation of variance (BPV) [42]," formulates statistical models as a set of independent, normally distributed process parameters P. These parameters control the variations seen in the device electrical performances through the behavior described in the TT compact models. With recent extensions [43], BPV is used to characterize physical process related compact model parameters. For accurate analysis of process variability induced circuit performance variability using BPV, the TT model file must be physical, the sensitivity matrix must be well-conditioned, and the variances of parameters must be physically consistent.

Thus, in the conventional variability modeling approaches, a standard set of model parameters are used for fixed corner modeling or a large number of model files are generated from ET data. The fixed corner models are inadequate whereas, ET-data based modeling is resource-intensive. Therefore, an analytical technique to obtain the process-sensitive compact model parameters of any compact model to generate compact variability model for circuit analysis is crucial for variability-aware circuit design as described in the following section.

IV. A GENERALIZED APPROACH FOR MOSFET PROCESS VARIABILITY MODELING

A generalized approach for process variability modeling is shown in Fig. 5. The method includes selection of target compact model; consideration of basic I_{ds} expression; derivation of a generalized expression of I_{ds} variance; selection of device parameters causing process-induced I_{ds} variation; mapping process-sensitive device parameters to corresponding compact model parameters; determination of variances for mismatch modeling and global variability modeling; and finally, build compact variability model.

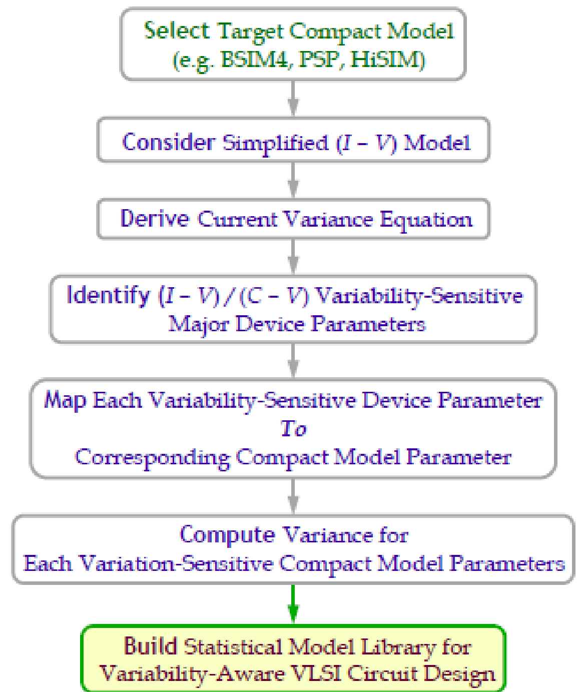

FIGURE 5. Generalized modeling approach for process-variability-aware VLSI circuit design; here, BSIM4 [17], PSP [44], and HiSIM [45] represent industry standard MOSFET compact models.

The modeling methodology outlined in Fig. 5 is described in the following section.

A. DETERMINATION OF PROCESS VARIABILITY-SENSITIVE MOSFET DEVICE PARAMETERS

It is clear from our discussions in section II that process variability causes variability in MOSFET device performance which in turn causes variability in VLSI circuit performance. Since, the MOSFET device performance is determined by I_{ds}, therefore, in order to determine the impact of process variability on circuit performance, we determine the process variability-sensitive device parameters causing I_{ds} variability. For the selection of major process variability-sensitive device parameters, we consider the basic I_{ds} model in the sub-threshold, linear, and saturation region of MOSFETs [38]:

$$I_{ds} \cong \begin{cases} \left(\frac{W}{L}\right) \mu_{eff} \eta e^{\frac{V_{gs}-V_{th}}{nkT}} \left(1 - e^{-\frac{V_{ds}}{kT}}\right); & \left(V_{gs} - V_{th}\right) \leq 0 \\ \left(\frac{W}{L}\right) \mu_{eff} C_{ox} \left(V_{gs} - V_{th} - \frac{V_{ds}}{2}\right) V_{ds}; & 0 < \left(V_{gs} - V_{th}\right) \leq V_{ds} \\ \left(\frac{W}{2L}\right) \mu_{eff} C_{ox} \left(V_{gs} - V_{th}\right)^2; & 0 < \left(V_{gs} - V_{th}\right) \geq V_{ds} \end{cases} \quad (7)$$

where η is a constant and depends on the channel depletion capacitance (C_d) and ambient temperature, T; n is the ideality factor of sub-threshold slope and depends on C_{ox} and C_d; and, the remaining parameters have their usual meanings as defined earlier. From Eq. (7), we determine the major device parameters most sensitive to process variability in each region of MOSFET device operation.

1) SELECTION OF LOCAL PROCESS VARIABILITY-SENSITIVE DEVICE PARAMETERS

The local process variability or mismatch between identically designed transistors is caused by microscopic process that makes every transistor different from its neighbors [8]–[12]. As a result, a device parameter P can be considered as consisting of a fixed component P_0 and a randomly varying component p resulting in different values of P for closely apart identical paired-transistors. Then the difference ΔP between two identical transistors within a die is a randomly varying parameter and is defined as the 'mismatch' in P between two identical-paired transistors. For a large number of samples, ΔP converges to a Gaussian distribution with zero mean. Then the mismatch in relative drain current, $\Delta I_{ds}/I_{ds}$ between paired-transistors due to P is given by [46]:

$$\sigma^2_{\Delta I_{ds}/I_{ds}} = \sum_{i=1}^{l}\left(\frac{1}{I_{ds}}\frac{\partial I_{ds}}{\partial P_i}\right)^2 \sigma^2_{\Delta P_i} + \frac{2}{I_{ds}^2}\sum_{i=1}^{l}\frac{\partial I_{ds}}{\partial P_i}\frac{\partial I_{ds}}{\partial P_{i+1}}\rho\left(\Delta P_i, \Delta P_{i+1}\right) \quad (8)$$

where l is the total count of ΔP contributing to I_{ds} mismatch; ΔP_i is the ith count of ΔP with standard deviation $\sigma_{\Delta P_i}$; and $\rho\left(\Delta P_i, \Delta P_{i+1}\right)$ is the correlation between ΔP_i and ΔP_{i+1}. Since ΔP_i is random and independent, therefore, the correlation $\rho\left(\Delta P_i, \Delta P_{i+1}\right) = 0$. In order to model I_{ds} mismatch between paired-transistors, we determine the major local process variability-sensitive device parameters P.

From Eq. (7), we find that for all regions of MOSFET device operation, the value of I_{ds} depends on a common set of parameters $\{V_{th}, W, L, C_{ox}, \mu_{eff}, V_{gs}, V_{ds}\}$. We know, $C_{ox} = \text{f}(T_{ox})$, then considering only parametric variation, in Eq. (8), ΔP represents any of the mismatch parameters of the set $\{\Delta V_{th}, \Delta W, \Delta L, \Delta T_{ox}, \Delta\mu_{eff}\}$. It is to be noted that the parameter set $\{\Delta W, \Delta L, \Delta T_{ox}, \Delta\mu_{eff}\}$ describes the current gain $\beta = \left((W/L)C_{ox}\mu_{eff}\right)$ mismatch. Again, V_{th} can be expressed as $V_{th} = \text{f}\left(V_{th0}, \gamma, \phi_S, V_{bs}\right)$, where V_{bs} is the applied body bias and $V_{th0} = V_{th}$ at $V_{bs} = 0$ whereas, γ and ϕ_S are the body effect coefficient and channel surface potential, respectively. Here, ΔV_{th0} describes the mismatch $\Delta I_{ds}(V_{bs} = 0)$ due to RDD of the channel doping concentration N_{CH} of MOSFETs whereas, $\Delta\gamma$ describes the mismatch in $\Delta I_{ds}(V_{bs})$ due to the variation in N_{CH} in the depletion region under the gate. We know that $\gamma = \text{f}(N_{CH}, V_{bs})$ and with the change in the value of V_{bs}, the width of the depletion layer under the gate changes [19]. As a result, the amount of bulk charge, qN_{CH} changes with the changes in V_{bs} as shown in Fig. 6 for the graded-retrograde channel doping profile [12]. Thus, RDD of the vertical channel doping profile under the gate contributes to the mismatch in $I_{ds}(V_{bs})$. Hence, $I_{ds}(V_{bs})$ mismatch between the identical paired-transistors due to variation in the vertical channel doping concentration must be modeled by γ.

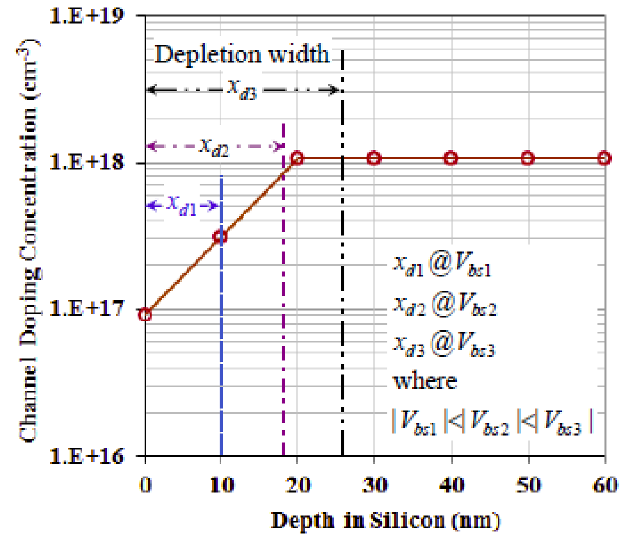

FIGURE 6. A typical graded-retrograde MOSFET channel doping profile from the silicon/silicon-dioxide interface at depth = 0 into the substrate; here x_{d1}, x_{d2}, and x_{d3} are the depletion width due to the applied body bias V_{bs1}, V_{bs2}, and V_{bs3}, respectively causing $V_{th}(V_{bs})$ variability due to RDD along the depth of the channel.

Thus, the set of major local process variability-sensitive device parameters contributing to the mismatch between identically designed paired-transistors within a die is $\{V_{th0}, W, L, T_{ox}, \mu_{eff}, \gamma\}$ as shown in Table 1. Here, ΔV_{th0} describes the variation in ΔI_{ds} due to RDD; ΔW and ΔL describes ΔI_{ds} due to LER and LWR; ΔT_{ox} defines ΔI_{ds} due to OTV; $\Delta\mu_{eff}$ defines ΔI_{ds} due to mobility variation caused

TABLE 1. Process variability-sensitive local device parameters mapped to the corresponding compact model parameters.

Device Parameter		Compact Model Parameter	
Symbol	Definition	Symbol	Definition
V_{th}	Threshold voltage	VTH0	V_{th} at $V_{bs} = 0$
W	Channel width	XW	W offset due to masking and lithography
L	Channel length	XL	L offset due to masking and lithography
T_{ox}	Gate oxide thickness	TOXE/TOXM	Equivalent T_{ox}
μ_{eff}	Inversion carrier mobility	U0	Low-field mobility
γ	Body bias coefficient	K1	1st order body bias coefficient

by SR scattering; and γ models $\Delta I_{ds}(V_{bs})$ due to RDD in the vertical channel doping profile. Therefore, we have used the basic $I-V$ relation to determine the major process variability-sensitive device parameters for modeling mismatch in VLSI circuits.

2) SELECTION OF GLOBAL PROCESS VARIABILITY-SENSITIVE DEVICE PARAMETERS

The global process variability is caused by non-uniform processing temperature as well as the variation of implant doses across wafers and relative location of devices [7], [8]. The global variation shifts the average or mean value of device performance. As a result, a device parameter within a chip varies for two identically designed devices. For a large count of P from a large number of on-chip measurement data, P converges to a Gaussian distribution with mean value P_0 and standard deviation $\sigma = \Delta P$. Then the chip mean variation in I_{ds} due to global process variability-sensitive parameter P is given by:

$$\sigma_{I_{ds}}^2 = \sum_{i=1}^{l} \left(\frac{\partial I_{ds}}{\partial P_i}\right)^2 \sigma_{P_i}^2 + 2\sum_{i=1}^{l} \frac{\partial I_{ds}}{\partial P_i}\frac{\partial I_{ds}}{\partial P_{i+1}} \rho\left(P_i, P_{i+1}\right) \quad (9)$$

where l is the total number of occurrence of the device parameters P contributing to global I_{ds} variation; P_i is the ith count of P with standard deviation σP_i from its mean value P_0; and $\rho\left(P_i, P_{i+1}\right)$ is the correlation between the occurrence P_i and P_{i+1}. In order to model the variation of I_{ds} around its mean value, we determine the major global process variability-sensitive parameters P.

Again, from Eq. (7), the chip mean variation of I_{ds} due to global process variability can be described by the parameter set $\left\{V_{th0}, W, L, C_{ox}, \mu_{eff}, \gamma\right\}$. In addition, the I_{ds} variability due to the variation in the S/D ion implantation dose and processing temperature across wafers are described by the variation in the S/D series resistance, R_{DS} of MOSFET devices. Furthermore, the gate delay, $\tau_{pd} \propto C_{load}$, where C_{load} is the load capacitance of the inverter circuit. Therefore, for an accurate simulation of digital circuits, the across the chip variation in MOSFET gate capacitance (C_g) along with the S/D junction capacitance (C_J) must be modeled. Now, the variability in the mean value of C_g is described by the gate overlap capacitance (C_{ov}) whereas, that in C_J is described by the S/D area as well as S/D side-wall and isolation-edge sidewall capacitances. Thus, the variation in the ac and transient performance of VLSI digital circuits are, also, described by an additional parameter set $\{C_{ov}, C_J\}$. Therefore, the set of major MOSFET device parameters sensitive to global process variability can be represented by $\left\{V_{th0}, W, L, T_{ox}, \mu_{eff}, \gamma, R_{DS}, C_{ov}, C_j\right\}$ as shown in Table 2.

B. MAPPING OF PROCESS VARIABILITY-SENSITIVE DEVICE PARAMETERS TO COMPACT MODEL PARAMETERS

In order to develop compact MOSFET model to analyze the impact of process variability in advanced VLSI circuits, the process variability-sensitive device parameters P selected in section IVA are mapped to the corresponding compact model parameter $\{M\}$ of the selected compact model. In this study, we select BSIM4 compact model to show the methodology of generating compact MOSFET variability model library for VLSI circuit CAD.

TABLE 2. Process variability-sensitive global device parameters mapped to the corresponding compact model parameters.

Device Parameter		Compact Model Parameter	
Symbol	Definition	Symbol	Definition
V_{th}	Threshold voltage	VTH0	V_{th} at $V_{bs}=0$
W	Channel width	XW	W offset due to masking and lithography
L	Channel length	XL	L offset due to masking and lithography
T_{ox}	Gate oxide thickness	TOXE/TOXM	Equivalent T_{ox}
μ_{eff}	Inversion carrier mobility	U0	Low-field mobility
γ	Body bias coefficient	K1	1st order body bias coefficient
R_{DS}	S/D extension resistance	RDSW	Zero-bias R_{DS}
C_{ov}	Gate overlap capacitance	CGSL/CGDL	S/D extension C_{ov}
		CGSO/CGDO	Non-SDE region C_{ov}
C_J	S/D junction capacitance	CJS/CJD	Area component of C_J
		CJSWS/CJSWD	Isolation-edge side-wall C_J
		CJSWGS/CJSWGD	Gate-edge side-wall C_J

1) MAPPING OF LOCAL PROCESS VARIABILITY-SENSITIVE DEVICE PARAMETERS TO COMPACT MODEL PARAMETERS

In section IVA1, we have presented an analytical approach to select the randomly variable set of device parameters, $\{V_{th0}, W, L, T_{ox}, \mu_{eff}, \gamma\}$, causing mismatch between identically designed paired-transistors. The corresponding set of BSIM4 MOS model parameters, shown in Table 1, is $\{V_{TH0}, XW, XL, TOX, U0, K1\}$; where, XW and XL are the channel width and length offset parameters due to masking and photolithography, respectively and account for the mismatch due to LER and LWR; whereas, $U0$ and $K1$ account for the variation in μ_{eff} and N_{CH} under V_{bs}, respectively. In order to build the compact model, the variance $\sigma_{\Delta M_{mismatch}}$ for each M is determined from a large set of data to account for the mismatch in identical paired-transistors.

2) MAPPING OF GLOBAL PROCESS VARIABILITY-SENSITIVE DEVICE PARAMETERS TO COMPACT MODEL PARAMETERS

In section IVA2, we have shown an analytical approach to determine the critical set of device parameters, $\{V_{th0}, W, L, T_{ox}, \mu_{eff}, \gamma, R_{DS}, C_{ov}, C_j\}$, impacting MOSFET device performance due to global process variability. The corresponding set of BSIM4 compact model parameters is {VTH0, XW, XL, TOX, U0, K1, RDSW, CGSO, CGDO, CGSL, CGDL, CJS, CJD, CJSWS, CJSWD, CJSWGS, CJSWGD}; where the parameter set {CGSO, CGDO, CGSL, CGDL} defines C_{ov}; {CJS, CJD} defines S/D junction area capacitance; and {CJSWS, CJSWD, CJSWGS, CJSWGD} defines S/D junction sidewall capacitance as shown in Table 2. For each M, the variance σM_{global} is obtained from a large set of ET data and added to the mean value, M_0 to analyze the impact of chip mean variation on VLSI circuits.

C. DETERMINATION OF VARIANCE FOR PROCESS VARIABILITY-SENSITIVE COMPACT MODEL PARAMETERS

The variance σM of the compact model parameter M due to process variability is included to the mean (TT) value M_0 to model the impact of process variability on VLSI circuit performance.

1) VARIANCE OF LOCAL PROCESS VARIABILITY-SENSITIVE COMPACT MODEL PARAMETERS

For a large number of samples $\Delta M_{mismatch}$ between paired-transistors is described by standard normal distribution, $N\left(0, \sigma_{\Delta M_{mismatch}}\right)$ where the variance $\sigma_{\Delta M_{mismatch}}$ is given by: $\sigma_{\Delta M_{mismatch}}\big|_{pair} \cong A_M/\sqrt{WL}$ [47], [48]; here the parameter A_M is a technology dependent constant of ΔM and is extracted from ΔM_i versus $\left(1/\sqrt{WL}\right)$ plot for a large number ($i = 1, 2, 3, \ldots l$) of sample ET data [8], [47], [49]. Thus, for the compact model parameter V_{TH0}, the variance of ΔV_{TH0} between two paired-transistors is given by:

$$\sigma_{\Delta VTH0}\big|_{pair} \cong \frac{A_{vt}}{\sqrt{WL}} \tag{10}$$

where A_{vt} is the area dependent constant of ΔV_{TH0}. Typically, mismatch $\Delta VTH0$, ΔXW, ΔXL, ΔT_{ox}, $\Delta U0$, and $\Delta K1$ are represented by Eq. (8). Again, since ΔM_i is random and independent, therefore, the correlation $\rho\left(\Delta M_i, \Delta M_{i+1}\right) = 0$ [49]. Then, for a single device we get:

$$\sigma M_{mismatch} = \frac{1}{\sqrt{2}}\sigma_{\Delta M_i} = \frac{1}{\sqrt{2}}\frac{A_M}{\sqrt{WL}}. \tag{11}$$

In (11), $\sigma M_{mismatch}$ represents the variance of ΔM due to within-die stochastic process variability. Thus, the variance of ΔV_{TH0} is given by:

$$\sigma V_{TH0,mismatch} = \frac{1}{\sqrt{2}}\sigma_{\Delta V_{TH0}} = \frac{1}{\sqrt{2}}\frac{A_{vt}}{\sqrt{WL}} \tag{12}$$

For statistical compact modeling, $\sigma M_{mismatch}$ for each variability-sensitive model parameter is added to the corresponding M_0 to compute the mismatch between paired-transistors. Typically, for each M, A_M is extracted from Pelgrom's plot from a large set of measurement data [47], [48]. For next generation technology development, a large set of data is obtained by calibrated numerical process and device CAD to compute $\sigma M_{mismatch}$ for each variability-sensitive compact model parameters [50]–[54].

TABLE 3. Typical parameter limits for worst-case BSIM4 fixed-corner model generation.

Compact Model Parameter	FF*	SS**
TOXE	Minimum	Maximum
TOXM		
XL	Minimum	Maximum
XW	Maximum	Minimum
VTH0	Minimum	Maximum
U0	Maximum	Minimum
K1	Minimum	Maximum
RDSW	Minimum	Maximum
CGSL	Maximum	Minimum
CGDL		
CGSO	Maximum	Minimum
CGDO		
CJS	Minimum	Maximum
CJD		
CJSWS	Minimum	Maximum
CJSWD		
CJSWGS	Minimum	Maximum
CJSWGD		

* FF: fast NMOS and fast PMOS; **SS: slow NMOS and slow PMOS

2) VARIANCE OF GLOBAL PROCESS VARIABILITY-SENSITIVE COMPACT MODEL PARAMETERS

For MC statistical modeling, M_{global} is described by normal distribution $N(M_0, \sigma M_{global})$, around its mean (TT) value M_0. The global variance σM_{global} is obtained from the statistical distribution of ET data for each M measured from multiple die, wafers, and lots over a period of time [7]. However, for the next generation technology development, ET data are scarcely available for statistical analysis. In this case, the numerical simulation data can be used for the computation of σM_{global} and generate rev0 compact model for circuit analysis of the target technology [50]–[54]. Typically, $n\sigma M_{global}$ is used to model global process variability with $3 \le n \le 6$.

D. FORMULATION OF COMPACT MODEL FOR PROCESS VARIABILITY-AWARE CIRCUIT DESIGN

As described in section IIIA, the TT model for circuit CAD consists of a set of parameters $\{M_0\}$ that models the device and circuit performance of centerline process of the target technology node. The set $\{M_0\}$ represents the nominal device specifications of the target technology. The local and global components of the variability-sensitive compact model

TABLE 4. Process variability-sensitive BSIM4 model parameters formatted for MC statistical analysis using Hspice.

Compact Model Parameter	Typical Value (M_0)	Local Component of Model Parameter		Global Component of Model Parameter		Compact Model Parameter for MC Statistical Analysis
		$\sigma M_{mismacth_z}$	PDF for MC Analysis	σM_{global_z}	PDF for MC Analysis	
TOXE	$toxe0$	$\sigma_{toxm_z} = \frac{1}{\sqrt{2}} \frac{A_{tox}}{\sqrt{WL}}$	$\sigma_{toxm_z} agauss(0{,}1{,}1)$	σ_{tox_z}	$\sigma_{tox_z} agauss(0{,}1{,}3)$	$toxe0 + \sigma_{toxm_z} agauss(01{,}1) + \sigma_{tox_z} agauss(0{,}1{,}3)$
TOXM	$toxm0$					$toxm0 + \sigma_{toxm_z} agauss(01{,}1) + \sigma_{tox_z} agauss(0{,}1{,}3)$
XL	$xl0$	$\sigma_{xlm_z} = \frac{1}{\sqrt{2}} \frac{A_{xl}}{\sqrt{WL}}$	$\sigma_{xlm_z} agauss(0{,}1{,}1)$	σ_{xl_z}	$\sigma_{xl_z} agauss(0{,}1{,}3)$	$xl0 + \sigma_{xlm_z} agauss(0{,}1{,}1) + \sigma_{xl_z} agauss(0{,}1{,}3)$
XW	$xw0$	$\sigma_{xwm_z} = \frac{1}{\sqrt{2}} \frac{A_{xw}}{\sqrt{WL}}$	$\sigma_{xwm_z} agauss(0{,}1{,}1)$	σ_{xw_z}	$\sigma_{xw_z} agauss(0{,}1{,}3)$	$xw0 + \sigma_{xwm_z} agauss(0{,}1{,}1) + \sigma_{xw_z} agauss(0{,}1{,}3)$
VTH0	$vth0$	$\sigma_{vthm_z} = \frac{1}{\sqrt{2}} \frac{A_{vt}}{\sqrt{WL}}$	$\sigma_{vthm_z} agauss(0{,}1{,}1)$	σ_{vth_z}	$\sigma_{vth_z} agauss(0{,}1{,}3)$	$vth0 + \sigma_{vthm_z} agauss(0{,}1{,}1) + \sigma_{vth_z} agauss(0{,}1{,}3)$
U0	$u00$	$\sigma_{u0m_z} = \frac{1}{\sqrt{2}} \frac{A_{u0}}{\sqrt{WL}}$	$\sigma_{u0m_z} agauss(0{,}1{,}1)$	σ_{u0_z}	$\sigma_{u0_z} agauss(0{,}1{,}3)$	$u00 + \sigma_{u0m_z} agauss(0{,}1{,}1) + \sigma_{u0_z} agauss(0{,}1{,}3)$
K1	$k10$	$\sigma_{k1m_z} = \frac{1}{\sqrt{2}} \frac{A_{k1}}{\sqrt{WL}}$	$\sigma_{k1m_z} agauss(0{,}1{,}1)$	σ_{k1_z}	$\sigma_{k1_z} agauss(0{,}1{,}3)$	$k10 + \sigma_{k1m_z} agauss(0{,}1{,}1) + \sigma_{k1_z} agauss(0{,}1{,}3)$
RDSW	rdsw0	*	*	σ_{rdsw_z}	$\sigma_{rdsw_z} agauss(0{,}1{,}3)$	$rdsw0 + \sigma_{rdsw_z} agauss(0{,}1{,}3)$
CGSL	cgl0	*	*	σ_{cgl_z}	$\sigma_{cgl_z} agauss(0{,}1{,}3)$	$cgl0 + \sigma_{cgl_z} agauss(0{,}1{,}3)$
CGDL						$cgl0 + \sigma_{cgl_z} agauss(0{,}1{,}3)$
CGSO	cgo0	*	*	σ_{cgo_z}	$\sigma_{cgo_z} agauss(0{,}1{,}3)$	$cgo0 + \sigma_{cgo_z} agauss(0{,}1{,}3)$
CGDO						$cgo0 + \sigma_{cgo_z} agauss(0{,}1{,}3)$
CJS	cj0	*	*	σ_{cj_z}	$\sigma_{cj_z} agauss(0{,}1{,}3)$	$cj0 + \sigma_{cj_z} agauss(0{,}1{,}3)$
CJD						$cj0 + \sigma_{cj_z} agauss(0{,}1{,}3)$
CJSWS	cjsw0	*	*	σ_{cjsw_z}	$\sigma_{cjsw_z} agauss(0{,}1{,}3)$	$cjsw0 + \sigma_{cjsw_z} agauss(0{,}1{,}3)$
CJSWD						$cjsw0 + \sigma_{cjsw_z} agauss(0{,}1{,}3)$
CJSWGS	cjswg0	*	*	σ_{cjswg_z}	$\sigma_{cjswg_z} agauss(0{,}1{,}3)$	$cjswg0 + \sigma_{cjswg_z} agauss(0{,}1{,}3)$
CJSWGD						$cjswg0 + \sigma_{cjswg_z} agauss(0{,}1{,}3)$

In $\sigma M_{mismatch_z}$ and σM_{global_z} ; $z = \begin{cases} n \text{ for nMOSFETs} \\ p \text{ for pMOSFETs} \end{cases}$

parameter are included in the nominal set $\{M_0\}$ to generate compact variability model for circuit CAD. The final model includes the nominal parameters with the components of process variability. Thus, a process variability-sensitive model parameter M including both local and global process variability components is given by:

$$M = M_0 + \sigma M_{mismatch} + n\sigma M_{global} \quad (13)$$

Equation (13) is used to build the compact model of the target technology for process variability-aware circuit analysis. Thus, for the compact model parameter V_{TH}, Eq. (13) yields:

$$V_{TH} = V_{TH0} + \sigma V_{TH0,mismatch} + n\sigma V_{TH0,global}. \quad (14)$$

Equation (13) is used to build statistical corner model for realistic analysis of process variability in scaled MOSFETs. Table 3 shows FF and SS corner limit of the set of process variability-sensitive model parameters obtained by analytical approach discussed in subsection IVB.

For Monte Carlo (MC) statistical compact modeling, the *probability distribution function* (PDF) of the mismatch component of M for HSPICE circuit CAD is obtained by [55]:

$$PDF(\sigma M_{mismatch}) = (\sigma M_{mismatch}) agauss(0, 1, 1) \quad (15)$$

Similarly, the PDF for the global component of M is expressed as:

$$PDF(\sigma_{global}) = (\sigma_{global}) agauss(0, 1, 3) \quad (16)$$

Equations (15) and (16) are used in (13) to formulate the variability-sensitive compact model parameters to develop the final model library for HSPICE circuit CAD. Table 4 shows the formulation of variability-sensitive BSIM4 model

parameters in the model library. Thus, for the variability-sensitive V_{TH}, we have:

$$V_{TH} = V_{TH0} + \frac{1}{\sqrt{2}}\frac{Avt}{\sqrt{WL}} agauss(0, 1, 1) + \sigma V_{TH0} agauss(0, 1, 3) \quad (17)$$

The above procedure is used to build BSIM4 MOSFET compact model library for the advanced CMOS technology reported in [3]–[5]. For the simplicity of showing the basic functionality of the present modeling approach, all mismatches are lumped into V_{th} mismatch and the correlation between the model parameters is ignored.

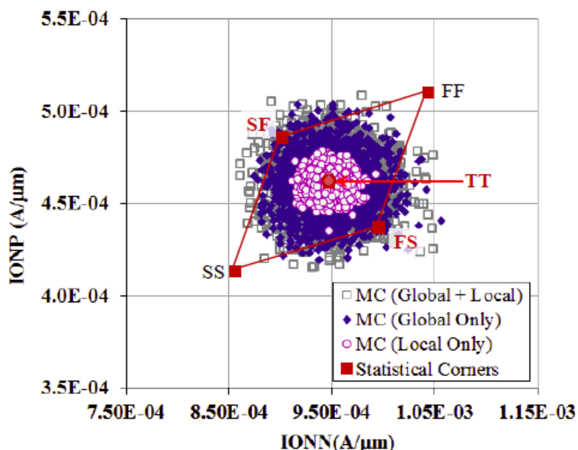

FIGURE 7. MC simulation data obtained by Hspice circuit CAD for an advanced CMOS technology; simulation data shows the distribution of ON currents for pMOSFETs (IONP) and nMOSFETs (IONN) for local only, global only, and both local and global process variability. The simulated statistical corners along with the nominal (TT) value of drain currents, are, also, superimposed on the plot using solid rectangular symbols.

V. SIMULATION RESULTS AND DISCUSSIONS

The model library developed in section IV is used for MC statistical analysis of advanced MOSFET devices [3]–[5]. Fig. 7 shows the distribution of IONN and IONP obtained by HSPICE circuit simulation [55]. Here, ION is defined at $|V_{gs}| = |V_{ds}| = 1$ V for 20 nm technology [5], [6]. The IONN *versus* IONP distribution in Fig. 7, clearly, shows the impact of local process variability or mismatch, global process variability or chip mean variation, and the local and global process variability combined. In Fig. 7, the simulation data from statistical corner values of IONN and IONP are, also superimposed on the plot for reference. In Fig. 7, FF and SS corner encloses the MC distribution of ON currents. Thus, in contrast to fixed pessimistic corners, shown in Fig. 4, the statistical corners offer realistic analysis of process variability similar to MC analysis as shown in Fig. 7. Fig. 7, also, shows that local variability is a significant factor of the total (global + local) variability as observed for advanced technologies [56]. Thus, it is critical to accurately model local fluctuations in advanced CMOS technologies.

VI. CONCLUSION

This paper presented a systematic procedure to determine process variability-sensitive compact model parameters and develop statistical compact models to investigate the impact of process variability on circuit performance. The present analytical approach to determine variability-sensitive compact model parameters is cost-effective and efficient compared to the time consuming and expensive PCA and ET data-based approaches for statistical compact modeling. The proposed method, also, allows generating realistic statistical corners compared to pessimistic fixed corners and can be used to generate statistical compact models from the basic expressions for device performance using numerical simulation data. This statistical corner models enable designers to assess the impact of process variability on circuit performance without time consuming MC analysis. The proposed approach is ideal for developing statistical compact model of next generation technology where data for statistical analysis are not available. The future consideration of this procedure is to include correlation factors among the process variability-sensitive global model parameters. And, include adequate process variability-sensitive sub-threshold region compact model parameters to analyze the impact of process variability on sub-threshold performance of analog circuits. The present statistical-modeling approach enables realistic assessment of the standard deviation of circuit performance and allows for tracking circuit performance due to process variability. In addition, the present methodology offers concurrent next generation technology and product development. Though the present methodology is used to generate statistical compact models using BSIM4, it can be applied to any compact models considering the basic equations for device performance.

ACKNOWLEDGMENT

Grateful thanks are due to Mr. Balasubramanian Murugan for valuable comments and suggestions during this work.

REFERENCES

[1] K. J. Kuhn, "Considerations for ultimate CMOS scaling," *IEEE Trans. Electron Devices*, vol. 59, no. 7, pp. 1813–1828, Jul. 2012.
[2] H. Iwai, "CMOS technology—Year 2010 and beyond," *IEEE J. Solid-State Circuits*, vol. 34, no. 3, pp. 357–366, Mar. 1999.
[3] S. Saha, "Scaling considerations for high performance 25 nm metal–oxide–semiconductor field-effect transistors," *J. Vac. Sci. Technol. B, Microelectron. Nanometer Struct.*, vol. 19, no. 6, pp. 2240–2246, Nov. 2001.
[4] S. Saha, "Design considerations for 25 nm MOSFET devices," *Solid-State Electron.*, vol. 45, no. 10, pp. 1851–1857, Oct. 2001.
[5] S. K. Saha, "Transistors having optimized source-drain structures and methods for making the same," U.S. Patent 6 344 405, Feb. 5, 2002.
[6] S. Saha, "Device characteristics of sub-20 nm silicon nanotransistors," *Proc. SPIE*, vol. 5042, pp. 172–179, Jul. 2003.
[7] S. K. Saha, "Modeling process variability in scaled CMOS technology," *IEEE Des. Test Comput.*, vol. 27, no. 2, pp. 8–16, Apr. 2010.
[8] K. J. Kuhn, M. D. Giles, D. Becher, P. Kolar, A. Kornfeld, R. Kotlyar, *et al.*, "Process technology variation," *IEEE Trans. Electron Devices*, vol. 58, no. 8, pp. 2197–2208, Aug. 2011.

[9] C. M. Mezzomo, A. Bajolet, A. Cathignol, R. Di Frenza, and G. Ghibaudo, "Characterization and modeling of transistor variability in advanced CMOS technologies," *IEEE Trans. Electron Devices*, vol. 58, no. 8, pp. 2235–2248, Aug. 2011.

[10] K. Bernstein D. J. Frank, A. E. Gattiker, W. Haensch, B. L. Ji, S. R. Nassif, *et al.*, "High-performance CMOS variability in the 65-nm regime and beyond," *IBM J. Res Dev.*, vol. 50, nos. 4–5, pp. 433–449, Sep. 2006.

[11] S. K. Springer, S. Lee, N. Lu, E. J. Nowak, J. O. Plouchart, J. S. Watts, *et al.*, "Modeling of variation in submicrometer CMOS ULSI technologies," *IEEE Trans. Electron Devices*, vol. 53, no. 9, pp. 2168–2178, Sep. 2006.

[12] S. Saha, "Effects of inversion layer quantization on channel profile engineering for nMOSFETs with 0.1 μm channel lengths," *Solid-State Electron.*, vol. 42, no. 11, pp. 1985–1991, Nov. 1998.

[13] K. Fujita, Y. Tori, M. Hori, J. Oh, L. Shifren, P. Ranade, *et al.*, "Advanced channel engineering achieving aggressive reduction of VT variation for ultra-low-power applications," in *Proc. IEEE IEDM*, Dec. 2011, pp. 749–752.

[14] K. Singhal and V. Visvanathan, "Statistical models for worst case files and electrical data," *IEEE Trans. Semicond. Manuf.*, vol. 12, no. 4, pp. 470–484, Nov. 1999.

[15] S. M. Kang and A. Dharchoudhury, "Worst-case analysis and optimization of VLSI circuit performances," *IEEE Trans. Comput. Aided Des. Integr. Circuits Syst.*, vol. 14, no. 4, pp. 481–492, Apr. 1995.

[16] I. N. Hajj, T. N. Trick, T.-K. Yu, and S. M. Kang, "Statistical performance modeling and parametric yield estimation of MOS VLSI," *IEEE Trans. Comput. Aided Des.*, vol. 6, no. 6, pp. 1013–1022, Nov. 1987.

[17] (2006). *BSIM4.6.0 MOSFET Model—User's Manual* [Online]. Available: http://www.device.eecs.berkeley.edu/bsim/Files/BSIM4/BSIM460/doc/BSIM460_Manual.pdf

[18] (2011). *International Technology Roadmap for Semiconductors (ITRS)* [Online]. Available: http://www.itrs.net/

[19] P. Stolk, F. Widdershoven, and D. Klaassen, "Modeling statistical dopant fluctuations in MOS transistors," *IEEE Trans. Electron Devices*, vol. 45, no. 9, pp. 1960–1971, Sep. 1998.

[20] T. Mizuno, J.-I. Okamura, and A. Toriumi, "Experimental study of threshold voltage fluctuation due to statistical variation of channel dopant number in MOSFETs," *IEEE Trans. Electron Devices*, vol. 41, no. 11, pp. 2216–2221, Nov. 1994.

[21] A. Asenov, "Random-dopant-induced threshold voltage lowering and fluctuations in sub-0.1 μm MOSFETs: A 3-D 'atomistic' simulation study," *IEEE Trans. Electron Devices*, vol. 45, no. 12, pp. 2505–2513, Dec. 1998.

[22] A. Asenov, S. Kaya, and A.R. Brown, "Intrinsic parameter fluctuations in decananometer MOSFETs introduced by line edge roughness," *IEEE Trans. Electron. Devices*, vol. 50, no. 5, pp. 1254–1260, May 2003.

[23] C. H. Diaz, H.-J. Tao, Y.-C. Ku, A. Yen, and K. Young, "An experimentally validated analytical model for gate line edge roughness (LER) effects on technology scaling," *IEEE Electron Device Lett.*, vol. 22, no. 6, pp. 287–289, Jun. 2001.

[24] M. Koh, W. Mizubayashi, K. Iwamoto, H. Murakami, T. Ono, M. Tsuno, *et al.*, "Limit of gate oxide thickness scaling in MOSFETs due to apparent threshold voltage fluctuation introduced by tunneling leakage current," *IEEE Trans. Electron Devices*, vol. 48, no. 2, pp. 259–264, Feb. 2001.

[25] A. Asenov, S. Kaya, and J. H. Davies, "Intrinsic threshold voltage fluctuations in decananometer MOSFETs due to local oxide thickness variations," *IEEE Trans. Electron. Devices*, vol. 49, no. 1, pp. 112–119, Jan. 2002.

[26] A. R. Brown, G. Roy, and A. Asenov, "Poly-Si-gate-related variability in decananometer MOSFETs with conventional architecture," *IEEE Trans. Electron Devices*, vol. 54, no. 11, pp. 3056–3063, Nov. 2007.

[27] Y. Zhang, J. Li, M. Grubbs, M. Deal, B. Magyari-Kope, B. M. Clemens, *et al.*, "Physical model of the impact of metal grain work function variability on emerging dual metal gate MOSFETs and its implication for SRAM reliability," in *Proc. IEEE IEDM*, Dec. 2009, pp. 57–60.

[28] V. S. Kaushik, B. J. O'Sullivan, G. Pourtois, N. Van Hoornick, A. Delabie, S. Van Elshocht, *et al.*, "Estimation of fixed charge densities in hafnium-silicate gate dielectrics," *IEEE Trans. Electron Devices*, vol. 53, no. 10, pp. 2627–2633, Oct. 2006.

[29] H. C. Wen, H. R. Harris, C. D. Young, H. Luan, H. N. Alshareef, K. Choi, *et al.*, "On oxygen deficiency and fast transient charge-trapping effects in high-k dielectrics," *IEEE Electron Device Lett.*, vol. 27, no. 12, pp. 984–987, Dec. 2006.

[30] L. Capodieci, "From optical proximity correction to lithography-driven physical design (1996-2006): 10 years of resolution enhancement technology and the roadmap enablers for the next decade," *Proc. SPIE*, vol. 6154, p. 615401, Mar. 2006.

[31] S. Nag, A. Chatterjee, K. Taylor, I. Ali, S. O'Brien, S. Aur, *et al.*, "Comparative evaluation of gap-fill dielectrics in shallow trench isolation for sub-0.25 μm technologies," in *Proc. IEDM*, Dec. 1996, pp. 841–845.

[32] J. Steigerwald, "Chemical mechanical polish: The enabling technology," in *Proc. IEDM*, Dec. 2008, pp. 37–40.

[33] Y. L. Tsang, S. Chattopadhyay, S. Uppal, E. Escobedo-Cousin, H. K. Ramakrishnan, S. H. Olsen, *et al.*, "Modeling of the threshold voltage in strained $Si/Si_{1-x}Ge_xSi_{1-y}Ge_x$ CMOS architectures," *IEEE Trans. Electron Devices*, vol. 54, no. 11, pp. 3040–3048, Nov. 2007.

[34] O. Weber, O. Faynot, F. Andrieu, C. Buj-Dufournet, F. Allain, P. Scheiblin, *et al.*, "High immunity to threshold voltage variability in undoped ultrathin FDSOI MOSFETs and its physical understanding," in *Proc. IEEE IEDM*, Dec. 2008, pp. 245–248.

[35] L.-T. Pang, K. Qian, C. J. Spanos, and B. Nikolic, "Measurement and analysis of variability in 45-nm strained-Si CMOS technology," *IEEE J. Solid-State Circuits*, vol. 44, no. 8, pp. 2233–2243, Aug. 2009.

[36] T. Tanaka, T. Usuki, T. Futatsugi, Y. Momiyama, and T. Sugii, "Vth fluctuation induced by statistical variation of pocket dopant profile," in *Proc. IEDM*, Dec. 2000, pp. 271–274.

[37] I. Ahsan, N. Zamdmer, O. Glushchenkov, R. Logan, E. J. Nowak, H. Kimura, *et al.*, "RTA-driven intra-die variations in stage delay and parametric sensitivities for 65nm technology," in *Symp. VLSI Technol. Tech. Dig.*, Jun. 2006, pp. 170–171.

[38] N. D. Arora, "MOSFET models for VLSI circuit simulation, Theory and Practice." Vienna, Austria: Springer-Verlag, 1993.

[39] J. C. Chen, C. Hu, C.-P. Wan, P. Bendix, and A. Kapoor, "E-T based statistical modeling and compact statistical circuit simulation methodologies," in *Proc. IEDM*, Dec. 1996, pp. 635–638.

[40] C.-H. Lin, M. V. Dunga, D. D. Lu, A. M. Niknejad, and C. Hu, "Performance-aware corner model for design for manufacturing," *IEEE Trans. Electron Devices*, vol. 56, no. 4, pp. 595–600, Apr. 2009.

[41] G. Rappitsch, E. Seebacher, M. Kocher, and E. Stadlober., "SPICE modeling of process variation using location depth corner models," *IEEE Trans. Semicond. Manuf.*, vol. 17, no. 2, pp. 201–213, May 2004.

[42] C. C. McAndrew, "Statistical modeling for circuit simulation," in *Proc. 4th ISQED*, Mar. 2003, pp. 357–362.

[43] C. C. McAndrew, I. Stevanovic, X. Li, and G. Gildenblat, "Extensions to backward propagation of variance for statistical modeling," *IEEE Des. Test Comput.*, vol. 27, no. 2, pp. 36–43, Mar. 2010.

[44] G. Gildenblat, X. Li, W. Wu, H. Wang, A. Jha, R. van Langevelde, *et al.*, "PSP: An advanced surface-potential-based MOSFET model for circuit simulation," *IEEE Trans. Electron. Devices*, vol. 53, no. 9, pp. 1254–1260, Sep. 2006.

[45] *HiSIM2 Users Manual*, Hiroshima Univ., Hiroshima, Japan, 2005.

[46] J. A. Croon, W. Sansen, and H. E. Maes, *Matching Properties of Deep Sub-Micron MOS Transistors*. Amsterdam, The Netherlands: Springer-Verlag, 2005.

[47] M. J. M. Pelgrom, A. C. J. Duinmaijer, and A. P. G. Welbers, "Matching properties of MOS transistors," *IEEE J. Solid-State Circuits*, vol. 24, no. 5, pp. 1433–1439, Oct. 1989.

[48] M. Pelgrom, H. Tuinhout, and M. Vertregt, "Modeling of MOS matching," in *Compact Modeling: Principles, Techniques and Applications*, G. Gildenblat, Ed. New York, NY, USA: Springer-Verlag, 2010.

[49] J. Mazurier, O. Weber, F. Andrieu, A. Toffoli, O. Rozeau, T. Poiroux, *et al.*, "On the variability in planar FDSOI technology: From MOSFETs to SRAM cells," *IEEE Trans. Electron Devices*, vol. 58, no. 8, pp. 2326–2336, Aug. 2011.

[50] S. K. Saha, "Introduction to technology computer aided design," in *Technology Computer Aided Design: Simulation for VLSI MOSFET*, C. K. Sarkar, Ed. Boca Raton, FL, USA: CRC Press, May 2013.

[51] S. Saha, C. S. Yeh, and B. Gadepally, "Impact ionization rate of electrons for accurate simulation of substrate current in submicron devices," *Solid-State Electron.*, vol. 36, no. 10, pp. 1429–1432, Oct. 1993.

[52] S. Saha, "Extraction of substrate current model parameters from device simulation," *Solid State Electron.*, vol. 37, no. 10, pp. 1786–1788, Oct. 1994.

[53] S. K. Saha, "Managing technology CAD for competitive advantage: An efficient approach for integrated circuit fabrication technology development," *IEEE Trans. Eng. Manag.*, vol. 46, no. 2, pp. 221–229, May 1999.

[54] S.K. Saha, "Modelling the effectiveness of computer-aided development projects in the semiconductor industry," *Int. J. Eng. Manag. Econ.*, vol. 1, nos. 2–3, pp. 162–178, Nov. 2010.

[55] *Simulation and Analysis User Guide*, HSPICE, Santa Clara, CA, USA, Mar. 2006.

[56] M. Kanno, A. Shibuya, M. Matsumura, K. Tamura, H. Tsuno, S. Mori, *et al.*, "Empirical characteristics and extraction of overall variations for 65-nm MOSFETs and beyond," in *Proc. IEEE Symp. VLSI Technol.*, Jun. 2007, pp. 88–89.

SAMAR K. SAHA received the Ph.D. degree in physics from Gauhati University, Guwahati, India, and the M.S. degree in engineering management from Stanford University, Stanford, CA, USA. He is currently a Technical Advisor with Ultrasolar Technology, Santa Clara, CA, and an Adjunct Professor with the Electrical Engineering Department, Santa Clara University, Santa Clara. Since 1984, he has worked in various positions for National Semiconductor, LSI Logic, Texas Instruments, Philips Semiconductors, Silicon Storage Technology, Synopsys, DSM Solutions, Silterra USA, and SuVolta. In academia, he worked as a faculty member with the Electrical Engineering Departments with the Southern Illinois University, Carbondale, IL, USA, the Auburn University, Auburn, AL, the University of Nevada at Las Vegas, NV, USA, and the University of Colorado at Colorado Springs, CO, USA. His current research interests include nanoscale device and process architecture, Technology CAD (TCAD), compact modeling, and TCAD and research and development management.