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Design criteria of high temperature integrated circuits using standard SOI CMOS process up to 300°C

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ABSTRACT — In this paper, we discuss the challenges at the device and circuit level that must be addressed to design reliable silicon CMOS integrated circuits operating in high-temperature environments. We present experimental results on representative devices fabricated with a 180 nm CMOS SOI platform, which have been characterized up to 300°C, discuss issues arising at high temperature, and propose possible solutions. A BJT-based temperature sensor core is also described and evaluated across the same extended temperature range. We also propose and discuss design criteria optimized for a wide range of operating temperature. A sufficient on/off current ratio can be achieved by taking advantage of the isolation provided by low-leakage CMOS SOI process, while operation at low current density must be ensured to mitigate electromigration effects. Within these conditions, low-power precise sensing circuits can be effectively implemented with operating temperature up to 300°C, that are extremely relevant for industrial, mobility, and space applications.

INDEX TERMS High temperature electronics; harsh environment electronics; CMOS SOI.

I. INTRODUCTION

The rising need for electronic systems able to operate in harsh environments is fostering research towards electronics with reliable high-temperature operation [1], posing challenges which are being addressed at several levels: from innovative semiconductor device materials [2], to integrated circuit (IC) design techniques [3] and printed circuit board (PCB) level circuit assembly of packaged ICs [4].

Electronic components for commercial applications usually cannot operate at temperatures exceeding 100-150°C (Fig. 1) [4]. However, in automotive and aerospace applications, in power management systems, and in oil and gas extraction equipment, the temperature can rise well above 200°C [4], [5]. On a physical level, materials different from silicon and aluminum could be used for active devices and intra-chip connections, respectively [4], [6]. Robust packages resilient to thermal stress, wire and board isolations, application-specific soldering materials and techniques are all required to provide a necessary protection against a harsh environment [4], [6], [7].

In the case of extreme high-temperature applications, e.g. in geothermal wells where temperatures over 600°C can be reached [5], wide bandgap (WBG) materials such as GaN and SiC are today employed to obtain reliable power devices [5], [6], while high strength and low density metal alloys (e.g. TiAl) are used for interconnections [4], [5].

Thanks to the excellent thermal properties and high voltage handling capabilities of SiC, analog and digital SiC CMOS processes are actively being developed [8], progressively reducing the large performance gap with respect to silicon CMOS [9]–[11]. Further improvements in terms of both semiconductor and packaging technology are needed to achieve sufficient reliability and low fabrication cost, for a specific SiC IC market to be established [12].

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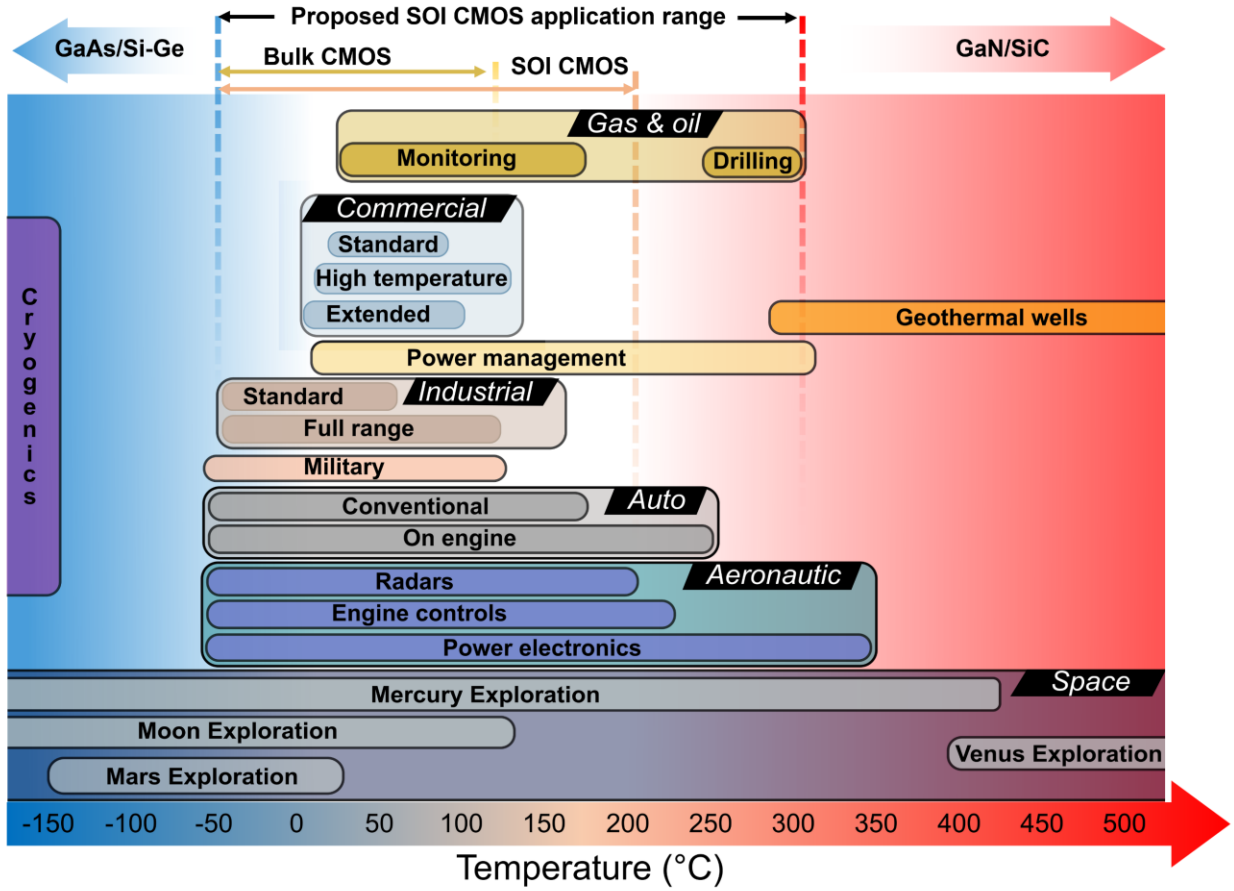

FIGURE 1. **Temperature ranges for various electronics applications.**

Moreover, device technology improvement is required to reduce the threshold voltage and therefore the supply voltage of WBG devices, enabling low-power electronics suitable for portable systems [5].

It is worth mentioning that high-temperature portable electronics poses complex challenges also from the power supply point of view, due to the reduced performance, short autonomy, and poor reliability of conventional lithium-ion batteries at high temperature. Alternative solutions such as innovative battery chemistry, supercapacitors, energy harvesting or wireless power transfer systems, are crucial to address this gap. In this regard, some lithium-based battery cells for very high temperature are being proposed [13], [14], but their usability is limited due to poor electrical characteristics, in terms of low output current, charging capability and reduced temperature range (i.e. 225°C rated batteries work only above 150°C [15]). On the other end of the spectrum, for cryogenic applications (below −150°C), GaAs and SiGe devices are promising [16], even though the suitability of silicon has been proven [17].

From the perspective of ICs realized with silicon devices, commercial CMOS technology platforms are normally qualified in the −40°C to 125/150°C temperature range (e.g. in line with grade 1 automotive range of AEC-Q100 [18]), since significant leakage current arises at higher temperature [6]. Silicon-On-Insulator (SOI) CMOS technologies have demonstrated a higher temperature capability (e.g. up to 175°C), since the limited substrate thickness enables low leakage currents.

The affordability and reliability of silicon technology continue to drive research towards the exploitation of standard CMOS over a wider temperature range, even if WBG materials have intrinsic advantages at high temperature. In [19], electrical characterization of 180-nm and 500-nm SOI CMOS devices up to 300°C shows good performance and the existing SPICE model BSIMSOI has been adapted to cover the extended temperature range. The work in [20] instead is more oriented to the design techniques for high temperature circuits, based on g_m/I_d methodology for Zero Temperature Coefficient (ZTC) biasing. The following work [21] by the same group extends the proposed design methodology up to an operation temperature of 250°C, assessing the functionality with chip measurements on a Voltage Controlled Oscillator. A temperature-dependent SOI MOSFET compact model has been developed in [22], considering the existing temperature dependence of device parameters, but only for long-channel MOSFETs based on old technology processes. Other high-temperature specific issues have been addressed by Denis Flandre et al. in [23], where low-frequency noise in

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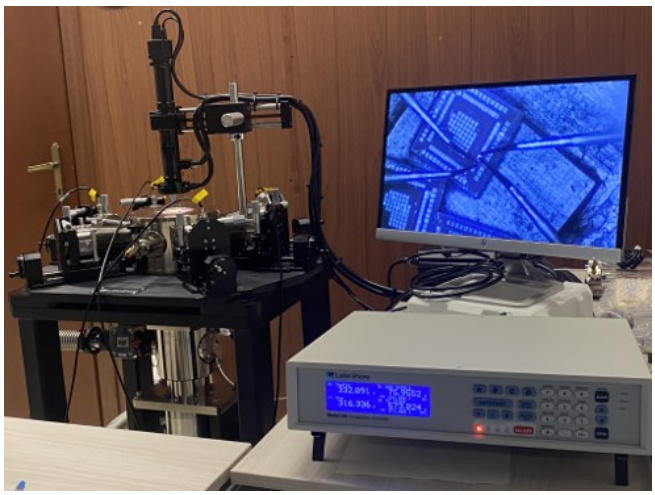

FIGURE 2. Measurement setup with the Lake Shore Probe Station (model CRX-6.5K) and Model 336 Temperature Controller.

submicron SOI devices has been characterized up to 230°C, and in [24], where special transistor layout geometries have been investigated to counteract the increase in leakage current at high temperature.

Fundamental analog building blocks, such as latched comparators [25], instrumentation amplifiers [26], low drop-out voltage regulators [27], bandgap references, Δ–Σ converters [28]–[30], and SRAM memory cells [31] have been recently proposed. Temperature sensor systems, capable of working outside the CMOS process qualification range, have also been proven in [28], [32], exploiting either Fully-Depleted (FD) or Partially-Depleted (PD) SOI CMOS processes.

To focus our analysis on the use of CMOS-SOI at high temperature on a tangible example, we consider a commercially available 180 nm technology with aluminum metal lines (XFAB XT018), and discuss the design criteria and the challenges associated to extending the region of operation of analog ICs up to a temperature of 300°C. It is important to consider that such XFAB process is qualified between -40°C and 175°C, and hence the process-design kit (PDK) device models are likely calibrated in the same temperature range. This means that, above 175°C, PDK models could not be able to accurately reproduce device behavior. Let us stress the fact that the considerations we will make on our example process can be extended and generalized to other processes and technology nodes.

We perform the analysis starting from the discussion of single device characteristics, including MOSFET and bipolar transistors, and of passive resistor implementations, measured up to 300°C with the test setup in Fig. 2. Design guidelines to counteract leakage currents are provided, also presenting simple analog building blocks specifically designed for a wide temperature range (e.g. a temperature sensor core). Compared with previous works, we introduce a novel approach focused on devices available in the PDK of a standard SOI process to implement temperature-resilient design techniques at the circuit level. The proposed techniques can be used together with ZTC biasing strategies, as the one proposed in [20], to effectively improve the robustness of ICs in extreme temperature environments.

The remainder of the paper is organized as follows. Section II reviews the issues associated with high temperature operation in silicon CMOS. High-temperature device-level figures of merit (from experiments and simulation) are discussed in Section III. Circuit-level design high-temperature compensation techniques are presented in Section IV. An example of circuit building block (i.e. a temperature sensor core), optimized for high-temperature operation, is presented in Section V. Finally, in Section VI, conclusions are drawn.

II. HIGH TEMPERATURE OPERATIONS OF SILICON DEVICES

Several issues are associated to CMOS high temperature operation. From a physical point of view, as the operating temperature is increased, the semiconductor material properties change [33]: the intrinsic carrier density and the carrier diffusion length increase, while the charge carrier lifetime and the thermal conductivity decrease. Such physical phenomena have a direct impact on the device performance degradation at high temperatures, introducing the need of a well-defined temperature range, where the CMOS electrical characteristics are guaranteed to fall within certain specifications. Even if Si can theoretically work at much higher temperatures [33], with a maximum limit determined by the material energy bandgap and the required blocking voltage, the device performance degradation may heavily affect the designed electronic circuits and poses practical bounds to the acceptable temperature range.

The most critical issues in high temperature CMOS design are the following:

- pn junction reverse saturation current increase;
- subthreshold channel leakage current increase;
- electromigration of metal lines.

The issues causing an increase of the leakage currents are related to the front-end-of-line (FEOL) devices, as depicted in NMOS and PMOS transistor cross-sections shown in Fig. 3(a); electromigration, instead, is the main challenge at the back-end-of-line (BEOL), affecting metal lines, contacts, and vias.

To evaluate the quantitative impact of these phenomena in design, a test chip has been designed and manufactured in the XFAB XT018 technology. The test chip includes single devices and test structures, specifically conceived for the characterization of temperature-dependent parameters. We show in Fig. 3(b-f) the representative electrical parameters of a 1.8-V NMOS, with channel width $W = 1\ \mu m$ and length $L = 1\ \mu m$, as a function of temperature, obtained from measurements and PDK-model simulations. We discuss these

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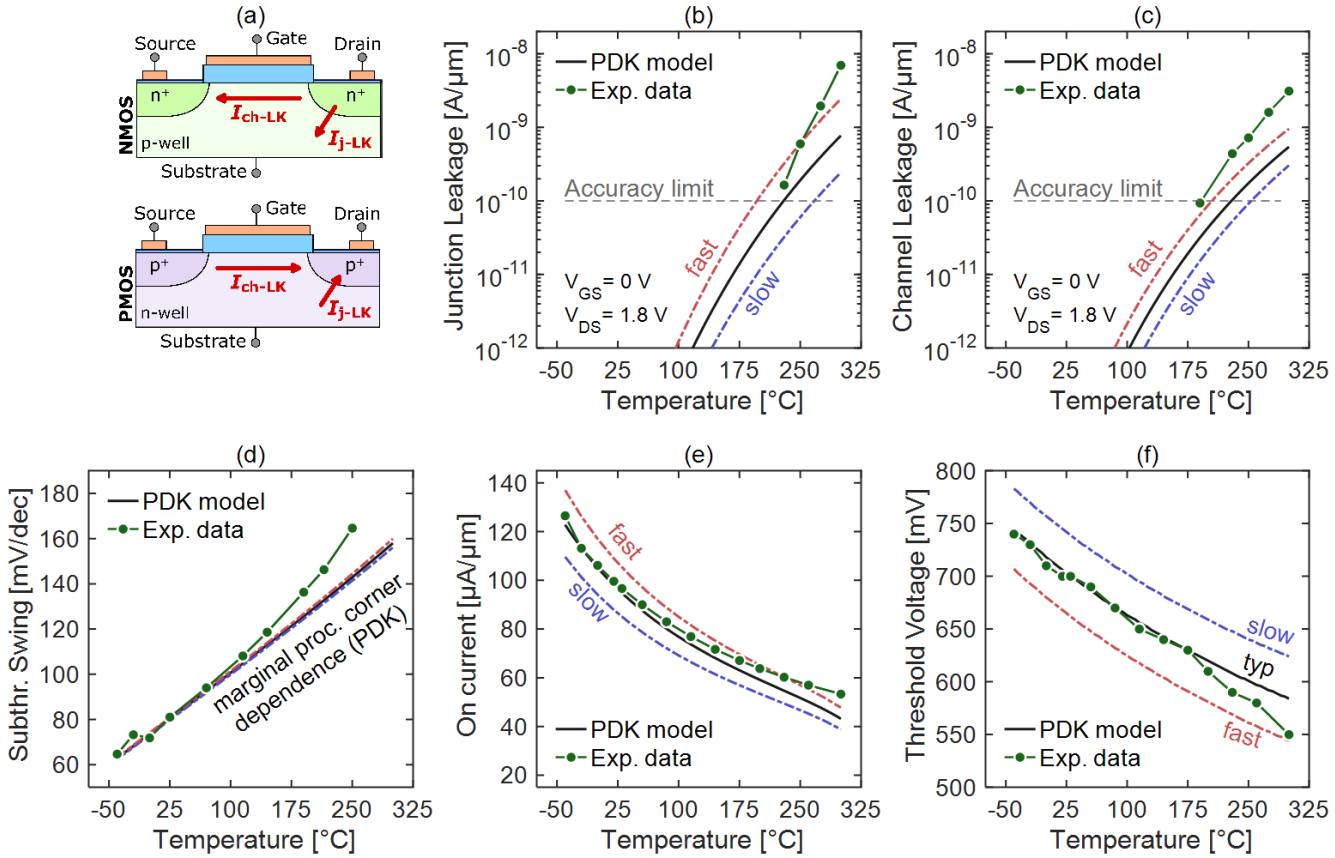

FIGURE 3. (a) NMOS and PMOS cross section sketches depicting the channel and junction leakage current effects. Impact of temperature variation (from −40°C to 300°C) on experimental 1.8-V NMOS ($L = 1\ \mu m, W = 1\ \mu m$) electrical parameters: (b) junction and (c) channel leakage currents at $V_{DS} = 1.8\ V, V_{GS} = 0\ V$; (d) subthreshold swing, extracted from I_S with $V_{SB} = 0\ V$ to avoid junction leakage; (e) drain on-current I_{ON} extracted at $V_{DS} = V_{GS} = 1.8\ V$; (f) threshold voltage extracted at constant off-current $I_{OFF}/W = 500\ nA/\mu m$. Simulated confidence-interval corners (PDK model process corners) are also shown in red (fast corner) and blue (slow corner).

behaviors in the following subsections focusing on six aspects: A) pn junction reverse current, B) subthreshold current leakage, C) subthreshold swing and on/off current ratio, D) threshold voltage, E) electromigration, and F) other temperature effects.

A. PN JUNCTION REVERSE CURRENT PATHS

Several p-n junctions are present in a CMOS device and are biased in reverse mode in normal operation, leading to several junction reverse current paths: drain-body, source-body and the well-to-well junctions. The reverse saturation current depends on junction doping and on temperature-dependent parameters [33]:

- the intrinsic carrier concentration n_i, which increases with temperature according to:

$$n_i \propto T^{\frac{3}{2}} \cdot e^{-\frac{E_G(T)}{2kT}} \quad (1)$$

  where T is the temperature in Kelvin, E_G is the silicon energy gap, which also shrinks with temperature [34], [35], and k is the Boltzmann constant;
- the hole and electron diffusion coefficients, increasing with increasing temperature.

The combination of the aforementioned effects determines the junction leakage current behavior, leading to a quasi-exponential increase with temperature, that limits the functionality of electronic circuits, increasing the static power consumption and the probability of latch-up phenomena. The substrate leakage current can lead to thermally induced latch-up, which produces overheating and degrades circuit reliability. This issue is limited by using an SOI CMOS process, which features junction leakage current reduction in the range from ~10× [33] to ~1000× [36] compared to a bulk CMOS process.

The high-temperature junction leakage of an experimental n-type PD SOI-MOSFET is shown in Fig. 3(b), where it is compared against the model provided by the PDK. At relatively low temperature, experimental data are not shown, as they are below the measurement resolution limit. An exponential increase is observed in both the experiment and the model: at 175°C the experimental point is close to the PDK model typical condition, while, when the temperature is further increased, the experimental leakage is higher than the one predicted by the model. As already mentioned, this is due to the fact that the PDK model does not faithfully reproduce

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the experimental junction leakage outside the calibration range: the 300°C leakage is about three times higher than the worst-case PDK model ("fast" corner).

B. SUBTHRESHOLD CHANNEL LEAKAGE

The transistor conduction in subthreshold operation is enabled by the diffusion current due to channel minority carriers, that depends on transistor terminal voltages and on the temperature, according to [37]:

$$I_{\mathrm{DS}} = \mu_0 C_{\mathrm{OX}} \frac{W}{L} (\eta - 1) \cdot V_{\mathrm{T}}^2 \cdot e^{\frac{V_{\mathrm{GS}} - V_{\mathrm{th}}}{\eta V_{\mathrm{T}}}} \cdot \left(1 - e^{\frac{V_{\mathrm{DS}}}{V_{\mathrm{T}}}}\right) \quad (2)$$

where μ_0 is the channel mobility, C_{OX} is the gate oxide capacitance, η is the gate coupling ratio, q is the elementary charge, $V_{\mathrm{T}} = kT/q$ is the thermal voltage and V_{th} is the threshold voltage. The subthreshold channel leakage increases with increasing temperature, mainly due to the first exponential term in (2). The resulting temperature dependence can be observed in Fig. 3(c), where the source current has been measured instead of the drain one to avoid the contribution of the drain-body junction reverse current. Also in this case, the 300°C leakage current is about three times higher than the fast-corner simulation value. However, the subthreshold leakage current temperature sensitivity and the leakage value itself are lower with SOI CMOS technology respect to a bulk CMOS [38], as a result of different effects, including a steep subthreshold slope.

C. SUBTHRESHOLD SWING AND ON/OFF CURRENTS

The subthreshold swing is defined as [38]:

$$\mathrm{SS} = \left\{\frac{d \log_{10} I_{\mathrm{DS}}}{dV_{\mathrm{GS}}}\right\}^{-1} \approx 2.3 \cdot \eta \cdot V_{\mathrm{T}} \quad (3)$$

for a constant V_{DS} and quantifies the transistor capability to reduce the channel current when passing from the on- to the off-state, as V_{GS} is pushed below the threshold voltage. According to (3), the subthreshold swing is proportional to the temperature, as it is well matched by the model data shown in Fig. 3(d). However, measurements show a stronger worsening of the switch-off capability at very high temperatures, leading to an increased subthreshold channel leakage (see again Fig. 3(c)). This result is in line with what has been shown in [36], [39], where the authors demonstrated that at high temperature a rise in the free carrier charge density and a decrease in the surface electric field in weak inversion cause an increase in the effective depletion capacitance, which in turn causes an increase of the gate coupling ratio η.

The drain on-current I_{ON} (i.e. I_{D} when $V_{\mathrm{GS}} = V_{\mathrm{DS}} = V_{\mathrm{DD}}$) is shown in Fig. 3(e). I_{ON} decreases with the temperature, due to electron mobility degradation. The 300°C experimental I_{ON} is less impacted by the high temperature than predicted by the PDK model, resulting also higher than the corresponding fast corner. Note that the drain off-current I_{OFF} is not shown, but it can be easily obtained from the sum of the junction and channel leakage components.

D. THRESHOLD VOLTAGES

The other MOSFET temperature-dependent fundamental parameter is the threshold voltage V_{th}, that for PD SOI CMOS devices can be expressed as [40]:

$$V_{\mathrm{th}} = \phi_{\mathrm{MS}} + 2\phi_{\mathrm{F}} - \frac{Q_{\mathrm{OX}}}{C_{\mathrm{OX}}} - \frac{Q_{\mathrm{DEP}}}{C_{\mathrm{OX}}}, \quad (4)$$

which depends on the poly-semiconductor work function difference (ϕ_{MS}), the Fermi potential (ϕ_{F}), the charge density in the gate oxide (Q_{OX}) and the depletion charge (Q_{DEP}). The main contribution to the V_{th} temperature dependence is due to ϕ_{F}, which can be expressed for a NMOS as:

$$\phi_{\mathrm{F}} = V_{\mathrm{T}} \cdot \ln\left(\frac{N_{\mathrm{A}}}{n_{\mathrm{i}}}\right) \quad (5)$$

with N_{A} being the acceptor doping concentration in the substrate. Note that the temperature affects both terms: V_{T} and the logarithmic term through the intrinsic carrier concentration (see Eq. 1).

Assuming a constant Q_{OX} and neglecting the energy gap temperature variation, through simple analytical manipulations of (4), the temperature sensitivity of the threshold voltage can be obtained, $\frac{\Delta V_{\mathrm{th}}}{\Delta T} \approx -2.5\ \mathrm{mV/°C}$ [36], [40]. The reported value is reasonable within the whole temperature range we have considered, as confirmed by experimental V_{th} in Fig. 3(f) (the V_{th} has been extracted for both experiments and models through the constant off-current method, by assuming $I_{\mathrm{OFF}}/W = 500\ \mathrm{nA/\mu m}$ and $V_{\mathrm{DS}} = 50\ \mathrm{mV}$).

E. ELECTROMIGRATION

Electromigration is another important issue arising from high-temperature operation. Electromigration can be induced by high current densities flowing in metal interconnections, triggered by scattering of the electrons with the metal atoms, leading to serious concerns: from reduced signal integrity, due to increased wire resistance, to circuit failure [41]. In fact, the effective cross-section area of a metal interconnect susceptible to electromigration is reduced due to removed metal atoms. It is evident that a destructive positive feedback can be triggered: the onset of electromigration progressively causes a rise of the interconnect effective resistance, exacerbating self-heating, thus favoring additional electromigration events. The metal-line electromigration issue poses a critical tradeoff between the maximum current density and the maximum operating temperature. Although Aluminum is the most commonly used metal for BEOL interconnection layers, the maximum current density which can be safely accepted at 175°C (automotive standard) is 20 times smaller than the value at 25°C [42]. Different metal composition, possibly with higher temperature

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melting point, can be considered to enhance the resilience to electromigration, such as Tungsten or Copper [33], [43].

At the circuit layout design level, for a given BEOL process, the width of the metal interconnections must be carefully sized. For the considered process, the maximum current density is of ~1000 μA/μm at 85°C, ~500 μA/μm at 100°C, ~200 μA/μm at 125°C and of ~100 μA/μm at 150°C. The available data have been extrapolated at temperature higher than 150°C using a reliable physics-based analytical model [44]:

$$J_{\mathrm{MAX}}^2 = \frac{A_{\mathrm{Fit}}}{T_{\mathrm{SAFE}}} e^{\frac{E_{\mathrm{A}}}{kT}} \quad (6)$$

where E_{A} is the activation energy, T_{SAFE} is the Mean Time To Failure (also indicated with MTTF) and A_{Fit} is a fitting constant. After fitting the analytical model on the available points, we have extracted a maximum current density slightly lower than 10 μA/μm at 300°C. This consideration practically puts a limit to the type of circuits that can be designed at 300°C: while it is reasonable to design low-power IC sensors and subthreshold digital circuits for industrial, space, or oil and gas applications, it is clear that high performance digital circuits are possible only in CMOS technologies with electromigration-resistant BEOL materials.

F. OTHER TEMPERATURE-RELATED EFFECTS

Other IC failure mechanisms happen at high temperatures. The chip lifetime is reduced by the degradation and breakdown of the oxides, beyond the already mentioned electromigration of metal lines [33]. During standard reliability tests for the qualification of a process technology or of an IC, the circuit under test is stressed at temperatures far above the standard operating conditions, in order to activate accelerated aging effects to estimate the MTTF in a time that is orders of magnitude shorter than the estimated MTTF itself. It is evident that in harsh environments the normal operating condition is represented by high temperature, which inevitably limits the effective IC lifetime.

Another example of a temperature-dependent failure mechanism for silicon ICs devices is the Negative Bias Temperature Instability (NBTI) [3]. It is especially critical for PMOS devices, as it occurs when a negative voltage is applied to the gate: during high temperature operations, charge trapping phenomena at the channel/gate oxide interface take place, resulting in a threshold voltage variation and in an increase of the leakage currents.

III. HIGH TEMPERATURE EFFECTS ON DEVICE PERFORMANCE

In this section we discuss the high-temperature performance degradation of representative device cases, including active devices such as MOSFETs and BJTs, and passive ones such as polysilicon and diffusion resistors, in an extended range up to 300°C, in order to analyze how devices behave above the qualification temperature limit.

A. MOSFETS

In order to analyze the impact of high temperature on the behavior of different types of MOSFETs, we show in Fig. 4 the experimental characteristics at 300°C of NMOS and PMOS with nominal supply voltage of 1.8 V and of 5 V (both available in the XT018 process). 1.8-V NMOS and PMOS transfer characteristics (for $|V_{\mathrm{DS}}| = 50$ mV and 1.8 V) are in Fig. 4(a) and (b), respectively, while output characteristics are reported in Fig. 4(c) (for $|V_{\mathrm{GS}}| = 1.8$ V). We also show characteristics from the PDK model for comparison. In strong inversion, the performance of experimental devices in both linear and saturation regions are close to the typical simulation corners, with a higher on-current with respect to typical-condition simulation (+25%) for the NMOS, as discussed in Section II.C, partially motivated by the lower value of the experimental V_{th} (see again Fig. 3(f)). The experimental vs. simulated characteristics mismatch is even higher for the PMOS I_{ON} (+70%), meaning that the NMOS/PMOS I_{ON} unbalance at high temperatures is reduced with respect to the one at room temperature. Similar experiments/simulations are reported for 5-V NMOS and PMOS transistors in Fig. 4(d-f). In this case, the experimental I_{ON} is closer to the one predicted by the PDK (typical condition), with the experimental data / model mismatch of $+(-)$ 10% for NMOS (PMOS). However, when transistors are operated in weak inversion, a substantial difference between measured and simulated drain currents is observed (over a decade increase at $V_{\mathrm{GS}} = 0$ V), mainly due to the higher-than-predicted junction leakage. The NMOS transfer-characteristics have been explored also for a slightly negative gate voltage (positive for PMOS): beyond the increased leakage, transistor measurements show an almost ambipolar behavior at 300°C, which is particularly marked for the two PMOS transistors. This behavior has been attributed to the gate induced drain leakage (GIDL) [45], as further discussed in Section IV.

B. BJTS

Two vertical BJT transistors (both PNP) with nominal supply voltage of 1.8 V and 5 V have been characterized up to 300°C. As expected, the input- and transfer-characteristics ($I_{\mathrm{B}} - V_{\mathrm{BE}}$ and $I_{\mathrm{C}} - V_{\mathrm{BE}}$) represented in Fig. 5(a) and (b) for a 1.8-V PNP, and in Fig. 5(d) and (e) for a 5-V PNP, show a close match of the measurements to the PDK model simulations in the nominal temperature range. The only exception is the collector-base reverse saturation current of the PDK model at 175°C, which predicts a sign change in the base current for low emitter-to-base voltage levels, which is not observed in experiments on devices at this temperature. Interestingly, at 300°C the good match of experiments to the PDK models seems confirmed only for collector current levels above

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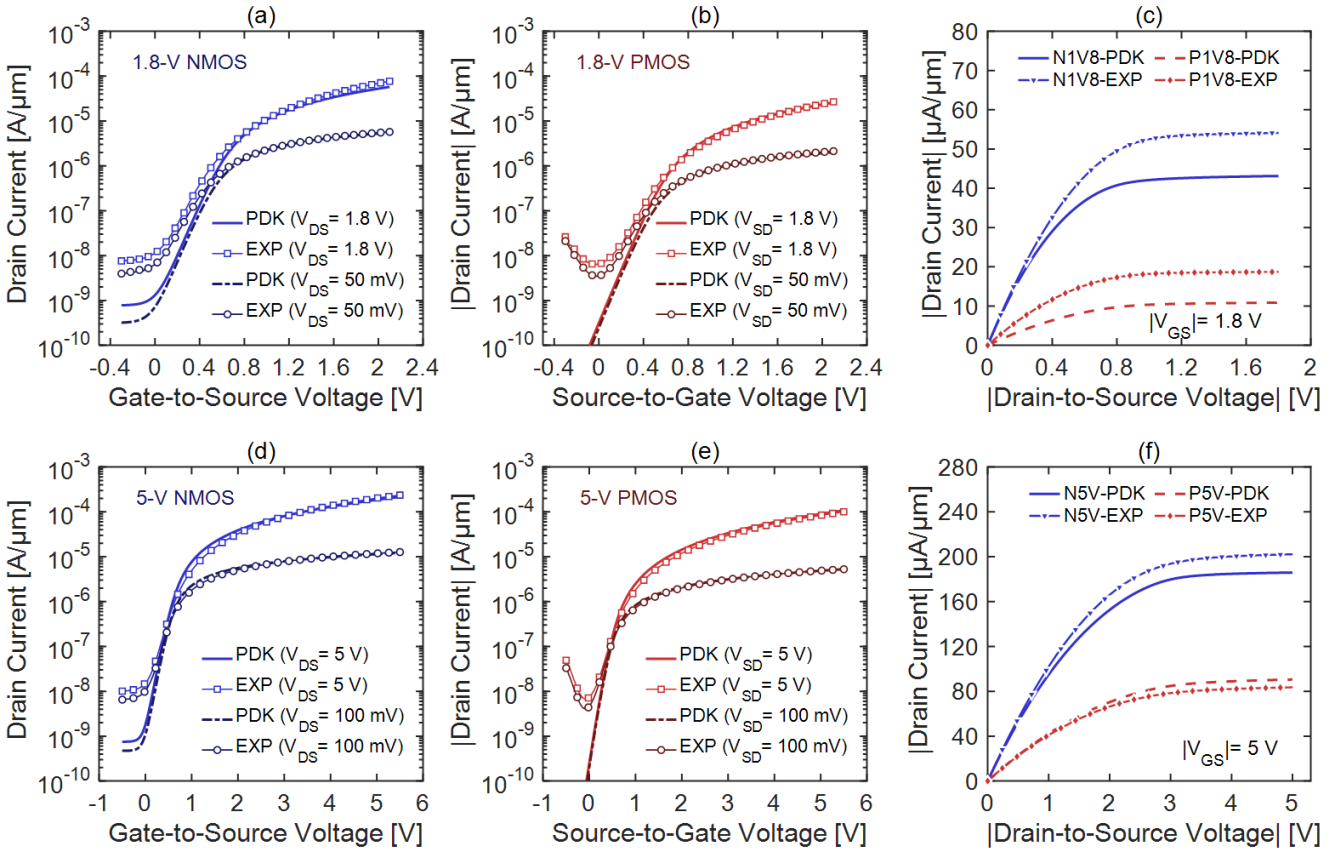

FIGURE 4. Experimental and simulated (PDK model) 1.8-V and 5-V MOSFET I-V characteristics at 300°C: 1.8-V NMOS (a) and PMOS (b) transfer-characteristics at $|V_{DS}|$ = 50 mV and 1.8 V, (c) 1.8-V NMOS and PMOS output characteristics at $|V_{GS}|$ = 1.8 V; 5-V NMOS (d) and PMOS (e) transfer-characteristics at $|V_{DS}|$ = 100 mV and 5 V, (f) 5-V NMOS and PMOS output characteristics at $|V_{GS}|$ = 5 V.

tens of μA. In fact, a noticeable mismatch is observed at lower current levels, because of the PDK reverse saturation current artifacts which become prevailing.

Finally, in Fig. 5(c) and Fig. 5(f), the forward voltage of the emitter-to-base junction (blue) and the DC current gain $\beta_F = \frac{I_C}{I_B}$ (red) are extracted at constant $I_B = 10$ μA. A reasonable experiment/model match is found up to very high temperatures, although at 300°C the β_F gain extracted from simulations appears to be much higher than the actually measured one; this is due to the fact that the simulated collector current is dominated by the huge reverse-current leakage (see flat green curves in Fig. 5(b) and Fig. 5(e)), and it is not really linked to the injected I_B.

C. RESISTORS

Both n-type polysilicon and diffusion resistors are available in the investigated CMOS technology. Two resistor serpentines (one for each resistor implementation) have been fabricated and characterized from −40°C to 300°C temperature range. The resistors have been sized to get the same nominal resistance value at room temperature (W/L = 5.23 μm / 500 nm and 4.82 μm / 420 nm for the polysilicon and diffusion resistors, respectively). Experimental and simulated resistance values are reported in Fig. 6. As expected, PDK models are well matched to experimental points up to a temperature of 175°C. Both resistance types show a strong temperature sensitivity, with an almost constant sensitivity of 114 Ω/°C for the diffusion resistor, and a negative derivative with respect to the temperature for the polysilicon resistance (an average $\Delta R/\Delta T$ of −195 Ω/°C is observed in the range between 25°C and 175°C). At temperatures above 175°C, there is still a reasonable match between the model and the experimental data for the diffusion resistor, with the exception of the point at 300°C (model +6.7% with respect to experiments). On the other hand, the high-temperature mismatch is larger for the polysilicon case, where at a temperature higher than 175°C the experimental resistance trend (the resistance continues to decrease with increasing temperature) is in the opposite direction compared to the one predicted by the PDK model (model +103% with respect to experiments at 300°C).

IV. CMOS DESIGN COMPENSATION METHODS

In high temperature environments, the CMOS I_{ON}/I_{OFF} current ratio worsening is mainly due to the exponential increase of temperature-dependent leakage sources contributing to I_{OFF}, while the I_{ON} reduction is a smaller effect. By recalling for instance the experimental 1.8-V NMOS transistor considered in Section II (Fig. 3), the I_{ON}/I_{OFF} ratio is ~6×10^5 at 175°C. However, as the

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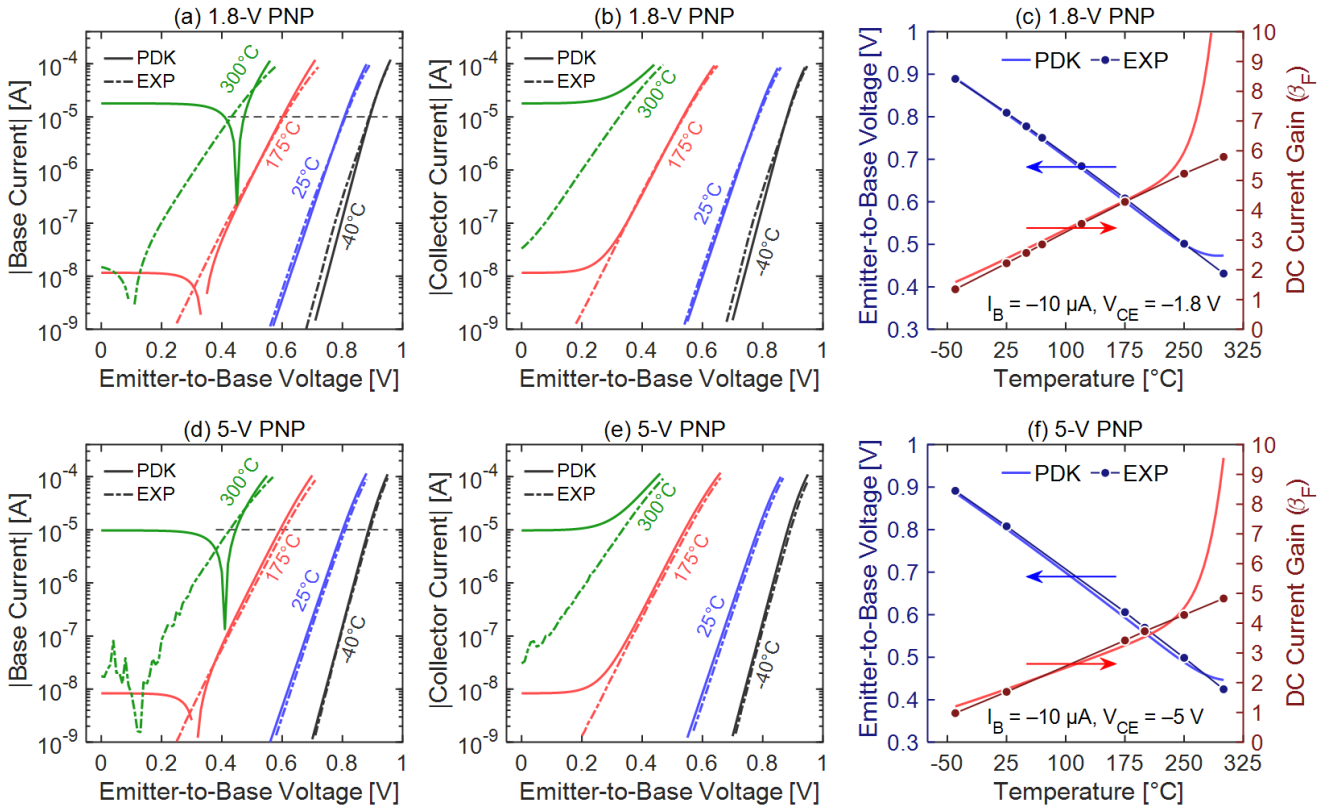

FIGURE 5. **Experimental and simulated (PDK model) 1.8-V and 5-V PNP transistors: (a) $I_B - V_{BE}$ input- and (b) $I_C - V_{BE}$ transfer-characteristics and (c) emitter-to-base junction forward voltage and DC current gain for 1.8-V PNP; (d) $I_B - V_{BE}$ input- and (e) $I_C - V_{BE}$ transfer-characteristics and (f) emitter-to-base junction forward voltage and DC current gain for 5-V PNP.**

temperature rises to 300°C, this ratio decreases by two orders of magnitude ($I_{ON}/I_{OFF} \approx 6{\times}10^3$). It is thus clear that a high-temperature resilient CMOS IC design must include solutions to minimize the impact of subthreshold channel and pn junction reverse leakage currents. These two effects can be addressed by relying on dedicated compensation techniques [45], which are normally investigated by considering pass-transistor (PT) configurations as a simple test vehicle.

On one side, the subthreshold channel leakage depends exponentially on the $V_{GS} - V_{th}$ voltage difference: a negative

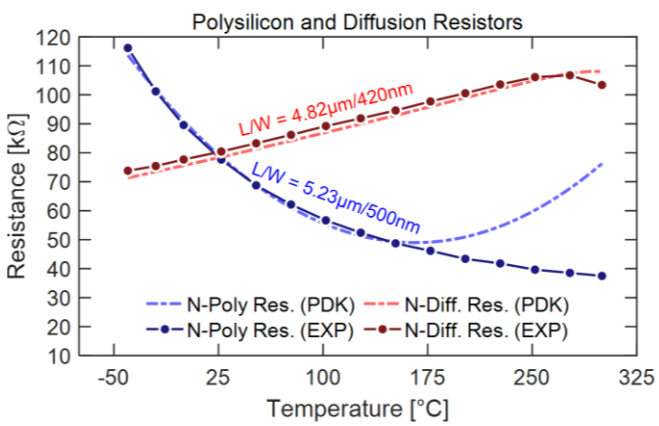

FIGURE 6. **Experimental and simulated resistance of n-type polysilicon (blue) and diffusion (red) resistor serpentines.**

V_{GS} for an NMOS, as well as a positive V_{GS} for a PMOS, leads to a drastically reduced channel leakage. This solution is known as clock boosting. Another option is to minimize the V_{DS} voltages, for instance by relying on transistor stacking, but this solution is not as effective as the clock boosting technique. Fig. 7(a) depicts a dual symmetric charge pump, based on two bootstrap capacitors, which implements the clock boosting technique. By pre-charging the two capacitors C_1 and C_2 with a V_{REF} voltage (with opposite polarity), the positive and negative pre-charged voltages are added and subtracted to V_{DD} and to GND, respectively, to get the boosted logic levels. The high level of *clk_boost* is $V_{DD} + V_{REF}$ (by means of C_1 connected in series to V_{DD}), while its low level is $-V_{REF}$, obtained by means of C_2 connected in series to ground (with flipped terminals with respect to the pre-charge phase).

On the other side, the pn junction reverse current can be reduced by short-circuiting either the drain-body or the source-body terminals, but this is not suitable for the twin-well CMOS processes and alters the symmetry of the PT: an asymmetric NMOS (or PMOS) PT can only block positive (negative) V_{DS}, as in the opposite V_{DS} condition the forward biased substrate-drain diode would turn on. Leakage compensation techniques based on dummy transistors are effective countermeasures to the source-body and the drain-body junction reverse currents in a PT: two nominally identical transistors (dummies) of the

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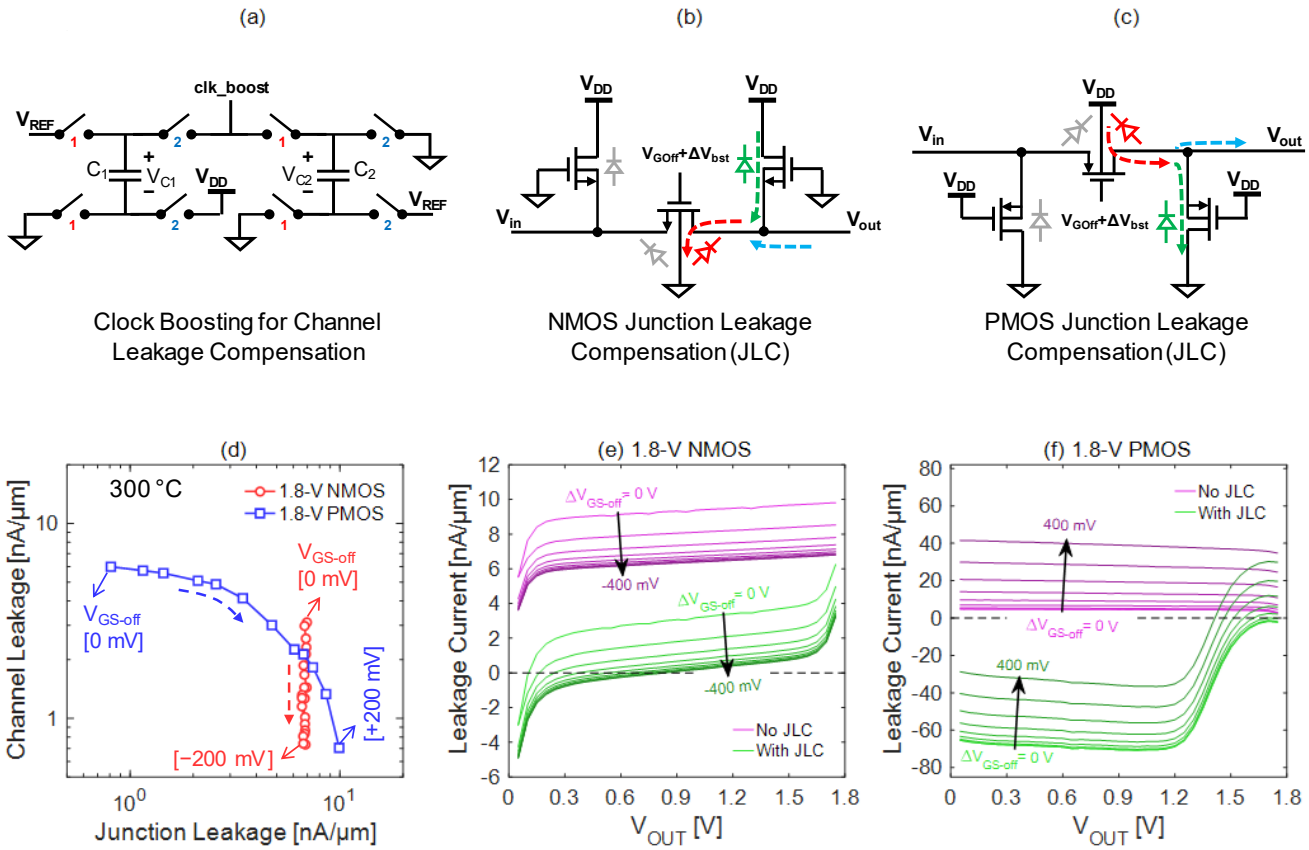

FIGURE 7. **Schematic of: (a) clock boosting circuit and of a NMOS (b) and PMOS (c) junction leakage dummy compensation techniques. (d) Impact of clock boosting on leakage currents in 1.8-V NMOS and PMOS devices at 300°C, combined impact of V_{GS-off} boosting and dummy compensation on a NMOS (e) and on a PMOS (f) leakage currents.**

same type of the PT, are connected between V_{DD} (NMOS) or GND (PMOS) to the drain and to the source terminals of the PT. For each dummy, the gate is biased to keep the device in the off state, and the body is short-circuited to the source. This configuration, depicted in Fig. 7(b) and Fig. 7(c) for a n-type and a p-type case, respectively, may enable the injection into the source and drain of the PT of two currents with values very similar to the one of its reverse biased source-body and drain-body junctions. Although the adopted solution is not beneficial from the point of view of power consumption (as opposite to the gate voltage boosting technique effectiveness with respect to the subthreshold leakage), it leads to the reduction of the off-state junction leakage fraction which is shown to neighboring circuits connected to the source and drain terminals. Furthermore, the adopted solution can be exploited also for standard CMOS logic gates (with pull-up and pull-down networks) and for more complex circuits.

The use of the proposed techniques for reducing the leakage of the XFAB MOSFETs has been investigated, and we have observed a different behavior for NMOS and PMOS devices. First, we have considered the impact of the clock boosting technique from experimental data at 300°C in Fig.7(d), where junction and channel leakage components have been plotted in the x- and y-axis, respectively, for both NMOS and PMOS biased at different off-state gate voltages (with a $|\Delta V_{GS-off}|$ boost from 0 up to 200 mV). In principle this technique should only be effective to scale the channel leakage, with no impact on the junction leakage. However, we have verified that this is true only for the investigated NMOS: looking at the NMOS trend, the V_{GS-off} reduction is totally beneficial, leading to a reduction of channel leakage by a factor 7, and with practically no impact on the junction leakage. Instead, the PMOS trend is quite different: although clock boosting brings a similar effect on the channel leakage (tenfold reduction), this benefit is overcompensated by a big variation of the junction leakage in the opposite direction. This different trend was also suggested by the $I_D - V_{GS}$ characteristics in Fig. 4(a) and (b) for 1.8-V MOSFETs (and (d) and (e) for 5-V MOSFETs), with PMOS transistors showing a much stronger degree of ambipolarity.

To provide the full picture on the clock boosting and dummy compensation techniques, when exploited together, the fully compensated PT configurations shown in Fig. 7(b) and Fig. 7(c) have been characterized, with the corresponding experimental data at 300°C shown in Fig. 7(e) and Fig. 7(f). In the NMOS, both the subthreshold and the reverse junction leakage currents are minimized by means of clock boosting and dummy transistor techniques, e.g. with ~6 nA/µm junction leakage compensated by the dummy transistor, and ~2 nA/µm channel leakage compensated by the clock boosting with $V_{GS-off} = -200$ mV. Unfortunately, due to

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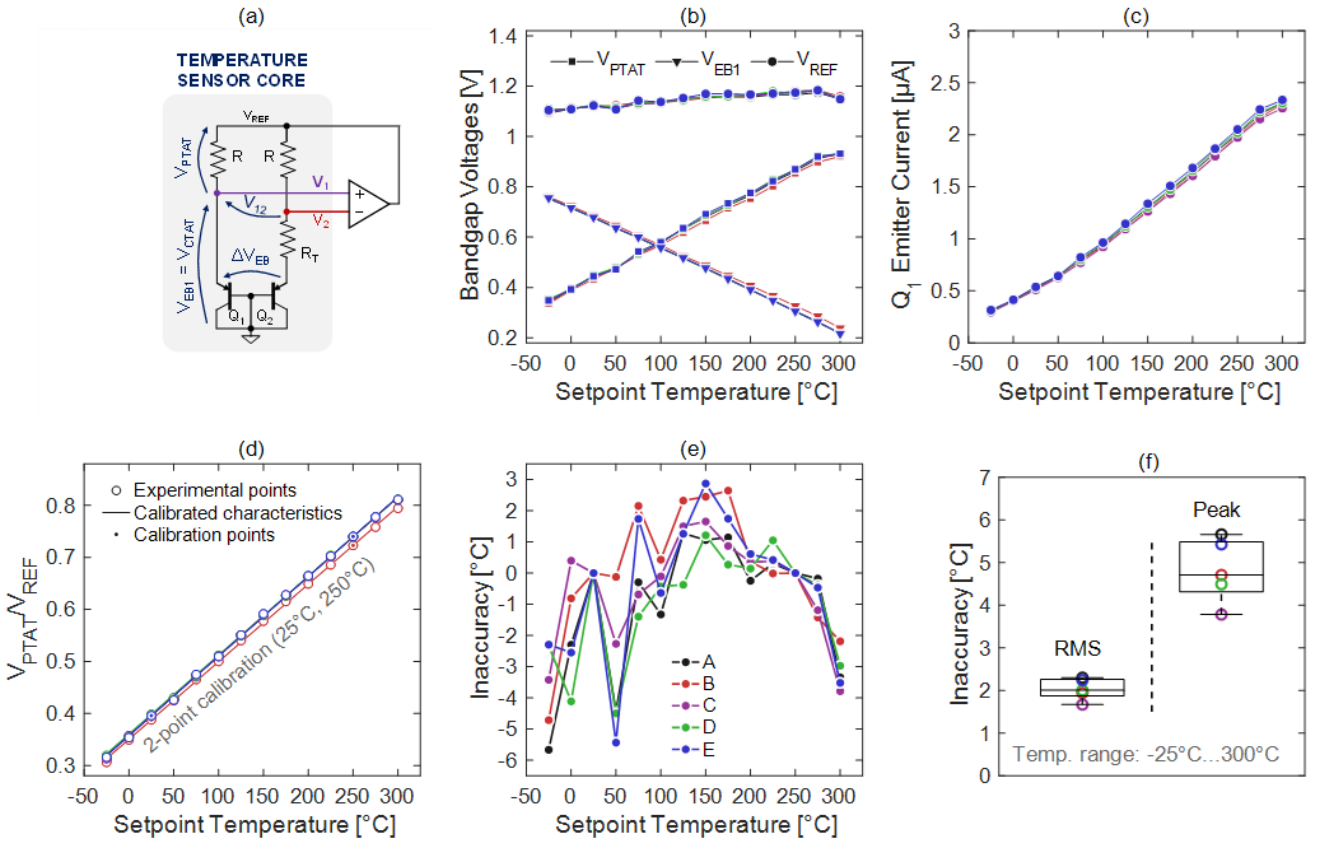

FIGURE 8. **(a) Schematic of a bandgap reference example structure. Simulations and measurements up to 300°C of the bandgap voltage reference temperature sensor core: b) CPTAT (V_{EB1}) and PTAT (ΔV_{EB}) voltage components, and the bandgap V_{REF} reference voltage; (c) Q_1 emitter current (I_{E1}); (d) temperature sensor core output V_{PTAT} measured with reference to V_{REF} scale; (e) inaccuracy extracted for each temperature point after two points calibration; (f) RMS and peak inaccuracy (5 samples).**

GIDL induced ambipolar behavior of the PMOS transistor, the investigated compensation techniques are not as effective as in the NMOS case. In fact, when not considering the junction leakage compensation dummies (Fig.7(f), no-JLC case) the ΔV_{GS-off} modulation does not provide any appreciable improvement up to 200 mV (due to junction leakage degradation totally covering the channel leakage improvement, see again Fig.7(d)), while it becomes detrimental for higher values of V_{GS-off}. When implementing the JLC, there is a huge overcompensation triggered by the ambipolar leakage of the dummy transistor. Although a knife-edge balance of the PT and dummy PMOS devices ambipolar contributions can be found (e.g. with JLC and $\Delta V_{GS-off} \approx 500$ mV), we believe that the intrinsic PMOS PT must be preferred over this delicate balance solution, also considering that a so high ΔV_{GS-off} cannot be accepted, as it would expose the transistors to biasing conditions beyond the safe voltage swing.

V. HIGH-TEMPERATURE CIRCUIT DESIGN

Designing high-temperature integrated circuits presents different obstacles depending on the specific circuit. Digital circuits are less susceptible to performance degradation because of their inherent resilience to disturbances and changes in device parameters. In terms of static power consumption, leakage currents exponentially increase with temperature. The adoption of SOI processes and special layout geometries [24] can only mitigate this issue, and this penalty must be considered at the system level. The delays of logic gates and bistable multivibrators have a temperature dependence that in general is a function of transistors' bias. There is a specific supply voltage at which the frequency of CMOS digital circuits remains constant regardless of the temperature [46]. More in general, the digital design flow is not altered if a proper characterization and modeling of the logic standard cells is provided at high temperatures. This may result in decreased performance in power consumption without requiring any topological changes.

The situation is different when it comes to the design of analog circuits and memory cells suitable for high temperature environments. For instance, the design of a SRAM cell capable of working up to 300°C needs several circuit modifications compared to the standard circuit [31]. In addition to the choice of the optimum supply voltage to improve resiliency against temperature, particular attention needs to be put on the impact of leakage current. The use of body bias and replica structures for offset compensation are perfect examples of ad-hoc techniques to counteract

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temperature effects. Additionally, the use of the leakage compensation methods described in the previous section can be adopted to improve resilience with respect to temperature.

Stable performance is crucial also in analog circuits such as instrumentation amplifiers. In this case, the choice of the architecture is crucial to guarantee at the same time gain accuracy, high bandwidth, and Common Mode Rejection Ratio (CMRR) over a wide temperature range. The indirect current feedback topology ensures high accuracy by relying only on resistor ratios and OTA transconductance matching [26]. Considering that the ratio of homogenous quantities can be considered temperature independent to a first order approximation, and that the mismatch of the main transistor parameters does not change significantly over temperature [47], gain accuracy is guaranteed over a wide temperature range. CMRR is ensured as well, since it mainly depends on mismatch parameters. The temperature dependence of the amplifier bandwidth can be managed by employing constant-gm biasing technique instead of Zero Temperature Coefficient (ZTC) biasing, as demonstrated in [29].

Low Drop-Out (LDO) regulators exhibit temperature sensitivity of their key parameters (line regulation, load regulation, and power supply rejection ratio). This behavior is systematically studied and characterized in reference [27]. Designing operational amplifiers with high DC gain across the whole temperature range is beneficial for the resilience of low-dropout regulators. To achieve high and consistent DC gain, it is recommended to use cascode structures and ZTC bias points, and to implement leakage compensations through the usage of dummy transistors. Similar to LDOs, it is essential also for bandgap voltage reference circuits to include high-gain operational amplifiers to ensure precise output voltage [28], [29]. Using two resistors with opposite temperature coefficients in the bias circuit allows a more constant bias current for reliable operations of the op-amp. Effective temperature compensation is ensured by the bipolar transistors, which exhibit a linear relationship between emitter-to-base voltage even at high temperatures, as shown in Section III.B. It is possible to resort to trimmable resistors in the bandgap core as tuning knobs to further adjust the temperature sensitivity of the output voltage [29].

To provide an example of high-temperature circuit, we designed a temperature sensor based on the bandgap voltage core [48] depicted in Fig. 8(a), experimentally validated in a range from −25°C to 300°C. Due to poor PDK device model predictability at so high temperature levels, it is essential to compare experimental data with circuit simulations. Bipolar transistors Q_1 and Q_2 have been implemented with parallel PNP structures (2 for Q_1 and 16 for Q_2), such that the $\Delta V_{\mathrm{EB}} = V_{\mathrm{EB1}} - V_{\mathrm{EB2}}$, under the condition of the same emitter current on Q_1 and Q_2, represents the Proportional to Absolute Temperature (PTAT) component of the sensor. This PTAT voltage corresponds to the voltage drop on the test resistor R_{T}, while enforcing $V_1 = V_2$ and $I_{\mathrm{E1}} = I_{\mathrm{E2}}$. The condition $V_1 = V_2$ is normally achieved by exploiting the virtual short-circuit enforced by the Operational Amplifier buffer, while $I_{\mathrm{E1}} = I_{\mathrm{E2}}$ is the results of $V_1 = V_2$ together with the use of the same resistance value for the polysilicon resistors connecting V_1 and V_2 to V_{REF}. V_{EB1} of transistor Q_1, instead, represents the Complementary To Absolute Temperature (CTAT) component. By means of a simple circuit topology inspection, it can be seen that the bandgap reference voltage V_{REF} is simply the sum of the $V_{\mathrm{CTAT}} = V_{\mathrm{EB1}}$ voltage and of the "$V_{\mathrm{REF}} - V_1$" voltage difference (defined as V_{PTAT}, as it can be calculated by the product of ΔV_{EB} with the R/R_{T} term). Fig. 8(b) shows the measured V_{PTAT}, V_{CTAT} and V_{REF} over the full temperature range, for 5 samples, while the corresponding Q_1 emitter currents (I_{E1}) are in Fig. 8(c). At the highest temperature, both V_{PTAT} and V_{CTAT} lose their theoretical linearity. Thus, also the bandgap reference voltage curves show an appreciable reduction at 300°C.

By assuming to perform a digital conversion of the V_{PTAT} voltage difference by using V_{REF} as the full-scale input of the analog-to-digital converter, the implemented temperature sensor core shows a quite linear behavior. This is shown in Fig. 8(d), where each temperature sensor core has been calibrated with a two-point approach at 25°C and 250°C. The extracted inaccuracy for each temperature point is reported in Fig.8(e), where each color refers to a different die, while in Fig.8(f) we have extracted the RMS (over the full temperature range, from −25°C to 300°C) and peak inaccuracy for each sample. Considering the broad temperature range, the measured temperature sensor shows excellent linearity, with a typical RMS error and maximum absolute error inaccuracy of 2°C and 4.8°C, respectively.

VI. CONCLUSION

This paper illustrates the complexities involved in the design of CMOS integrated circuits suitable for high-temperature operations. We have discussed important temperature-dependent electrical parameters and physical phenomena, together with proper design techniques for temperature effects compensation, in order to achieve a successful CMOS design operating up to 300°C.

High-temperature measurements have shown significant differences with respect to the PDK models: main mismatches were found for leakage currents of CMOS devices (in particular for PMOS cases, with more than two order of magnitude of mismatch), while the ON-current difference was quantified in +25% for 1.8-V NMOS and in +70% for 1.8-V PMOS (at 300°C). Differences have been also evidenced for BJTs and passive resistors. The available PDK models have been calibrated for temperatures well below the ones we have reached during the characterization, and this explains the discrepancy between experiments and predicted results. Temperature-related effects have been compensated with clock boosting techniques and junction leakage dummy circuits, with opposite results for NMOS and PMOS configurations.

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Furthermore, we have shown that a temperature sensor core based on a bandgap voltage reference can be designed so that it exhibits a significant level of linearity across the temperature range from -25°C to 300°C (after a 2-point calibration). The sensor shows a typical inaccuracy with a standard root mean square (RMS) value of 2°C and a maximum absolute value of 4.8°C.

This discussion on analog and mixed-signal integrated electronic design for high temperature applications shows that reliable CMOS design for extreme temperature environments is feasible, considering temperature-dependent effects and employing robust circuit techniques for effective leakage compensation. This achievement holds the potential to promote the use of cost-effective silicon-based processes in several unconventional yet important applications across multiple fields, encompassing industrial, mobility, and space applications.

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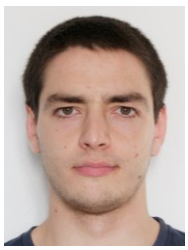

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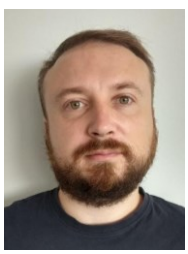

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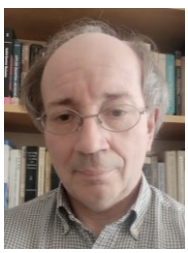

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