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An Energy-based Analysis of High Voltage Resonant-based Pulsed Low Power Converter for Water Treatment Application

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ABSTRACT Usage of ozone is an effective way of treating wastewater, and the silent discharge technique is one of the most efficient and reliable methods for ozone production. Ozone is generated in a Dielectric Barrier Discharge (DBD) chamber through the silent discharge technique and is powered by a high voltage (in the range of −2.5 kV to −5 kV) pulse generator. The pulse generator has two conversion stages, i.e., a high-frequency pre-processing stage and a pulse-frequency post-processing stage. In a high voltage pulse generator, a significant amount of energy from the input is utilised by the converter's parasitic capacitance and leakage inductance, which reduces the energy delivered to the load for each pulse cycle. This paper proposes an energy-based analysis exploring the potential usage of the flyback converter-based high voltage pulse generator for an application with power requirements under 150W, and water treatment is such an application. An energy-based approach is appropriate to describe the behaviour of the pulse generator in terms of circulating energy and energy exchanges in each stage and energy exchanges between the two stages (i.e. pre and post-processing stages). The proposed analysis is used to derive the essential parameters of the pulse generator and thereby arrive at an appropriate control scheme for the pre and post-processing stages. The proposed energy-based analysis and the derived analytical expressions of the high voltage pulse generator are verified experimentally for a pulsed output voltage of −5 kV having a Pulse Repetitive Rate (PRR) of 1000 Hz and pulse width of 15 µs fed from a 12 V battery source.

INDEX TERMS energy-based analysis, flyback converter, capacitive load, programmable pulsed high voltage, pulse power, resonant converter

NOMENCLATURE

ε	Permittivity of the dielectric medium
A	Area of the DBD chamber
C_o, R_o	Output load capacitance and resistance
V_{dc}	Input voltage of HV pulse generator
L_{lkf}, L_{mf}	Leakage and magnetising inductance of transformer T_1 referred to primary
v_l, i_l	Voltage and current through L_{mf} of T_1 referred to primary
n_f	Turns ratio of HV flyback transformer T_1
C_{sw}	Switch S_1 and diode D_1 node capacitance
C_d	Diode D_1 node capacitance
C_w	Winding capacitance of HV flyback transformer T_1 referred to secondary
C_{link}	DC link capacitance
v_{link}, i_{link}	Voltage and current through the DC link capacitance
$I_{pk,f}$	Peak current through L_{mf}
v_{S1}	Drain to source voltage across switch S_1
C_{eff}	Equivalent parasitic capacitance of HV flyback converter
V_{dcl}	Maximum DC link capacitor voltage
$T_{chrg,f}$	Charging time of the DC link capacitor to charge from V'_{dcl} to V_{dcl}
L_2, C_1	Series resonant inductance and capacitance of post-PS
L_{mr}, C_{wd}	Magnetising inductance and winding capacitance of T_2 referred to primary
L_{lkr}	Leakage inductance of resonant transformer T_2 referred to primary

n_r	Turns ratio of resonant transformer T_2
v_{C_1}	Voltage across the resonant capacitor C_1
$V_{C_{1,max}}$	Maximum voltage across C_1
i_{L_2}	Current through the resonant inductor
v_o, i_o	Pulsed output voltage and current through the load
$V_{o,max}$	Peak voltage across the pulsed output
$E_{L_{mf}}$	Energy stored by the magnetising inductance of T_1 during switch S_1 turn-on
$E_{C_{eff}}$	Energy utilised by the parasitic capacitance of pre-PS
P_{pk}	Peak power rating of the pre-PS

I. INTRODUCTION

WATER is one of the basic resources of all living organisms on this planet. According to the UN, 2.2 billion people lack safely managed drinking water in 2022, and 2.4 billion people live in water-stressed countries in 2020 [1]. Water treatment (includes chemical, physical, biological, and electrical treatment [2]–[4]) is the process of improving water quality by removing the microbial pathogens present in the wastewater. Treating water for end-use purposes like drinking, industrial applications, medical applications, etc., is essential due to drinking water shortages (0.4 % of water on this planet) and the increasing needs of the growing population. In the electrical treatment of water, ozonization is preferred over other water treatment technologies due to its effectiveness and speed in treating water. Ozone water treatment does not add chemicals to water; hence, it is free of chemicals and pollutants [5]. A comparative study of the techniques available for removing contaminants from water shows that the ozonization technique removes 95 % of toxic and harmful elements from the wastewater [6]. The quantity of ozone required to remove waste effectively depends on the type of contaminated waste.

In the literature, various ozonization techniques, including silent discharge, corona discharge, and pulse streamer discharge, are explored in this paper [7]–[10]. All three methods utilize a DBD chamber for ozone production. Notably, the silent discharge technique stands out by incorporating a dielectric layer in its setup. This dielectric layer enhances the charge storage capacity of the DBD chamber, allowing it to withstand a higher maximum voltage for a chamber of the same size, ultimately leading to increased ozone production and efficiency compared to the other techniques. Conversely, in the silent discharge technique, the inception voltage required for a given ozone concentration is lower. This characteristic results in reduced power and voltage demands from the pulse generator [11]. In terms of efficiency, for a constant applied voltage and DBD chamber size, silent discharge achieves close to 95 % ozone production efficiency, a notable contrast to the 40 % efficiency observed in the corona and pulse streamer discharge. Another advantage of the silent discharge technique lies in the wider reaction chamber, facilitating a discharge that occurs over a broader area. This design eliminates the need for an additional cooling system [6]. In summary, the silent discharge contributes to its superior performance in terms of ozone production efficiency, stronger ionisation, reduced power consumption and no cooling system requirement compared to other ozonization techniques.

The silent discharge technique for ozonization requires a Dielectric Barrier Discharge (DBD) chamber, constituting two metal electrodes separated by air and a dielectric layer. When oxygen is passed into the chamber, and High Voltage (HV) is applied across the two ends of the metal electrodes, it leads to the breaking down of oxygen atoms, and ozone is generated at the output [12]. The high voltage applied across the two electrodes can either be pulsed with a defined Pulse Repetitive Rate (PRR) and pulse width or sinusoidally non-pulsed with a defined frequency. In literature, a comparative analysis has been done between the above two techniques, and the use of short (pulse width less than 15 µs) HV pulses features a higher amount of ozone concentration and increased ozone production efficiency [13]. Both the metal plates in the DBD chamber resemble a capacitive load and demand a programmable pulsed HV (in the range of −2.5 kV to −5 kV) for ozone production. So, a suitable HV pulse power converter topology needs to be identified for the silent discharge-based ozone generator, which features lightweight, compact, programmable, and controllable, and the motivation for the same is given in the next section. In this work, the input to the HV pulse power converter is fed from a battery with an input voltage of 12 V, which gives an added advantage of portability.

II. MOTIVATION AND OBJECTIVE

HV pulse power for various applications is still evolving in literature. It finds application in water and air treatment, plasma generators, radar power supplies, and microwave tubes. Table 1 shows several HV pulse power applications, which vary in peak voltage and power requirement. One such application is the water treatment (by the usage of ozone) where typically the power is of the order of 10 watts and peak output voltage varies from −2.5 kV to −5 kV. An energy-based analysis is presented in this paper exploring the potential usage of the flyback converter-based pulse generator for an application with power requirements under 150 W. Notably, water treatment is one such pulse power application that falls within this power range. Hence, in this paper, the analysis is being taken for a water treatment application. The process of water treatment using pulsed power technology has the advantage of fast-rising power at the load end, making the treatment faster and more efficient.

TABLE 1. High voltage pulsed load applications

Application	Power	Peak Output Voltage
Water Treatment [14]	10 W	10 kV
Plasma Generator [15]	600 W	8 kV
Radar Power Supply [16]	6 kW	1 kV
Microwave Tube Applications [17]	25 kW	−2.5 kV

A typical HV pulse generator block diagram is proposed in Fig. 1. The power processing unit consists of two stages; the first stage is a high-frequency pre-processing stage (pre-PS), where the DC input voltage from the battery is stepped up to a voltage required by the second stage. The second stage is a pulse frequency post-processing stage (post-PS), where the output of the post-PS is converted into pulsed HV with a specific PRR, pulse width and pulse rise time [13].

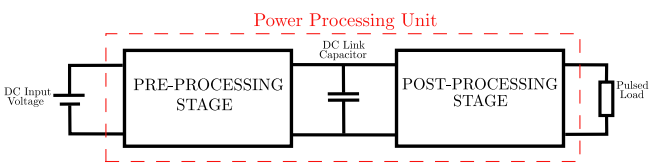


FIGURE 1. A block diagram of a typical high voltage pulse generator

Converter topologies for pre-PS and post-PS are discussed in the literature [17]–[24]. A few prominent converter topologies for the pre-PS are the interleaved boost with voltage multiplier topology, the boost flyback converter topology, high gain DC-DC step-up topology, boost chopper fed DC-DC topology and boost full bridge type topology; and the Marx generator circuit, pulse frequency modulated full bridge and the usage of an HV switch for obtaining a pulsed high voltage are used for the post-PS.

Topologies investigated for pre-PS features largely valued capacitors for reducing ripple, which result in a higher amount of current drawn from the source and are capable of reasonably low current production in the output. Control becomes complex due to the converter configuration [25]–[28]. The topologies investigated for post-PS feature a lower PRR (less than 500 Hz) due to higher charging time constraints. The achievable efficiency may be affected due to the higher resistance (typically in hundreds of ohms), inbuilt high-valued snubbers and minimum pulse width constraint [29]. In addition, increased overshoots and undershoots during transients [30] may result in a miscalculated amount of ozone production in the output. Most of the topologies in literature for the HV pulse generator are suited for high pulse power applications in the range of 1 kW to 5 kW. However, converter topologies for low-pulse power applications like water treatment (power in the order of tens of watts) are still evolving in the literature [31].

HV flyback converter for the pre-PS and series LLC resonant-based post-PS is an attractive solution for HV low pulse power applications. The flyback converter features a compact structure with a lesser component count, galvanic isolation and is efficient for low-power applications (less than 150 W) [32]. The series LLC resonant-based post-PS features high efficiency, high PRR and pulse width as required by the pulse power application. No overshoots/undershoots are observed, making the pre-PS free from the usage of lossy snubbers. Table 2 and Table 3 give a comparison between the topologies present in literature for pre-PS and post-PS, respectively, with that of the proposed pulse generator for a low-power application.

Due to larger secondary turns and winding arrangement in the HV flyback transformer, the turn-turn winding capacitance and the leakage inductance increase. The parasitic capacitance (winding capacitance of the HV flyback transformer and the switch node capacitances) affects the converter performance for a capacitive load. In HV low-power applications, neglecting the parasitic capacitances in the initial design stage will either lead to not attaining the desired output voltage in desired charging cycles or not attaining the output voltage (parasitic capacitance limits the output voltage) with continuous charging cycles. This is due to a significant amount of energy being drawn by the parasitic capacitance from magnetising inductance, which reduces the energy delivered to the load per cycle. To address the above, an energy-based analysis for an HV pulse generator with an appropriate control is proposed in this work. The parasitic capacitance in the HV flyback converter results in additional resonant intervals with respect to the ideal flyback converter intervals, where energy exchange between the parasitic capacitance and the magnetising inductance occurs. In the series LLC resonant converter, the energy flow from the DC link capacitor to the output load and the change in energy discharged by the resonating capacitor during pulsing is essential for designing the parameters of the post-PS and arriving at a proper control strategy. The circuit-based analysis of both flyback-based pre-PS and resonant-based post-PS is accurate, but it neither gives straightforward solutions to the control parameter nor defines the operating point of the HV pulse generator. The circuit-based approach doesn't give insight into the energy exchanges that take place in the HV pulse generator.

Hence, an energy-based analysis governing the energy exchanges in the HV pulse generator with parasitic capacitance effect is proposed in this paper. A control strategy for both pre-PS and post-PS, controlling the energy flow from input to the pulsed output, is proposed. The proposed energy-based analysis is simple and aids in arriving at straightforward expressions for the control implementation and judicious choice of flyback converter

TABLE 2. Pre-Processing stage topologies for HV pulse power generator

Topology	Voltage Gain Capability	Semiconductor Switches	Component Count	High Frequency Isolation
Interleaved Boost with Voltage Multiplier [18]	$\|M\| < 5$	2 Active 6 Passive	20	No
Boost Flyback Converter [19]	$\|M\| < 10$	2 Active 1 Passive	7	No
HV Flyback based Pre-PS	$10 < \|M\| < 100$	1 Active 1 Passive	5	Yes

TABLE 3. Post-Processing stage topologies for HV pulse power generator

Topology	Smooth Transition	Pulse Repetitive Rate	Snubbers	Power Rating
Marx Generator [23]	High Overshoots*	< 500 Hz	Yes	> 20 kW
High Voltage Switch [29]	Minimal with snubber circuits	> 1000 Hz	Yes	> 10 kW
Proposed Resonant based Post-PS	Minimal	> 1000 Hz	No	< 100 W

*Higher overshoots are observed due to the presence of a spark gap

for the pre-PS and series LLC-based resonant converter for the post-PS. The proposed analysis aids in arriving at essential parameters of the HV pulse generator, like the minimum number of charging cycles, minimum input energy required to charge the DC link capacitor in the pre-PS, and the change in energy discharged by the resonating capacitor during pulsing.

The analysis summarised above confirms a study for an efficient pre-PS and post-PS, which defines the primary objectives of the work. The energy-based analysis with a hybrid control scheme for the high voltage pulse generator is shown in Fig. 2, with the research contribution highlighted in blue colour. The contributions of the work are summarised as follows:

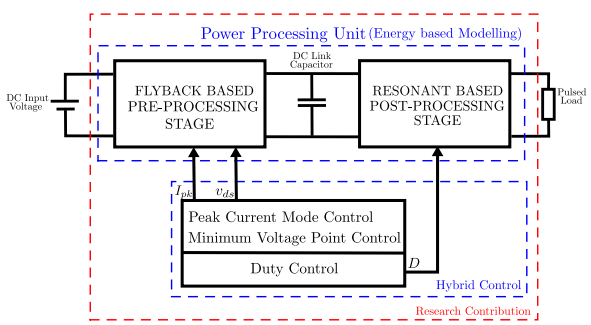


FIGURE 2. Block diagram of a typical high voltage pulse generator and the proposed research work

1) A combined energy-based approach is proposed to define the pre and post-PS converter behaviour. The proposed energy-based analysis enables real-time implementation of the control scheme.
2) The proposed analysis analyses the effect of parasitic capacitance on the HV pulsed loads feeding low pulse power applications.
3) The proposed analysis is used to derive analytical closed-form expressions of the essential parameters, peak power ratings and hence the efficiency of the power processing unit.
4) The proposed analysis is used to analyse the potential usage of the HV flyback converter for the pre-PS and series LLC resonant converter for post-PS.
5) The proposed analysis, the control scheme and computation of essential parameters are validated on HV pulses of -2.5 kV to -5 kV (Peak-Peak), with PRR of 1 kHz and pulse width or Full Width at Half Maximum (FWHM) of 15 µs, through simulation and hardware results.

III. CIRCUIT BASED ANALYSIS OF HIGH VOLTAGE PULSE GENERATOR

The HV pulse generator consists of input voltage, power processing unit and load. The power processing unit consists of 2 stages, i.e. pre-PS and post-PS. In this section, the focus is on the circuit-based analysis of the power processing unit. However, it is essential to understand the load parameters presented in the preceding subsection.

A. OZONE CHAMBER PARAMETERS

The silent discharge of oxygen is made to happen in a chamber called Dielectric Barrier Discharge (DBD) chamber or ozone chamber, which requires a pulsed HV applied to the ozone chamber. The analysis of the DBD chamber is essential for designing the power processing unit and is presented in this section.

Fig. 3 shows a DBD chamber connected to the power processing unit. The chamber consists of (1) an active

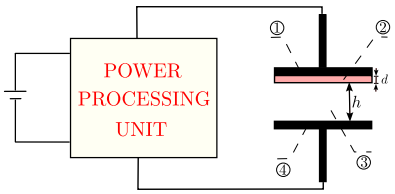


FIGURE 3. DBD chamber connected to power processing unit

electrode, (2) a dielectric layer, (3) a discharge gap and (4) a ground electrode [33], which is electrically represented as a capacitance (C_o), given in (1) [34].

$$C_o = \varepsilon\varepsilon_o A/(d + \varepsilon h) \quad (1)$$

There will be dielectric losses associated with the DBD chamber; this loss component is presented as a high-valued parallel resistance across the capacitor. Hence, the electrical equivalent circuit of a DBD or ozone chamber is represented as an R-C circuit, which forms the load for the power processing unit, as shown in Fig. 4.

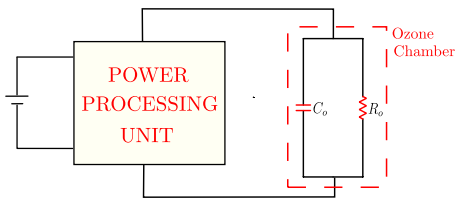


FIGURE 4. Electrical equivalent circuit of DBD chamber

In the literature, ozone concentrations ranging from 1 to 5 mg/L have demonstrated significant efficacy in reducing pollutants in drinking water [35]. For swimming pool water, applying ozone at concentrations of 0.5 to 1 mg/L has proven effective [36]. In sewage water treatment, ozone concentrations ranging from 5 to 10 mg/L are commonly applied, while for industrial waste treatment, concentrations of 10 to 15 mg/L have shown notable pollutant reduction [37]. Ozone has been found to extend the life cycle of granulated activated carbon by over 21 months, with recommended dosages falling between 6 and 8 mg/L [38]. For the aforementioned applications, an appropriate DBD chamber is selected to accommodate the specified ozone concentrations.

In Fig. 5, a single dielectric barrier discharge (DBD) chamber is depicted, featuring electrodes with a diameter of 30 cm. The chamber incorporates a 1 mm thick glass dielectric layer, with a 2 mm gap separating the two layers. From the above specifications, the chamber is electrically presented as a capacitance, estimated at approximately 300 pF (from 1). Oxygen is introduced through the inlet at a consistent flow rate of 2 L/min, while a pulsed high voltage (in the range of -2.5 kV to -5 kV) is applied across the two electrodes [39]–[41].

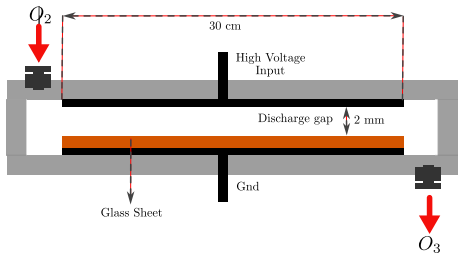


FIGURE 5. DBD chamber with single dielectric [39]

Ozone is collected at the chamber outlet, and Fig. 6 illustrates a graph correlating ozone concentration with the applied pulsed voltage.

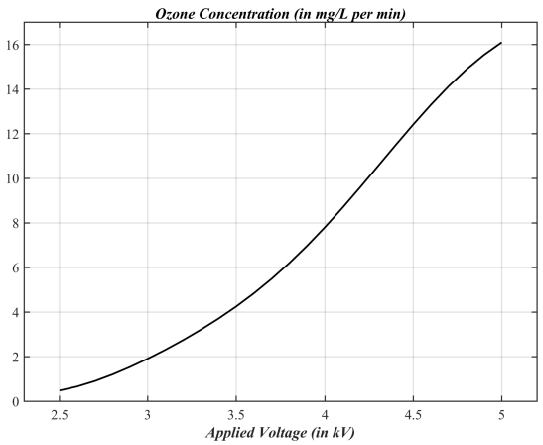


FIGURE 6. Pulse voltage (in negative kV) vs Ozone Concentration [40]

From Fig. 6, it is evident that an applied pulse voltage ranging from -2.5 kV to -5 kV yields ozone concentrations ranging from 0.48 to 16.1 mg/L. These concentrations are deemed adequate for treating water in the above-mentioned applications.

B. ANALYSIS OF POWER PROCESSING UNIT

The power processing unit consists of two stages, i.e. pre-PS, which charges the DC link capacitor and post-PS, in which the DC link capacitor is discharged and converted into pulsed output voltage with the desired gain. The following section describes the circuit-based analysis of the pre-PS and post-PS.

1) Analysis of pre-processing stage

An HV flyback converter considering the transformer's parasitic capacitance and leakage inductance is shown in Fig. 7. In a switching cycle of the HV flyback converter, the magnetizing inductance (L_{mf}) stores energy ($E_{L_{mf}}$) during the turn-on time of switch S_1 and this energy in the magnetizing inductance charges the DC link capacitor (C_{link}) during the turn-off time of switch S_1. Apart from the switching intervals, the magnetis-

ing inductance undergoes resonance with the parasitic capacitance. During this interval, a notable amount of energy interchange happens between L_{mf} and the parasitic capacitance. This reduces the energy delivered per cycle to C_{link}. Selecting a lower value of $E_{L_{mf}}$ might result in not attaining the desired DC link voltage in a specified charging time, which results in uneven peak pulse amplitude in the pulsed output. To ensure soft switching and efficient charging of the DC link capacitor, a Minimum Voltage Point (MVP) switching technique with Peak Current Mode Control (PCMC) technique is preferred due to the presence of parasitic capacitance and leakage inductance [42].

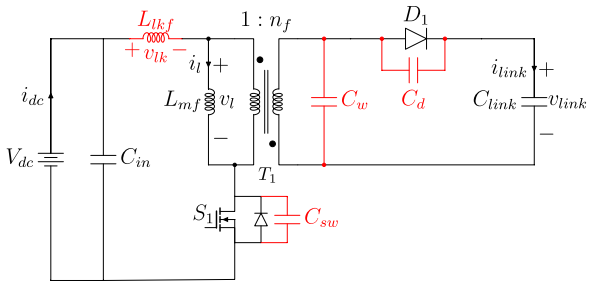


FIGURE 7. A non-ideal HV flyback based pre-PS with parasitic capacitance & leakage Inductance of the HV pulse generator

The following assumptions are considered while deriving the analytical equations:

a) The dominant non-idealities such as the parasitic capacitance (includes switch capacitance (C_{sw}), diode capacitance (C_d) and transformer winding capacitance (C_w)) and the leakage inductance of the transformer (L_{lkf}) is considered in the analysis.
b) The input capacitance (C_{in}) and the DC link capacitance (C_{link}) are considered large such that the ripple on the input and output voltage is negligible.

The operating principle of the HV flyback converter features switch S_1 and diode D_1 conduction along with two resonant conduction intervals. The analytical equations of each interval are derived using circuit analysis and is given in Table 4.

Time Interval 1 ($t_{0,f} - t_{1,f}$): Switch S_1 is turned on at $t = t_{0,f}$ with Zero Voltage Switching (ZVS) (shown in fig 9(a)). The magnetising inductance (L_{mf}) starts storing the energy, and current through the magnetising inductance linearly increases (as shown in Fig. 8). When current through the magnetising inductance (i_l) reaches $I_{pk,f}$, the switch (S_1) is turned off. This is done by using a high-speed comparator which compares i_l with the set reference current $I_{pk,f}$ and generates a trigger pulse when $i_l > I_{pk,f}$. This trigger pulse is used to turn-off the switch S_1. This switching technique is called PCMC switching.

Time Interval 2 ($t_{1,f} - t_{2,f}$): When the switch S_1 turns off, some portion of the energy stored in the magnetising inductance during interval 1 is used to charge the parasitic capacitance (C_{eff}) from $-n_f V_{dc}$ to

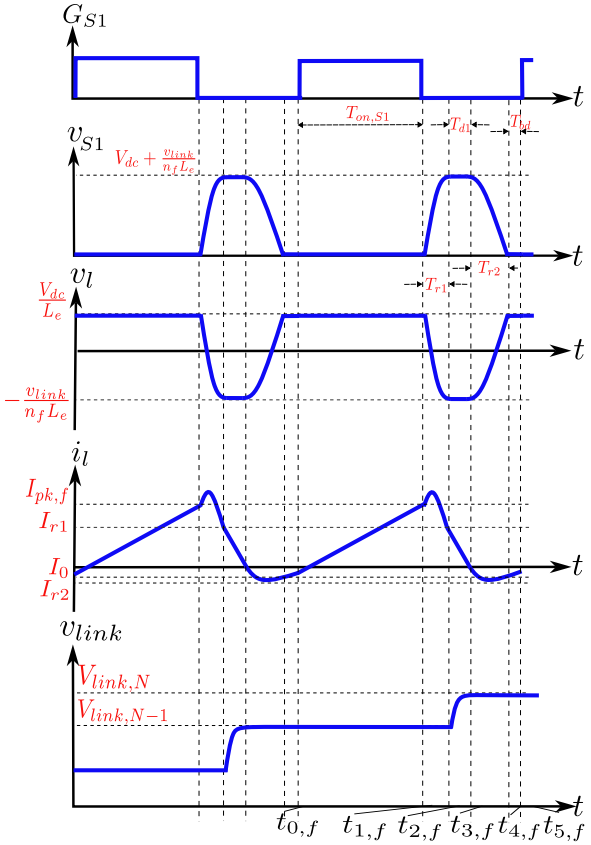


FIGURE 8. Analytical waveforms of the HV flyback-based pre-PS of the HV pulse generator

v_{link} (as shown in Fig. 9(b)). This reduces the energy available in the magnetising inductance; the current through the magnetising inductance reduces from $I_{pk,f}$ to I_{r1} (as shown in Fig. 8). The simplified equivalent circuit of interval 2 is shown in Fig. 9(e) and the parasitic capacitance (referred to secondary) is given by $C_{eff} = \frac{C_{sw}}{n_f^2} + C_w + C_d$.

Time Interval 3 ($t_{2,f} - t_{3,f}$): At $t = t_{2,f}$, diode D_1 starts conducting as the voltage across the equivalent parasitic capacitance gets clamped to v_{link} (as shown in Fig. 9(c)). A simplified equivalent circuit of interval 3 is shown in Fig. 9(f). In this interval, the remaining energy from the magnetizing inductance charges the DC link capacitor (C_{link}).

Time Interval 4 ($t_{3,f} - t_{4,f}$): When diode D_1 stops conducting, the energy stored in the parasitic capacitance (during interval 2) discharges to the magnetising inductance (as shown in Fig. 9(b)). At the end of this interval, as $v_{link} > n_f V_{dc}$, the body diode of the switch S_1 starts conducting.

Time Interval 5 ($t_{4,f} - t_{5,f}$): When the body diode conducts, it transfers the energy stored in the magnetizing inductance (during interval 4) back to the source (as shown in 9(d)). The gating pulses are given to switch S_1 during this interval, ensuring ZVS turn-on (shown in

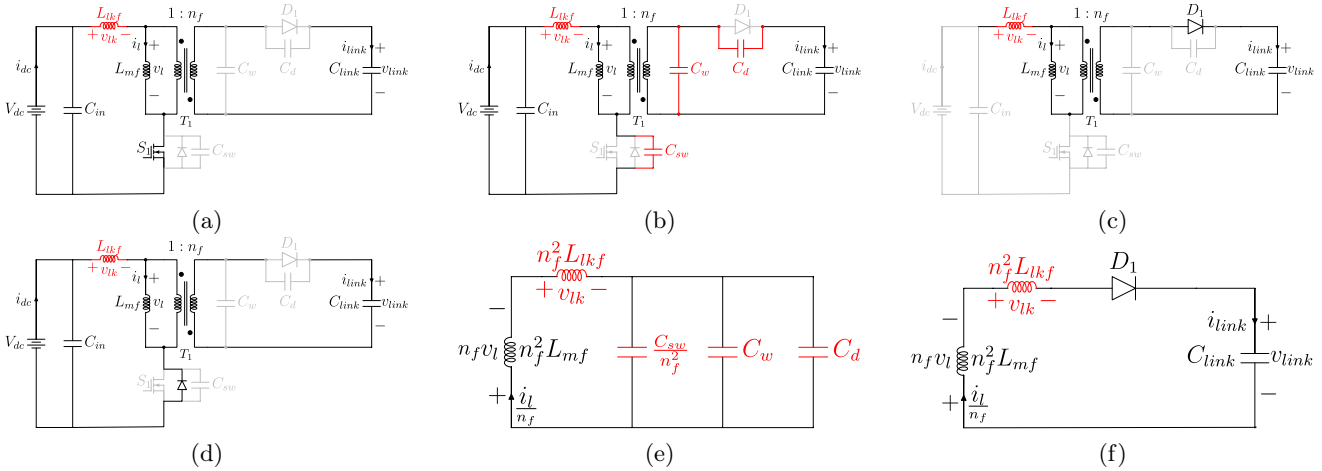


FIGURE 9. Equivalent circuit of HV flyback based pre-PS for various time intervals of the HV pulse generator (a) Interval 1, (b) Interval 2 & 4, (c) Interval 3, (d) Interval 5, (e) More simplified equivalent circuit during interval 2 & 4, (f) More simplified equivalent circuit during interval 3

TABLE 4. Analytical Equations of HV Flyback based pre-PS of the HV pulse generator

Time Interval	Voltage across magnetising inductance of Flyback Converter (v_l)	Current through magnetising inductance of Flyback Converter (i_l)
$t_{0,f} - t_{1,f}$	$v_l(t) = V_{dc}\left(\frac{L_{mf}}{L_{mf}+L_{lkf}}\right)$	$i_l(t) = \begin{cases} \frac{V_g}{L_{mf}+L_{lkf}}(t-t_{0,f}) & , v_{link} \le n_f V_{dc} \\ I_0 + \frac{V_g}{L_{mf}+L_{lkf}}(t-t_{0,f}) & , v_{link} > n_f V_{dc} \end{cases}$
$t_{1,f} - t_{2,f}$	$v_l(t) = V_{m1}\cos\left(w_1(t-t_{1,f})+\phi_1\right)$ $V_{m1} = w_1 L_{mf} I_{m1}$ $w_1 = \frac{1}{\sqrt{n_f^2(L_{mf}+L_{lkf})C_{eff}}}$ $C_{eff} = \frac{C_{sw}}{n_f^2} + C_w + C_d$	$i_l(t) = I_{m1}\sin\left(w_1(t-t_{1,f})+\phi_1\right)$ $I_{m1} = \sqrt{I_{pk,f}^2 + \left(\frac{V_{dc}}{w_1(L_{mf}+L_{lkf})}\right)^2}$ $\phi_1 = \tan^{-1}\left(\frac{I_{pk,f}}{V_{dc}} w_1 (L_{mf}+L_{lkf})\right)$
$t_{2,f} - t_{3,f}$	$v_l(t) = -V_{m2}\sin\left(w_2(t-t_{2,f})+\phi_2\right)$ $V_{m2} = w_2 L_{mf} I_{m2}$ $\phi_2 = \tan^{-1}\left(\frac{V_{link,N-1}}{n_f(L_{mf}+L_{lkf})I_{r1}w_2}\right)$	$i_l(t) = I_{m2}\cos\left(w_2(t-t_{2,f})+\phi_2\right)$ $I_{m2} = \sqrt{\frac{I_{r1}^2}{n_f^2} + \frac{V_{link,N-1}^2}{n_f^2(L_{mf}+L_{lkf})^2 w_2^2}}$ $w_2 = \frac{1}{\sqrt{n_f^2(L_{mf}+L_{lkf})C_{link}}}$
$t_{3,f} - t_{4,f}$	$v_l(t) = V_{3m}\sin\left(w_1(t-t_{3,f})\right)$ $V_{3m} = w_1 L_{mf} I_{3m}$	$i_l(t) = I_{3m}\sin\left(w_1(t-t_{3,f})\right)$ $I_{3m} = w_2 I_{m2}\cos\left(w_2 T_{d1}+\phi_2\right)$
$t_{4,f} - t_{5,f}$	$v_l(t) = \begin{cases} \text{N.A.} & v_{link} \le n_f V_{dc} \\ V_{dc}\left(\frac{L_{mf}}{L_{mf}+L_{lkf}}\right) & v_{link} > n_f V_{dc} \end{cases}$	$i_l(t) = \begin{cases} \text{N.A.} & v_{link} \le n_f V_{dc} \\ I_{r2} + \frac{V_g}{L_{mf}+L_{lkf}}(t-t_{4,f}) & v_{link} > n_f V_{dc} \end{cases}$

Fig. 8). This is done by using a high-speed comparator which compares v_{S1} and V_{dc}, generating a trigger pulse when $v_{S1} < V_{dc}$. This trigger pulse is delayed by $\frac{\pi}{w_1}$ and given to switch S_1 ensuring ZVS turn-on of S_1. This switching technique is called the MVP switching scheme.

Time interval $t_{0,f}$ to $t_{5,f}$ is repeated in the subsequent cycles till the output voltage across the DC link capacitor gets charged to the voltage required by the post-PS unit. The time required to charge the DC link capacitor is given by $T_{chrg,f} = N(t_{5,f} - t_{0,f})$, where N is the number of switching cycles of the HV flyback converter. When the controller detects that v_{link} has reached V_{dcl} (input voltage required by the post-PS), it disables the HV flyback converter and V_{dcl} is maintained at the output.

2) Analysis of post-processing stage

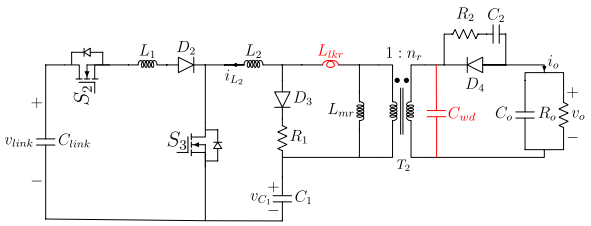


FIGURE 10. Structure of resonant-based pulsed switching module for the post-PS of the HV pulse generator

A series resonant-based post-PS is proposed in Fig. 10. The pre-PS charges the DC link capacitor to the V_{dcl}, following which the switch S_2 is turned on, and

the energy in the DC link capacitor charges the resonant capacitor (C_1). When switch S_3 is turned on, a resonant loop is formed, and the energy in C_1 gets discharged, and a pulsed HV is observed at the output (v_o).

The following assumptions are considered while deriving the analytical equations:

a) The dominant non-idealities, such as parasitic capacitance and the leakage inductance of the transformer that affects the converter performance, are considered in the analysis.
b) The magnetising inductance of the transformer T_2 (L_{mr}) is very large and is neglected in the circuit analysis.
c) The DC link voltage (v_{link}) is always charged to V_{dcl} by the pre-PS.

The operating principle of the resonant-based post-PS is given below. The analytical equation of each interval are derived using circuit analysis and is given in Table 5.

Time Interval 1 ($t_{0,r}$ to $t_{1,r}$): The voltage across the resonant capacitor C_1 is charged to $V_{C_{1,max}}$ before the turn-on of the switch S_3. At the turn-on of switch S_3, diode D_4 is forward biased, and resonance occurs with the resonant frequency defined by $w_{r1} = \sqrt{\frac{n_r^2 C_s + C_1}{(L_2 + L_{lkr}) n_r^2 C_s C_1}}$. (as shown in Fig. 12(a)). The voltage across the resonant capacitor gets discharged, and the voltage across the output capacitance rises to $V_{o,max}$ (as shown in Fig. 11).

Time Interval 2 ($t_{1,r}$ to $t_{2,r}$): The voltage across the resonant capacitor C_1 discharges to $V_{C_{1,min}}$ at $t = t_{1,r}$. At $t = t_{1,r}$, the body diode of the switch is turned on due to the reversal of i_{L_2} current, diode D_4 gets reversed biased, and the voltage across the output starts discharging (as shown in fig 11). The resonant capacitor charges to $V_{C_{1,itm}}$ by DC link capacitor (as shown in Fig. 12(b)). The switch S_3 is turned off during this interval to ensure Zero Current Switching (ZCS).

Time Interval 3 ($t_{2,r}$ to $t_{3,r}$): At $t = t_{3,r}$, the body diode of switch S_3 stops conducting and the resonant capacitor charges to $V_{C_{1,max}}$ by the DC link capacitor (as shown in Fig. 12(c)). The output voltage discharges with a time constant defined by Ro and Co. (as shown in fig 11).

Time Interval 4 ($t_{3,r}$ to $t_{4,r}$): The resonant capacitor gets clamped to $V_{C_{1,max}}$, as the diodes D_2 and D_3 gets reversed biased at $t = t_{3,r}$ (as shown in Fig. 12(d)). At the end of this interval, the output voltage is discharged to zero.

Time Interval 5 ($t_{4,r}$ to $t_{5,r}$): In this interval, none of the semiconductor switches conducts and the voltage across the resonant capacitor stays at $V_{C_{1,max}}$ till the next switching cycle of the switch S_3. This process is repeated through the subsequent cycles, and high voltage pulses are observed across the output.

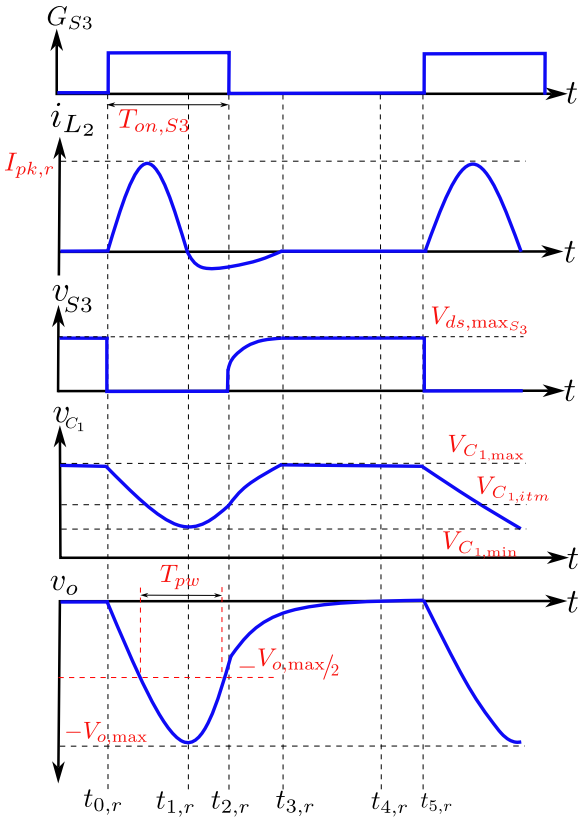


FIGURE 11. Analytical waveforms of the resonant-based pulse switching module for the post-PS of the HV pulse generator

C. LIMITATIONS OF CIRCUIT-BASED ANALYSIS

1) Analysing the circuit-based approach, results in solving transcendental equations (as observed from Table 1 and Table 2), which does not give a straightforward solution to the control parameters of the power processing unit.
2) The circuit-based analysis fails to provide the parasitic capacitance's effect in the pre and post-PS and the energy exchanges in the HV pulse generator.
3) In the pre-PS, the computation of parameters like charging time, the final output voltage, and change in the output voltage in each cycle requires information on the previous cycles, which the analysis fails to provide.
4) The analysis fails to provide a combined pre and post-PS approach, which helps in computing essential parameters of the HV pulse generator.

An energy-based analysis is proposed and presented in the next section to address the above limitations in the circuit-based analysis.

IV. ENERGY BASED ANALYSIS AND DESIGN

Analysing the HV flyback converter along with the resonant-based post-PS in an energy-based approach gives more insight into whether the pre-PS will be capable of charging the DC link capacitor voltage within the

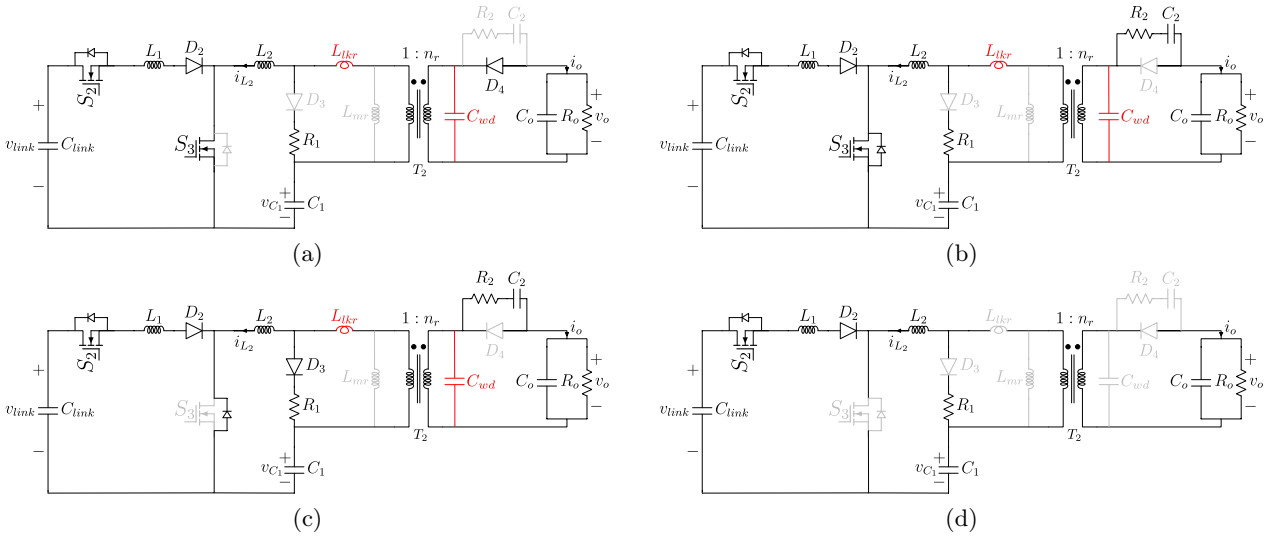


FIGURE 12. Equivalent circuit of resonant-based pulse switching module for the post-PS for various time intervals of the HV pulse generator (a) Interval 1, (b) Interval 2, (c) Interval 3, (d) Interval 4 & Interval 5

TABLE 5. Analytical equations of resonant-based pulse switching module for the post-PS of the HV pulse generator

Time Interval	Output Voltage across Ozone Load (v_o)	Resonant Inductor Current (i_{L_2})
$t_{0,r} - t_{1,r}$	$v_o(t) = \frac{n_r C_1}{n_r^2 C_s + C_1} V_{C_{1,max}} \left[\cos\left(w_{r1}\left(t - t_{0,r}\right)\right) - 1\right]$	$i_{L_2}(t) = \frac{\sqrt{n_r^2 C_s C_1 (L_2 + L_{lkr})\left(C_1 + n_r^2 C_s\right)}}{L_1\left(C_1 + n_r^2 C_s\right)} V_{C_{1,max}} \sin\left(w_{r1}\left(t - t_{0,r}\right)\right)$
	$w_{r1} = \sqrt{\frac{n_r^2 C_s + C_1}{(L_2 + L_{lkr}) n_r^2 C_s C_1}}$	$C_s = C_o + C_{wd}$
$t_{1,r} - t_{2,r}$	$v_o(t) = \frac{n_r C_1}{n_r^2 C_p + C_1} V_{C_{1,min}} \left[\cos\left(w_{r2}\left(t - t_{1,r}\right)\right) - 1\right]$	$i_{L_2}(t) = \frac{\sqrt{n_r^2 C_p C_1 (L_2 + L_{lkr})\left(C_1 + n_r^2 C_p\right)}}{L_1\left(C_1 + n_r^2 C_p\right)} V_{C_{1,min}} \sin\left(w_{r2}\left(t - t_{1,r}\right)\right)$
	$w_{r2} = \sqrt{\frac{n_r^2 C_p + C_1}{(L_2 + L_{lkr}) n_r^2 C_p C_1}}$	$C_p = \frac{C_o C_2}{C_o + C_2} + C_{wd}$
$t_{2,r} - t_{3,r}$	$v_o(t) = \frac{V_{o,max}}{R_2 C_2'}\left[\frac{K_1 R_2 C_2' - 1}{K_1 - K_2} e^{-K_1\left(t - t_{2,r}\right)}\right] + \frac{V_{o,max}}{R_2 C_2'}\left[\frac{1 - R_2 C_2' K_2}{K_1 - K_2} e^{-K_2\left(t - t_{2,r}\right)}\right]$	$i_{L_2}(t) = \frac{V_{dc1} - V_{C_{1,itm}}}{(L_1 + L_2) w_{r3}} \sin\left(w_{r3}\left(t - t_{2,r}\right)\right) + I_0 \cos\left(w_{r3}\left(t - t_{2,r}\right)\right)$
	$C_2' = \frac{C_2 C_{wd}}{C_2 + C_{wd}}$	$I_0 = \frac{V_{dc1}}{L_1}\left(t_{2,r} - t_{0,r}\right)$
	$K_1, K_2 = \frac{-b \pm \sqrt{b^2 - 4ac}}{2a}$	$w_{r3} = \frac{1}{\sqrt{(L_1 + L_2) C_1}}$
	$a = 1, b = \frac{R_o C_o + R_2 C_2' + R_o C_2'}{R_o R_2 C_o C_2'}, c = \frac{1}{R_o R_2 C_o C_2'}$	
$t_{3,r} - t_{4,r}$	$v_o(t) = \frac{V_{o,max}}{R_2 C_2'}\left[\frac{K_1 R_2 C_2' - 1}{K_1 - K_2} e^{-K_1\left(t - t_{2,r}\right)}\right] + \frac{V_{o,max}}{R_2 C_2'}\left[\frac{1 - R_2 C_2' K_2}{K_1 - K_2} e^{-K_2\left(t - t_{2,r}\right)}\right]$	0
$t_{4,r} - t_{5,r}$	0	0

next switching cycle of the post-PS. So, an energy-based analysis of the power processing unit, which describes the energy exchanges and circulating energy in the pre-PS and post-PS, is proposed in this section. An energy-based approach describes the energy discharging phase in the post-PS and the energy charging phase of the pre-PS; which enables computing of essential parameters of the HV pulse power converter associated with the load.

A. ENERGY EXCHANGES IN POST-PROCESSING STAGE

1) Interval 1: (Energy discharging interval)
At the turn-on of switch S_3, the resonant capacitor discharges from $V_{C_{1,max}}$ to $V_{C_{1,min}}$ and pulsed voltage is obtained across the output voltage with a peak amplitude of $V_{o,max}$. The energy required to charge the load capacitor to the maximum output voltage ($V_{o,max}$) is given by (2) [34].

$$E_{C_o} = \frac{1}{2} C_o V_{o,max}^2 \tag{2}$$

During this interval, the resonant capacitor (C_1) supplies energy to charge the load capacitor and some fraction of energy is used by the leakage inductor (L_{lkr}) and the magnetising inductance (L_{mr}) of resonant-based post-PS. So the net energy discharged by C_1 is obtained in (3).

$$E_{C_1} = \frac{E_{C_o}}{\varphi} \tag{3}$$

where φ is the energy efficiency factor for C_1, and the value of φ can be between 0.8 to 0.9.

2) Interval 2: (Energy charging interval) At the turn-off of switch S_3, the resonant capacitor charges to $V_{C_{1,max}}$ to ensure that constant peak pulse amplitude is maintained at the output throughout the cycles. The DC link capacitor charges inductor L_1 to I_1 and the resonant capacitor to $V_{C_{1,max}}$; this discharges the voltage across the DC link capacitor from V_{dcl} to V'_{dcl} during the period $t_{0,r}$ to $t_{3,r}$ (as shown in Fig. 13). The net energy the DC link capacitor discharges is given by (4) [34].

$$E_{C_{link}} = \frac{1}{2}C_{link}\left(V_{dcl}^2 - {V'_{dcl}}^2\right) = E_{C_1} + \frac{1}{2}L_1 I_1^2 \quad (4)$$

where I_1 is the peak current of inductor L_1 which occurs at $t = t_{2,r}$.

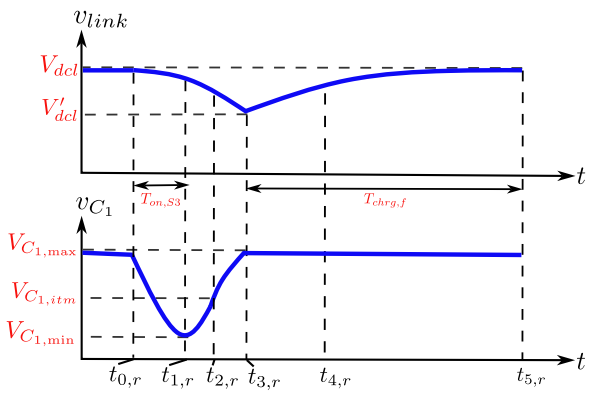


FIGURE 13. Analytical waveforms DC link capacitor and resonant capacitor voltage of resonant based post-PS of the HV pulse generator

From the above energy charging and discharging intervals, analytical close-form equations of some of the post-PS's essential parameters are derived and is given below.

1) Predicting the change in energy discharged by the resonant capacitor for small changes in the peak output voltage

This parameter is essential as a small change in the peak output voltage demands more energy from the resonant capacitor (C_1). Hence, the DC link capacitor should be able to charge the resonant capacitor in a pre-defined time, determined by the charging time of the pre-PS ($T_{chrg,f}$).

Putting $V_{o,max} = V_{o,max} + \Delta v_o$ in (2), where Δv_o is a small increment in the peak output voltage.

$$E'_{C_o} = \frac{1}{2}C_o(V_{o,max} + \Delta v_o)^2 \quad (5)$$

$$\Delta E_{C_o} = E'_{C_o} - E_{C_o} = \Delta v_o V_{o,max} C_o \quad (6)$$

Hence, the change in energy discharged by the resonant capacitor is given in (7).

$$\Delta E_{C_1} = \frac{\Delta E_{C_o}}{\varphi} = \frac{\Delta v_o V_{o,max} C_o}{\varphi} \quad (7)$$

2) Predicting the voltage attained by the DC link capacitor at $t = t_{3,r}$ due to small change in the peak output voltage

The voltage across the DC link capacitor reduces every time it charges the resonant capacitor. The DC link capacitor should be charged to the required voltage before the desired charging time ($T_{chrg,f}$). Hence, predicting the voltage attained by the DC link capacitor due to a small change in the peak output voltage is vital. From (6),

$$E'_{C_o} = E_{C_o} + \Delta v_o V_{o,max} C_o \quad (8)$$

Putting (7) in (3) and (4),

$$V'_{dcl,new} = \sqrt{V_{dcl}^2 - \frac{2\left(E_{C_{link}} + \frac{\Delta v_o V_{o,max} C_o}{\varphi}\right)}{C_{link}}} \quad (9)$$

where $V'_{dcl,new}$ is the voltage attained by the DC link capacitor at $t = t_{3,r}$.

The pre-PS should charge the DC link capacitor voltage from V'_{dcl} to V_{dcl} within the time $T_{chrg,f}$ given by $t_{5,r} - t_{3,r}$. The charging time $T_{chrg,f}$ varies for a variable pulsed output voltage. Hence, the computation of energy exchanges in the pre-PS is essential in order to meet the charging time and load requirements in every cycle.

B. ENERGY EXCHANGES IN PRE-PROCESSING STAGE

The value of the peak current through the magnetising inductance ($I_{pk,f}$) of the HV flyback converter depends on the peak pulse output voltage ($V_{o,max}$), pulse width (T_{pw}) and the PRR (T_{pulse}) of the HV pulse generator. For a variable peak pulse output voltage (i.e. from $-2.5\,kV$ to $-5\,kV$), $I_{pk,f}$ needs to be varied by the controller such that the charging time does not exceed ($t_{5,r} - t_{3,r}$) (as shown in Fig. 14) and the power does not exceed 150 W. In an HV flyback converter, additional energy exchange intervals, apart from the energy storage and release interval, are observed due to the parasitic capacitance. The computation of these energy exchanges that occur in the HV flyback converter within a single charging cycle is essential to compute the essential parameters of the pre-PS.

1) Interval 1 (Energy storage interval): The voltage across the parasitic capacitance (C_{eff}) is clamped to $-n_f V_{dc}$. During the turn-on of switch S_1, the magnetising inductance of the HV flyback converter stores energy $E_{L_{mf}}$, given by (10) with the set peak current ($I_{pk,f}$) reference through the magnetising inductance regulated by the PCMC.

$$E_{L_{mf}} = \frac{1}{2}L_{mf} I_{pk,f}^2 \quad (10)$$

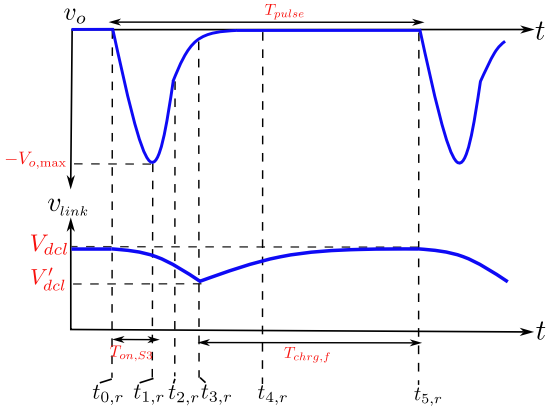


FIGURE 14. **Analytical waveforms of output voltage and DC link capacitor voltage of the HV pulse generator**

2) Interval 2 (First resonant energy interval): During this interval, some fraction of energy stored in the magnetising inductance is used to charge the equivalent parasitic capacitance (C_{eff}) from $-n_f V_{dc}$ to v_{link}. This fraction of energy utilised by the parasitic capacitance (called the circulating energy) is given by (11).

$$E_{C_{eff}} = \frac{1}{2} C_{eff} \left(v_{link}^2 - n_f^2 V_{dc}^2 \right) \tag{11}$$

3) Interval 3 (Energy release interval): The remaining energy from the magnetising inductance is delivered to the DC link capacitor through diode D_1 conduction. The energy delivered to the DC link capacitor in a single HV flyback converter switching cycle is given by (12).

$$\begin{aligned} E_{C_{link},cycle} &= E_{L_{mf}} - E_{C_{eff}} \\ &= \frac{1}{2} L_{mf} I_{pk,f}^2 - \frac{1}{2} C_{eff} \left(v_{link}^2 - n_f^2 V_{dc}^2 \right) \end{aligned} \tag{12}$$

4) Interval 4 (Second resonant energy interval): Post the diode D_1 conduction interval, the energy stored in the parasitic capacitance during interval 2 i.e. $\frac{1}{2} C_{eff} \left(v_{link}^2 - n_f^2 V_{dc}^2 \right)$ discharges to the magnetising inductance. The equivalent parasitic capacitance discharges from v_{link} to $-n_f V_{dc}$. The energy circulation stops with the conduction of the body diode of switch S_1 when $v_{link} > n_f V_{dc}$.
5) Interval 5 (Circulating energy interval): When $v_{link} > n_f V_{dc}$, the body diode of switch S_1 conducts to deliver the energy available in the magnetising inductance (during interval 4) back to the source.

Fig. 15(a) shows that the fraction of energy stored in the magnetising inductance ($E_{L_{mf}}$) is utilised to charge the parasitic capacitance and is given by $E_{C_{eff}}$. This energy is delivered back to the magnetising inductance in interval 4, and the remaining energy is delivered to the DC link capacitor. In each switching cycle, the

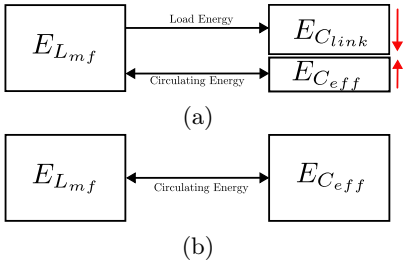


FIGURE 15. **Energy exchanges in the pre-PS of the HV pulse generator**

voltage across the DC link capacitor (v_{link}) increases, which results in increasing of the circulating energy $E_{C_{eff}}$ (obtained in (11)). Hence energy delivered to the load ($E_{C_{link}}$) decreases (obtained in (12)). As the output voltage builds up, at a certain time instant, the energy delivered to the load decreases to zero, and circulating energy becomes equal to the magnetising inductance energy (as shown in Fig. 15(b)). At this instant, the voltage across the load will be constant. So the minimum peak current through the magnetising inductance of the flyback converter required to charge the DC link capacitor from V'_{dcl} to V_{dcl} is obtained by (13) and is given in (15).

$$E_{L_{mf}} = E_{C_{eff}}|_{v_{link}=V_{dcl}} \tag{13}$$

$$\frac{1}{2} L_{mf} I_{pk,f}^2 = \frac{1}{2} C_{eff} \left(V_{dcl}^2 - n_f^2 V_{dc}^2 \right) \tag{14}$$

$$I_{pk,f(min)} = \sqrt{\frac{C_{eff} \left(V_{dcl}^2 - n_f^2 V_{dc}^2 \right)}{L_{mf}}} \tag{15}$$

The time required to charge the DC link capacitor from V'_{dcl} to V_{dcl} is obtained from Fig. 14 and is given in (16).

$$T_{chrg,f} = T_{pulse} - (t_{3,r} - t_{0,r}) \tag{16}$$

From Fig. 11 and 14, $t_{3,r} - t_{0,r} \gg T_{pw}$; hence (16) is rewritten as (17).

$$\Rightarrow T_{chrg,f(max)} < T_{pulse} - T_{pw} \tag{17}$$

The HV flyback converter charges the DC link capacitor from V'_{dcl} to V_{dcl} if it is operated at the peak current obtained in (15), but it takes longer time to charge i.e. greater than $(T_{pulse} - T_{pw})$, as obtained in (17). So, an optimal peak current through the magnetising inductance needs to be designed such that the charging time is within limits (as obtained in (17)) and the power does not exceed 150 W.

The HV flyback converter charges the DC link capacitor within the charging time $T_{chrg,f}$ and the peak power required to charge is given (18) [42]. The total energy is delivered in a sequence of cycles given by (19) [42].

$$P_{pk} = \frac{E_{C_{link}}}{T_{chrg,f}} \tag{18}$$

$$E_{cycle} = \frac{P_{pk}}{f_{S_1}} = \frac{E_{C_{link}}}{T_{chrg,f} f_{S_1}} \tag{19}$$

The HV flyback converter delivers some fraction of energy (i.e. $E_{C_{eff}}$) to charge the parasitic capacitance. Hence, the maximum energy delivered by the magnetising inductance of the HV flyback converter ($E_{L_{mf}}$) is derived analytically and is given by (20).

$$E_{L_{mf}} = \frac{1}{\eta}\left[\frac{E_{C_{link}}}{T_{chrg,f} f_{S_1}} + \frac{1}{2} C_{eff}\left(V_{dcl}^2 - n_f^2 V_{dc}^2\right)\right] \tag{20}$$

$$\Rightarrow \frac{1}{2} L_{mf} I_{pk,f}^2 = \frac{1}{\eta}\left[\frac{E_{C_{link}}}{T_{chrg,f} f_{S_1}} + \frac{1}{2} C_{eff}\left(V_{dcl}^2 - n_f^2 V_{dc}^2\right)\right] \tag{21}$$

Hence, the peak current through the magnetising inductance of the HV flyback converter is derived from (21) and is given in (22).

$$I_{pk,f} = \sqrt{\frac{2}{\eta L_{mf}}\left[\frac{E_{C_{link}}}{T_{chrg,f} f_{S_1}} + \frac{1}{2} C_{eff}\left(V_{dcl}^2 - n_f^2 V_{dc}^2\right)\right]} \tag{22}$$

where f_{S_1} is the switching frequency of switch S_1. With the set peak current, the pre-PS is operated, ensuring the charging of the DC link capacitor within allowable charging time $T_{chrg,f}$. The peak current in (22) must be greater than the minimum peak current obtained in (15).

Let v_x be the initial voltage of capacitor C_{link} at $t = t_{3,r}$ (as shown in Fig. 13) which is equal to V'_{dcl} and v_{x+1} is the voltage attained by capacitor C_{link} at the end of a first switching cycle of the flyback converter. The energy balance equation of the flyback converter from the above 5 energy intervals is given by (23).

$$E_{C_{link}(x+1)} = E_{C_{link}(x)} + E_{L_{mf}} - E_{C_{eff}(x+1)} \tag{23}$$

where, $E_{C_{link}(x+1)}$ is the energy attained by the capacitor C_{link} after the first switching/charging cycle of the HV flyback converter, $E_{C_{link}(x)}$ is the initial energy of capacitor C_{link} and $E_{C_{eff}(x+1)}$ is the fraction of energy utilised by the parasitic capacitance in the first switching/charging cycle of flyback converter.

$$E_{C_{link}(x+1)} = \frac{1}{2} C_{link} v_{x+1}^2 \tag{24}$$

$$E_{C_{link}(x)} = \frac{1}{2} C_{link} v_x^2 = \frac{1}{2} C_{link} {v'_{dcl}}^2 \tag{25}$$

$$E_{C_{eff}(x+1)} = \frac{1}{2} C_{eff}\left(v_{x+1}^2 - n_f^2 V_{dc}^2\right) \tag{26}$$

Putting (24) to (26) in (23),

$$\begin{aligned} E_{C_{link}(x)} + E_{in} &= \frac{1}{2} C_{eff} v_{x+1}^2 + \frac{1}{2} C_{link} v_{x+1}^2 \\ &= \frac{1}{2} C_{link} v_{x+1}^2 \left(1 + \frac{C_{eff}}{C_{link}}\right) \end{aligned} \tag{27}$$

where,

$$E_{in} = \frac{1}{2}\left(L_{mf} I_{pk,f}^2 + C_{eff} n_f^2 V_{dc}^2\right) \tag{28}$$

Putting $q = \left(1 + \frac{C_{eff}}{C_{link}}\right)$ in (27),

$$E_{C_{link}(x)} + E_{in} - q E_{C_{link}(x+1)} = 0 \tag{29}$$

From the above energy equations (10) - (29), analytical close-form equations of some of the pre-PS's essential parameters are derived and are given below.

1) Predicting number of charging cycles required to charge the DC link capacitor voltage from V'_{dcl} to V_{dcl}

Let N be the number of charging cycles required to charge the DC link capacitor voltage from V'_{dcl} to V_{dcl}.

From (29), similary writing the equations for N^{th} switching cycle,

$$E_{C_{link}(x+N)} = \frac{E_{C_{link}(x)} + E_{in}\left(1 + q + q^2 + ... + q^{N-1}\right)}{q^N} \tag{30}$$

Solving for N in (30), the number of charging cycles is given by,

$$N = \frac{\log\left(\frac{\frac{E_{in}}{q-1} - E_{C_{link}(x)}}{\frac{E_{in}}{q-1} - E_{C_{link}(x+N)}}\right)}{\log(q)} \tag{31}$$

where,

$$E_{C_{link}(x+N)} = \frac{1}{2} C_{link} v_{dcl}^2 \tag{32}$$

2) Predicting the increment in voltage per switching /charging cycle in pre-PS

Putting $v_{x+1} = v_x + \Delta v_{link}$ in (27), where Δv_{link} is the increment in voltage per switching or charging cycle in the HV flyback converter,

$$\frac{1}{2} C_{link} v_x^2 + E_{in} = \frac{1}{2} q C_{link} (v_x + \Delta v_{link})^2 \tag{33}$$

$$\Rightarrow \Delta v_{link} = \frac{E_{in} - \frac{1}{2} C_{eff} v_x^2}{q C_{link} v_x} \tag{34}$$

The features of the proposed energy-based analysis can be summarised as given below,

1) The proposed energy-based analysis gives an insight into the energy exchanges and circulating energy in pre and post-PS.

2) The proposed combined energy-based analysis is used to achieve programmability of pulse voltage profiles by maintaining an optimal charging time of the pre-PS.
3) The energy-based analysis provides a simplified expression than the circuit-based analysis, which helps determine several essential parameters of the HV pulse generator.
4) The energy-based analysis is derived by taking care of the dominant parasitics in the HV pulse generator.

C. DESIGN METHODOLOGY OF HV PULSE GENERATOR

TABLE 6. Specification for water treatment application

Load equivalent resistance (R_o)	190 kΩ
Load equivalent capacitance (C_o)	300 pF
Maximum output voltage ($V_{o,max}$)	-2.5 to -5 kV
Pulse width or FWHM (T_{pw})	15 μs
Pulse repetitive rate (F_{pulse})	1000 Hz

The design parameters of the pre-PS and the post-PS are derived based on the specification of a typical water treatment application shown in Table 6.

1) Design of resonant-based pulse switching module

- Design of resonant capacitor (C_1):
The voltage across the resonant capacitor C_1 defines the pulse voltage profile (as shown in Fig. 11); hence the value of the resonant capacitor is chosen such that $\frac{C_1}{n_r^2 C_o} > 2$.
The maximum value of the resonant capacitor is derived from output voltage expression for the time interval $t_{0,r}$ to $t_{1,r}$ and is given by (35).

$$V_{C_{1,max}} = \frac{V_{o,max}}{2n_r C_1}\left(n_r^2 C_s + C_1\right) \tag{35}$$

- Turn-on time for the switch S_3 ($T_{on,S3}$):
The pulse width (T_{pw}) is the difference between the time interval between the rising and falling instant of a pulse at which the voltage reaches 50 % of the value at its peak (as shown in Fig. 16). It is defined as the Full Width at Half Maximum (FWHM) of a pulse. The pulse width (T_{pw}) is derived from Fig. 17 and is given by,

$$T_{pw} = t_{p2} - t_{p1} = (t_{1,r} - t_{p1}) + (t_{p2} - t_{r,1}) \tag{36}$$

The time interval $(t_{1,r} - t_{p1})$ and $(t_{p2} - t_{1,r})$ are obtained by equating $v_o(t) = -\frac{V_{o,max}}{2}$ at $t = t_{p1}$ and $t = t_{p2}$ during the interval $t_{0,r}$ to $t_{1,r}$ and $t_{1,r}$ to $t_{2,r}$ respectively.

$$T_{pw} = \frac{T_{on,S3}}{2\beta} + \frac{\pi}{3w_{r2}} \tag{37}$$

Hence, the turn-on time for the switch S_3 is given in (38).

$$T_{on,S3} = 2\beta\left(T_{pw} - \frac{\pi}{3w_{r2}}\right) \tag{38}$$

where β is the delay in the switch S_3 turn-off, ensuring ZCS turn-off.

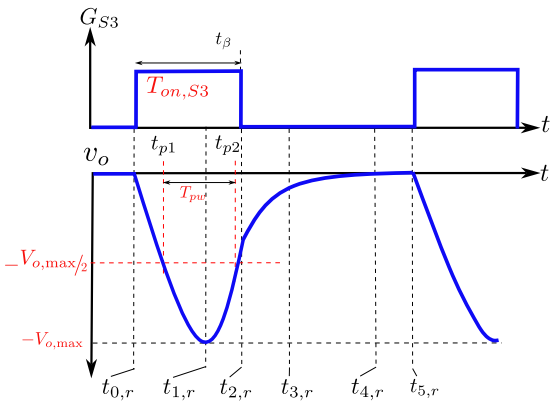


FIGURE 16. Analytical waveform of output voltage and S_3 gate pulse of the post-PS of the HV pulse generator

- Condition for ZCS for switch S_2 and the value of β:
During the interval $t_{1,r}$ to $t_{2,r}$, the body diode of the switch S_3 conducts when current through switch S_3 goes negative and this happens only when $i_{L_1} + i_{L_2} = 0$, where i_{L_1} is the current through inductor L_1. This is the condition for ZCS; hence, the value of β is derived from Fig. 16 and is given in (39).

$$\begin{aligned}\beta &= \frac{t_\beta - t_{0,r}}{t_{1,r} - t_{0,r}} = \frac{(t_\beta - t_{1,r}) + (t_{1,r} - t_{0,r})}{t_{1,r} - t_{0,r}} \\ &= 1 + \frac{t_\beta - t_{1,r}}{t_{1,r} - t_{0,r}} = 1 + \frac{w_{r1}}{\pi}(t_\beta - t_{1,r})\end{aligned} \tag{39}$$

The value of $(t_\beta - t_{1,r})$ is obtained by putting $i_{L_1} + i_{L_2} = 0$ at $t = t_\beta$ during the interval $t_{1,r}$ to $t_{2,r}$.
- Value of resonant inductor (L_2):
The value of the resonant inductor is obtained by putting,

$$w_{r_1}(t_{1,r} - t_{0,r}) = \pi \tag{40}$$

where,

$$t_{1,r} - t_{0,r} = \frac{T_{on}}{\beta} \tag{41}$$

$$w_{r1} = \sqrt{\frac{n_r^2 C_s + C_1}{(L_2 + L_{lkr})\, n_r^2 C_s C_1}} \tag{42}$$

Hence inductor L_2 is derived from (40) and is given in (43).

$$L_2 = \left(\frac{T_{on,S3}}{\pi\beta}\right)^2 \left(\frac{n_r^2 C_s + C_1}{n_r^2 C_s C_1}\right) - L_{lkr} \tag{43}$$

- Design of inductor L_1:
  The inductor L_1 is calculated from the turn-off period of switch S_3 and is obtained by putting,

$$w_{r_3}\left(t_{3,r} - t_{2,r}\right) = \frac{\pi}{2} \tag{44}$$

  where,

$$w_{r3} = \frac{1}{\sqrt{(L_1 + L_2)C_1}} \tag{45}$$

  Hence inductor L_1 is derived from (44) and is given by (46).

$$L_1 + L_2 \ll \left(\frac{2 * \left(T_{pulse} - \frac{T_{on,S3}}{\beta}\right)}{\pi\sqrt{C_1}}\right)^2 \tag{46}$$

- Maximum value of DC link voltage (V_{dcl}):
  The value of the maximum DC link voltage (V_{dcl}) is obtained from the voltage equation of the resonant capacitor voltage during the turn-off period and is given by (47).

$$V_{dcl} = \frac{V_{C_{1,max}}}{1 + \sqrt{\frac{T_{on,S3}^2}{\beta^2 C_1 L_1^2}(L_1 + L_2)}} \tag{47}$$

2) Design of flyback converter

- Selection of magnetising inductance (L_{m_f}) and peak current through the magnetising inductance (I_{pk_f}) of flyback converter:
  Fig. 17 shows the design flow chart of the HV pulse generator. The magnetising inductance, peak current and the charging time ($T_{chrg,f}$) are derived iteratively in the design stage of the flow chart. The maximum peak power ($P_{pk,max}$) for an HV flyback converter is always kept less than 150 W. The derived peak current (I_{pk_f}) from the design stage is used as a control parameter for the HV pulse generator.
- Selection of turns ratio of the flyback transformer (n_f):
  The turns ratio n_f is selected based on the voltage stress on the switch S_1 and diode D_1. The voltage across the switch S_1 and diode D_1 during the turn-off condition is given by (48) and (49) [43], respectively.

$$V_{S1,max} = V_{dc} + \frac{V_{link,max}}{n_f} + V_{lkp} \tag{48}$$

$$V_{D_1,max} = V_{link,max} + (n_f V_{dc}) \tag{49}$$

  where V_{lkp} is the voltage spike caused due to leakage inductance and parasitic capacitance of the flyback converter during the charging process [43]. The maximum voltage stress across switch S_1 and diode D_1 should be greater than the voltage across them respectively. So the equations for maximum and minimum turns ratio is given by (50) and (51), respectively.

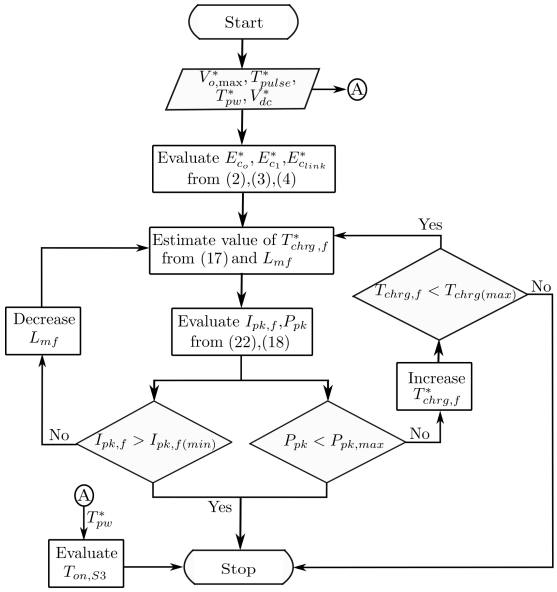


FIGURE 17. Design flowchart of HV pulse generator

$$n_{f_{max}} = \frac{(\sigma_{D1}.V_{BD,D1}) - V_{link,max}}{V_{dc}} \tag{50}$$

$$n_{f_{min}} = \frac{V_{link,max}}{(\sigma_{S1}.V_{BD,S1}) - V_{dc} - V_{lkp}} \tag{51}$$

where $V_{link,max}$ is the maximum voltage the DC link capacitor has to charge, equal to V_{dcl}. $V_{BD,D2}$ and $V_{BD,S1}$ is the breakdown voltage of diode D_1 and switch S_1 respectively. σ_{S1} and σ_{D1} is the margin factor which is less than 1 has been considered for maintaining $V_{S1,max}$ less than $V_{BD,S1}$ and $V_{D_1,max}$ less than $V_{BD,D2}$ respectively.

3) Parametric values of HV pulse generator

The specification of a typical water treatment application is shown in Table 6. Table 7 gives the design guideline of the pre-PS and the post-PS parameters. Referring to the equations in Table 7, the post-PS parameters are designed and are shown in Table 8. The maximum voltage stress across the switches S_2 and S_3 is the maximum DC link voltage ($V_{C_{1,max}}$); hence switches with breakdown voltage greater than 189.16 V is selected. The core of the inductors (L_1, L_2) and the transformer core are selected based on the area product. The capacitors (C_1 and C_{link}) are selected based on the voltage stress seen across them. Table 9 shows the details of the component used in the post-PS.

Similarly, referring to the equations in Table 7, the pre-PS parameters are designed and are shown in Table

TABLE 7. Design guidelines using the energy-based Analysis

Rating	Parameter	Ref. Eqn.	Description
Post-PS	E_{C_o}	Eqn. (2)	Load capacitor energy
	ΔE_{C_1}	Eqn. (7)	Change in energy discharged by C_1
	$V'_{dcl,new}$	Eqn. (9)	Change in V'_{dcl} due change in peak output voltage
Pre-PS	$I_{pk,f(min)}$	Eqn. (15)	Minimum peak current of L_{mf}
	$T_{chrg,f}$	Eqn. (16)	Charging time of C_{link}
	$I_{pf,f}$	Eqn. (22)	Operated peak current of L_{mf}
	N	Eqn. (31)	Number of charging cycles to charge C_{link}
	Δv_{link}	Eqn. (34)	Increment in voltage per switching cycle

TABLE 8. Designed values of the post-PS

Resonant inductance (L_1)	35 μH
Resonant capacitance (C_1)	0.3 μF
Inductance (L_1)	1 mH
Maximum resonant capacitor voltage ($V_{C_{1,max}}$)	189.16 V
Turns ratio (n_r)	20
Switch S_3 turn-on time ($T_{on,3}$)	12.5 μs
Switching frequency of switch S_3	1000 Hz
Maximum DC link voltage (V_{dcl})	120 V
Leakage inductance of transformer (L_{lkr})	70 μH
Winding capacitance of transformer (C_{wd})	85 pF

TABLE 9. Details of component used in post-PS

Description	Component
MOSFETs S_2 and S_3	AIMW120R080M1XKSA1 (SiC, 1200 V)
Inductor L_1	ETD 49/25/16 (TDK)
Xmer core with sectioned bobbin	URR 59/36/17 (TDK)
DC link capacitor C_{link}	4 x R76QR3220SE30K
Resonant inductor L_2	PQ 32/30 (TDK)
Resonant capacitance C_1	3 x R413N310050T0K

10. The maximum voltage stress across switch S_1 is $V_{dc} + \frac{V_{dcl}}{n_f}$; hence switch S_1 is selected with the breakdown voltage greater than 36 V. The maximum voltage stress across the diode D_1 is $n_f V_{dc} + V_{dcl}$; hence diode D_1 is selected with the breakdown voltage greater than 180 V. The transformer core for the flyback converter is selected based on the area product of the core. Table 11 shows the details of the component used in the pre-PS.

TABLE 10. Designed values of the pre-PS

Magnetizing inductance (L_{m_f})	102 μH
Peak current ($I_{pk,f}$)	2 A
Turns ratio (n_f)	5
Input voltage (V_{dc})	12 V
Leakage inductance of transformer (L_{lkf})	747 nH
Winding capacitance of Transformer (C_w)	19 pF

TABLE 11. Details of component used in pre-processing stage

Description	Component
MOSFETs S_1	FDS2672
Diode D_1	GAP3SLT33-214
Transformer core	E 30/15/7

V. CONTROL METHODOLOGY AND IMPLEMENTATION

The control parameters $I_{pk,f}$ and $T_{on,S3}$ obtained in Fig. 17 are utilized for control implementation, detailed in this section.

A. CONTROL STAGE DESIGN OF THE POWER PROCESSING UNIT

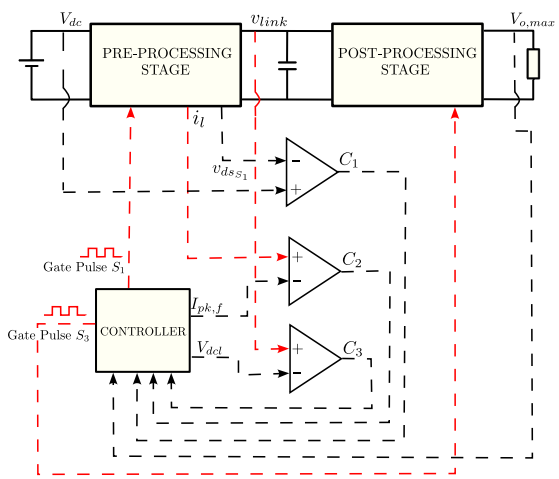


FIGURE 18. Control scheme of the of the HV pulse generator

The control scheme for the power processing unit is shown in Fig. 18 and is detailed as follows:

1) The maximum output voltage ($V_{o,max}$) is sensed and taken to the controller. For the sensed $V_{o,max}$, the controller then generates the maximum DC link capacitor voltage reference (V_{dcl}) and a peak current reference (I_{pk}) for the switch S_1, such that the charging time does not exceed $T_{pulse} - T_{pw}$ and the power of the pre-PS doesn't exceed 150 W.
2) The controller generates the gating pulse for switch S_3 (refer to Fig. 19) according to the desired pulse width and ensures ZCS turn-off of switch S_3.

3) Three high speed comparators are used where comparator C_1 compares the switch S_1 drain to source voltage (v_{S1}) with the input voltage V_{dc} and a trigger pulse is generated when v_{S1} goes less than V_{dc}. This trigger pulse is delayed by the controller and given to switch S_1, ensuring MVP and ZVS turn-on of S_1.
4) Comparator C_2 compares the current through the magnetising inductance (i_l) with the reference peak current (I_{pk}) set by the controller and a trigger pulse is generated when i_l is greater than the set I_{pk}. This trigger pulse is taken into the controller and given to switch S_1, ensuring PCMC turn-off of switch S_1.
5) Comparator C_3 compares the DC link voltage (v_{link}) with the reference maximum DC link voltage (V_{dcl}) set by the controller and a trigger pulse is generated when v_{link} goes higher than set V_{dcl}. This trigger pulse is used to disable the DC link capacitor voltage charging, ensuring a constant voltage seen at the input of the post-PS.

The ZCS turn-off of switch S_3, and the ZVS turn-on of switch S_1 make the HV pulse generator more efficient.

B. CONTROL ALGORITHM

The MVP with constant PCMC of an HV flyback converter is a variable frequency switching scheme [44]. Fig. 19 shows the control algorithm of the of HV pulse generator. In the control stage, the peak current ($I_{pk,f}$), drain to source voltage of switch S_1 and v_{link} is compared with the set reference values, and given to modulator which generates the gating pulses for switch S_1. The gating pulse for switch S_3 is derived by determining $T_{on,S3}$ during the design stage and along with F_{pulse}, is then forwarded to the modulator.

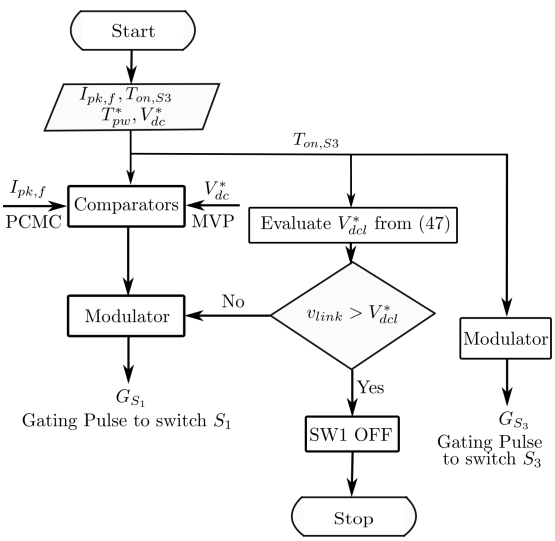


FIGURE 19. Control algorithm of the HV pulse generator

VI. ENERGY-BASED ANALYSIS VALIDATION

The essential parameters of the HV pulse generator are designed in the above section, and the analysis is verified through simulation results.

A. CONSTRAINT ON CHARGING AND MINIMUM PEAK CURRENT THROUGH THE MAGNETISING INDUCTANCE IN PRE-PS

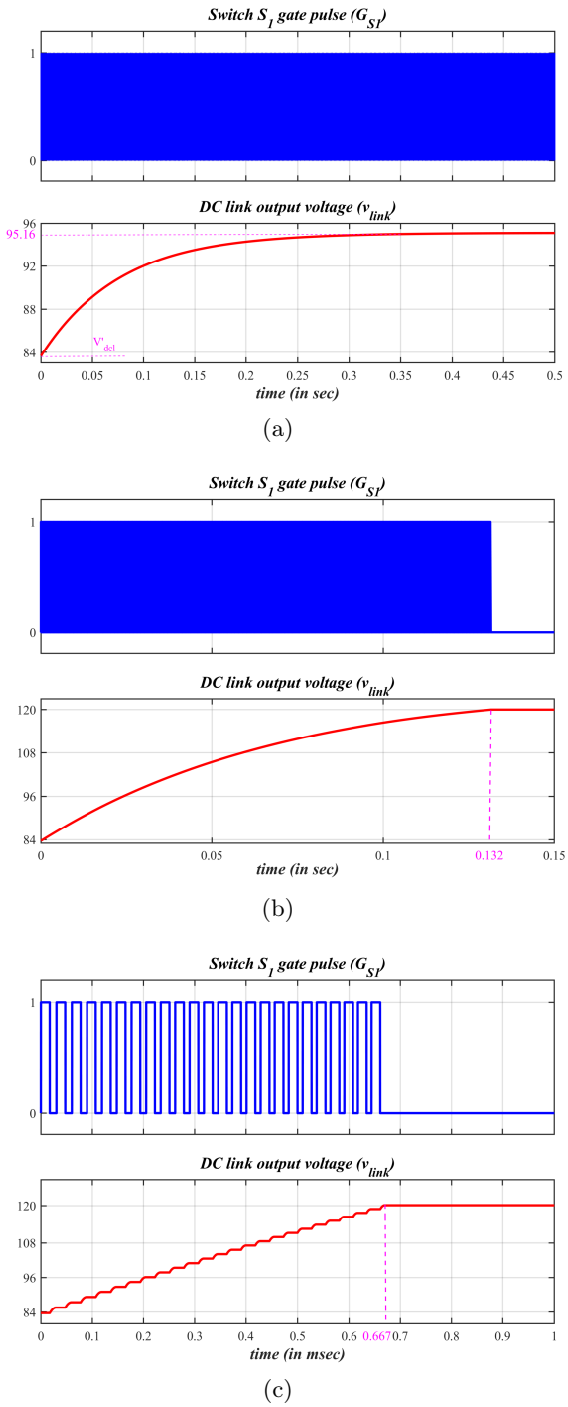


FIGURE 20. Simulation results of pre-PS (a) $I_{pk,f} < I_{pk,f(min)}$ (b) $I_{pk,f} = I_{pk,f(min)}$ (c) $I_{pk,f} > I_{pk,f(min)}$

TABLE 12. Comparative analysis for different peak current levels in the pre-PS

Figure	$I_{pk,f}$	Peak Current Constraint	V_{dcl}	$T_{chrg,f}$	Charging Time Constraint	Peak Power (P_{pk})	Observations
Fig. 20(a)	30 mA	$I_{pk,f} < I_{pk,f(min)}$	95.16 V	0.36 s	$T_{chrg,f} > T_{chrg,f(max)}$	20.36 mW	The pre-PS neither able to charge V_{dcl} to the desired voltage (i.e. 120 V) nor meet the charging time constraint
Fig. 20(b)	44.85 mA	$I_{pk,f} = I_{pk,f(min)}$	120 V	0.132 s	$T_{chrg,f} > T_{chrg,f(max)}$	88.63 mW	The pre-PS is able to charge V_{dcl} to the desired voltage but not able to meet the charging time constraint
Fig. 20(c)	2 A	$I_{pk,f} > I_{pk,f(min)}$	120 V	0.667 ms	$T_{chrg,f} < T_{chrg,f(max)}$	20.54 W	The pre-PS is able to charge V_{dcl} to the desired voltage and also able to meet the charging time constraint. P_{pk} is less than $P_{pk,max}$ (150 W). $I_{pk,f}$ is obtained from (22)

The maximum achievable DC link capacitor voltage (V_{dcl}) in the pre-PS is limited by the parasitic capacitance (refer Fig. 15); hence the minimum peak current through the magnetising inductance required to achieve the desired DC link voltage is obtained in (15).

From the designed values in Table 10 and the desired V_{dcl}, the minimum peak current through the magnetising inductance to charge the DC link capacitor from V'_{dcl} to V_{dcl} is obtained as 44.85 mA. The maximum allowable charging time ($T_{chrg,f(max)}$) is obtained from (17) and is less than 0.985 ms. Table 12 shows the comparative analysis of choosing $I_{pk,f} < I_{pk,f(min)}$, $I_{pk,f} = I_{pk,f(min)}$ and $I_{pk,f} > I_{pk,f(min)}$.

B. PREDICTING THE NUMBER OF CHARGING CYCLES TO CHARGE THE DC LINK CAPACITOR IN PRE-PS

The HV flyback converter is subjected to a peak current of $I_{pk,f} = 2$ A, which corresponds to $E_{L_{mf}}$ of 204 µJ per cycle. The DC link capacitor demands an energy of 4.81 mJ to charge from V'_{dcl} to V_{dcl}. The energy delivered to the load decreases due to the energy demanded by the parasitic capacitance increases in every cycle. The number of charging cycles required to reach the desired DC link capacitor voltage is given in (31). Hence,

$$N = \frac{\log\left(\frac{\frac{E_{in}}{q-1} - E_{C_{link(x)}}}{\frac{E_{in}}{q-1} - E_{C_{link(x+N)}}}\right)}{\log(q)} = 24 \qquad (52)$$

Fig. 21 shows the simulation result of the DC link capacitor voltage charged to 120 V, and a counter is implemented to count the number of charging cycles. The counter is incremented with every rising edge of the gate pulses to switch S_1, and each counter step corresponds to 1 charging cycle. As v_{link} reaches 120 V, the counter indicates 24 charging cycles, thus matching the analytical results obtained in (52).

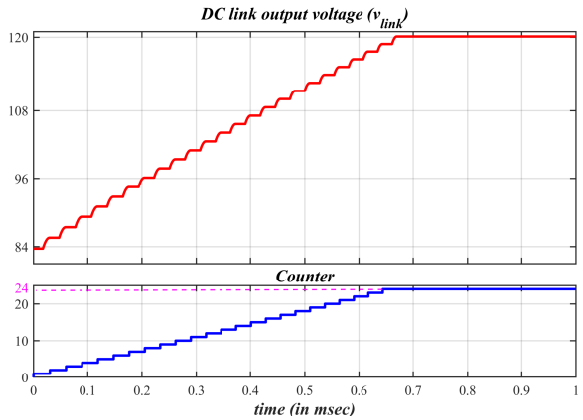


FIGURE 21. Simulation results DC link capacitor voltage charged to 120 V **and number of charging cycles with** $I_{pk,f} = 2$ A

C. PEAK POWER CONSTRAINT IN THE PRE-PS DUE TO CHANGE IN PEAK PULSE VOLTAGE

From the flow chart (shown in Fig. 17), during the design stage, if $P_{pk} > P_{pk,max}$ the $T_{chrg,f}$ is increased till the peak power (P_{pk}) becomes less than $P_{pk,max}$. But when $P_{pk} > P_{pk,max}$ and $T_{chrg,f} > T_{chrg(max)}$, the desired $V_{o,max}$ can't be achieved as the maximum power the pre-PS is limited to $P_{pk,max}$ (in this case, it is 150 W). If an application demands power more than $P_{pk,max}$, the flyback converter is not a preferred choice, but high power converters topologies like bridge converters could be used as a pre-PS [45].

VII. SIMULATION AND EXPERIMENTAL RESULTS

The HV pulse generator for water treatment applications is simulated for the specification shown in Table 6. The HV pulse generator is simulated using SIMULINK software, and the results are discussed in the below subsections.

A. SIMULATION RESULTS

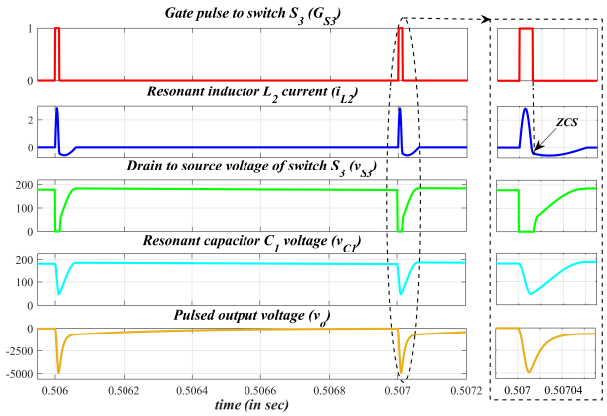


FIGURE 22. Simulation results for the HV pulse generator

Fig. 22 shows the HV pulse generator simulation results. During the turn-on of switch S_3, the output voltage reaches $-5\,\text{kV}$, and the voltage across the resonant capacitor (v_{C_1}) falls from 189.16 V to 69.31 V. The switch S_3 turns off at ZCS, which is an added advantage in the resonant circuit. After switch S_3 turns off, the voltage across the resonant capacitor charges again to $V_{C_{1,\max}}$.

The DC link capacitor discharges its energy to inductor L_1 and resonant capacitor C_1 during the interval $t_{0,r}$ to $t_{3,r}$. The HV flyback converter is operated continuously till the voltage across the DC link capacitor charges back to V_{dcl} as per the design. Fig. 23 shows the waveforms of the magnetising inductance of the flyback converter and the charging of the DC link capacitor. A peak current of 2 A through the magnetising inductance of the HV flyback converter is maintained constant throughout the charging process in order to charge the DC link capacitor well within the charging time ($T_{chrg,f}$).

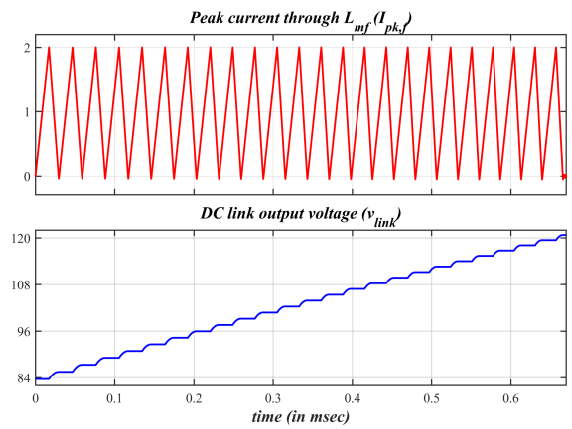


FIGURE 23. Simulation results for charging of the DC link capacitor voltage by the flyback converter

Fig. 24 shows the output voltage waveform and the enlarged view of a certain portion of it. It can be observed that the FWHM or the pulse width is 15 μs. The time the output voltage takes to reach the peak of the pulse is 11 μs, which is the rising time of the pulse.

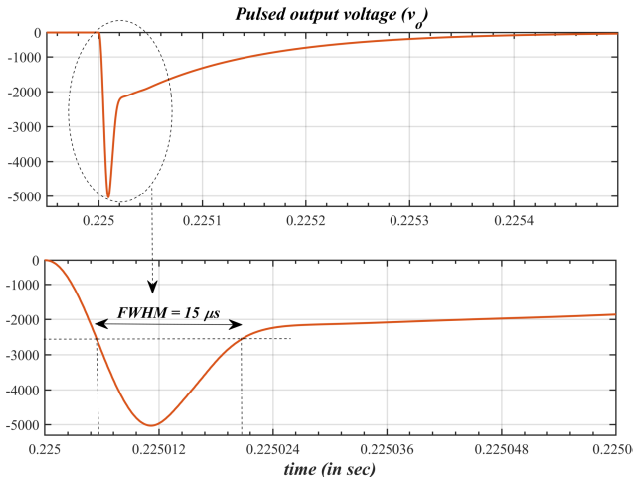


FIGURE 24. Output voltage waveform

Fig. 25 shows the programmable capability of the HV pulse generator. The output voltage changes from $-5\,\text{kV}$ to $-4\,\text{kV}$ with a step change in v_{link} from 120 V to 96 V. Similarly, programmability in the output voltage profile from $-5\,\text{kV}$ to $-2.5\,\text{kV}$ is achieved by changing v_{link}. When v_{link} changes from 120 V to 60 V, v_o takes a single cycle of PRR to achieve the desired pulsed voltage. But when v_{link} changes from 60 V to 120 V, v_o takes 3 to 4 cycles of the PRR to achieve the desired pulsed voltage. This is due to when v_o changes from $-5\,\text{kV}$ to $-2.5\,\text{kV}$, the DC link capacitor is charged to sufficient voltage (i.e. 120 V) such that it can discharge and take care of these transients, but when v_o changes from $-2.5\,\text{kV}$ to $-5\,\text{kV}$, the DC link capacitor requires some cycles to charge to the required voltage.

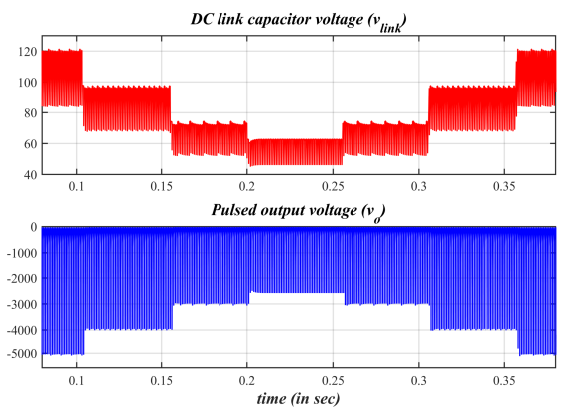


FIGURE 25. Simulation results of programmable pulsed output voltage from $-5\,\text{kV}$ to $-2.5\,\text{kV}$

B. EXPERIMENTAL RESULTS

The HV pulse generator prototype is built and is shown in Fig. 26. The gating signals for switches and MVP switching scheme with constant PCMC are implemented using the Altera MAX V CPLD board. The pre-PS and post-PS blocks in Fig. 2, are distinguished by blue and pink boxes, respectively in the experimental prototype shown in Fig. 26.

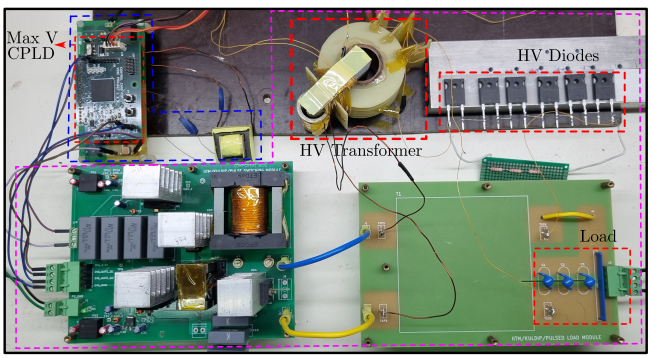
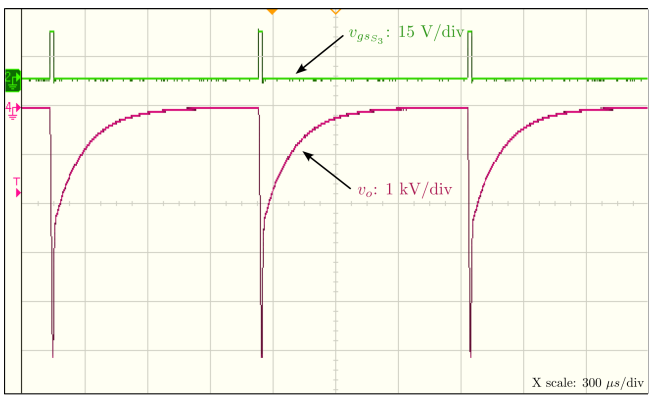
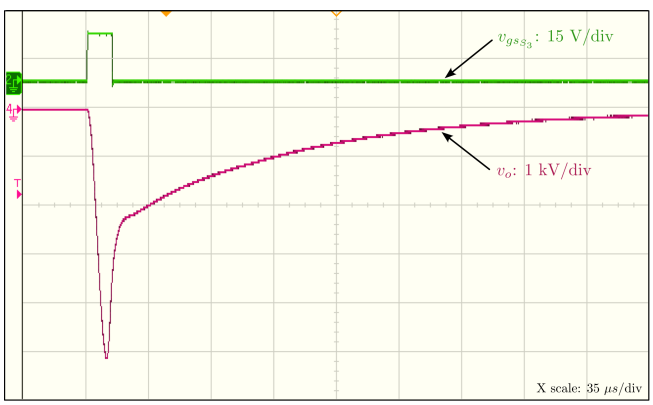


FIGURE 26. Experimental prototype of HV pulse generator

1) Results of the post-PS



(a)

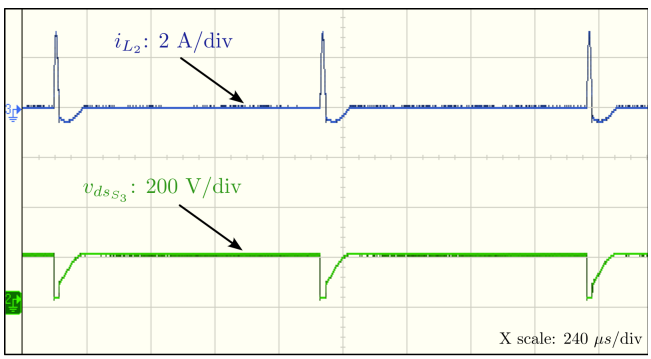


(b)

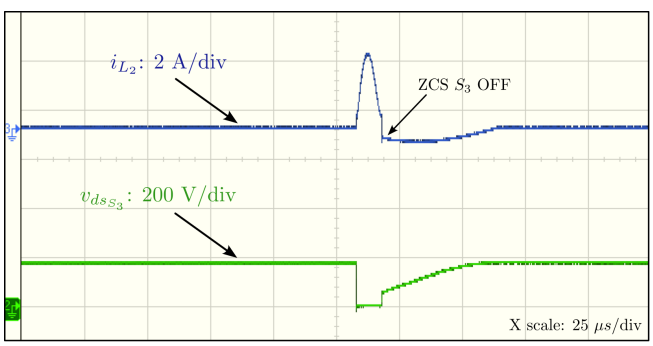
FIGURE 27. Experimental results of HV pulse generator (a) S_3 gate pulse and output voltage (b) enlarged experimental results of the same

Fig. 27(a) shows the pulsed output of −5 kV with PRR of 1000 Hz and the gate pulse S_3. Fig. 27(b) shows the enlarged view, and it is seen that the turn-on time of switch S_3 is 12.5 µs and the FWHM of the output voltage is 15 µs. In the post-PS, as depicted in Fig. 27(b), with the turn-off of switch S3 gate pulse, the time constant of the decaying pulse output voltage changes evidenced by the analytical results present in Fig. 11.

Fig. 28(a) shows the drain to source voltage for switch S_3 and the resonant current, and Fig. 28(b) shows the enlarged view of it. ZCS turn-off of switch S_3 is observed, which is advantageous in the HV pulse generator. In Fig 28(b), the switch S3 is turned off during the negative switch current, indicating ZCS turn off of switch S3 observed in the analytical results present in Fig. 11.



(a)



(b)

FIGURE 28. Experimental results of HV pulse generator (a) drain to source voltage of S_3 and resonant current (b) enlarged experimental results of the same

Fig. 29 shows the voltage across the resonant capacitor. It is seen that the voltage across C_1 reduces when the pulsed output voltage is obtained and it is charged again to 189.16 V by the DC link capacitor within the turn-off period of switch S_3. The voltage across the resonant capacitor falls with the rise in output pulse voltage. Subsequently, the resonant capacitor is charged by the DC link capacitor, as seen in the analytical results presented in Fig. 13 and Fig. 14.

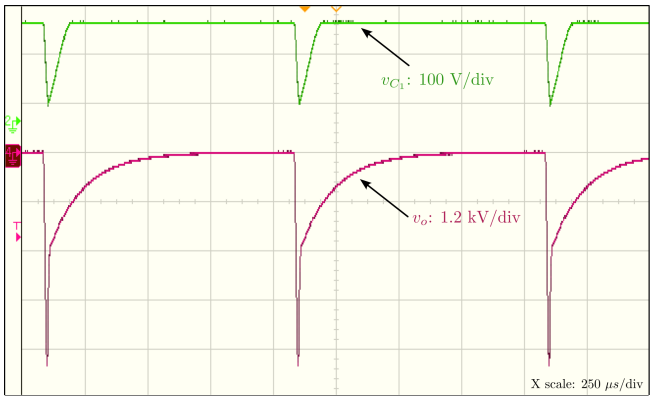


FIGURE 29. Experimental results of HV pulse generator resonant capacitor voltage and output voltage

2) Results of the pre-PS

Fig. 30 shows the HV flyback converter's experimental results for charging the DC link capacitor. The charging of the DC link capacitor to 120 V is ensured by MVP switching scheme with PCMC of pre-PS. In Fig. 30, each gate pulse of switch S1, causes the output capacitor to increase until it reaches the desired value, as depicted from Fig. 8.

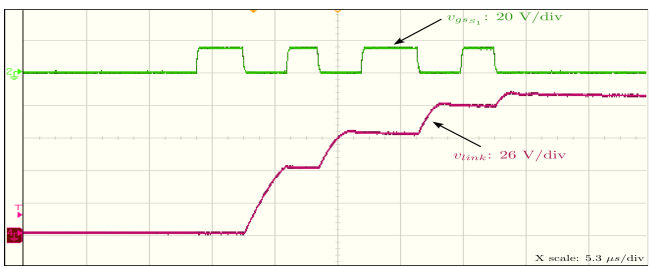


FIGURE 30. Experimental results of S_1 gate pulse and the charging of DC link capacitor

The hardware results match the simulation results for the desired specifications of the water treatment application, ensuring the charging of pre-PS within the desired charging time and not exceeding the pre-PS peak power rating.

VIII. CONCLUSION

An energy-based analysis of a flyback converter in the pre-PS and a resonant converter in the post-PS for an HV pulse generator in ozonization-based water treatment applications is presented in this paper. Drawing insights from the pulse load profile, an energy-based analysis and control scheme for the pre-PS and the post-PS is proposed in this paper, exploring the potential usage of the flyback converter-based pulse generator for water treatment applications. The energy-based analysis aids in deriving the essential parameters and reference peak current in the design stage, ensuring the desired pulsed voltage profile adhering to specified charging time and pulse width, steady-state gain and limited voltage overshoots/undershoots. The MVP switching scheme with PCMC and ZCS turn-off of the resonant switch ensures higher efficiency and improved charging time of the converter. The proposed analysis and the control scheme are verified experimentally for a pulse load of −5 kV with a pulse repetitive rate of 1000 Hz and pulse width of 15 µs fed from an input voltage of 12 V DC. The energy-based analysis is valid for a flyback-based pulse power converter, which can cater to a load requirement of less than 150 W. For power exceeding 150 W, exploring energy-based analyses for high-power converter topologies could be a promising avenue for future investigation.

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