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High step-up ZVT Converter Based on Active switched Coupled inductors

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ABSTRACT To meet the requirements of high voltage boosting and high efficiency, a novel high step-up zero voltage transition (ZVT) DC/DC converter based on active switched-inductor (ASL) is proposed. This converter combines ASL and coupled inductor structure, thus can reduce the voltage and current stress of power switch, and the active clamping technology provides zero voltage transition (ZVT) for all switches. The coupled inductors can realize relatively high voltage gain with appropriate turns ratio while all magnetic components can be integrated in one core. In addition, thanks to the leakage inductance, the reverse recovery problem of diodes is resolved. The working principle of the proposed converter is analyzed in detail, also the characteristics including voltage gain, the condition of ZVT is discussed. Then, a family of derived converters are listed and compared to each other. According to the proposed converter, a 500W prototype with 100kHz switching frequency is established in the lab, and the experimental results are given to verify the analysis.

INDEX TERMS High step-up voltage gain; Active switched-coupled inductor; ASL; Coupled inductor; Zero voltage transition

I. INTRODUCTION

Because of environmental problems, new clean energy sources have been developed rapidly. However, for some new energy power system such as fuel cell and photovoltaic, the output voltage of are relatively low. In order to inject these powers into the grid or fed to local loads, it is necessary to convert low voltage DC into high level DC voltage [1]. It is hard to achieve high voltage conversion ratio and high efficiency at the same time with the traditional boost converter, therefore high-step-up DC/DC converters have been widely used [2].

In applications where galvanic isolation is not necessary, non-isolated DC/DC converter is preferred. Most of high step-up converters are derived from Boost converter [3-7]. A high step-up converter with two or more boost converter cascaded in series is given in [8], these kinds of converters are called cascaded boost converter or quadratic boost converter, the disadvantages of them are too many components and complex structure, which causes low efficiency. Boosting units are usually used as another method, including the switched-inductor (SL), switched-capacitor (SC). The voltage gain can be extended to one or more times by single or multi-stage SL and SC units [9-12]. However, more diodes are utilized in SL or SC and conducts high current in high step-up applications, thus decreases the efficiency. Boost converter with coupled inductor can raise the voltage gain easily by increase the turns ratio [13-17], also the reverse-recovery problem of the diodes is partly solved due to the leakage inductor.

Compare to conventional boost converter, a dual switches converter with active switched-inductor (ASL) unit was proposed in [18]. ASL converter has a higher voltage gain and lower voltage and current stress on the components compared to Boost converter. The inductors operate in parallel charge and series discharge without additional diodes, thus ASL converter have simpler structure and fewer components compared to previous converters. Various voltage boosting unit has been utilized in ASL converter. Two kinds of improved ASL converters with SC to achieve higher gain have also been developed [18-19], but they only suitable for low power applications because of the inrush current introduced by SC.

Coupled inductor is also utilized in ASL converters widely. A basic ASL converter combined with switched

inductor units and coupled inductors has been introduced in [20], by replacing the inductors with SLs and coupled inductors, the voltage gain of converter is greatly increased, in addition, the current ripple is also reduced, however, a number of components and hard switching make the efficiency performance not good. A quasi-active switched coupled inductors(Q-AS-CL) converter has been presented in [21], the primary sides of two coupled inductors operate in parallel connection and charged by the input source, when the switches are OFF, the secondary sides of two coupled inductors operate in series connection and discharged to the load with the input source together, which can provide a high gain with low voltage stress of the power switches. However, these researches on ASL converters are all focused on hard switching topologies which go against the development of high efficiency converter, soft switching ASL converter is still need to be developed.

In this paper, a family of novel high step-up converters based on the active switched-coupled inductor (AS-CL) is given. The structure of ASL decrease the current stress on the switches during charging time interval. The winding in primary side is divided into two windings in two arm, so the current flowing through windings is low, which is beneficial to couple inductors. The magnetic component is simplified by coupling all the windings in one core, which brings advantages like reducing the volume of the converter and enlarging power density. The active clamping is utilized to achieve zero voltage transition (ZVT) for all switches. Moreover, the reverse-recovery problem of the output diodes can be alleviated by the leakage inductance.

This paper is outlined as follows. Operation principle is explained in Section II. External characteristics and soft-switching conditions are derived in Section III. A family of AS-CL and coupled-inductor converters are listed in Section IV. A proof of experimental prototype rated at 500 W is built and tested in the laboratory and results are demonstrated in Section V to show the converter performance.

II. OPRATION PRINCIPLE

As shown in Fig.1, an active switched-inductor(ASL) high-step-up DC/DC converter with coupled inductors has been presented. The converter realizes zero voltage transition(ZVT) by the active clamping switches S_3 and S_4, high voltage gain can be get by changing the turns N_2, coupled inductors simplify the structure by using one core.

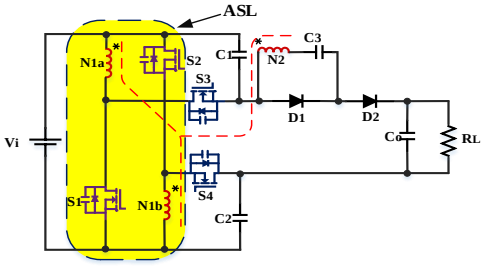

FIGURE 1. The proposed converter

In order to facilitate the analysis, all the components are supposed to be ideal:

1) the input voltage V_i, output voltage V_o are constant;

2) The switching signal of the power switches are exactly synchronous;

3) the capacitances of switches are ignored, and the diodes are ideal.

4) n_{1a} is exactly the same as n_{1b}, n_{1a}: n_{1b}: n_2=1:1: n.

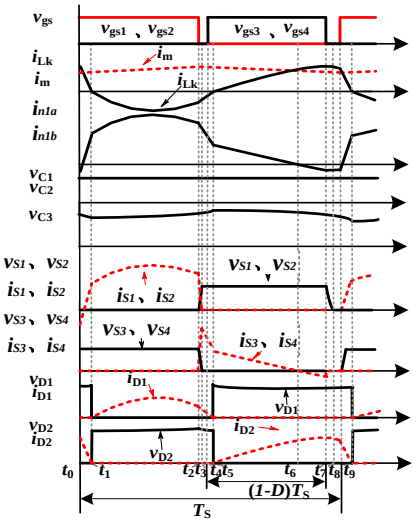

FIGURE 2. Operation waveforms of the proposed converter

Define the turns ratio as 1:1: n, according to key waveforms and equivalent circuits shown in Figs. 2&3, operation modes are analyzed as follows:

1) Mode 1: [t_0~t_1] As shown in Fig.3(a), during this time interval, S_1, S_2 turned on, inductors in primary side N_{1a} and N_{1b} are charged in parallel, the current through N_{1a} and N_{1b} is increasing, since the body diodes turned on before t_0, S_1 and S_2 turned to conducted with ZVS. The capacitor C_3 and the leakage inductor L_k are in resonance state until the leakage inductor current i_{Lk} reduced to zero.

$$\begin{cases} V_{N1a} = V_{N1b} = V_i \\ V_{C3} = nV_{N1a} = nV_i \end{cases} \tag{1}$$

2) Mode 2: [t_1~t_2] As shown in Fig.3(b), there are still current flowed through S_1 and S_2. At t_1, i_{Lk} reduced to zero, D_2 turned off to be reverse-braised, the leakage inductor solved the reverse-recovery problem by absorbing the energy. From t_1 to t_3, the state equation can be expressed as:

$$\begin{cases} L_k \dfrac{di_{Lk}}{dt} = v_{C3} - nV_i \\ C_3 \dfrac{dv_{C3}}{dt} = -i_{Lk} \end{cases} \tag{2}$$

From (1), i_{Lk} and v_{c3} can be derived as follows:

$$\begin{cases} i_{Lk} = \dfrac{v_{C3}(t_1) - nV_i}{Z_r} \sin \omega_r (t - t_1) \\ v_{C3} = -nV_i + [nV_i - v_{C3}(t_1)] \sin \omega_r (t - t_1) \end{cases} \tag{3}$$

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Where Z_r and ω_r are defined as: $Z_r = \sqrt{L_k / C_3}$, $\omega_r = \sqrt{1/L_k C_3}$.

3) Mode 3: [t_2-t_3] The equivalence circuit is shown in Fig.3(c), at the time of t_2, S_1 and S_2 turned off. And i_{n1a}、i_{n1b}, the current flow through N_{1a} and N_{1b} and charges the parasitic capacitors C_{S1}, C_{S2}, at the same time, the parasitic capacitors C_{S3}, C_{S4} are discharging. The voltage across S_3 and S_4 start to decrease, this time interval lasts until the V_{S3} and V_{S4} decreased to zero.

4) Mode 4: [t_3-t_4] The equivalence circuit is shown in Fig.3(d), at the time of t_4, the body diode of the switches S_3 and S_4 start to conduct, the current i_{n1a} and i_{n1b} charge the capacitors C_1 and C_2 respectively.

$$\begin{cases} V_{C1} = V_{N1a} \\ V_{C2} = V_{N1b} \end{cases} \tag{4}$$

5) Mode 5: [t_4-t_5] The equivalence circuit is shown in Fig.3(e), at the time of t_4, considering the body diodes are conducted, S_3 and S_4 turned on with ZVT. the current i_{n1} and i_{n2} keep charge the capacitor C_1 and C_2 respectively. This time interval lasts until i_{Lk} increases to zero,

6) Mode 6: [t_5-t_6] The equivalence circuit is shown in Fig.3(f), at the time of t_5, i_{Lk} equals to 0, and the reverse recovery problem of D_1 is partly solved due to the leakage inductor. L_k and C_3 are in the resonance state, the equations can be written as:

$$\begin{cases} L_k \dfrac{di_{Lk}}{dt} = nV_{C1} + V_i + V_{C1} + V_{C2} + v_{C3} - V_o \\ C_3 \dfrac{dv_{C3}}{dt} = -i_{Lk} \end{cases} \tag{5}$$

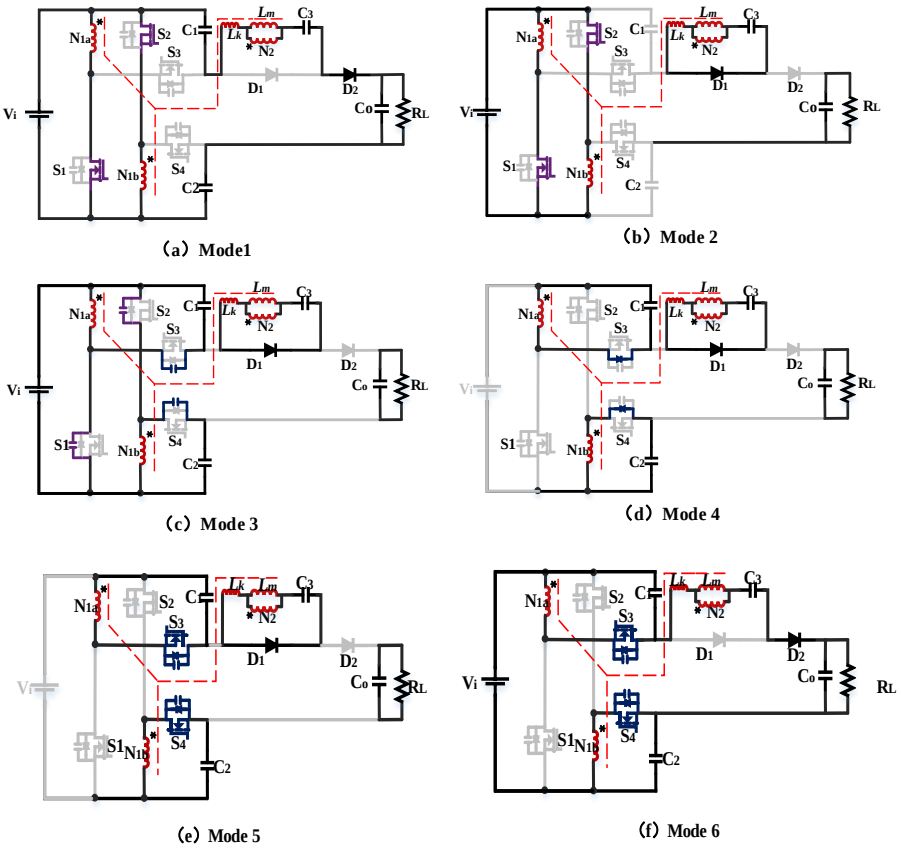
Simplified (3):

$$\begin{cases} i_{Lk} = \dfrac{(n+1)V_{C1} + V_i + V_{C2} + v_{C3}(t_4) - V_o}{Z_r} \sin \omega_r (t - t_5) \\ v_{C3} = [(n+1)V_{C1} + V_i + V_{C2} - V_o] - [(n+1)V_{C1} + V_i \\ \quad + V_{C2} + v_{C3}(t_4) - V_o] \sin \omega_r (t - t_5) \end{cases} \tag{6}$$

7) Mode 7: [t_6-t_7] The equivalence circuit is shown in Fig. 3(g), at the time of t_6, in1a and in1b decreased to 0 and then start to be reversed, i_{Lk} and v_{C3} still can be express as (6).

8) Mode 8: [t_7-t_8] The equivalence circuit is shown in Fig.3(h), at the time of t_7, S_3 and S_4 turn off, i_{n1a} and i_{n1b} go on decreasing, the energy stores in the all parasitic capacitor.

9) Mode 9: [t_8-t_9] The equivalence circuit is shown in Fig.3 (i), at the time of t_8, the voltage across S_1 and S_2 decreased to 0, then the body diodes start to conduct.



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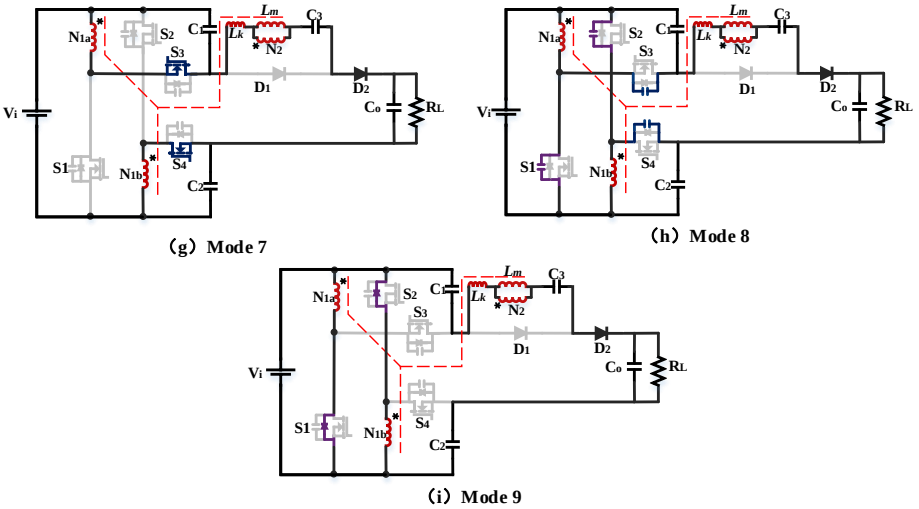

FIGURE 3. Equivalence circuit of the proposed converter

III. CIRCUIT PERFORMANCE ANALYSIS

A. EXTERNAL CHARACTERISTICS

In the ideal condition, the inductors are perfectly coupled, the leakage inductance is assumed to be zero, the operation mode can be divided into two modes according to the state of the switches S_1 and S_2.

While the switches S_1 and S_2 are on, the magnetizing inductor is charged:

$$V_{N1a} = V_{N1b} = V_i \tag{7}$$

According to the voltage-second balance on the N_{1a} and N_{1b}, their relation with V_i can be expressed as:

$$\begin{cases} V_{C1} = \dfrac{1}{1-D}V_i - V_i = \dfrac{D}{1-D}V_i \\ V_{C2} = \dfrac{D}{1-D}V_i \end{cases} \tag{8}$$

According to the turn ratio 1:1: n, we can get:

$$V_{C3} = nV_i \tag{9}$$

While the switches S_1 and S_2 are off, the magnetic inductor L_m is demagnetized, the voltage across the L_m is:

$$V_{Lm} = V_i + V_{C1} + V_{C2} + V_{C3} - V_o = 2 \cdot \frac{1+D}{1-D}V_i + nV_i + V_i - V_o \tag{10}$$

From formulas (7) and (10), the voltage gain in ideal condition is:

$$G_{ideal} = \frac{V_o}{V_i} = \frac{1+n+D}{1-D} \tag{11}$$

The leakage inductance will cause loss of duty cycle, which will affect the voltage gain. In order to simplify the calculation, according to the switching on and off of the switches S_1 and S_2, there are only two operation modes, and the main waveforms are shown in fig. 4.

During the time interval [t_0-t_2], S_1, S_2, and D_1 are conducted, while S_3, S_4 and D_2 are reverse-biased, considering the average current of the capacitor is zero, the peak current of D_1 is:

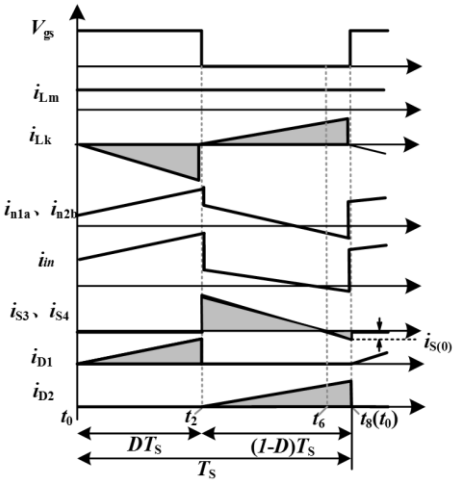

FIGURE 4. Simplified waveforms of the proposed converter

$$i_{peak\text{-}D1} = \frac{2I_o}{D} \tag{12}$$

The voltage across L_k during the time stage [t_0-t_2] can be expressed as：

$$V_{Lk(0\text{-}2)} = L_k \frac{-i_{peak\text{-}D3} - 0}{DT_s} = -\frac{2L_k I_o f_s}{D^2} \tag{13}$$

C_3 is the charge pump capacitor, the operating frequency is lower than the resonant frequency. According to formulas (6) and (11), the voltage across the capacitor C_3 can be expressed as:

$$V'_{C3} = nV_i - \frac{2L_k I_o f_s}{D^2} \tag{14}$$

During the time stage [t_2-t_8], S_1, S_2 and D_1 are turned off, while S_3, S_4 and D_2 are on, the peak current of D_2 is:

$$i_{peak\text{-}D2} = \frac{2I_o}{1-D} \tag{15}$$

According to (15), the voltage across the leakage inductor during [t_2-t_8] is:

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$$V_{Lk(2\text{-}8)}=L_k\frac{i_{peak\text{-}D2}-0}{(1-D)T_s}=\frac{2L_kI_of_s}{(1-D)^2} \quad (16)$$

According to (16), the expression of the output voltage can be deduced:

$$V_o=V_i+V_{C1}+V_{C2}+V'_{C3}+nV_{C1}-V_{Lk(2\text{-}8)} \quad (17)$$

Defined $\tau=\frac{L_kf_s}{R_L}$, combined (14) and (17):

$$V'_o=\frac{1+n+D}{1-D}\cdot\frac{1}{1+2\tau/D^2+2\tau/(1-D)^2} \quad (18)$$

The selection all capacitors are based on current ripple, according to ΔQ=CΔV=IΔt, the all capacitors selection equations can be derived as

$$C_1=C_2>\frac{I_{in}(1-D)}{2f_s\Delta V_{C1}} \quad (19)$$

$$C_3>\frac{I_o(1-D)}{f_s\Delta V_{C3}} \quad (20)$$

$$C_o>\frac{I_o(1-D)}{f_s\Delta Vo} \quad (21)$$

In the condition that the output power is 500W, the output voltage is 400V and the switching frequency is 100kHz, the voltage gain will change due to the change of leakage inductance and turn ratio, as shown in Fig. 5. With the increase of leakage inductance and turn ratio, the voltage gain keeps decreasing.

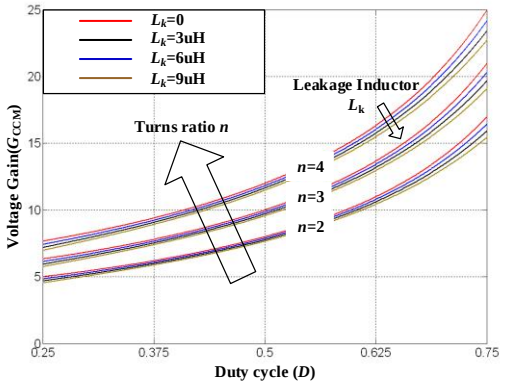

FIGURE 5. The Effects of leakage inductance on voltage gain

B. THE CONDITION OF ZVT FOR THE SWITCHES

In order to realize ZVT of S_1 and S_2, the circuit meets two conditions: firstly, the leakage inductor stores enough energy at the turn-off transition to ensure the charging and discharging of the parasitic capacitance(C_s) of S_1 and S_2; secondly, sufficient dead time interval is needed for charging and discharging C_s.

During the very short time interval [t_6-t_7], the magnetizing current can be treated as constant because that the magnetizing inductor L_m is large. Thus, the stored energy in the leakage inductor should satisfy:

$$\frac{1}{2}\cdot\frac{L_k}{n^2}\cdot\frac{n^2}{4}\cdot[\frac{2I_o}{1-D}-\frac{4I_o}{N(1-D)}]^2\geq\frac{1}{2}C_s(\frac{V_i}{1-D})^2 \quad (22)$$

From (19), the leakage inductor L_k should satisfy:

$$L_k\geq\frac{C_sV_i^2}{I_o^2(1-\frac{2}{N})^2} \quad (23)$$

In order to achieving ZVT of S_1 and S_2, the dead time should satisfy:

$$t_8-t_6\geq\frac{\frac{C_sV_i}{1-D}}{\frac{n^2}{4}\cdot[\frac{2I_o}{1-D}-\frac{4I_o}{n(1-D)}]^2}=\frac{C_sV_i(1-D)}{I_o^2(n-2)^2} \quad (24)$$

In the condition that the input voltage is 40V, parasitic capacitance is 300pF. Fig. 6 shows the relationship between leakage inductance, turns ratio and load. It can be seen from fig.6 that ZVT can be realized in the region higher than the curve under different turns ratio.

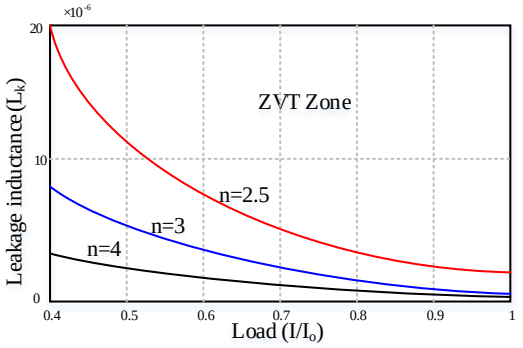

FIGURE 6. The ZVS condition of the proposed converter with different turns ratio

C. VOLTAGE/CURRENT STRESS

According to the above analysis, the voltage stress across power switches and diodes can be obtained:

$$V_{S1}=V_{S2}=V_{S3}=V_{S4}=\frac{1}{1-D}V_i=\frac{1}{1+n+D}V_o \quad (25)$$

The average current through S_3 and S_4 is:

$$I_{avg\text{-}S3}=I_{avg\text{-}S4}=I_o \quad (26)$$

According to the flux-balance and the Fig.4, the following equation can be deducted:

$$N_{1a}I_{s(a\text{-}b)}+N_{1b}I_{s(a\text{-}b)}-N_2\frac{I_o}{D}=N_{1a}\frac{I_o}{1-D}+N_{1b}\frac{I_o}{1-D}+N_2\frac{I_o}{1-D} \quad (27)$$

Where $I_{s(0\text{-}2)}$ is the average current through N_{1a} and N_{1b}, simplified (27), $I_{s(0\text{-}2)}$ can be obtained:

$$I_{s(0\text{-}2)}=\frac{0.5n+D}{D(1-D)}I_o \quad (28)$$

According to (28), the RMS value of S_1 and S_2 is:

$$I_{RMS-S1}=I_{RMS-S2}=\sqrt{\frac{1}{T_s}\int_0^{DT_s}(I_{s(0\text{-}2)}-\frac{1}{2}\Delta i_L+\frac{\Delta i_L}{DT_s}t)^2dt}$$
$$=\frac{0.5n+D}{\sqrt{D}(1-D)}\cdot\frac{P_o}{V_o}\cdot\sqrt{\frac{1}{12}K_i^2+1} \quad (29)$$

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Where K_i is the coefficient of inductor current ripple, which is defined as $\Delta i_L=K_i I_{s(0\text{-}2)}$, the voltage stress and current stress of D_1 are:

$$\begin{cases} V_{D1}=V_o-V_i-V_{C1}-V_{C2}=\dfrac{n}{1+n+D}V_o \\ I_{avg\text{-}D1}=I_o \end{cases} \tag{30}$$

The voltage stress and current stress of D_2 are:

$$\begin{cases} V_{D2}=V_o-V_i-V_{C1}-V_{C2}=\dfrac{n}{1+n+D}V_o \\ I_{avg\text{-}D2}=I_o \end{cases} \tag{31}$$

According to formula (6) and Fig. 2, the input current can be derived as

$$\Delta I_{in}=\frac{2}{1+D}I_{in}-\frac{3(1-D)(2n+3)\sin(\omega_r(1-D))}{n(1+n+D)Z_r f_s}V_o \tag{32}$$

IV. TOPOLOGY DERIVATION

The proposed AS-CL converter is novel, the topology has some good advantages, for example, operation of four switches make it realize soft switching, which has a good influence on the efficiency; Two same inductors L_{1a} and L_{1b} are coupled with third inductor L_2 by using one core, which is beneficial to reduce the size and weight. Moreover, as shown in Fig. 7, the proposed converter is very flexible and can derive a family of converters.

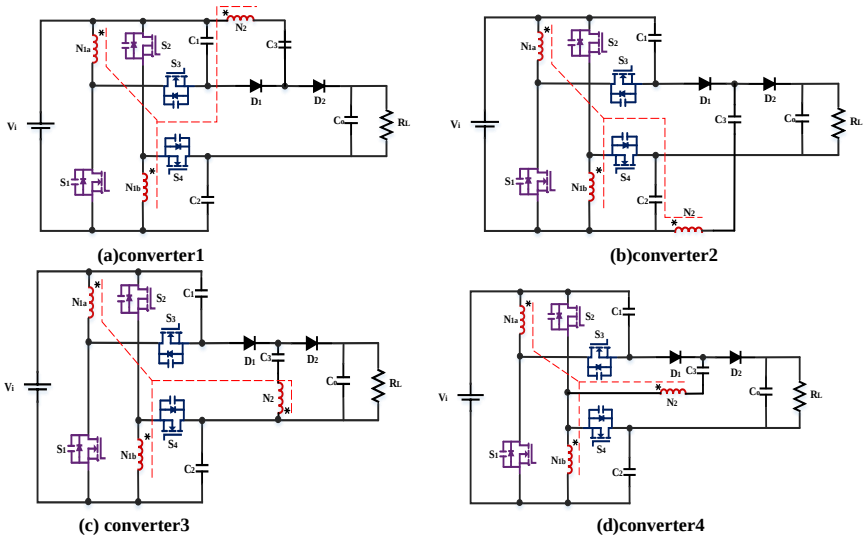

FIGURE 7. A family of AS-CL converters

TABLE I
COMPARISON OF DERIVATIVE CONVERTERS

peremeter	proposed converter	converter1	converter2	converter3	converter4
Gain	$\frac{1+n+D}{1-D}$	$\frac{1+n+D}{1-D}$	$\frac{1+n+D}{1-D}$	$\frac{1+n+D}{1-D}$	$\frac{n+D}{1-D}$
Vs1&s2-stress	$\frac{Vo}{1+n+D}$	$\frac{Vo}{1+n+D}$	$\frac{Vo}{1+n+D}$	$\frac{Vo}{1+n+D}$	$\frac{Vo}{n+D}$
Vs3&s4-stress	$\frac{Vo}{1+n+D}$	$\frac{Vo}{1+n+D}$	$\frac{Vo}{1+n+D}$	$\frac{Vo}{1+n+D}$	$\frac{Vo}{n+D}$
V_{Do}-stress	$\frac{nVo}{1+n+D}$	$\frac{nVo}{1+n+D}$	$\frac{nVo}{1+n+D}$	$\frac{nVo}{1+n+D}$	$\frac{DVo}{n+D}$
Vc1&c2-stress	$\frac{DVo}{1+n+D}$	$\frac{DVo}{1+n+D}$	$\frac{DVo}{1+n+D}$	$\frac{DVo}{1+n+D}$	$\frac{DVo}{n+D}$
Vc3-stress	$\frac{n(1-D)Vo}{1+n+D}$	$\frac{(n-nD+D)Vo}{1+n+D}$	$\frac{(n-nD+D)Vo}{1+n+D}$	$\frac{(n-nD+D+1)Vo}{1+n+D}$	$\frac{(n-nD+D)Vo}{1+n+D}$

Four more converters are derived from the proposed converter, all of them have similar structure and the ability to achieve soft switching. As shown in Table I, it is easy to find that the performance of this family is similar. In general, the proposed converter shows the best performance among these converters.

As shown in Fig. 8, the windings N_{1a} and N_{1b} in the primary side are separated from winding N_1, which aims to reduce the current across switches and wire diameter. The turns ratio relationship between windings is N_{1a}:N_{1b}:N2=1:1:n. Thus, the essence of this windings also belongs to two windings coupled structure.

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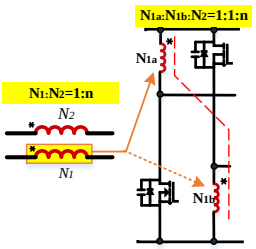

FIGURE 8. The essence of the windings in the proposed converter

Table II shows the comparison of five different converters with ASL units. It is obvious that ASL and ASL-C have better performance than boost converter. The rest three converters combining ASL with coupled inductors, show higher voltage gain with introduction of turns ratio. The main difference is that converters [20] & [21] use two sets of two windings coupled inductors to get higher voltage gain, while the proposed converter only uses one coupled inductor by separating primary winding into two windings. Actually, it is still one coupled inductor. So, to compare these converters under same conditions, the turns ratio of the proposed converter should be twice as the turns ratio of converters [20] & [21]. The comparison of voltage gain is shown in Fig. 9, the proposed converter has higher voltage gain than other two ASL-CL converters. What's more, the proposed converter can realize soft switching of all switches. The input current ripple of the proposed converter is similar to other ASL converters. Therefore, the proposed converter has better overall performance.

Table III shows the comparison of other converters with two-windings and three-windings coupled inductors. Under the same operating conditions including input voltage, output voltage and duty cycle, the voltage stresses of switches are same for all converters except [23], which has highest voltage stress on the switch. Current stress across switches of the proposed converter are also the lowest compared to other converters. Moreover. among the converters listed in Table III, only the proposed converter can realize the ZVT.

TABLE II
COMPARISON WITH CONVERTERS IN ASL SERIES

Converter	conventional(ASL)	ASL-C[19]	AS-CL[20]	Q-AS-CL[21]	proposed converter
No. of switches	2	2	2	2	4
No. of diodes	1	2	5	3	2
No. of magnetic elements	2L	2L	2*2W	2*2W	1*2W
Gain	(1+D)/(1-D)	$(1+3D)/(1-D)$	$(1+(2n+1)D)/(1-D)$	$(1+(2n+1)D)/(1-D)$	$(1+n+D)/(1-D)$
$V_{stress\text{-}S}(/V_O)$	1/(1+D)	$1/(1+3D)$	$1/(1+(2n+1)D)$	$1/(1+(2n+1)D)$	$1/(1+n+D)$
Input current ripple	$I_o/(1+D)+A_1(1-D)V_o$	$I_o/(1-D)+A_2(1-D)V_o$	$I_o/(1+D)+A_3(1-D)V_o$	$I_o/(1+D)+A_4(1-D)V_o$	$(1+n+D)I_o/(1-D^2)+A_5(1-D)V_o$
Soft switching /frequency	No/100kHz	No/50kHz	No/50kHz	No/100kHz	ZVT/100kHz

Where, $A_1=3D/[2Lf_s(1+D)]$; $A_2=(1/4L_2+(5D+D^2-1)/[2(1+D+D^2)L_1f_s]$; $A_3=(3D^2+1)/[(1+(2n+1)D)f_s]$; $A_4=(3D^2+1)/[2(1+(2n+1)D)f_s]$; $A_5=3(2n+3)\sin(\omega_r(1-D))/[n(1+n+D)Z_rf_s]$

TABLE III
COMPARISON WITH OTHER CONVERTERS WITH COUPLE INDUCTOR

Converter	No. of components					G	$V_{stress\text{-}S}/Vo$	$I_{stress\text{-}S}/Io$	ZVT
	D	C	S	CL	L				
[22]	2	1	2	1*2W	0	(1+n)/(1-D)	1/[(1-D)G]	(3n+1)/(1-D)	No
[23]	2	4	2	1*2W	1	(2n-1)/(n-1)(1-D)	(n+1)/[(1-D)(n-1)G]	$(n/(n-1)+D)/(D-D^2)+I_L$	No
[24]	4	4	1	1*2W	0	(1+n+nD)/(1-D)	1/[(1-D)G]	D(1+n+nD)/(1-D)	No
[25]	5	5	1	1*3W	0	$(1+2n_2+n_3D)/(1-D)$	1/[(1-D)G]	$D(1+2n_2+n_3D)/(1-D)$	No
[26]	4	3	1	1*3W	0	$(2+2n_2+n_3D(1+n_2)D)/(1-D)$	1/[(1-D)G]	$D(2+2n_2+n_3D(1+n_2)D)/(1-D)$	No
[27]	5	5	1	1*3W	1	$(3+2n_2+n_3)/(1-D)$	1/[(1-D)G]	$(4-D+(2n_2+n_3)(2-D))/D(1-D)+I_L$	No
Proposed converter	2	4	4	1*2W	0	(1+n+D)/(1-D)	1/[(1-D)G]	0.5n+D/(1-D)	Yes

Where, D=Diode; C=Capacitor; S=Switch; CL=Coupled Inductor; L= Inductor; 3w=3-winding; 2w=2-winding; $I_L=DV_{in}/2L_{m}f_sI_o$.

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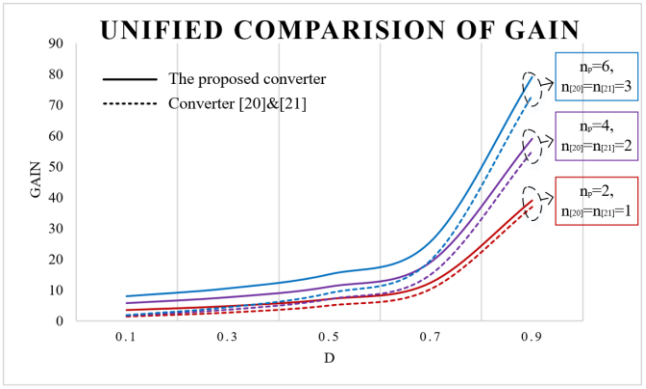

FIGURE 9. Unified comparison of the proposed converter with other AS-CL converter

V. EXPERIMENT RESULT

In order to verify the precision of the analysis, experiments have been conducted. Fig.10 shows the prototype board. The basic condition, component parameters and specific model selection of the experiment are showed in table IV.

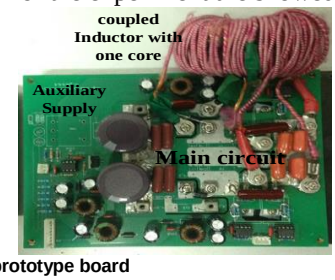

FIGURE 10. The prototype board

The input voltage is set as 30V, and the main waveform is shown in Fig. 11. Fig.11(a) shows the switching signal V_{gs1} and V_{gs3}, the switches voltage V_{ds1} and V_{ds3}. As can be seen from the figure, the voltage stress of the two switches is about 85V, and both S_1 and S_3 realize ZVT, Fig.11(b) shows the switching signal V_{gs2} and V_{gs4}, the switches voltage V_{ds2} and V_{ds4}. Same as S_1 and S_3, the voltage stress of the two switches is about 85V, and S_2 and S_4 also realize ZVT. The switching signal V_{gs1}, the inductor current i_{n1a}, i_{n1b} and i_{n2} are shown in Fig.12(a). When the switch is on, L_1 and L_2 are charged, i_{n1a} and i_{n1b} both increase; when the switches are off, i_{n1a} and i_{n1b} decrease. The waveforms of the voltage and current of D_1 and D_2 are given in Fig.12(b), the turn-off current falling rate of D_1 and D_2 is limited by the leakage inductor.Fig.13 shows the voltage stress on capacitors C_1, C_2 and C_3, V_{C1} and V_{C2} are about 60V, V_{C3} is about 100V, the output voltage is equal to 400V.

The input voltage is set as 30V, 40V and 50V, the efficiency curve of the circuit is shown in Fig. 14. As can be seen from the figure, when the output power is 300W. Among the three curves, when the input is 50V, the efficiency is the highest and the maximum power can reach 96.6%.

TABLE IV
EXPERIMENT CONDITIONS

components	parameters	components	parameters
Input voltage(V_i)	30V-50V	Clamping capacitor (C_1、C_2)	4.7uF/63V(CBB)
Output voltage (V_o)	400V	Turns ratio	N_{1a}:N_{1b}:N_2 =1:1:3
Rated output power(P_o)	500W	L_m(magnetizing inductor, N_2 side)	600μH
Switching frequency (f_s)	100kHz		
Power switches(S_1, S_2)	IPP111N15N3G	L_k (leakage inductor, N_2 side)	22μH
Active clamping switches (S_3, S_4)	IPP111N15N3G	Capacitor (C_3)	1uF/250V (CBB)
Diode (D_1)	FR304	Filter Capacitor (C_o)	470uF/450V(Electrolysis) 1.5uF/450V(CBB)

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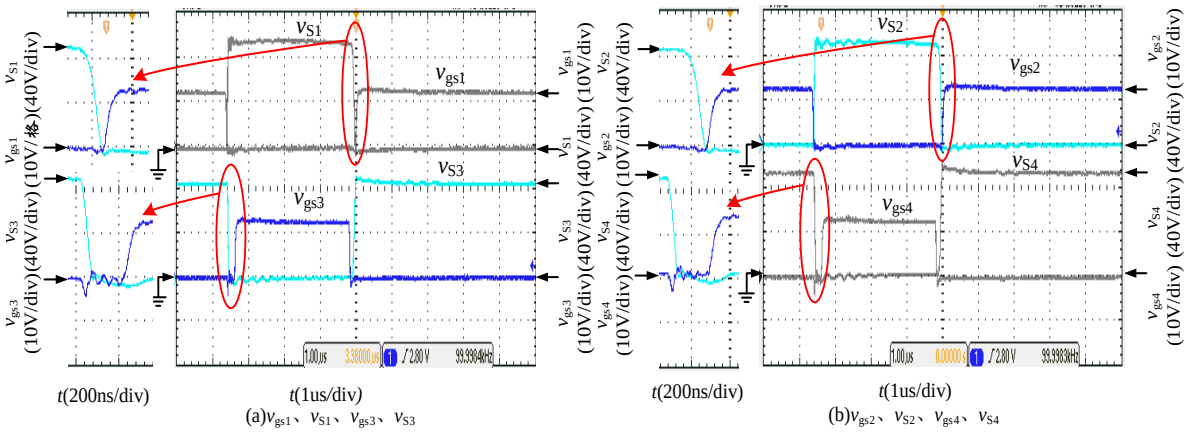

FIGURE 11. Experiment waveform of ZVT

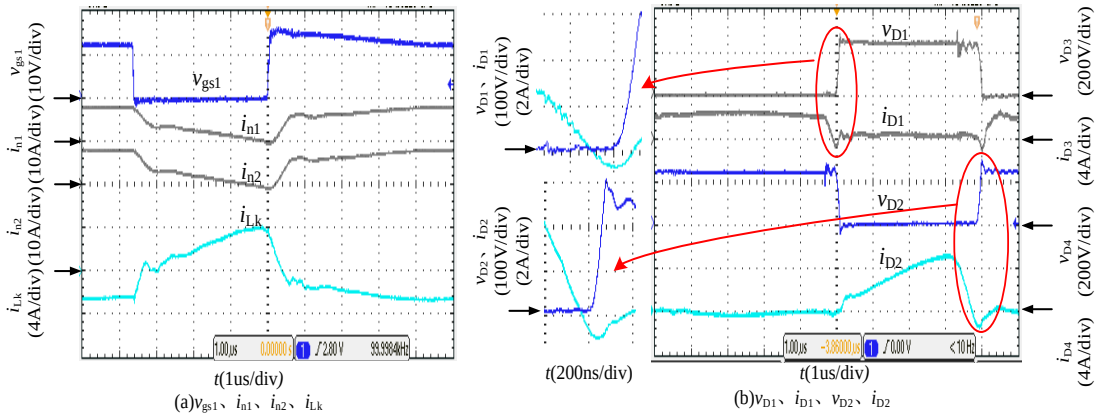

FIGURE 12. Experiment waveform of coupled inductors and diodes

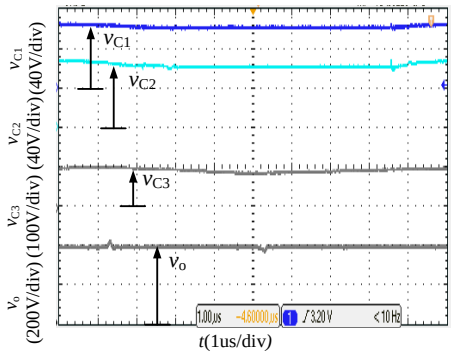

FIGURE 13. Voltage waveforms of all capacitors and output voltage

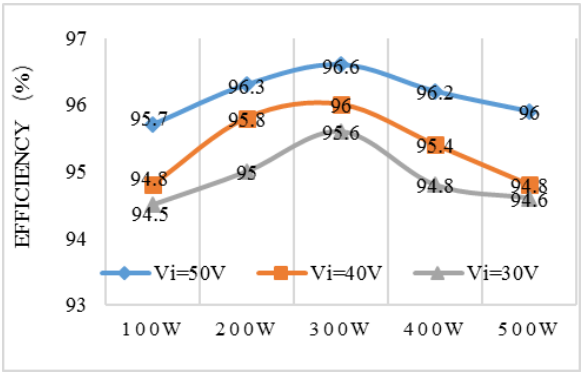

FIGURE 14. Efficiency of the proposed converter

VI. CONCLUSION

This paper has studied a novel coupled inductors DC-DC converter with high voltage gain, the structure of the proposed converter is simple. The characteristics of the converters are shown as following:

1)The power loss on switches are effectively reduced because of that all switches can turn on with ZVT.

2) The proposed converter can realize high voltage gain with appropriate turns ratio and small duty cycle, which makes peak current reduced and the efficiency improved.

3) The voltage stress of the diodes is relatively low which solves the reverse problem effectively.

4) Due to the structure of ASL, voltage and current stress of the power devices are low.

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