Received February 3, 2013, accepted April 14, 2013, published May 10, 2013.

Digital Object Identifier 10.1109/ACCESS.2013.2259891

Memristor-Based Nonvolatile Random Access Memory: Hybrid Architecture for Low Power Compact Memory Design

SYED SHAKIB SARWAR, SYED AN NAZMUS SAQUEB, FARHAN QUAIYUM (Student Member, IEEE), AND A. B. M. HARUN-UR RASHID (Senior Member, IEEE)

Department of Electrical and Electronic Engineering, Bangladesh University of Engineering and Technology, Dhaka 1000, Bangladesh.

Corresponding author: S. S. Sarwar (syed.shakib@ieee.org)

This work was supported by the Ministry of Science and Technology, Government of Bangladesh, under the Science and Technology Special Research Grant for 2012–2013.

ABSTRACT In this paper, a new approach toward the design of a memristor based nonvolatile static random-access memory (SRAM) cell using a combination of memristor and metal-oxide semiconductor devices is proposed. Memristor and MOSFETs of the Taiwan Semiconductor Manufacturing Company's 180-nm technology are used to form a single cell. The predicted area of this cell is significantly less and the average read–write power is ∼25 times less than a conventional 6-T SRAM cell of the same complementary metal-oxide semiconductor technology. Read time is much less than the 6-T SRAM cell. However, write time is a bit higher, and can be improved by increasing the mobility of the memristor. The nonvolatile characteristic of the cell makes it attractive for nonvolatile random access memory design.

INDEX TERMS CMOS, memory element, memristor (M), NVRAM, SPICE model.

I. INTRODUCTION

Chua [1] hypothesized the existence of a fourth passive two-terminal circuit element called the memristor in 1971 (the other three elements being the resistor, capacitor and inductor). In 2008, researchers at Hewlett Packard (HP) Labs reported that the memristor was realized physically using two-terminal titanium-di-oxide (TiO_2) nanoscale device [2]. HP Labs described the first experimental demonstration of a physical memristor, finally confirming Chua's theory and sparking much excitement in the electronics and business circles [3]. Basically the memristor is a resistance with memory; when a voltage is applied to this element, its resistance changes and remains on that particular value when the source is removed. The main difference between the memristor (M) and the three traditional circuit elements (R, L, C) is its nonlinear input-output characteristics.

The HP memristor exploits certain nanoscale properties of a titanium-di-oxide TiO_2 thin film. Other physical embodiments of memristors may also be possible and it has been recently proposed that coupling of current flow and spin transport at nanoscale dimensions can be used to realize memristance [4], [5]. Analog circuit applications incorporating the memristor are rapidly emerging in the literature. Witrisal considered Memristors in an ultra-wideband receiver to reduce signal processing power [6]. Memristors are also used as programmable resistive loads in a differential amplifier [7]. Varghese and Gandi used memristor as a source degeneration element in a complementary metal-oxide semiconductor (CMOS) differential pair [8]. Reference [9] shows a variety of programmable analog functional blocks based on analog memristor memory including an Op-Amp based variable gain amplifier (VGA). Pulse-programming methods for memristive analog memory in a differential pair amplifier are considered in [10].

Memristors have been studied intensively among many researchers because of their possibilities, especially as a strong candidate for future memories [11]. Non-volatile property and high packing density in a crossbar array particularly excites the researchers. The main feature of our proposed circuit is its non-volatility. The data is stored in the memory even when the power is turned off for an indefinite time. Another feature is its reduced size compared to the conventional 6T-SRAM. As only three transistors are used in each

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cell of the proposed circuit, its area can be much less than the conventional SRAM cells. The power consumed by the proposed structure is significantly less than the conventional SRAM structure. All these features are discussed further later on in this paper.

The paper starts off with the introduction of memristors and its characteristics. After that some related works were discussed. Then it goes straight into the structure of our proposed circuit, its working principle and its functionality, then it discusses the perspectives, draws some comparisons, and finally it concludes with the possible future prospects of the circuit.

II. MEMRISTOR AS A MEMORY ELEMENT

Strukov *et al.* [2] presented a physical model of the memristor. They have shown that the memristor can be characterized by an equivalent time-dependent resistor whose value at a time t is linearly proportional to the quantity of charge q that has passed through it. They realized a proof-of-concept memristor, which consists of a thin nanolayer (2 nm) of TiO_2 and a second oxygen deficient nanolayer of TiO_{2-x} (8 nm) sandwiched between two Pt nanowires. Oxygen ($O_2{}^-$) vacancies are +2 mobile carriers and are positively charged. A change in distribution of $O_2{}^-$ within the TiO_2 nanolayer changes the resistance. By applying a positive voltage, to the top platinum nanowire, oxygen vacancies drift from the TiO_{2-x} layer to the TiO_2 undoped layer, thus changing the boundary between the TiO_{2-x} and TiO_2 layers. As a consequence, the overall resistance of the layer is reduced corresponding to an "ON" state. When enough charge passes through the memristor that ions can no longer move, the device enters a hysteresis region and keeps q at an upper bound with fixed memristance, M (memristor resistance). By reversing the process, the oxygen defects diffuse back into the TiO_{2-x} nanolayer. The resistance returns to its original state, which corresponds to an "OFF" state. The significant aspect to be noted here is that only ionic charges, namely oxygen vacancies ($O_2{}^-$) through the cell, change memristance. The resistance change is non-volatile hence the cell acts as a memory element. Fig. 1(a) shows the doped and undoped region of a memristor. If a voltage is applied across the memristor

$$v(t) = M(t)i(t) \ [2] \tag{1}$$

$$M(t) = R_{ON}\frac{w(t)}{D} + R_{OFF}\left(1 - \frac{w(t)}{D}\right) \tag{2}$$

where R_{ON} is the resistance of completely doped memristor and R_{OFF} is the resistance of completely undoped memristor, w(t) is given by

$$\frac{dw(t)}{dt} = \mu_v \frac{R_{ON}}{D} i(t) \tag{3}$$

μ_v is the average dopant mobility and D is the length of the memrsitor. To consider the nonlinearity produced from the edge of the thin film, a window function [2], [12], [13] should be multiplied to the right side of (3).

$$f\left(\frac{w(t)}{D}\right) = 1 - \left(2\frac{w(t)}{D} - 1\right)^{2p}. \tag{4}$$

The spice model [13] which makes use of non-linear dopant drift in modelling is used for simulation. Change of resistance of a memristor applying 3.6 V p–p square wave across it is shown in Fig. 1(b). Following parameters were used for simulation: R_{ON} = 100 Ω, R_{OFF} = 20 kΩ, p = 10, D = 3 nm and $\mu_v = 350 \times 10^{-9}$ m^2/s/V.

Resistance of the memristor changes from 20 kΩ to 100 Ω in positive cycle. This change occurs in reverse direction when the square pulse reverses its direction.

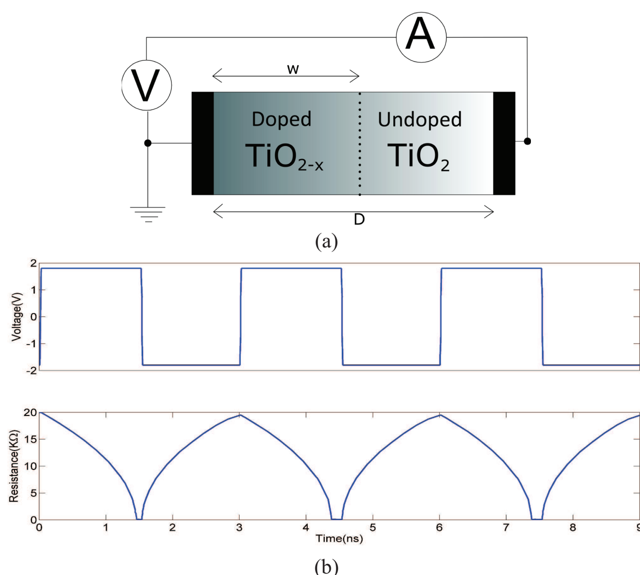

FIGURE 1. (a) Characterizing the memristor and (b) change of resistance when a 3.6 V p–p square wave is applied.

III. RELATED WORKS

SRAM is a form of semiconductor memory widely used in electronics, microprocessor and general computing applications. This form of semiconductor memory gains its name from the fact that data is held in there in a static fashion, and does not need to be dynamically updated as in the case of DRAM memory. While the data in the SRAM memory does not need to be refreshed dynamically, it is still volatile, meaning that when the power is removed from the memory device, the data is not held, and will disappear. The operation of the SRAM memory cell is relatively straightforward. When the cell is selected, the value to be written is stored in the cross-coupled flip-flops. The cells are arranged in a matrix, with each cell individually addressable. Most SRAM memories select an entire row of cells at a time, and read out the contents of all the cells in the row along the column lines. Access to the SRAM memory cell is enabled by the Word Line. This controls the two access control transistors which control whether the cell should be connected to the bit lines. These two lines are used to transfer data for both read

and write operations. The most commonly used SRAM type is the 6T SRAM which offers better electrical performances from all aspects (speed, noise immunity, standby current). The smallest 6T-SRAM cell that has been fabricated till today has an area of 0.08 μm^2 and it was fabricated in the 22 nm process using immersion and EUV lithography [15]. The main disadvantages of the 6T SRAM structure are its large size and high power consumption. To overcome these limitations, memristive-RAMs are being developed recently. According to HP, resistive random access memory (ReRAMs), which are memristor-based versions of both DRAM and SRAM, ought to speed up computers immensely. Along with HP, Samsung and many other companies are working on memristor technology.

There are several researches on memristor based memories. In [16], a complementary resistive switch was introduced. It consists of two anti-serial memristive elements which validates the construction of large passive crossbar arrays with a drastic reduction in power consumption. Junsangsri *et al.* [17] presented a novel memory cell consisting of a memristor and ambipolar transistors. Macroscopic models were utilized to characterize the operations of that memory cell. In [18], Kamran Eshraghian *et al.* provided a new approach towards the design and modeling of memristor based content addressable memory (MCAM) using a combination of memristor and MOS devices to form the core of a memory/compare logic cell. This cell forms the building block of the CAM architecture. The non-volatile characteristic and the minuteness together with compatibility of the memristor with CMOS processing technology increases the packing density, provides new approach towards power management through disabling CAM blocks without loss of stored data, which reduces power dissipation. This inspired us to design a SRAM cell using Memristor-MOS hybrid architecture exploiting the non-volatile characteristic and the nanoscale geometry of a memristor.

IV. PROPOSED SRAM CELL

Electrical scheme of the proposed SRAM cell is shown in Fig. 2(a). Two memristors are used as memory element. The arrangement is in such a way that during write cycle, they are connected in parallel but in opposite polarity [Fig. 2(b)] and during read cycle, they are connected in series [Fig. 2(c)]. These connections are established by two NMOS pass transistors T1 and T2. A third transistor T3 is used to isolate a cell from other cells of the memory array during read and write operations. The gate input of T3 is the Comb signal which is the OR of RD and WR signals. If a bit is to be written, RD is taken to the LOW state and WR and Comb are taken to the HIGH state. As a result, circuit of Fig. 2(b) is formed. The voltage across the memristors is $(V_D - VDD/4)$. Depending on the data, it can be positive (if $D = 1$ i.e. $V_D = VDD$) or negative (if $D = 0$ i.e. $V_D = 0$ V). As polarities of the memristors are opposite, change of memristances (or resistances) will also take place in the opposite direction. Now if the data is to be read, RD and Comb are

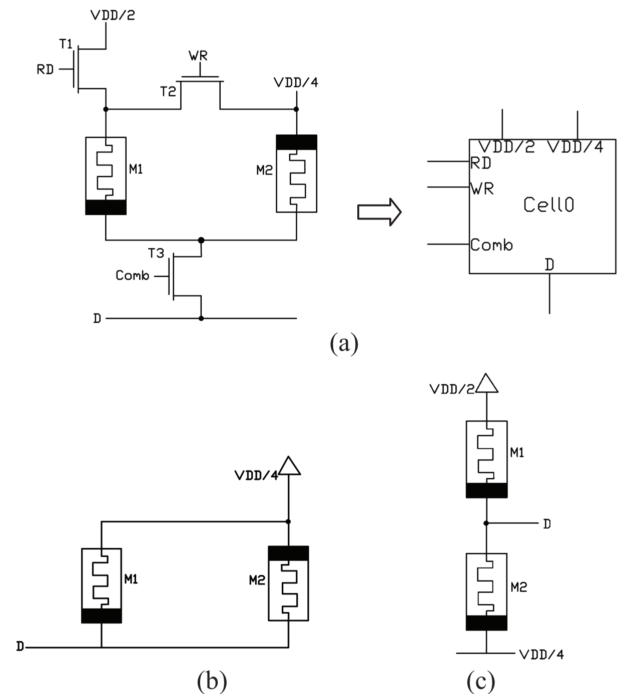

FIGURE 2. (a) Three transistor–two memristor SRAM cell (b) circuit when RD = 0, WR = 1, and Comb = 1. (c) Circuit when RD = 1, WR = 0, and Comb = 1.

taken to the HIGH state and this forms the circuit shown in Fig. 2(c). Voltage at D is now:

$$V_D = \left(\frac{V_{DD}}{2} - \frac{V_{DD}}{4}\right) \times \frac{R2}{(R1 + R2)} + \frac{V_{DD}}{4} \quad (5)$$

where, $R1$ and $R2$ are the resistances of $M1$ and $M2$ respectively. If "1" was written during write cycle, $R2$ becomes significantly greater than $R1$ and then V_D is greater than $VDD/4$. If "0" was written, $R1$ becomes significantly greater than $R2$ which makes V_D to be as close as $VDD/4$. A comparator can be used as a sense amplifier to interpret these voltages as HIGH or LOW correctly.

V. SIMULATIONS AND ANALYSIS

In Fig. 3, a 16 × 16 array is formed for the verification of array structure of our proposed NVRAM cell. Data is fed through wordlines/bitlines. Switching between i/p and o/p is done with the help of CMOS transmission gate controlled by Vdt and Vdtb signals which are complement of each other. In practical circuits, this purpose is served through encoders. Several simulations were done to test the validity of our proposed SRAM structure and compare it with the traditional SRAM structures. In the simulations data was written and read to calculate several important parameters such as write time, read time, power consumption etc. A comparator can be used as a sense amplifier to interpret these voltages as HIGH or LOW correctly. The reference of the comparator should be tied to 0.26 V. Simulations of the circuits are based on the following parameters: $R_{ON} = 100\ \Omega$, $R_{OFF} = 20\ k\Omega$, $p = 10$, $D = 3$ nm and $\mu_v = 350 \times 10^{-9}$ m^2/s/V. The NVRAM cell has been implemented using TSMC 180 nm technology.

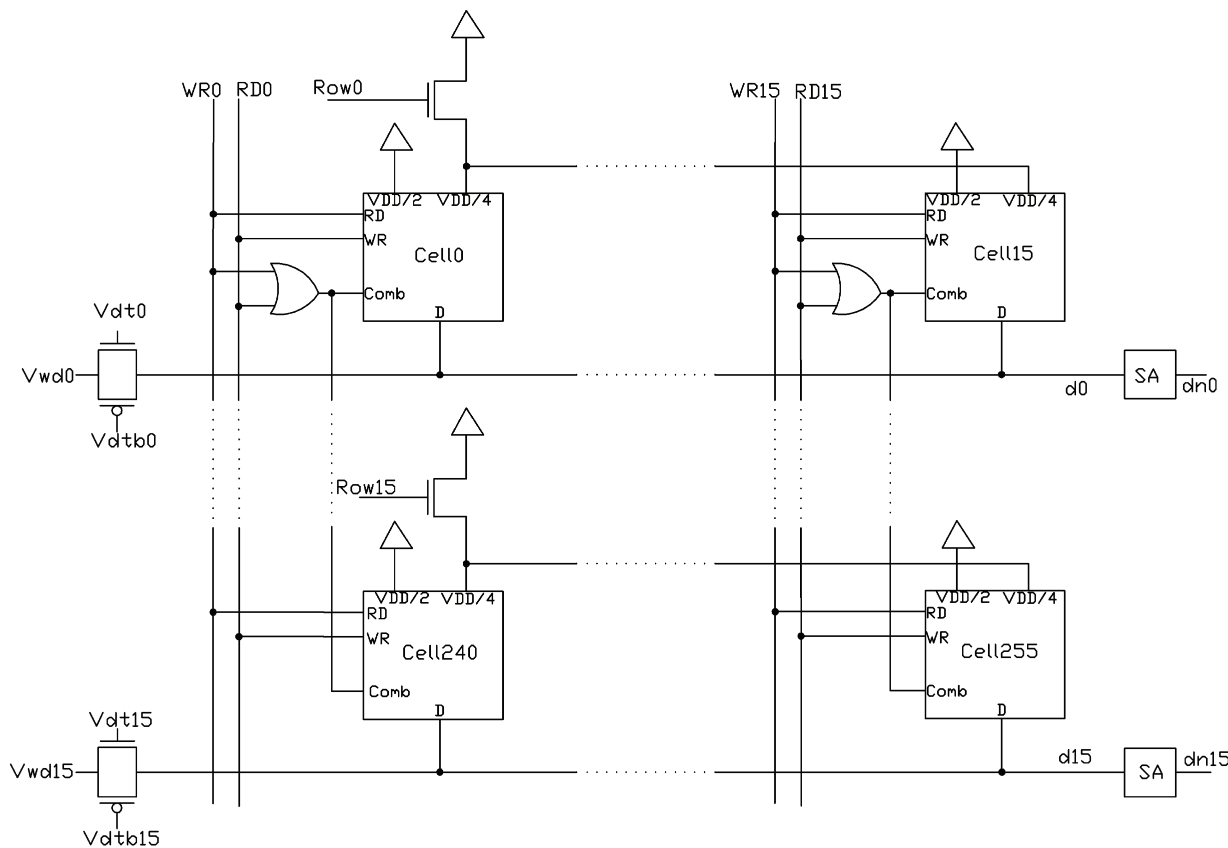

FIGURE 3. 16 × 16 array structure.

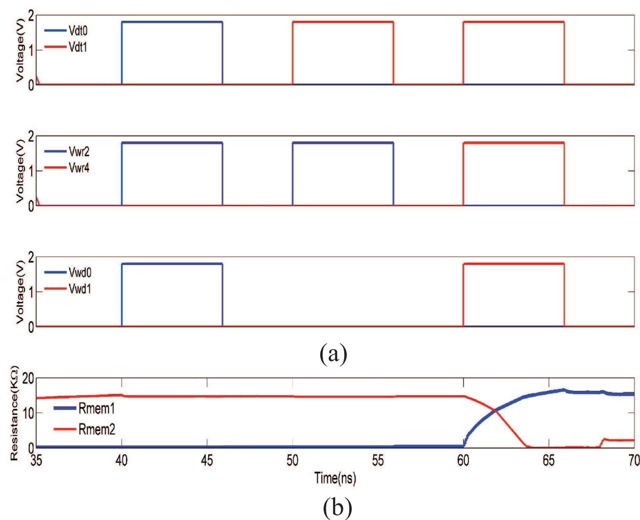

FIGURE 4. (a) Timing diagram of input pulses during write operation. (b) Change of resistance of the two memristors of cell20 during write operation.

A. WRITE OPERATION

In the first write cycle, "1" was written to cell2. Vwr2, Vrow0 and Vdt0 were set to HIGH state to select this cell. Timing diagram in Fig. 4(a) shows Vwr2, Vdt0 pulses and also shows the data in d0 which is Vwd0. This write cycle starts from 40 ns and during this cycle, Vwr2 = 1, Vdt0 = 1 and Vwd0 = 1. In the next cycle, a "0" was written to cell18 (from 50 ns) and to do this, Vwr2, Vrow1, Vdt1 were set to HIGH state and Vwd1 was set to LOW state. Finally a "1" was written to cell20 (from 60 ns). For this, Vwr4, Vrow1, Vdt1 and Vwd1, all were set to HIGH state. In Fig. 4(b), plot of the resistance of two memristors in cell20 shows the alteration of resistance while writing "1" into it.

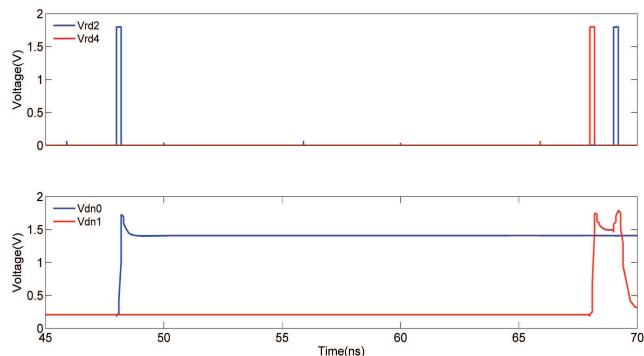

FIGURE 5. Timing diagram of read operation.

B. READ OPERATION

After writing "1" in cell 2, the stored data was read (from 48 ns). For this, Vrd2 was set to HIGH state and data at dn0 is checked. In Fig. 5, timing diagram of read cycles is shown.

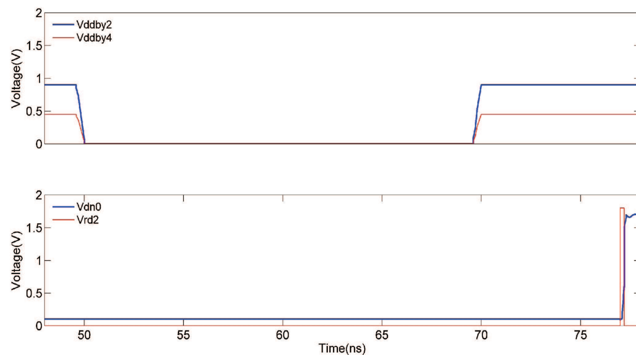

FIGURE 6. Evidence of non-volatility of the memristor SRAM cell. After writing "1" in cell 18, all the power sources are turned off during the time interval 50–69 ns. A read operation is done after turning on the power sources and found "1" in cell 18.

During read operation at cell2, dn0 was found HIGH. Then after two write cycles, cell20 was read (from 68 ns) and found HIGH at dn1. Finally, cell18 was read (from 69 ns) and found LOW at dn1. So after reading a cell, data was found to be exactly the same as it was written previously in that cell. Thus, the array structure shows proper functionality both in read and write operations.

VI. PERSPECTIVES

Our proposed memristor based memory cell is non-volatile in nature.

After writing "1" in cell 18, all the power sources were turned off during the time interval 50–69 ns (Fig. 6). A read operation is done after turning on the power sources and found "1" in cell 18. This proves the non-volatile nature of the cell.

The write and read times were measured and compared in Table 1:

TABLE 1. Write/read time comparison.

Operation	Proposed SRAM Cell (ns)	6-T Cell [19] (ns)
Write	5.9	0.85
Read	0.2	1.23

The proposed NVRAM cell requires a bit more time for the write cycle than the conventional SRAM cells. By further increasing the mobility of the memristors, the write cycle time can be considerably reduced. Fig. 7 shows the inverse relation between mobility of the memristor and the write cycle time. The read cycle time depends on the sensitivity and responsiveness of the sense amplifier.

From simulation the power dissipation curve was found and integration was done to get the energy dissipated for separate operations (writing and reading "1" & "0"). And then the energy values were divided by respective operation cycle times to get the corresponding power dissipations (Table 2).

The obtained values were then averaged to get the total power dissipation. This was compared with the value of the conventional SRAM cell in Table 3.

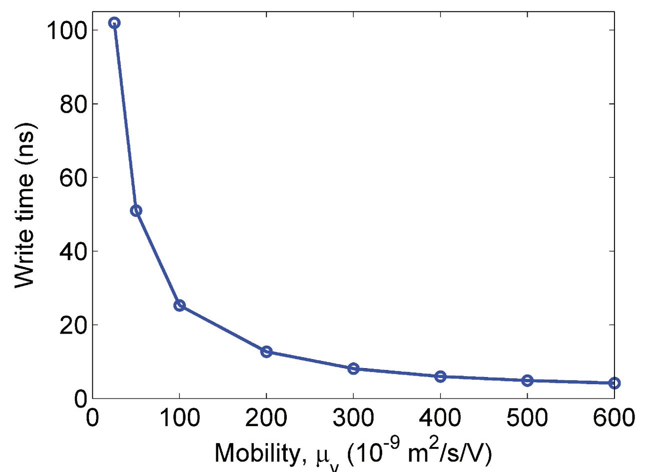

FIGURE 7. Inverse relation between mobility of the memristor and the write cycle time.

TABLE 2. Power dissipation during different operations.

Operation	Wr0	Wr1	Rd0	Rd1
Energy (fJ/cycle)	191.01	803.49	61.36	68
Power (μW)	32.37	136.18	306.85	340
Peak power (mW)	0.935	2.5	5.8	5.9

TABLE 3. Power comparison.

Operation	Proposed SRAM Cell (mW)	6-T Cell [19] (mW)
Power	0.407	10.373

Power consumption is much less than 6-T cell which can be reduced more by designing a faster comparator which would reduce the read time.

The area of the proposed memory cell can be predicted to be much less than the area of conventional 6-T SRAM cell, as only three transistors are used along with two memristors. As memristors can be as small as 3 nm, the area can be further reduced if we can switch to more recent fabrication technologies such as 22 nm technology.

VII. CONCLUSION

In this paper, we proposed a new idea of NVRAM cell using memristor. The read time is much faster compared to a conventional SRAM and the power consumption is also much smaller. However the writing speed is not satisfactory compared to existing SRAM cells due to the low mobility of the memristor in the SPICE model we used. Recent researches suggest that the write time can be significantly reduced [14], [20] using state-of-the-art fabrication techniques. The comparator used to read the data can be replaced by a more compact and efficient sense amplifier which in turn would further decrease the read time. There are further scopes to work on

power consumption as well. Overall, it can be said that our proposed NVRAM is a combination of new technology and innovative design which can open a new door in the field of memory design.

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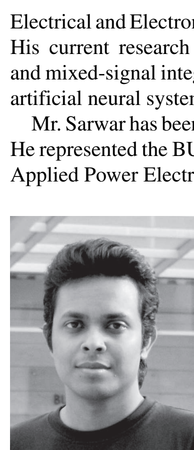
SYED SHAKIB SARWAR (S'11) was born in Dhaka, Bangladesh, in 1989. He received the B.Sc. degree in electrical and electronic engineering from the Bangladesh University of Engineering and Technology (BUET), Dhaka, Bangladesh, in 2012. He is currently pursuing the M.Sc. degree in electrical and communication Engineering from the Department of Electrical and Electronic Engineering, BUET.

Since 2012, he has been a Faculty Member of Electrical and Electronic Engineering Department, BRAC University, Dhaka. His current research interests include high frequency, low power analog and mixed-signal integrated circuits, FPGA based digital circuit prototyping, artificial neural systems, and image processing.

Mr. Sarwar has been with the IEEE Solid State Circuits Society since 2012. He represented the BUET team in the IFEC-2011 Workshop during the IEEE Applied Power Electronics Conference in Dallas, TX, USA.



SYED AN NAZMUS SAQUEB (S'11) was born in Natore, Bangladesh, in 1988. He received the B.Sc. degree in electrical and electronic engineering from the Bangladesh University of Engineering and Technology (BUET), Dhaka, Bangladesh, in 2012.

Since 2012, he has been a Faculty Member of the Electrical and Electronic Engineering Department, University of Asia Pacific, Dhaka. He is pursuing the M.Sc. degree in electrical and communication engineering from the Department of EEE, BUET. His current research interests include analog and mixed-signal circuit design, neuromorphic circuits, biomedical VLSI systems, and circuit design with novel devices.

Mr. Saqueb has been with the IEEE Solid State Circuits Society since 2012.

FARHAN QUAIYUM (S'11) was born in Dhaka, Bangladesh, in 1989. He received the B.Sc. degree in electrical and electronic engineering from the Bangladesh University of Engineering and Technology, Dhaka, Bangladesh, in 2012.

He has been an ASIC Design Engineer with Fastrack Anontex Ltd., since June 2012. He is pursuing the M.Sc. degree in electrical and communication engineering from the Department of EEE, BUET. His current research interests include high speed digital circuit design, ultra-low-power/low voltage circuits, and embedded systems.

A. B. M. HARUN-UR RASHID (M'89–SM'02) received the B.Sc. degree in electrical and electronic engineering from the Bangladesh University of Engineering and Technology (BUET) Dhaka, Bangladesh, in 1984, the M.Sc. degree in electronic engineering from Oita University, Japan, in 1988, and the Ph.D. degree in electronic engineering from the University of Tokyo, Tokyo, Japan, in 1996.

He has been as a Faculty Member with the Department of Electrical and Electronic Engineering, BUET, where he is a Professor since 2006. He served as a Design Engineer with Texas Instruments Japan Ltd., from 1988 to 1993, where he worked on the research and development of 1.2μm Bi-CMOS process for mixed signal VLSI circuits. He was a Research Fellow with the Research Center for Nanodevices and Systems, Hiroshima University, Tokyo, Japan, from 2001 to 2003, where he worked in the design and demonstration of on-chip wireless interconnect. His current research interests include high speed and low power circuit design using novel nanodevices, very high frequency analog integrated circuit design, and on-chip wireless interconnect design.