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RESEARCH ARTICLE

Series Hybrid Modular Multilevel Converter for HVDC Transmission Systems

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ABSTRACT In this paper, a multilevel Voltage Source Converter for HVDC transmission systems is proposed. The topology is based on a string of full-bridge submodules in addition to an unfolder on the converter's AC-side. Compared to the modular multilevel converter, it has fewer components and has the advantage that almost two third of the switches operate in soft switching mode. Furthermore, for the same level of stress on converter and transformer, it provides a DC-link voltage 3.33 times higher than AC-side rms-voltage. A control strategy is proposed to regulate the active and reactive power exchanged with the grid while the capacitor voltage balancing is ensured. The viability of the proposed converter, as well as the effectiveness of the voltage balancing control strategy are confirmed by simulation and experiment.

INDEX TERMS High power converter, HVDC system, transmission lines, modular multilevel converter, soft switching.

I. INTRODUCTION

High Voltage DC (HVDC) transmission is a long-standing technology for bulk power transmission over long distances, with many installations around the world. Over the past few years, significant breakthroughs in the Voltage-Source Converters (VSCs) along with their attractive features have made the HVDC technology even more promising in providing enhanced reliability and functionality and reducing power losses [1], [2], [3], [4], [5]. Currently, the Modular Multilevel Converter (MMC), which is built based upon stack of identical half- or full-bridge submodules (SMs), is the dominant VSC topology for HVDC transmission because of its salient features including (i) scalability/modularity to meet any voltage/power-level requirements, (ii) excellent harmonic performance, (iii) very high efficiency, and (iv) redundancy in the converter configuration [6], [7], [8], [9], [10], [11].

Notwithstanding advantages offered by the MMC, a few variants of the MMC have also been proposed and investigated to address its deficiencies for HVDC transmission. Those variants mainly include the Parallel Hybrid MMC (PHMMC) [12], [13], hybrid MMC based on combination of various SM circuits [14], [15], Series Bridge Converter (SBC) [16], and Alternate Arm Multilevel Converter (AAMC) [17], [18], [19]. These topologies, while preserving salient features of the MMC, can offer reduced number of component parts and, consequently, improved efficiency [12], [13], or capability to interrupt the DC-side short-circuit faults [17], [20], [21], [22]. Nevertheless, the PHMMC, due to its circuit topology, inherits low-order harmonics on its DC-bus voltage and cannot fully regulate the DC voltage/power. The hybrid MMC and AAMC need various types of series-connected SMs/switches and their full modularities are dismissed.

This paper recognizes the drawbacks associated with the existing MMC-derived topologies and proposes a converter topology as an add-on feature to the existing ones. In this paper, a novel multilevel VSC for HVDC transmission called Series Hybrid Modular Multilevel Converter (SHMMC) is proposed. This converter is based on cascaded connection of multiple full-bridge submodules (FBSMs) in addition to a soft-switched unfolder on the AC-side of the converter. Compared to the conventional MMC, this topology not only has fewer components, but also offers soft-switching operation for almost 66% of the semiconductor devices. In addition, it provides a DC-link voltage almost 3.33 times

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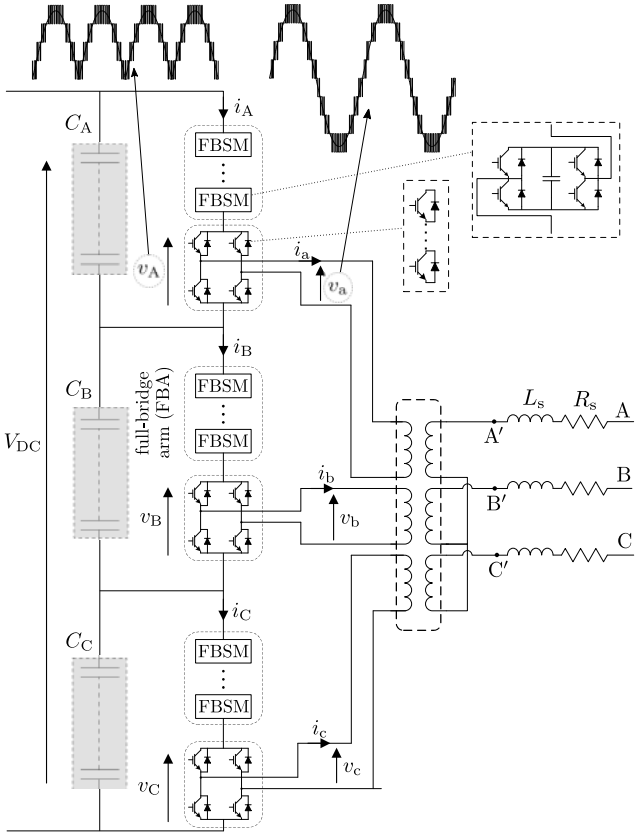

FIGURE 1. Schematic diagram of the SHMMC.

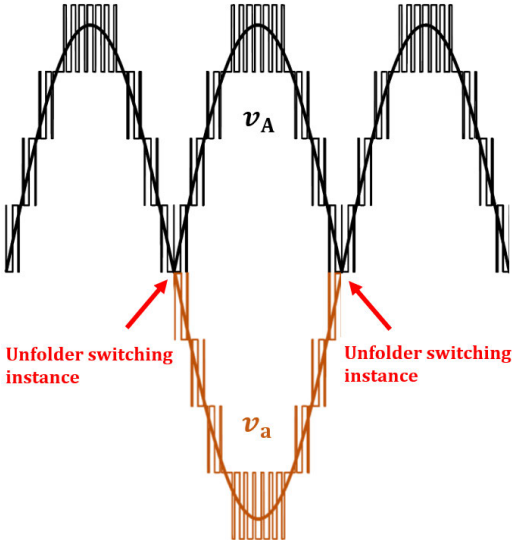

FIGURE 2. Unfolder switching occurs only when the synthesized voltage crosses zero.

higher than AC-side rms-voltage which makes it suitable for HVDC systems. Based on the theoretical analysis of the topology, a control strategy is developed to provide the four-quadrant operation of the converter while the capacitor voltage balancing is guaranteed. The feasibility of the proposed converter, as well as the effectiveness of the control strategy are validated by simulation and experimental results.

II. DESCRIPTION OF SERIES HYBRID MODULAR MULTILEVEL CONVERTER

Fig. 1 shows the schematic diagram of the proposed Series Hybrid Modular Multilevel Converter (SHMMC). Each phase of the converter consists of an H-bridge unfolder, a full-bridge arm (FBA) and a DC branch. The unfolder is switched at the zero point of the voltage synthesized across it. The FBA is formed by series connection of full-bridge submodules (FBSMs). The DC branch can be realized as a string of multiple SM capacitors. The number of capacitors in this branch is equal to the number of FBSMs in the FBA. The output voltage of the FBA is synthesized such that its sum with the fixed DC branch voltage would provide a rectified AC voltage (e.g. see v_A in Fig. 1). The unfolders can further apply the absolute phase voltages or their reverse values to the AC-sides (e.g. v_a for phase A). In other words, the absolute value of phase voltages are synthesized by controlling the number of inserted FBSMs, while their polarities are controlled by the corresponding unfolders. This allows the unfolders to be soft switched at the line frequency and near the voltage zero-crossing [23], [24]. Similar to PHMMC [12], a transformer provides the necessary isolation between the unfolders. Unlike the delta or star configuration, there is no internal/external connection between phases, as this transformer is designed such that the converter-side windings are isolated from each other. Thus, terminals from different windings must be able to withstand the phase-to-phase voltages.

In an n-level SHMMC, if the zero-voltage level is excluded, $(n-1)/2$ levels could drop across the unfolder arms. Since the unfolder operates with a voltage higher than the available switch ratings, $(n-1)/2$ switches are connected in series to tolerate the desired voltage. Thus, steady-state and transient voltage sharing among the series switches must be ensured, as most power switches do not hold voltages above their ratings and their recovery characteristics could differ. Steady-state voltage sharing can be achieved by installing high-value parallel resistors. Generally, an additional circuitry has to be provided to ensure equal transient voltage sharing. Here, there is no need for extra components, since all of the switchings in the unfolders occur in zero-voltage switching (ZVS) mode regardless of the operating condition [24]. Therefore, without any extra circuitry, transient voltage sharing is achieved.

A. ZERO VOLTAGE SWITCHING

Each phase of the proposed inverter is composed of three main components: DC link, FBA and Unfolder. The power switches used in the FBA are hard-switched and operate at the required switching frequency that limits the output harmonic content. The voltage across FBA is subtracted from the DC link voltage, so the rectified full-wave AC voltage

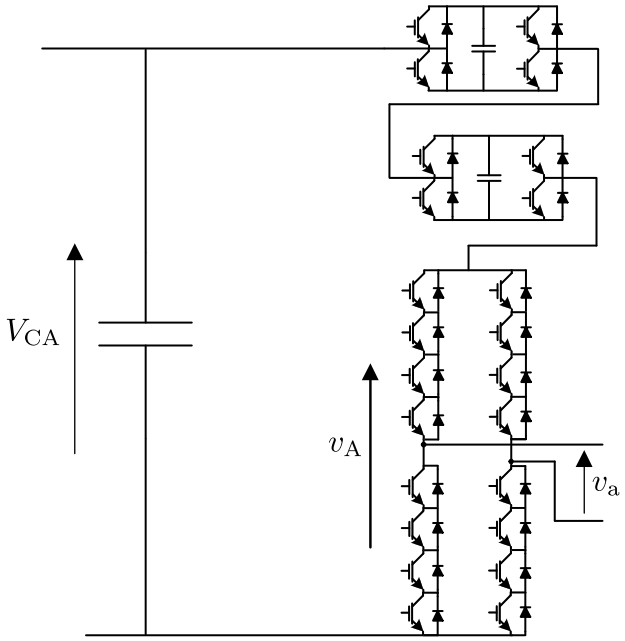

FIGURE 3. One phase of a 9-Level proposed converter.

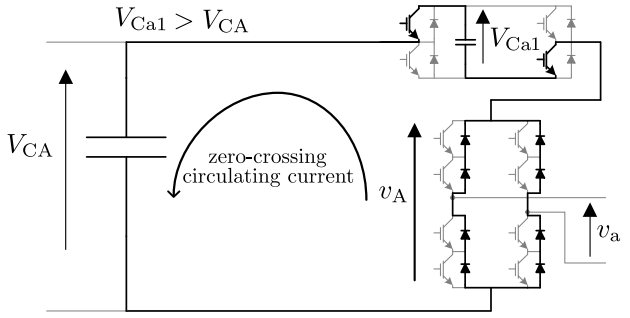

FIGURE 4. Zero-crossing circulating current in one phase of the converter.

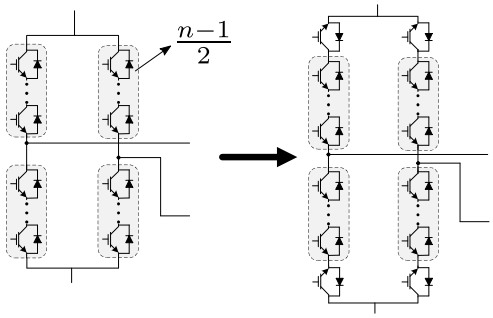

FIGURE 5. The schematic diagram of the modified unfolder.

v_A is synthesized for the next stage which is the unfolder. It must be emphasized that the unfolder is not concerned with synthesizing the rectified voltage, so its switches' gate signals remain unchanged until v_A crosses zero. Fig. 2 demonstrates the instances when the unfolders' switching occurs. This allows the unfolders to be soft switched at the line frequency and near the voltage zero-crossing.

The number of FBSMs and consequently power switches utilized in the converter depend on the system voltage and requirement. For instance, to have a 9-Level phase voltage on the AC-side, 2 FBSMs (i.e. 8 switches) are required in each phase (see Fig. 3). Furthermore, the unfolder needs 4 switches in each arm (i.e. 16 total switches). In general, for a $2k + 1$ level single-phase converter, $6k$ switches are used where two-third of them operate in ZVS mode in the unfolder.

It is worth mentioning that as a result of capacitor voltage variation, the voltage across the unfolder might be slightly higher than zero, when $v_A = 0$ is required. In practice, this small voltage is divided between the high number of series switches used in the unfolder arm, when switching occurs. The switching states of a 5-level proposed inverter is explained in more depth in Section II-C.

B. ZERO-CROSSING CIRCULATING CURRENT

Unlike MMC, there is no circulating current among different phases of the SHMMC as they are isolated from each other by a 3-phase transformer. However, is it inherently possible for current to circulate inside each phase of the SHMMC. This current which is called zero-crossing circulating current (i_{zcc}), is not continuous and only may flow when the phase voltages cross zero. For instance, the phase A of a 5-level converter is shown in Fig. 4, when $v_A = 0$ is required. In this switching state, if V_{CA} is slightly smaller than V_{Ca1}, which can happen as a result of capacitor voltage variation, v_A becomes a small negative voltage. This negative voltage turns on the unfolder diodes, thus the current can circulate through the FBA. Adding one reversed IGBT in each arm of the unfolder as shown in Fig. 5, could block the possible small negative v_A. It should be noticed that the maximum voltage-drop across the reversed IGBT occurs, when the HBA and FBA capacitors are within their lowest and highest acceptable voltage range, respectively. Therefore, this IGBT must withstand the predefined capacitor voltage ripple, ΔV_{ripp} multiplied by the number of FBSMs which equals to $(n-1)/2 \times \Delta V_{ripp}$. This implies that in case of high number of levels, more than one reversed IGBT might be required. Furthermore, to achieve the desired reliability, extra IGBTs, could be also considered as redundancies.

Fig. 6 demonstrates the switching principle of the unfolder at voltage zero-crossing transition for both cases of leading and lagging currents. It can be seen that at any stage of unfolding transition, there is at least one reversed IGBT blocking the zero-crossing circulating current.

C. SWITCHING PRINCIPLE IN A 5-LEVEL SHMMC

The phase A of a 5-level SHMMC is shown in Fig. 7. The voltage of the DC-link and FBSM capacitors are both equal to E. The switching function $d_i (i = 1, 2)$ is defined so that $d_i = 1$, when upper switch of the SM-leg is ON and the lower switch is OFF and $d_i = 0$, for the reverse case. In addition, $s_a = 1$ when $v_a \geqslant 0$ and $s_a = 0$ when $v_a < 0$. Therefore, v_a can take any of the values of 0, $\pm E$ or $\pm 2E$.

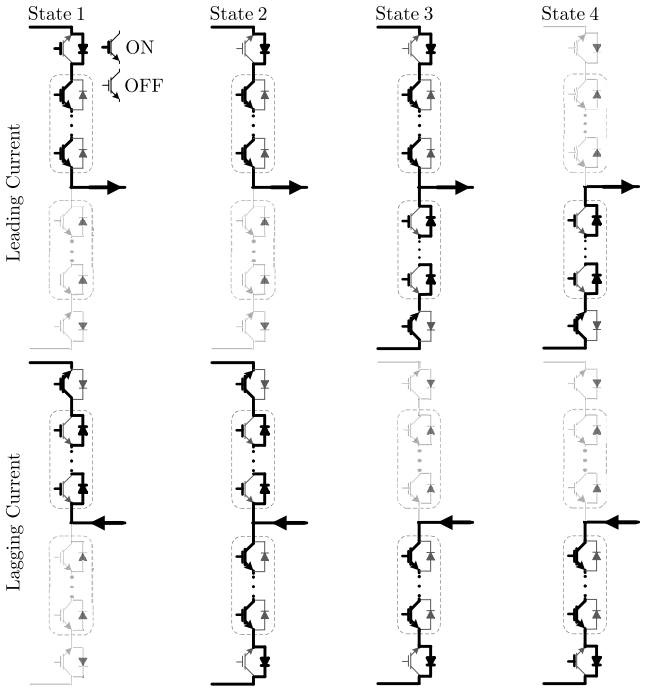

FIGURE 6. Description of zero-crossing transition in the modified unfolder.

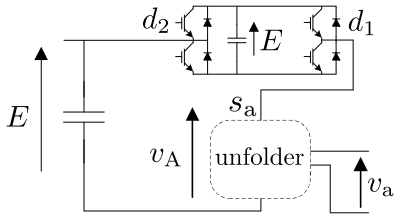

FIGURE 7. The schematic diagram of a 5-level single-phase SHMMC.

TABLE 1. Switching states of a 5-level SHMMC.

Switching state	d_1	d_2	s_a	v_A	v_a
1	0	1	0	0	0
2	0	0	1	E	$+E$
	1	1	1	E	$+E$
3	0	0	0	E	$-E$
	1	1	0	E	$-E$
4	1	0	1	$2E$	$+2E$
5	1	0	0	$2E$	$-2E$

Table 1 lists all the possible switching states in one phase of the converter. Similar tables could be developed for the other phases independent from each other.

D. COMPONENT COUNT COMPARISON WITH ALTERNATIVES

Table 2 presents the component count of the MMC, PHMMC, SHMMC and hybrid NPC/MMC topologies based on their total number of capacitors which is a strong indicator of the energy storage requirement. In a 3-phase MMC constructed

TABLE 2. Component count compariosn between MMC, NPC/MMC, PHMMC and SHMMC.

Parameter	MMC	NPC/MMC	PHMMC	SHMMC
# of arm inductors	6	6	0	0
# of capacitors	g	g'	g''	g'''
# of switches*	$2g$	$2g'$	$2g''$	$2g'''$
# of switches**	0	$4g'$	$4g''$	$4g'''$
DC filter	×	×	✓	×
$V_{DC}/V_{C\text{-}SM}$	$g/6$	$g'/4$	$2g''/\pi$	$g'''/2$
Voltage gain V_{DC}/V_{AC_rms}	2.45	3.14	2.70	3.33

* high-frequency hard-switched
* line-frequency soft-switched

with the HBSMs, if the total number of capacitors is g, then the total number of hard-switched IGBTs would be $2g$, as there are two IGBTs per capacitor in each submodule. Also, the DC-link voltage equals the sum of all capacitor voltages in one arm. As there are 6 arms in an MMC, the DC-link voltage equals $gV_{C\text{-}SM}/6$, where $V_{C\text{-}SM}$ is the average voltage of the HBSM capacitor [25]. Similar information is obtained for PHMMC [12], hybrid NPC/MMC [26] and SHMMC. The DC-link capacitors in the SHMMC are also counted as a string of multiple SM capacitors. To be able to compare these converters, they must be designed for the same HVDC system, i.e. equal DC-link voltage and current. Thus,

$$g/6 = g'/4 = 2g''/\pi = g'''/2 \rightarrow \mathbf{g' \approx 0.66g}\ ,\ \mathbf{g'' \approx 0.26g}\ ,\ \mathbf{g''' \approx 0.33g}.$$

It can be concluded that both the PHMMC, and SHMMC have fewer components compared to the MMC. Although, the SHMMC requires more capacitors and switches, it provides a harmonic-free DC-link voltage, which obviates the necessity of a DC filter. Moreover, the SHMMC provides a DC-link voltage 3.33 times higher than the AC-side phase-voltage (Section III).

III. CAPACITOR VOLTAGE BALANCING

In [27], the capacitor voltage balancing of an AC/AC multilevel converter is studied analytically. Similar studies are done here for the proposed converter in this section. The phase A voltage and current in Fig. 1 are presented as:

$$\begin{cases} v_a = \sqrt{2}V\sin(\omega t)\ ,\ v_A = \lambda_a.v_a\ ,\ \lambda_a = \text{sign}(v_a) \\ i_a = \sqrt{2}I\sin(\omega t - \varphi)\ \ ,\ \ i_A = \lambda_a.i_a. \end{cases} \quad (1)$$

According to Fig. 1, the instantaneous power going through phase A FBA, $p_{FA}(t)$, is calculated as:

$$p_{FA}(t) = i_A \times (v_A - v_{CA}) \quad (2)$$

where v_{CA} is the voltage across C_A and it is assumed to be equal to $V_{DC}/3$. Under the steady-state conditions, the stored energy of the FBA must be constant. This leads to the

following equations to estimate the gain of the converter:

$$\begin{aligned} 0 &= \int_T p_{\mathrm{FA}}(t).dt = \int_T i_{\mathrm{A}} \times (v_{\mathrm{A}} - \frac{V_{\mathrm{DC}}}{3}).dt \\ &= VI\cos(\varphi) - \frac{2\sqrt{2}}{3\pi} V_{\mathrm{DC}} I \cos(\varphi) \\ \Rightarrow V_{\mathrm{ratio}} &= \frac{V_{\mathrm{DC}}}{V} = \frac{3\pi}{2\sqrt{2}} \approx 3.33 \end{aligned} \tag{3}$$

Therefore, achieving capacitor voltage balancing requires the converter to have a fixed voltage ratio of 3.33. However, for any practical application, voltage gain control is required, especially, to adjust the reactive power exchange with the AC network. The AC-side voltage can be controlled by injecting harmonics, such that the ratio between the average rectified AC voltage and its fundamental component is regulated. Meanwhile, the unfolders are remained soft switched (i.e., no PWM). The injected harmonics are required to be cancelled in line-line voltages and thus triplen harmonics (3, 9, 15, …) are only accepted. In the simplest case, the voltage control is performed using only third harmonic addition. This method is recently used for increasing loadability of existing HVAC lines by 33% [28]. Based on this strategy, the AC-side voltages in a 3-phase converter shown in Fig. 1 can be represented as:

$$\begin{cases} v_{\mathrm{a}} = \sqrt{2}V\sin(\omega t) + \sqrt{2}V_3\sin(3\omega t + \beta) \\ v_{\mathrm{b}} = \sqrt{2}V\sin(\omega t - 2\pi/3) + \sqrt{2}V_3\sin(3\omega t + \beta) \\ v_{\mathrm{c}} = \sqrt{2}V\sin(\omega t - 4\pi/3) + \sqrt{2}V_3\sin(3\omega t + \beta) \\ v_{\mathrm{U}} = \lambda_{\mathrm{u}} v_{\mathrm{u}} \ , \quad \lambda_{\mathrm{u}} = \mathrm{sign}(v_{\mathrm{u}}) \ , \quad u = a, b, c. \end{cases} \tag{4}$$

The neutral terminal of the transformer is not grounded, thus the added third harmonic voltage would not contribute to the power flow. Similar to the previous section, the capacitor voltage balancing criterion is studied as:

$$\begin{aligned} 0 &= \int_T p_{\mathrm{FA}}(t).dt = VI\cos(\varphi) \\ &\quad - \frac{\sqrt{2}V_{\mathrm{DC}}}{3} \int_T \lambda_{\mathrm{a}} I \sin(\omega t - \varphi) \\ \Rightarrow V_{\mathrm{ratio}} &= \frac{V_{\mathrm{DC}}}{V} = \frac{3\cos(\varphi)}{\sqrt{2}\int_T \lambda_{\mathrm{a}}\sin(\omega t - \varphi)} \end{aligned} \tag{5}$$

where λ_{a} may be represented as:

$$\begin{cases} \lambda_{\mathrm{a}} = \mathrm{sign}(V\sin(\omega t) + V_3\sin(3\omega t + \beta)) \\ \quad = \mathrm{sign}(\sin(\omega t) + \gamma\sin(3\omega t + \beta)) \\ \gamma = V_3/V \ , \quad -\pi \le \beta \le \pi \end{cases} \tag{6}$$

Adding third harmonic voltage appears as a phase-angle shift in λ_{a}, such that the zero-crossing point of the AC voltage is shifted by δ without affecting the fundamental component (see Fig. 8a). Different values of δ could be achieved by adjusting γ and β in Eq. (6) as shown in Fig. 8b. Considering the impact of power factor in Eq. (5), the converter's voltage gain is sketched versus β when $\gamma = 0.3$ and also versus power factor when $\beta = 0.8\pi$ in Figs. 8c and 8d, respectively.

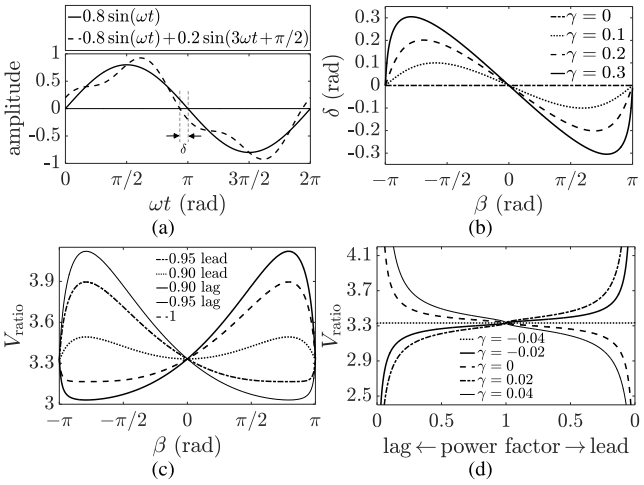

FIGURE 8. (a) Adding third harmonic voltage shifts the zero-crossing point (b) δ in terms of different β and γ (c) voltage gain in terms of different β and power factor ($\gamma = 0.3$) (d) voltage gain in terms of different γ ($\beta = 0.8\pi$).

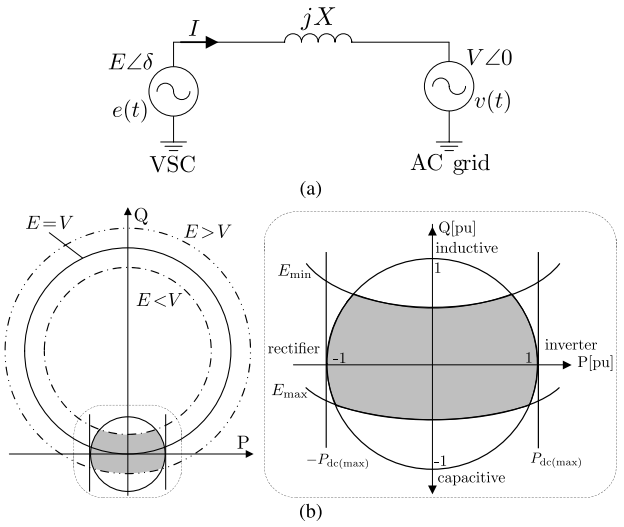

FIGURE 9. (a) Simplified single-line diagram of converter-grid circuit (b) *PQ* chart of the converter considering VSC limitation.

A. POWER CAPABILITY OF THE PROPOSED CONVERTER

Fig. 9a shows the simplified single-line diagram of the VSC-HVDC station connected to the AC grid. The injected real and reactive powers to the grid are calculated as:

$$P = \frac{EV}{X}\sin\delta \ , \ Q = \frac{V^2 - EV\cos\delta}{X}. \tag{7}$$

where $E\angle\delta$ and $V\angle 0$ are the voltage phasors of the converter and AC grid, respectively and X is the filter reactance. In rectifier mode, $e(t)$ is leading $v(t)$ and active power flows from the AC to the DC side while in inverter mode, $e(t)$ is lagging $v(t)$. Also, the converter can support the AC system with reactive power injection/consumption by regulating its voltage amplitude and phase angle (E, δ). The PQ chart of the proposed converter considering its limitation is sketched

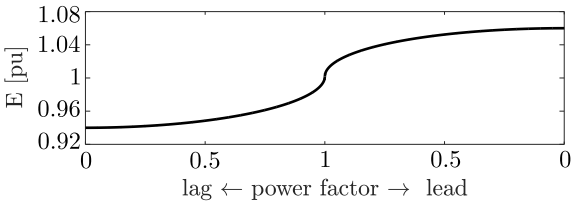

FIGURE 10. VSC's output voltage (*E*) in different power factor (inverter mode).

in Fig. 9b. The first one is the maximum allowable current of the IGBT which can be interpreted as maximum MVA circle in the power plane with the radius of 1 pu. The minimum/maximum output voltage magnitude ($E_{\min}, E_{\max}$) determines the reactive-power capability of the converter as shown in Fig. 9b which depends on the DC-link voltage and modulation index. In the proposed converter, the filter reactance is designed to be $X = 0.06$ pu. In this case, to assure the power capability of the converter is only limited by its maximum allowable current of the IGBT, the output voltage magnitude must be adjustable within $0.94 \text{ pu} \leqslant E \leqslant 1.06 \text{ pu}$, as shown in Fig. 10 for inverter mode. From the previous section, it can be shown that this voltage range can be provided by a third harmonic injection in the range of $-0.12 \leqslant \gamma \leqslant 0.12$.

IV. CONTROL STRATEGY

The SHMMC could be controlled in either the *abc* frame where a PR controller is used [29], [30] or in the *dq* frame as shown in Fig. 11. To control the AC-side currents in the *dq* frame, a synchronization mechanism is achieved through a Phase-Locked Loop (PLL) on each side of the converter with capability of input DC-error rejection [31]. A reference generator is utilized to provide the reference currents ($i_{\text{d,q}}$) for the next control stage. Here, P_{ref} determines the amount and direction of transferred real power, whilst the reactive power, Q_{ref} is regulated at an arbitrary value within the ratings of converter. A standard current controller in the *dq* frame is depicted in Fig. 11, which provides the expected active and reactive power exchange with the grid. If the capacitor voltages have some oscillations, harmonics can be rejected from the AC-side currents and voltages if a modified PWM is used [32]. To ensure the power balance, a slow outer control loop is employed such that the total energy stored in the capacitors is effectively regulated at all time. As mentioned in the previous section, the power flow in the FBA could be controlled by injecting a third harmonic voltage. Fig. 11 also illustrates the process of providing γ, which is then used to generate the third harmonic component. n_{C} is the total number of capacitors in each FBA, which is equal to $(n-1)/4$ in an n-level converter. It is also necessary to evenly distribute the FBA energy among the SM capacitors by selecting the proper SMs at each time. This is done based on the sorted queue of capacitor voltages and FBA current direction [33].

TABLE 3. Parameters of the study system.

Parameter		Rating
Power rating	$S_{\text{conv.}}$	40 MVA
Grid voltage (line-line rms)	V_{s}	27 kV
DC-link voltage	V_{DC}	54 kV
SM capacitor	C_{SM}	4 mF, 2 kV
DC-link capacitor	$C_{\text{A,B,C}}$	0.5 mF, 18 kV
No. of SMs in FBA	n_{C}	9
Mean SM capacitor voltage	E	2 kV
Filter+Grid inductance	L_{s}	0.5 mH
Filter+Grid resistance	R_{s}	10 mΩ

V. SIMULATION RESULTS

Simulation results are obtained using MATLAB/Simulink for a 37-level 40 MVA SHMMC shown in Fig. 12. Nine FBSMs per phase have been used in the simulated model. In practical HVDC system, the number of level could be higher. However, to demonstrate the converter's principal of operation, selecting a 37-level version is satisfactory. In the nominal operating condition, the SM capacitors are set to an average voltage of 2 kV. Table 3 lists the main parameters used for the simulation studies. A multi-carrier SPWM strategy obtained by the control diagram shown in Fig. 11 is used to regulate transferred active and reactive powers. The switching frequency of the SM-IGBTs is approximately 200 Hz, while the unfolder switches operate at the AC line frequency (here 60 Hz). In practice, the number of levels is higher due to the higher grid voltage and power ratings and as a result, the switching frequency of the SM-IGBTs is reduced. Currently, IGBTs wuth power rating of 4.5 kV and 3000 A are offered for MMC topologies up to multiple GWs and higher [34].

A. STEADY-STATE OPERATION

Fig. 13 shows the steady-state results for a case that 32 MW active power is injected to the grid, while power factor is unity. The grid ($v_{\text{sA,sB,sC}}$) and the converter phase voltages ($v_{\text{A',B',C'}}$) are presented in Fig. 13. It can be seen that the third harmonic components of the phase voltages are cancelled out and the desired fundamental voltage is well synthesized. The total harmonic distortion (THD) of the line current is 1%. The peak-to-peak ripple SM-capacitor voltages (see Fig. 13) of the phase A is approximately 8%, which may vary due to the PQ operating point of the converter. In practice, similar to the MMC, the number of levels could be as high as few hundred levels. Thus, the voltage and current output waveforms become almost sinusoidal and AC filters may not be required.

B. TRANSIENT OPERATION

A number of active and reactive power changes (P_{ref} & Q_{ref} in Fig. 11), are applied to the converter. The transient response of the converter are presented for the line currents in the *dq* frame (i_{d}^*, i_{d}, i_{q}^* and i_{q}, in Fig. 11) and the total energy

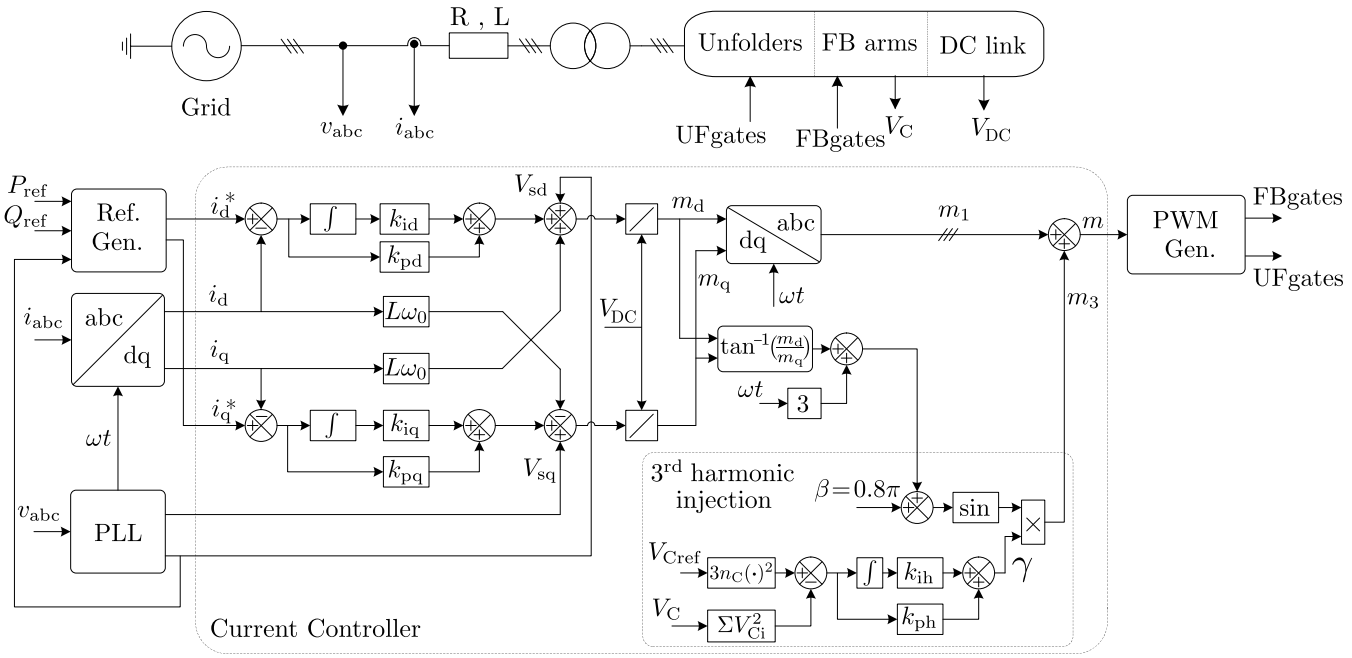

FIGURE 11. The schematic diagram of the control strategy.

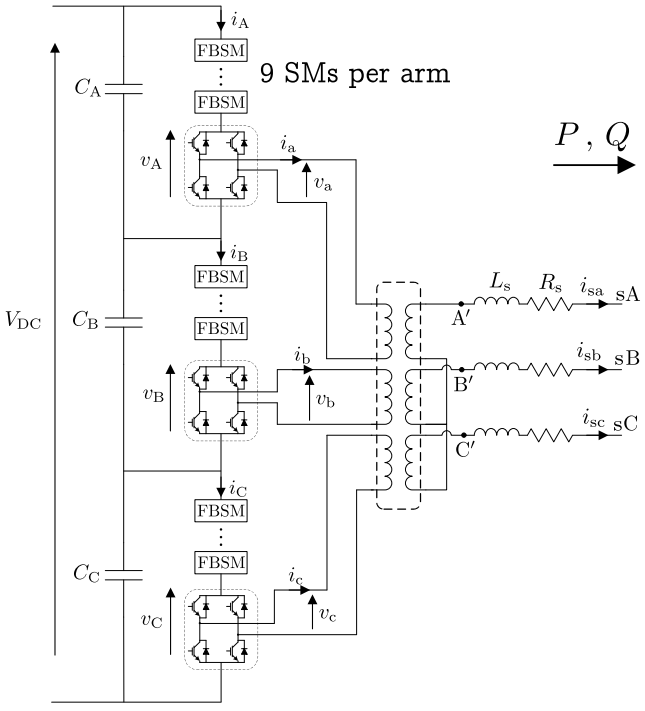

FIGURE 12. Schematic diagram of the studied SHMMC.

stored in the SM-capacitors. As shown in Fig. 14, the line currents track their references well, so the active and reactive powers are properly controlled. During each transient, a small error may occur in the total energy stored in the capacitors as shown in Fig. 14, which will be compensated in a few cycles. Thus, the implemented control strategy is able to ensure that the converter stored energy is properly regulated during transients.

TABLE 4. Experimental parameters.

Parameter		Rating
Power rating	$S_{conv.}$	0.5 kVA
SM capacitor	C_{SM}	820 μF
No. of SMs in FBA	n_C	2
Filter inductance	L_S	5 mH

VI. EXPERIMENTAL RESULTS

The SHMMC topology is proposed for high-power HVDC applications with a few hundreds of levels. As it was not feasible to build such a converter in our laboratory, a low-scale single-phase converter shown in Fig. 15 with a power rating of 0.5 kVA was constructed for experimental studies. However, it was made sure that the combination of simulation and experimental studies would cover different aspects of the proof of concept. The control system is implemented on a dSPACE-MicroLabBox unit. The DC link is connected to a DC grid (100 V), while the AC-side feeds a resistive load operating in 90 Vrms and 60 Hz. The parameters of the experimental setup can be found in Table 4. The switching frequency of the SM-IGBTs is approximately 2.5 kHz, while the unfolder switches are operating at AC line frequency (60 Hz). In practice, the number of levels is higher, thereby reducing the switching frequency. For a single-phase SHMMC without third-harmonic injection, the voltage ratio is constant and almost equals $V_{DC}/V_{AC\_rms} \approx 1.11$. The converter AC-side waveforms in the steady-state condition

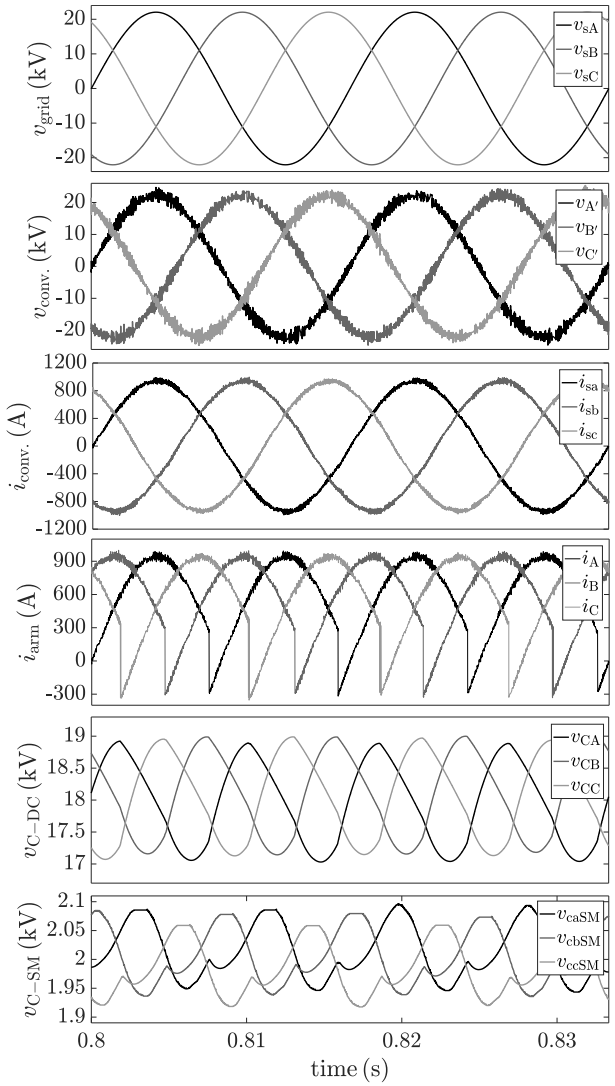

FIGURE 13. Steady-state simulation results ($P = 32$ MW, $Q = 0$ MVAR).

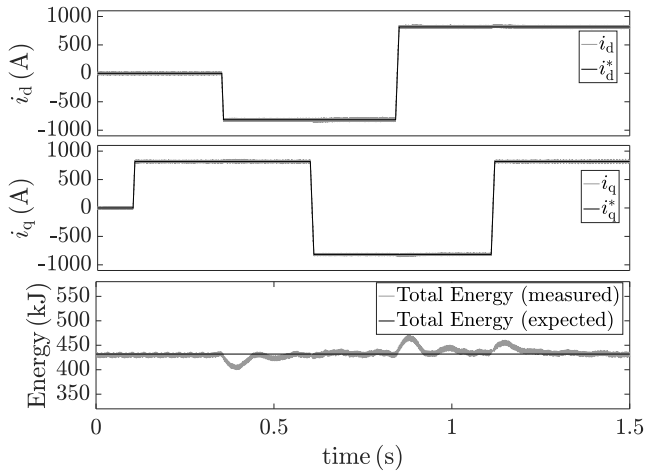

FIGURE 14. Transient simulation results.

are shown in Figs. 16a and 16b respectively. It can be seen that the output voltage is well synthesized with the expected amplitude and frequency. The submodule capacitor must be

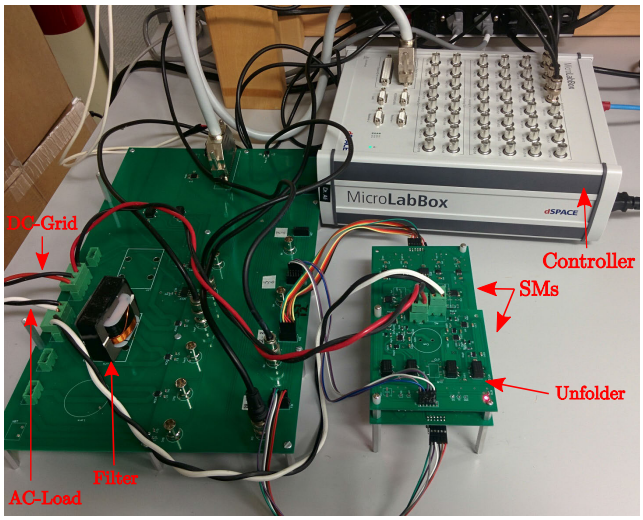

FIGURE 15. A view of the experimental setup.

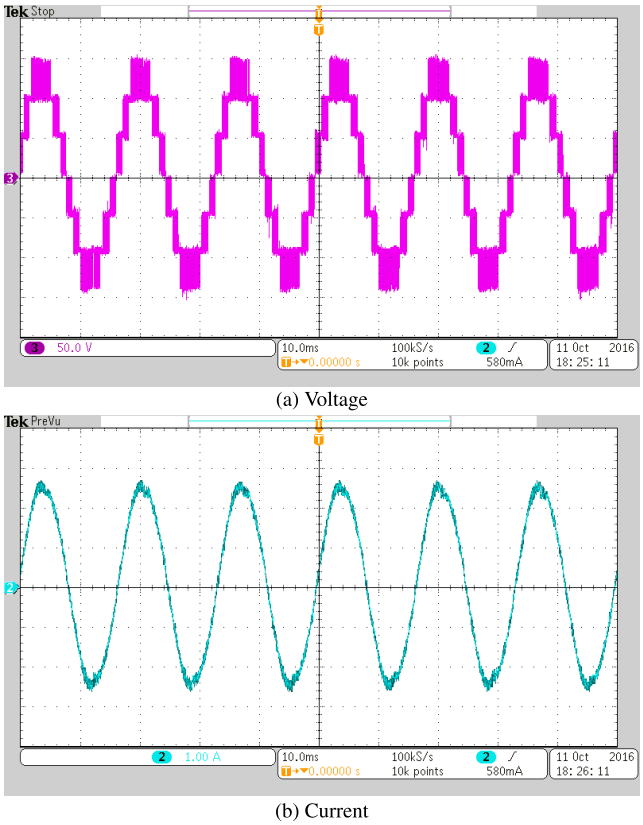

FIGURE 16. Converter AC-side in steady state.

properly sized to meet the required regulatory power system requiremnt for voltage ripple. The filter inductor is designed such that the harmonic content of the AC current is acceptable (THD of 2.9%). In practice, with increase in system voltage and number of levels, smaller or even no inductor could be used. In order to evaluate the dynamic response of the capacitor voltage balancing strategy, the load is suddenly increased/decreased while the SM capacitor voltages are

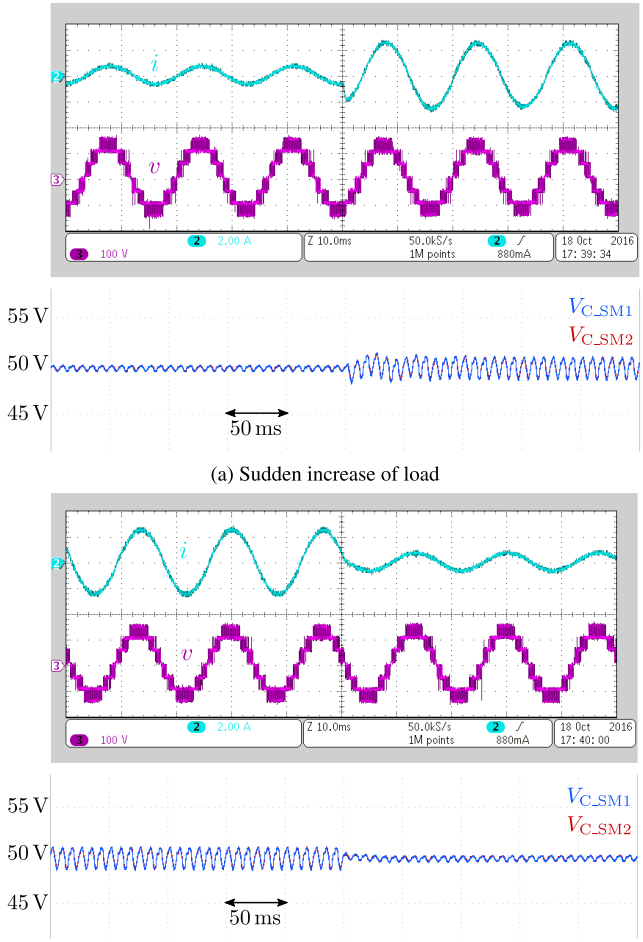

FIGURE 17. Dynamic response of the converter to the load change.

monitored. As shown in Fig. 17, the proposed control strategy (see Fig. 11) is well capable of carrying the capacitor voltage balancing task.

VII. CONCLUSION

In this paper, a novel converter called the SHMMC intended for HVDC systems is proposed. The SHMMC requires fewer components compared to the MMC and offers soft switching for almost two third of its power switches. Although the SHMMC has more components compared to PHMMC, it does not require any DC filter and provides a higher DC-link voltage. The proposed control strategy ensures capacitor voltage balancing is achieved while providing the required voltage ratio regulation. The capability and salient features of the proposed converter along with its control strategy are confirmed by simulation and experimental results.

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