IEEE Access
Multidisciplinary | Rapid Review | Open Access Journal

Received 26 April 2024, accepted 21 May 2024, date of publication 28 May 2024, date of current version 10 June 2024.

Digital Object Identifier 10.1109/ACCESS.2024.3406583

SURVEY

Built-In Self-Test of Millimeter-Wave Integrated Front-End Circuits: How Far Have We Come?

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The work was supported by the Open Access Publication Fund of TU Braunschweig.

ABSTRACT With automotive radar and 5G/6G communications, mass-market applications for millimeter-wave circuits in silicon technologies have been identified or established in recent years. For high-volume, millimeter-wave integrated circuits, operating roughly between 30 GHz and 300 GHz, testability is a major concern, both from an overall cost as well as a quality assurance perspective. A solution for cost effective, low-overhead test of millimeter-wave integrated circuits is the integration of built-in self-test (BIST) features into the high-frequency front-end. Because BIST is an emerging topic in high-frequency circuit design, the field is still very fragmented. A plethora of different system concepts as well as building blocks have been proposed in recent years. This paper tries to provide a comprehensive overview of the state of the art in millimeter-wave BIST in an attempt to drive the field towards identification of standardized self-test solutions.

INDEX TERMS Built-in self-test, CMOS, millimeter-wave transceivers, SiGe, silicon.

I. INTRODUCTION

Automotive radar with a market volume around $7B in 2022 [2], with millions of integrated circuits (ICs) being shipped [3], [4], has become the standard-bearer for mass-market applications in the millimeter-wave frequency range ($\approx$ 30 GHz $-$ 300 GHz). For communications, frequency bands around 40 GHz have been licensed [5]. There is an on-going vivid debate about the standardization and commercialization of new high-volume millimeter-wave applications up to and above 100 GHz [6], [7]. Different research groups have already demonstrated the technical feasibility of radar and communications circuits at 60 GHz [8], [9], [10], [11], [12], [13], 120 GHz [8], [14], [15], [16], and 140 GHz [17], [18], [19], [20], [21].

Launching a high-volume product is synonymous with the need for automated test. Quality assurance is central in preventing the shipment of defective or out-of-specification chips to customers. At millimeter-wave frequencies, reliable and repeatable measurement of integrated circuits is a challenge in itself. Recently, on-wafer broadband network analysis solutions from DC to 220 GHz that support automatic wafer stepping have started to become commercially available [22], [23]. Nevertheless, it can be expected that automatic test of millimeter-wave ICs will continue to be a complicated and expensive procedure in the near future. For example, estimations for more traditional mixed-signal chips already show that test can make up to 50 % of the total IC cost [24]. Additionally, even if the die is found to be functional before shipping, its performance after it has been deployed in a complex system or after it has been subjected to environmental influences for some time is not guaranteed.

Integration of built-in self-test (BIST) functionality into millimeter-wave front-end circuits is an attractive prospect because of the issues highlighted above. It promises to reduce the cost of production test and enable in-situ monitoring of internal signals and calibration of millimeter-wave ICs. While BIST has been a standard feature of digital ICs for a long time [25], [26], [27], [28], [29], its proliferation into millimeter-wave circuits is naturally hindered by the complex realities of high-frequency circuit design. Nonetheless, the number of publications concerning this topic has steadily been rising in recent years. Kissinger et al. outlined their vision for BIST of millimeter-wave ICs as early as 2010 [30].

The associate editor coordinating the review of this manuscript and approving it for publication was Jagadheswaran Rajendran.

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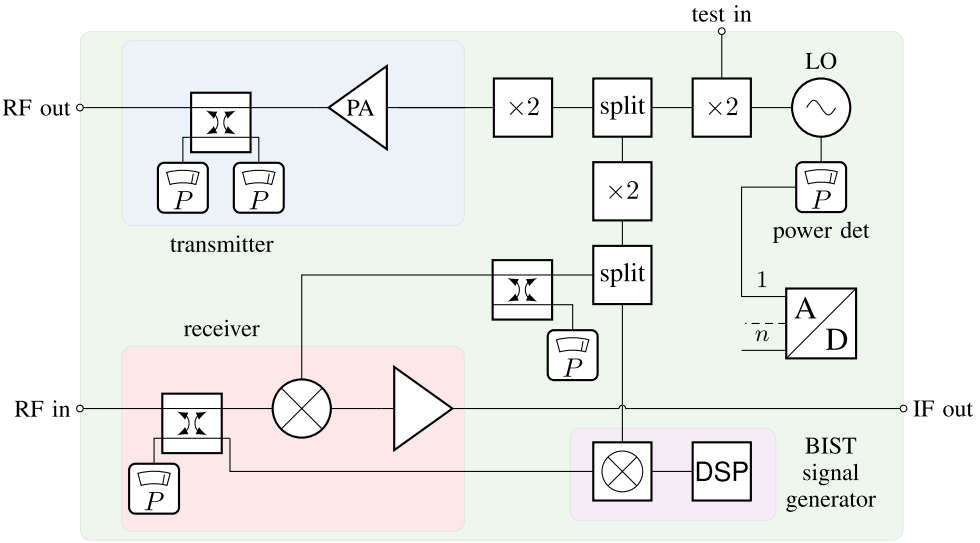

FIGURE 1. Simplified block diagram of the BIST structure of the radar transceiver from [1]. Several different direct test methods are used.

Since more than a decade has passed, it seems to be time for another review of the state of the art in millimeter-wave built-in self-test.

To give the reader an idea of what millimeter-wave BIST looks like today, an example of an automotive radar transceiver self-test is shown in Fig. 1. It is a simplified block diagram of the 2-transmitter, 6-receiver chip presented in [1]. Starting with the local oscillator (LO) in the top right corner, its functionality can be monitored via a power detector that is attached to the oscillator tank. The LO output is then fed to a frequency doubler which can also be driven by an external test signal. After a signal splitter and another doubler, the transmit signal reaches the power amplifier (PA). Positioning a directional coupler with power detectors at the coupled and isolated ports between radio-frequency (RF) output and PA enables the measurement of both transmitted and reflected power.

The other half of the LO signal, split off before the transmitter, is directed to both the receive mixer and a dedicated BIST signal generator for receiver test. Before it reaches the receiver, the signal's power is again measured via another coupler and power detector combination. A third directional coupler is placed between the RF input and the receive mixer. At its isolated port, as seen from the mixer, a power detector is placed whereas the output of the BIST signal generator is fed to the coupled port. Via the power detector, the signal strength of the test signal can be determined, and, knowing the coupling factor of the direction coupler, the conversion gain of the receiver can be extracted from the intermediate frequency (IF) output. The digital interfaces necessary for the radar signal processing are leveraged to digitize the outputs of the power detectors and generate the test signal for the receiver.

From this example, it is clear that to monitor a complete signal chain, several different types of blocks have to be added to the circuit. These encompass sensors, couplers, and test signal generators. To warrant this overhead in both chip and design resources, the BIST needs to result in a measurable simplification of the IC test while still providing sufficient accuracy. As the BIST components are located on the IC under test, they have to be robust against process, voltage, and temperature (PVT) variations themselves. Critical blocks, such as PA and LNA, have high enough impact on the system performance that specific tests can be developed for them. In other places of the signal chain, generic, low-overhead approaches are more appropriate. The re-use of BIST components inside a single design as well as between different designs (possible even at different frequencies) can help to minimize the design effort. Furthermore, the BIST components should not interfere with the normal operation of the circuit under test (CUT). This means that the impact on the matching conditions of the CUT's interfaces as well as the signal levels has to be minimal. Finally, the power and area consumption of the BIST has to be kept as low as possible.

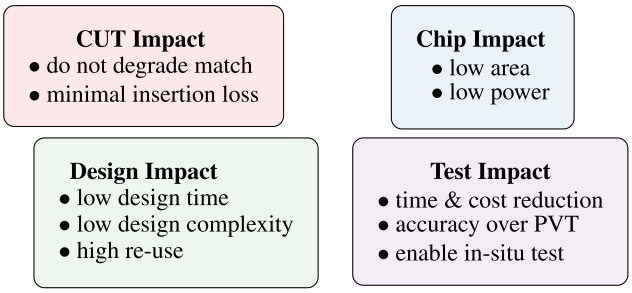

FIGURE 2. Requirements on millimeter-wave BIST.

All these requirements are summarized in Fig. 2. As we delve into the remainder of this paper, it becomes evident that published BIST methods and building blocks have

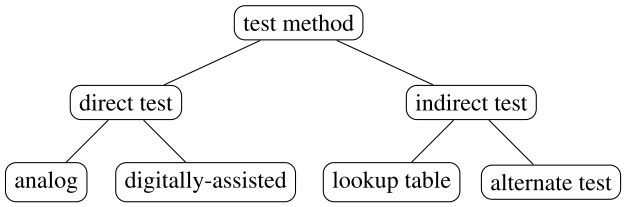

FIGURE 3. Classification of test methods.

predominantly focused on fulfilling the criteria labeled as "CUT Impact" and "Chip Impact". However, the broader impact on testing the IC is rarely quantified. Unfortunately, the influence of BIST on design time and complexity often receives insufficient attention. Given that BIST for digital circuits derives significant benefits from its largely automated insertion into the system, future research in millimeter-wave BIST should prioritize design automation. As we explore different building blocks, we will highlight opportunities in this direction. Finally, any novel BIST approach must be evaluated for its resilience against variations. For example, if the uncertainty of an integrated power measurement is larger than the expected variation of the measured power, the addition of the BIST does not provide any advantage.

In the following, we will walk through the different components of millimeter-wave BIST systems focusing on implementations in silicon technologies (CMOS, SiGe). The lower integration density of typical III-V millimeter-wave ICs will likely not warrant the overhead of including BIST (although this could change in the future as research on heterogeneous integration of silicon and III-V technologies is heating up [31], [32], [33], [34]). Due to the prevalence of automotive radar, many examples focus on the 76 GHz − 81 GHz bands. Nevertheless, the large number of test circuitry that has been developed at both lower and higher millimeter-wave frequencies is featured to give an overall rounded picture of the state of the art. Section II, directly following this introduction, tries to categorize BIST approaches on a high level of abstraction. In Section III, different ways to generate test signals are presented. The injection of the generated test signals into the CUT and ways to interface sensors with the CUT are the focus of Section IV. Section V deals with different detectors and sensors proposed for millimeter-wave BIST before Section VI concludes this review.

II. TEST METHODS

In general, we can classify test approaches into direct and indirect methods (see Fig. 3). Direct methods directly interface with the high-frequency path of the CUT. The previous example in Fig. 1 applies several direct test methods. Direct test is popular because it lends itself to straightforward extraction of typical performance metrics such as gain. However, the design of the required components is laborious as they need to be able to process millimeter-wave signals without disrupting the sensitive

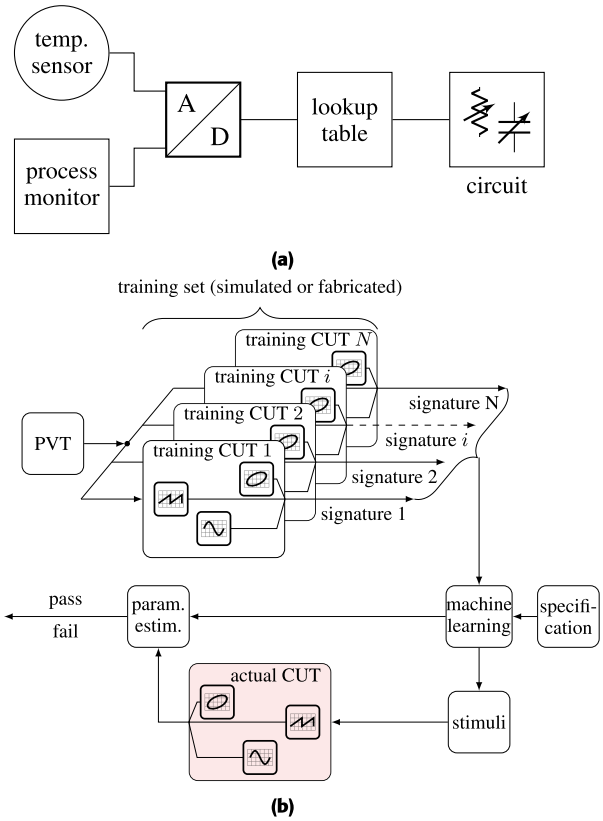

FIGURE 4. Indirect test methods: Calibration via lookup table (a) and alternate test (b).

CUT by degrading the matching, introducing loss or noise. Additionally, the required BIST components operate at millimeter-wave frequency and are therefore area and power hungry. Nonetheless, many published BIST systems take the direct approach. Consequently, most components discussed in the following sections are geared towards direct test. While direct test can be purely analog, modern transceiver ICs already contain significant digital signal processing power. BIST components should unquestionably leverage these capabilities. The accuracy of most sensor types can be improved by digitally-assisted trimming and calibration.

On the other hand, there are approaches to extract high-frequency performance parameters via low-frequency circuits that are not directly connected to the CUT. We can classify these as indirect methods. Indirect test relies on low-frequency sensors that can detect process, voltage, and temperature (PVT) variation. The simplest way to leverage the collected sensor information is to pre-characterize the relationship between high-frequency performance and sensor outputs. This can be achieved with simulation or measurement of a sample batch. Calibration values can then be stored in a lookup table (LUT) to tune the performance of the high-frequency blocks, as illustrated by Fig. 4. Because the LUT is pre-computed, the computational overhead is low. The calibration can be repeated regularly even while the IC is deployed in the system. Accurate modeling

of all components is mandatory as there is no feedback whether the high-frequency part responds in the desired way. A lack of direct monitoring of the signal path also means that failures occurring during operation, such as trace breakage or overheating, cannot be detected. The automotive radar transceiver from [35] is an example for this indirect approach: a temperature sensor, threshold voltage monitor, and capacitance monitor are used to calibrate power detectors and amplifiers, complimenting other direct test features.

An alternative approach to indirect test, the aptly named "alternate" test, has been successfully applied to analog circuits for quite some time [36], [37]. It relies heavily on the use of machine learning. As shown in Fig. 4b, a training set of the CUT is subjected to PVT variation. This can either be done in (Monte Carlo) simulation or via the fabrication of a test batch. The outputs of the different sensors in each of the training set's CUTs form a signature for that specific CUT. Together with the specification for the different performance parameters (gain, noise figure, etc.), these signatures are fed to a machine learning algorithm. The resulting computer model is used for both: identification of a set of time domain stimuli driving the actual CUT and the estimation of the CUT's performance parameters from the responses of its internal sensors to these stimuli.

Due to its automated nature, alternate test is able to find complexly shaped time-domain stimuli that allow the extraction of several performance parameters with a low number of measurements, minimizing the actual test time. A disadvantage of this approach is that it hinges on the quality of the training data. If the models are not sufficiently accurate or the sample size is too small, the predictive power of the machine-learning algorithm suffers greatly [37].

Examples of alternate test in millimeter-wave circuits include [38] where different process monitors such as common-source and cascode stages, resistors, capacitors, etc. are placed on the same 65 nm-CMOS die as a 60 GHz LNA. The process monitors are completely transparent to the CUT. A simulation study shows that the approach is able to extract the linear and nonlinear performance parameters of the LNA with sufficient accuracy. In [39], a similar approach is used to test a 65 GHz-PA in 55 nm-CMOS. In contrast to [38], the approach is verified with a fabricated batch of 21 samples.

Clearly, both direct and indirect methods have their advantages and disadvantages. The penalty in area, power, and design time of direct test is high if it is implemented on a large scale. However, it gives direct information about the CUT at the time of test. Indirect test always relies on the accuracy of models or previously collected test data, but can more easily scale in large and complex systems. For these complex systems, a combined approach, as shown in Fig. 5, should be investigated. With recent advances in artificial intelligence (AI), it might also be feasible to use the data generated by direct monitors as an input to the indirect test components during the time of test to improve their accuracy. In the other direction, the results of the indirect monitors might be used to re-calibrate the direct ones.

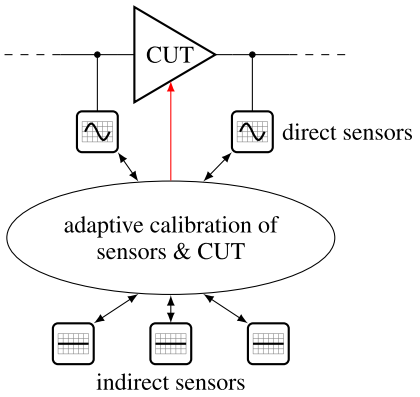

FIGURE 5. Adaptive calibration of sensors and CUT by fusing direct and indirect test approaches.

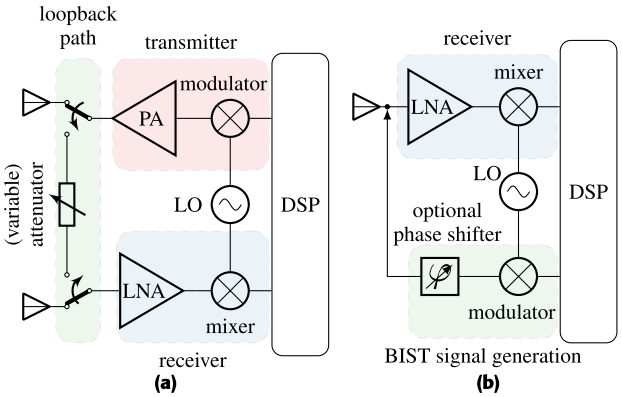

FIGURE 6. Test signal generation: Loopback transceiver test (a) and dedicated BIST signal generation for receiver test (b).

III. STIMULUS GENERATION

Stimulus generation is the first step in implementing a millimeter-wave BIST system. Broadly categorizing, the two options are re-using existing components as BIST generators, usually called loopback, or implementing dedicated hardware. Both variants are conceptually depicted in Fig. 6 and will be examined in the following. As signal generation comes with a significant overhead in area and power, re-use, testing as many blocks as possible with a minimum amount of signal generation hardware, is of prime importance. For the same reason, practical BIST systems usually leverage the existing VCO chain. As a consequence, all uncaught errors in the LO generation and distribution directly translate onto the BIST. That is one of the reasons why the example in Fig. 1 inserts several monitors into the LO chain.

A. LOOPBACK

For transceiver test, stimulus generation via loopback is one of the simplest approaches imaginable. It has, therefore, been around for a long time [40], [41]. As shown in Fig. 6a, the idea is to feed the output of the transmitter into the receiver, testing the complete signal chain simultaneously. At lower millimeter-wave frequencies, loopback production test can

be implemented as simply as via an external high-frequency cable. For an entirely integrated implementation, on-chip duplexers that switch between normal and loopback path are required. Often, the receiver will not be able to cope with the high transmitter output power. An attenuator has to be included in the loopback path.

Because it re-uses the complete signal-generation chain of the transmitter as well as the existing baseband infrastructure, the minimal overhead of loopback testing makes it an attractive proposition. Additionally, as a scaled version of the actual output signal is analyzed by the receiver, more complex problems in the waveform can be found. This is an advantage to purely measuring the PA's output power (see Section IV). On the other hand, it can be difficult to accurately locate the origin of an issue as the whole signal chain is being tested at the same time. This problem can be mitigated somewhat by distributing power sensors throughout the CUT. For more targeted characterization of certain blocks, it should be considered to combine loopback testing with dedicated BIST signal generation approaches.

One of the main challenges for on-chip loopback is the implementation of low-loss, high-isolation millimeter-wave switches. This is especially true for SiGe technologies as HBTs are not well-suited for switching applications while fast FETs are usually not available. An overview of different switch architectures for BIST will be given in Section IV. However, we can already state that at millimeter-wave frequencies, it is usually easier to implement a high-quality passive coupler than a switch.

Another major issue in loopback architectures is the minimization of leakage over the loopback path. Transmitter-to-receiver leakage by itself is already a major problem [42], [43] in millimeter-wave ICs, especially in radar where it mimics as a strong close-range target. Consequently, care has to be taken that the loopback path does not leak excessive signal power into the receiver during normal operation [30]. For example, typical transmitter output powers in automotive radar can be as high as 20 dBm while the input compression point of a very linear receiver might reach 0 dBm [44]. If the disabled loopback path does not provide an isolation significantly larger than 20 dB, the receiver will certainly saturate during normal operation.

A textbook example of integrated loopback self-test is given in [45]. Around 90 GHz, a monostatic transceiver is implemented. The loopback path and attenuator are integrated into the front-end antenna duplexer which is described in detail in [46]. Another loopback architecture, targeted at automotive radar, is presented in [47]. It implements two loopback paths: one before, the other after the PA. The system can therefore switch between receiver (without the PA) and transmitter test mode (including the PA).

B. BIST SIGNAL GENERATORS

As an alternative to loopback, dedicated test signal generators can be implemented. This is especially popular for receiver test. When testing transmitters, usually, the existing signal generation is re-used (although dedicated BIST signal generators have also been reported in literature [48]). The concept for attaching a BIST signal generator to a receiver as shown in Fig. 6b was originally proposed in [30]. A modulator, possibly followed by a phase shifter, is driven by the signal processor. Its output signal is coupled into the input of the LNA (either using a capacitive or a directional coupler, see Section IV). If the output signal of the modulator is well-known, the performance of the receiver can be inferred by measuring the IF output. Compared to loopback, this approach carries larger overhead due to the added signal generation while providing greater flexibility as the test signal can be tailored to a specific CUT. Additionally, the input of the receiver is better isolated from the transmitter, reducing crosstalk.

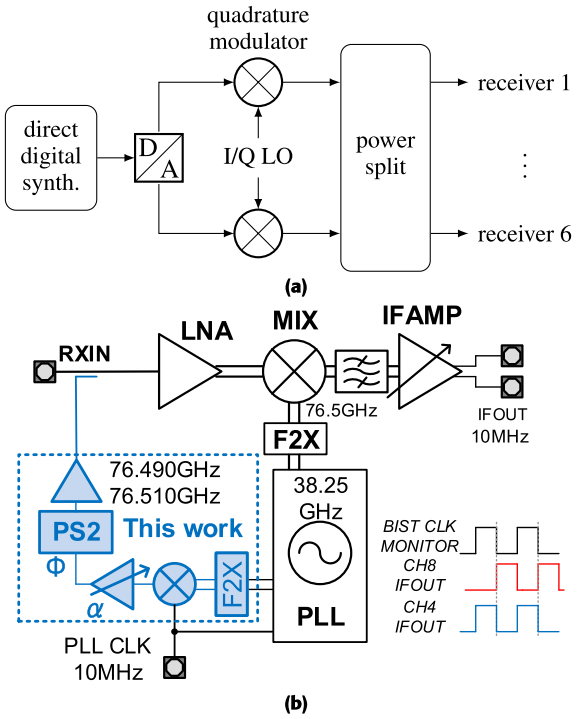

FIGURE 7. Published test signal generators for automotive radar: Direct digital synthesis and quadrature modulator [1] (a) and signal generator with a single mixer followed by a phase shifter (from [50]) (b).

Several commercial automotive radar receivers, e.g. [49] and [35], do not implement an I/Q mixer. In this case, control of the BIST signal generator's phase is vital: The IF output amplitude of a typical current-commutating mixer is proportional to $\cos(\varphi_{\mathrm{LO}} - \varphi_{\mathrm{RF}})$, where φ_{LO}, φ_{RF} are the phases at the LO and RF ports of the mixer. The phase φ_{RF} comprises all phase shifts in the BIST signal generation and injection path. If this phase is not well-controlled through careful layout or a signal generator with phase-tuning capability, the signal level at the IF output of the mixer in test mode can be very low.

In the automotive radar transceiver chip from [1], a complex BIST signal generator allows measurement of both

amplitude and phase response of the six receive channels over frequency (see Fig. 7a). A quadrature modulator in conjunction with a dedicated on-chip direct-digital frequency synthesizer is used to generate the test signals from the internal LO. The generated signal is then distributed to the receivers. A power detector at the input of each receiver ensures that the injected signal power is well known (see Section IV for signal injection techniques).

Another automotive radar with integrated BIST generator is presented in [50]. Its test signal generation is shown in Fig. 7b. Instead of a quadrature modulator, the test signal is generated using a simple mixer that either allows feed-through of the LO signal for single-tone test or modulation with a 10 MHz clock. Because this simple modulator is not able to control the phase, as explained above, a phase shifter is placed after the BIST mixer. The test signal is then distributed to the eight receivers on the chip.

Note that in both examples, a single BIST signal generator is used to distribute the test signal to all receivers present on the IC. Besides minimizing overhead, this also enables the determination of offsets between the different channels. As the distribution of the high-frequency test signal over the whole chip comes with (frequency-dependent) phase offsets, both systems feature phase tunability for the reason given above.

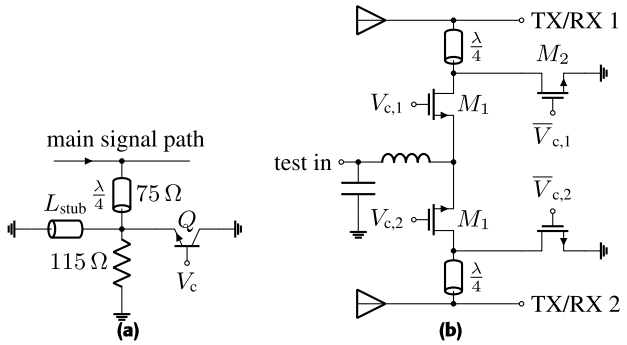

FIGURE 8. Switching element in the loopback switch from [51] (a) and shunt/series switch with high isolation from [48] (b).

TABLE 1. Performance of switches in published BIST systems.

	[48]	[52]	[51]
freq. (GHz)	90 – 100	70 – 87	82 – 110
techn.	SiGe	CMOS	SiGe
node (nm)	120	45	90
device	MOSFET	MOSFET	HBT
type	SPDT	SPST	SPDT
ins. loss (dB)	6 10	12	1.8
isolation (dB)	32 35	30	19
$P_{1\,\text{dB}}$ (dBm)	-	16	19
area (mm^2)	0.05 -	0.29	0.14

IV. TEST SIGNAL INJECTION AND COUPLING CONCEPTS

Injection of the generated test signals is the next task in the implementation of a millimeter-wave BIST system. It is usually accomplished either via switches or couplers. In the latter category, both capacitive and directional couplers have been employed with success. Typically, injection structures also provide convenient means to connect power detectors to the signal path under test. A special type of coupling structure, usually used for testing PAs, will be presented under the designation "I/V couplers" below. These structures generate signals that are proportional to the current and voltage of the PA output signal. They can be used to correctly determine the PA's output power even under heavy load variation.

Coupling is one of the most critical functions in developing a millimeter-wave BIST because it constitutes the point where the test path and the signal under test interact. It should ideally ensure that the test path is transparent to the CUT while at the same time providing low insertion loss to the test signals. Because there are many coupling points in a complex transceiver as in the initial example from Fig. 1, couplers also have significant impact on the area footprint of the BIST.

A. SWITCHES

Millimeter-wave switches are an active area of research [53]. Due to space constraints, we will focus on circuits that are specifically targeted to loopback and test signal routing. An example of an HBT-based switching element is shown in Fig. 8. It is one of the switches used in the combined transmit/receive and loopback duplexer from [51] and [46]. The switch branches off from the path under test using a quarter-wavelength 75 Ω-transmission line. At its end, an HBT parallel with a short-circuit stub and a 115 Ω resistor are placed. The transistor is used in reverse-saturated configuration which has experimentally been shown to provide better off-state impedance than the more traditional forward-saturated one [54]. When the control voltage V_c is high, the low impedance of the transistor is transformed into an open by the quarter-wave transformer. When Q is switched off, on the other hand, the signal path sees an impedance of $75\,\Omega^2/115\,\Omega \approx 50\,\Omega$, which terminates the path. The short-stub transmission line resonates with the off-state capacitance of the transistor at the operating frequency.

The switch shown in Fig. 8b is used in the phased array BIST from [48] to route the test signal between adjacent array elements. In this location, it is imperative to minimize the leakage between TX/RX 1 and TX/RX 2 when the BIST path is disabled, i.e. during normal operation. To maximize the off-state impedance, shunt-series switches consisting of M_1 and M_2 are combined with quarter-wavelength transmission lines. The insertion loss between the injection test signal and the transceivers is relatively high with approximately 10 dB. However, a switch isolation of 35 dB and, even more important, a transceiver-to-transceiver isolation of more than 60 dB is achieved. The loss introduced by the switch to the path between transceiver and antenna is approximately 0.5 dB.

The performance of four different switches used in millimeter-wave BIST schemes is given in Table 1. Besides the switch from Fig. 8b, [48] reports a second switch

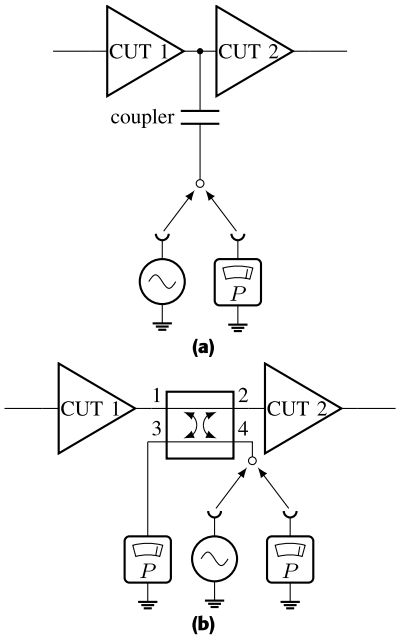

FIGURE 9. The two coupler types encountered in millimeter-wave BIST: Capacitive (a) and directional (b) couplers.

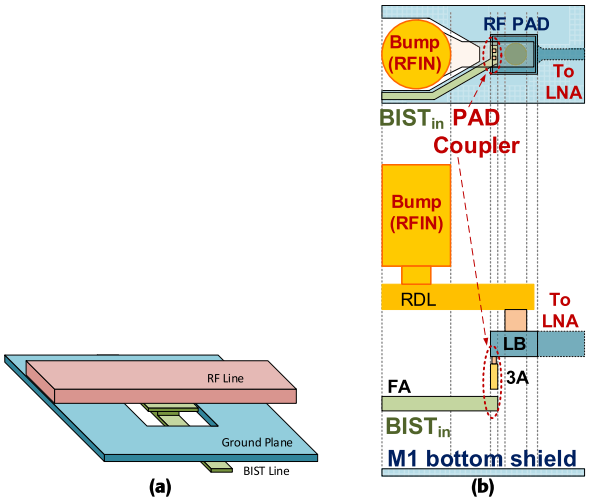

FIGURE 10. Capacitive coupler implemented in [56] and pad coupler from [50] (top and side view).

architecture with less isolation and insertion loss, more suited for general routing of BIST signals in places where isolation is less important. The two MOSFET-based switches provide significantly better isolation compared to the HBT implementation, in return suffering from higher insertion loss. The trend of low isolation in SiGe switches can be seen in other use cases [54], too. Consequently, switch-based loopback should not be the first choice in SiGe technologies because it has a higher likelihood of introducing unwanted leakage, and passive couplers are the better choice. In loopback, the high insertion loss of MOS switches is not necessarily a problem. For general BIST signal routing a reduction of routing loss should be targeted as every decibel lost in routing is wasted power, i.e. BIST overhead. Compared to the capacitive and directional couplers discussed in the following two sections, the area overhead of switches is generally larger. Together with the significantly higher design complexity of an active switch compared to a passive coupler, the usage of switches for test signal injection or coupling should be minimized if possible.

B. CAPACITIVE COUPLING

As illustrated by Fig. 9a, a capacitive coupler can either be used to inject a test signal into the input of a CUT or to attach a power detector to the output of a CUT. Because these couplers do not provide any directivity, their usage can be problematic in injection setups (see Fig. 6b) where as much power would be spuriously radiated by the antenna as coupled into the LNA. In [55], signal injection with a capacitive coupler resulted in the signal component traveling into the unwanted direction, being reflected, and canceling with the injected signal. Consequently, the overall test signal power at the CUT input was extremely low. This means that additional design time to investigate the environment has to be spent when a capacitive coupler is used for injection purposes. Nevertheless, these couplers enjoy great popularity because of their significantly lower area footprint compared to switches and directional couplers together with their straightforward realization.

A very typical implementation of a capacitive coupler is shown in Fig. 10a [56]. RF and BIST signal lines are isolated by the ground plane except at the location of the coupler where a hole in the ground plane together with a wider metal sheet below the RF line form the capacitive coupler. A typical design target for these couplers is a coupling factor of 20 dB with an insertion loss of 0.2 dB. Implementations in several different technologies and frequency bands have been demonstrated [46], [47], [48], [55], [56], [57], [58]. In [59], a 200 fF metal-insulator-metal (MIM) capacitor is used to achieve the same effect. An interesting approach to capacitively couple the BIST signal to the RF path has been demonstrated in the automotive radar transceiver from [50]: Couplers are integrated into the RF bond pads as shown in Fig. 10b. The BIST line is located between ground plane and pad, only overlapping the pad at the very edge. Care is taken to route the BIST signal around the solder bump to minimize unwanted coupling. A similar 17 dB-coupler is used in [60] in a PA power calibration loop.

In [61], a tighter coupling[1] of 15 dB was achieved by approaching the design as a spiral transformer (see Fig. 11). Consequently, the dynamic range requirements on the power detector or signal generation are relaxed while more loss is introduced to the path under test. The footprint of the transformer-based coupler is quite small for a design operating slightly below 30 GHz with an area of $65 \times 55\ \mu m^2$.

[1] A smaller (positive) value for the coupling factor means more power arriving at the coupled port.

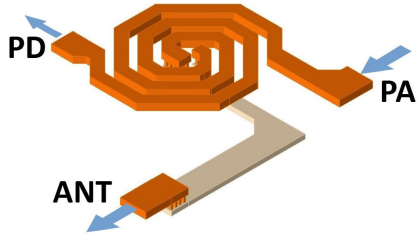

FIGURE 11. Transformer-based coupler from [61] (PA: power amplifier, ANT: antenna, PD: power detector).

While the integration of capacitive couplers into existing structures such as bond pads is an excellent choice from the perspective of area overhead, the issue is that the circuit designer has to identify suitable locations where such a coupler can be integrated and specifically design it. As millimeter-wave systems are growing in complexity, this approach results in a large design time for the BIST. From this point of view, generic couplers that can easily be introduced into the signal chain should be a focus of future research.

For comparison of capacitive with directional couplers in the next section, we can define a figure of merit (FOM)

$$\mathrm{FOM}_{\mathrm{coup}} = \frac{c_0/f_c}{\sqrt{\mathrm{A}}} \cdot \frac{1}{\mathrm{CF}_{\mathrm{lin}} \cdot \mathrm{IL}_{\mathrm{lin}}}. \tag{1}$$

Here, c_0 is the vacuum speed of light, f_c the center frequency of the coupler's operating range, and A its area footprint. $\mathrm{CF}_{\mathrm{lin}}$ and $\mathrm{IL}_{\mathrm{lin}}$ are the coupling factor and insertion loss on a linear scale (i.e. not in dB). The rationale behind this figure of merit is that the area footprint of a coupler should decrease with frequency to achieve the same coupling factor. Furthermore, coupling factor and insertion loss trade off and have to be considered together for a fair comparison of the coupler architectures. Unfortunately, most publications do not include enough information to compute this FOM. However, we can calculate a $\mathrm{FOM}_{\mathrm{coup}} \approx 9$ for the 18 dB-coupler operating at 90 GHz from [48]. Its area is about 0.002 mm^2. The coupler in [55] is very small, about 0.0001 mm^2, which results in a FOM of 16 at 80 GHz for CF = 26 dB. In both cases, the insertion loss is about 2 dB and the area had to be estimated from layout drawings.

C. DIRECTIONAL COUPLERS

The directivity of directional couplers together with the fact that they can be simultaneously impedance-matched at each of their four ports [62] makes them ideal for signal injection scenarios, as shown in Fig. 9b. When the signal generator is connected to Port 4 of the coupler, its output signal is both coupled into Port 2 and measured by the power detector at Port 3. If coupling factor and insertion loss of the coupler are well-known, the power injected into CUT 2 can be calculated with high precision. Ideally, Port 1 is isolated from the injected signal preventing issues from backward-traveling signals. A second use case for directional coupler is connecting power detectors to both Ports 3 and 4. In this

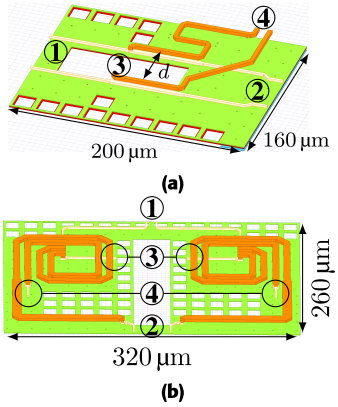

FIGURE 12. Directional couplers for BIST in automotive radar transceivers (from [63]) with 20 dB (a) and 10 dB (b) of coupling.

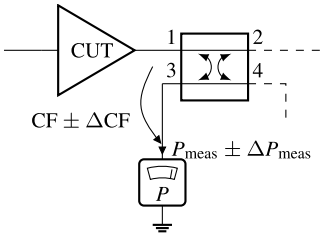

FIGURE 13. Variation of the coupling factor limits the accuracy of power measurement.

case, both the transmitted and reflected power of CUT 1 can be determined.

Two differential directional coupler topologies targeted at BIST for automotive radar transceivers [63] and designed for low area overhead are shown in Fig. 12. The interfaces on Ports 1 and 2 allow direct connection to pre-existing radar transceiver blocks [64]. Additionally, in both cases the space in-between the two differential signals lines is large enough to accommodate a power detector connected to Port 3. At Port 4, either a second detector or the output of a signal generator can be connected. This allows the couplers to be as close as possible to "drop in" parts simplifying the BIST insertion.

The coupling factor has to be chosen with regard to the dynamic range of the available power detectors and the expected signal levels at the CUT [44]. Additionally, tighter coupling results in higher insertion loss to the path under test. For example, the coupler in Fig. 12a uses short broadside-coupled lines for 21.5 dB coupling and an insertion loss of 0.2 dB. The other topology in Fig. 12b, provides a tighter coupling of 10 dB at the cost of a higher loss around 2 dB. Together, both couplers can cover a larger range of applications.

Process and frequency variation of the coupling factor directly impact the accuracy of the BIST. As shown in Fig. 13, the uncertainty in the coupling factor sets a lower limit for the accuracy of the power measurement. Unfortunately, this data is rarely reported. For example, the coupler in Fig. 12a has a variation of the coupling factor over process and frequency

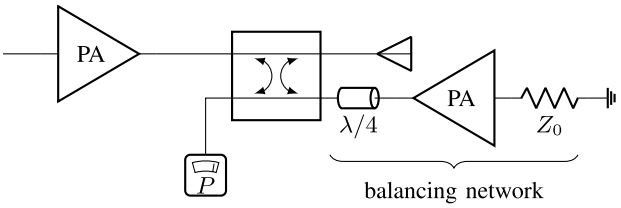

FIGURE 14. Compensating the effect of a probe card in production test by placing a balancing network at the isolated port of the output directional coupler as proposed in [66].

of 21.5 dB ± 0.4 dB. That means it is not possible to measure the power with a 1 dB error bar using this coupler (less than 0.1 dB error for a power detector is unrealistic). The stability of the second coupler from Fig. 12b is much better with 10 dB ± 0.1 dB. More data, ideally comparing different coupler approaches, is required to find the optimal coupling strategy.

Table 2 compares published directional couplers targeted at BIST. Typical coupling factors range between 10 dB and 20 dB. Unfortunately, many publications do not specify the area footprint of the coupler. In the previous section, the FOMs calculated for the capacitive couplers using (1) were nine and sixteen, respectively. The FOMs for all directional couplers in Table 2 are lower than this, the design from [65] coming out on top with a FOM of seven. This is due to the larger footprint of directional couplers and their typically higher insertion loss for the same coupling factor. In general, the coupler's size increases with higher directivity (capacitive couplers do not provide any directivity). Notably, directional couplers in CMOS technologies are difficult to find compared to their SiGe counterparts. Due to the high cost per area, the smaller footprint of capacitive couplers is favored. Additionally, as discussed above, MOS technologies offer higher quality switches as an alternative to passive couplers.

A good example for test signal injection with a directional coupler is given in [1]. Here, 27 µm-long coupled transmission lines with a coupling factor of 22 dB and a directivity of 6 dB are used. Output power measurement via directional couplers is one of the most popular BIST features. It has been implemented up to very high frequencies, e.g. [1], [47], [67], [68], [69], and [70]. Usually, the coupler has to be co-designed with the PA to ensure that the optimum output impedance of the amplifier is not impacted.

In production test, all pads, including the transmitter output, are usually contacted with the pins of a probe card not optimized for high-frequency operation. Even if the power measurement is carried out with the integrated directional coupler and power detector combination, the output impedance shift introduced by the probe card impacts the measurements accuracy. In [66], only one power detector is placed at the coupled port of the directional coupler while the isolated port is used to implement a balancing network that cancels the de-tuning of the probe card. As shown in Fig. 14, the proposed balancing network consists of a dummy PA in series with a quarter-wave transmission line.

Another load-impedance-aware approach is presented in [71]: The application, in this case, is detecting a changing output impedance due to coupling between adjacent phased array channels. In contrast to the conventional approach from Fig. 9b, the antenna is connected to the coupled port in an attempt to minimize the sensitivity to voltage standing wave ratio (VSWR) variations. Another VSWR-aware approach, [72], proposes a two-tap coupler that is much shorter than traditional directional couplers ($\lambda/20$ vs. $\lambda/4$) by capacitively tapping the transmission line at the PA output in two places. This enables the extraction of the forward and backward traveling waves. In essence, the approach encompasses the advantages of capacitive and directional couplers.

Similar to capacitive couplers, the design of generic directional couplers that can be inserted into signal chains with comparative ease is desirable to minimize the design impact of BIST insertion and should be a focus of future research. While critical parts like the PA output or the LNA input will probably still require specialized designs in the future, the excellent matching properties of directional couplers mean that the risk of disturbing the signal chain under test is low. If the area footprint of directional couplers for BIST can be further reduced with new coupler architectures, they would be competitive to capacitive couplers while providing the added benefit of directivity. Otherwise, directional couplers will be employed where their directivity results in a significant advantage (for example when spurious emission over an antenna is a possibility) while the bulk of coupling in the system is capacitive.

D. I/V COUPLERS

What we will call I/V coupler in the following, is an approach to output power measurement over antenna load variations which is different from directional couplers. In effect, a combination of capacitive and inductive coupling is used to derive two signals that are proportional to the output voltage and current of the power amplifier. A mixer can be used to multiply the two signals for coherent power detection. Because the main challenge in implementing this type of power sensing lies in the coupling structure, it is discussed in this section. More traditional amplitude-based power detectors are covered in Section V-A.

The first millimeter-wave implementation of the I/V approach at 75 GHz was published in [73]. Its concept is shown in Fig. 15. A current sensing coil is integrated into the output transformer of the PA. The magnetic coupling ensures that the current in the coil is proportional to the PA's output current. A capacitive divider allows measurement of the output voltage. Both signals are fed to a passive mixer to derive the output signal proportional to the actual power delivered to the load. Because at millimeter-wave frequencies additional phase shifts are introduced by the two coupling a structures, a phase shifter, not shown in the figure, follows the capacitive divider.

TABLE 2. Published directional couplers in BIST systems.

	[1]	[65]	[66]	[67]	[63]		[68]
frequency (GHz)	76 – 81	120 – 180	60 – 61	141.6 – 161	76 – 81		110 – 170
technology	SiGe	SiGe	-	SiGe	SiGe		SiGe
node (nm)	130	130	-	130	130		130
coupling factor (dB)	22	16.5	14.4	12.2	21.5	9.6	22
insertion loss (dB)	-	0.5	1 dB	0.6	0.2	2.0	1.2
directivity (dB)	6	20	19.6	18.6	10	20	-
area (mm^2)	-	0.002	-	-	0.03	0.08	0.03
FOM_{coup}	-	7	-	-	2.5	5	0.9

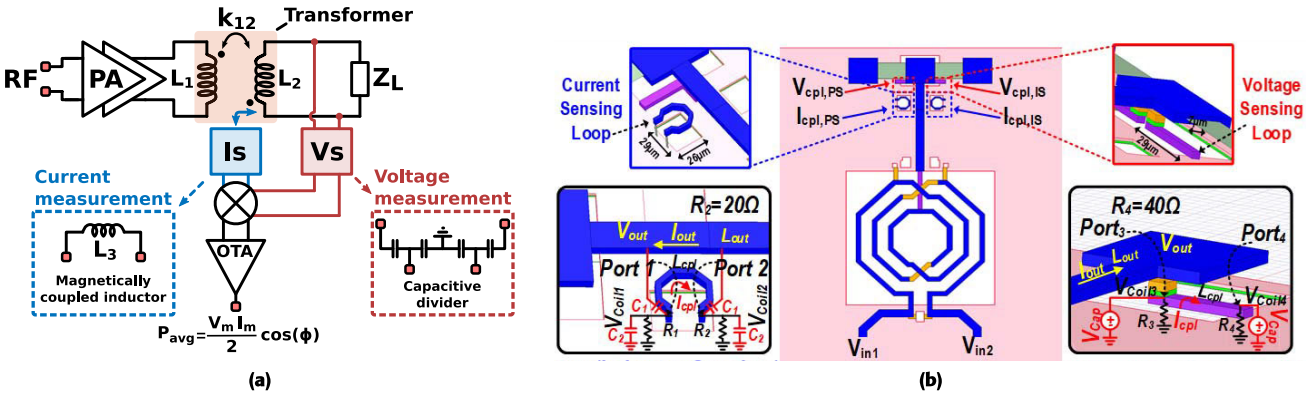

FIGURE 15. Concepts for I/V couplers from [73] (a) and from [74] (b). The former uses one magnetic current sensing and one capacitive voltage sensing coupler to measure power. In the latter case, two coupler pairs, one on each side of the transmission line, also allow measurement of the load impedance.

In [74], a similar concept (Fig. 15b) is implemented for a frequency of 33 GHz. Two current sensing coils are placed left and right of the output transmission line close to the GSG signal pad. The two corresponding capacitive couplers are located below the pad. Clever termination of the current and voltage sensing loops ensures minimal phase offsets so that this implementation does not need a phase shifter. The outputs of the coupler pair on the left side is fed to a double-balanced Gilbert cell, extracting the power of the output signal like in [73]. The outputs of the two couplers on the right of the signal trace are connected to a Dickson rectifier whose output can be used to measure the antenna load impedance.

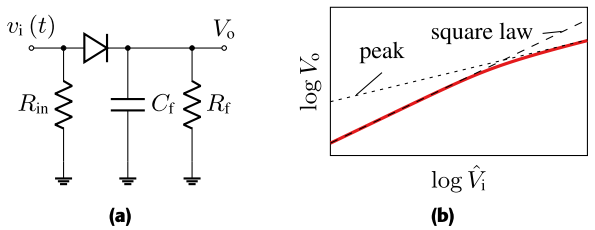

FIGURE 16. Schematic of a diode detector (a) and its typical output voltage over input power characteristic (with square-law and peak detector asymptotes) (b).

V. DETECTORS AND SENSORS

Exact measurement of millimeter-wave power plays a central role in many of the BIST systems reviewed so far. However, in contrast to power sensors for test and measurement equipment [75], where large dynamic ranges and high accuracy can be achieved, the requirements on circuit size and power, keeping the chip impact (Fig. 2) minimal, limit the achievable performance of BIST power sensors. In addition, the highest performing power sensors are usually not implemented in silicon but in specialized technologies [76], [77].

Designs based on a single diode or transistor are popular as they can operate at high-frequencies with low area and current consumption. These types of detectors are the main focus of the discussion below. A recent analysis on the state of the art of transistor-based power measurement in CMOS technologies, including designs well-below the millimeter-wave frequency range, can be found in [78]. Alternative power measurement and sensor concepts, based on thermal effects, that have been used in millimeter-wave BIST are presented towards the end of this section.

A. DIODE- AND TRANSISTOR-BASED DETECTORS

Diode-, and even more so, transistor-based detectors make up the bulk of power sensors in current millimeter-wave BIST applications. This is due to their small size and high operating frequency. A drawback of these types of power detectors is that they are usually very sensitive to process and temperature variation [44]. Although often called "power detector", the output of a diode- or transistor-based detector depends on the amplitude of the input signal. To include variations of the load impedance for true power measurement, the detector circuit

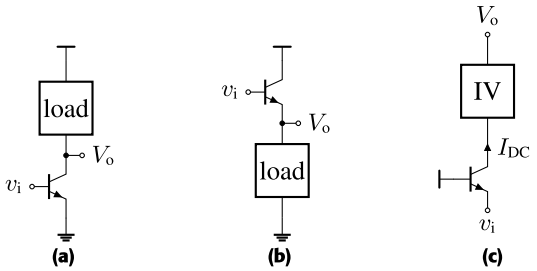

FIGURE 17. Different transistor configurations for power detection: (a) common emitter, (b) common collector, and (c) common base. Analogous versions exist for MOS transistors.

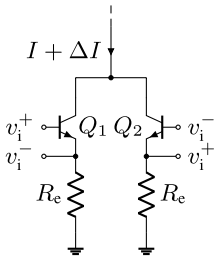

FIGURE 18. Differential power detector concept.

has to be used together with one of the VSWR-aware coupler approaches from Sections IV-C and IV-D.

As a starting point, the well-known diode detector concept is shown in Fig. 16a. The high-frequency input signal $v_i(t)$ with amplitude $\hat{V}_i$ is applied to the diode (potentially using the resistor R_{in} for input matching or application of a bias voltage). Due to the nonlinearity of the diode characteristics, the zero-frequency component of the diode current is a function of $\hat{V}_i$ [79]. Using the low-pass filter consisting of C_f and R_f, the current is translated into a voltage V_o while simultaneously removing high-frequency components from the output signal. Depending on bias and input power level, the diode detector has two distinct operating regions as shown in Fig. 16b: For low signals, the red detector characteristic follows a square-law behavior, i.e., V_o is proportional to the square of the input amplitude ($V_o \sim \hat{V}_i^2$). At larger inputs, the characteristic morphs into a peak detector where the output voltage is directly proportional to the input amplitude ($V_o \sim \hat{V}_i$). An example of a square-law diode-based detector for BIST at 157 GHz is [67].

The majority of detectors for BIST applications are based on transistors, either MOSFETs or HBTs, depending on the technology and operating frequency. In principle, the transistor can be used in common-emitter/source, common-collector/drain, or common-base/gate configuration, as shown Fig. 17. An advantage the former two configurations have compared to the common-base/gate and the diode detector is simpler biasing as well as separation of the input from the output signal; the current containing the information on the signal power does not flow through the same terminal the input signal is applied to. Depending on the configuration, the transistor-based detector can show a behavior similar to the diode detector, with both square-law and peak detector ranges, or only one of the two operating modes. For MOS transistors, there is an additional degree of design freedom in the bias point between weak, where they mirror the behavior of their bipolar counterparts, and strong inversion.

Table 3 compiles several published diode- and transistor-based power detectors. In general, the performance achieved by the detectors is not very frequency-dependent up to at least 170 GHz. Noticeably, the dynamic ranges of most designs, independent of device type, configuration, or operating mode, fall between 30 dB and 40 dB. Circuit area can vary widely depending on whether the detector input is high-impedance (voltage interface) or matched (power interface), the latter case usually requiring large-area passive networks. An interesting case in this regard are the recently demonstrated differential power detectors [44], [84], [88], conceptually depicted in Fig. 18. They are able to measure the differential part of the input power by applying the signal over the base-emitter diodes of complementary HBTs. The common mode is rejected. It has been shown [88] that broadband input matching of the detector can be achieved by setting the emitter resistor R_e to 50 Ω. Therefore, the detector can be very compact while still being matched.

As mentioned above, power measurement accuracy is an important concern in BIST applications. When we envision full-scale BIST of a complex millimeter-wave transceiver, a large number of power detectors will be required. The success of the BIST will depend on the reliability of these detectors to produce correct measurement results. That means the sensitivity of the detectors to different types of variation (process, temperature, etc.) has to be investigated. Power detector variation depends on the device type and architecture. For example, the differential common-emitter detector from [88] shows a power prediction error of ±1 dB over process and ±1.3 dB over the automotive temperature range (−40 °C − 125 °C). In practice, these errors overlap resulting in large uncertainties of up to ±5 dB, i.e., a 10 dB error bar [89].

A power measurement uncertainty of 10 dB is clearly unacceptable for BIST applications. To combat this issue, several calibration procedures have been proposed in literature that improve the accuracy of power detectors: In [79], the common-collector peak detector contains a reference path. By offsetting the bias points between main and reference path, the temperature error is minimized. Another purely analog approach to temperature compensation, in this case for SiGe square-law detectors, is proposed in [90]. It is based on a translinear current divider and a current reference. However, this type of compensation is very sensitive to mismatch. In effect, the better accuracy over temperature is bought by introducing a higher process dependence.

Moving to digitally-assisted calibration, a piece-wise linear model with two coefficients is fitted to the

TABLE 3. Comparison of published diode- and transistor-based millimeter-wave power detectors.

	technology	node (nm)	architecture	type[a]	input impedance	frequency (GHz)	dynamic rng. (dB)	static power (mW)	area (mm^2)
[80]	CMOS	90	CG	sl	high	60	30	0	-
[81]	CMOS	45	diode	sl	high	80-110	29	-	3×10^{-4}
[82]	SiGe	55	CB/CG	sl+peak	high	50-67	38	0.09	0.006
[83]	CMOS	65	diode	sl	high	80-110	30	-	2×10^{-5}
[69]	SiGe	130	CE	sl	high	100-130	38	0.1	0.06
[84]	SiGe	180	CE	sl	-	20-44	20	5.2	0.24
[85]	SiGe	130	CC	sl+peak	matched	72-82	35	0.6	0.1
[86]	SiGe	130	CE	sl	matched	76-81	30	0.9	0.11
[87]	CMOS	22	CD	peak	high	61	25	0.006	0.001
[67]	SiGe	130	diode	sl	matched	145-161	-	1.2	-
[88]	SiGe	130	CE	sl	matched	76-81	30	0.5	0.005
[68]	SiGe	130	CE	sl	matched	110-170	> 25	1	0.02
[44]	SiGe	130	CC	sl+peak	matched	76-81	46	0.5	0.004

[a] sl: square-law

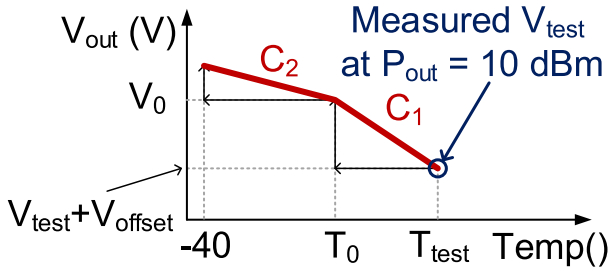

FIGURE 19. Digital calibration of power detectors: Modeling the temperature behavior with two linear coefficients (from [60]).

common-source square-law detector in [60] as shown in Fig. 19. Calibration is then performed based on this model. In [70], two common-source square-law detectors are used to measure the output power of a PA (implementing the approach shown in Fig. 19b). Digital calibration is employed to reduce the offset between these two detectors. Additionally, their temperature error is minimized by directly converting the output currents of the detectors into the digital domain. This removes any temperature error that would be introduced in analog current-to-voltage conversion, e.g. via a resistor. Another digital temperature and process compensation for HBT-based square-law detectors is proposed in [89]. It relies on accurate modeling of the main detector output voltage and a reference path that tracks the process and temperature variation of this main output voltage. With this approach the power measurement uncertainty of the detector over process and temperature is improved from ±5 dB to ±1 dB.

With the large amount of signal processing hardware already present in millimeter-wave systems digitally-assisted is clearly the way to proceed forward. It circumvents the trade-off between temperature and process variation that is often inherent to analog approaches. Nevertheless, every new power detector architecture should be evaluated for its robustness against process and temperature variation. In addition, more data points by how much a certain calibration improves the detector accuracy are required.

Another important concern is the frequency behavior of the detector. Depending on the BIST architecture, the frequency of the signal under test can be unknown; the uncertainty of the power measurement is increased. In [68], the directional coupler the detector is connected to is designed so that the frequency-dependence of the coupling factor compensates for the detector's frequency roll-off. The resulting BIST covers the complete 60 GHz bandwidth of D-band. If future co-designed couplers and detectors can cover large bandwidths with high accuracy, the components could easily be transferred between transceiver designs. For example, the same BIST circuits would be used in both 60 GHz as well as 79 GHz radar transceivers. A big step in minimizing the design impact of BIST circuits.

B. OTHER SENSORS

There are several alternative power sensing concepts tied to different temperature effects. Because temperature can be directly linked to dissipated power, these sensors can measure the power of arbitrarily shaped waveforms. Typically, temperature effects have slower response times compared to diode- and transistor-based detectors as well as a lower dynamic range [75]. Furthermore, when testing complete transceivers, thermal coupling effects between different circuit blocks can reduce the accuracy of these sensors.

Differential temperature sensors have been investigated as means to extract the frequency-dependent gain of millimeter-wave PAs. In the design from [91], shown in Fig. 20, a differential temperature sensor in a standard 65 nm-CMOS technology is used for this purpose. The two bipolar transistors Q_1 and Q_2, marked on the die micrograph, form a differential pair. However, the balance of the pair is not offset by an input voltage, but by the temperature difference between the two transistors. Q_1 is placed closely to the output stage of a 60 GHz-PA. The second transistor Q_2 is placed far enough away from the PA that it can be considered at a stable reference temperature. Note that there is no electrical connection between the sensor and the PA. In the referenced publication, a two-tone signal consisting of f_1 and $f_1 + 5$ kHz

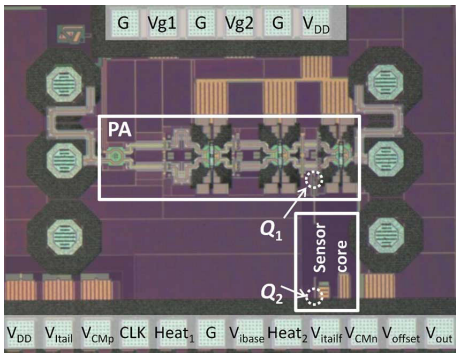

FIGURE 20. Using a temperature sensor to extract the gain of a PA (from [91]). The hot transistor Q_1 and the cold transistor Q_2 form a differential pair.

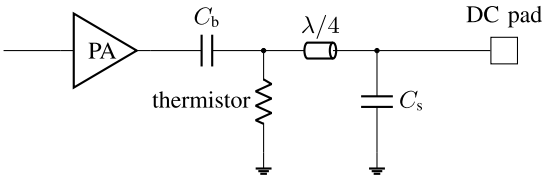

FIGURE 21. A thermistor at the output of a PA can be a reference for diode/transistor-based power detectors.

is swept over the operating bandwidth of the PA. After calibration of signal-independent offsets, the temperature sensor is able to pick up the 5 kHz difference frequency and extract the frequency-dependent gain from the temperature measurement. In [92], the method is extended to also work with a single-tone signal that is easier to generate.

A somewhat similar approach is considered in [93]. In a 130 nm-SiGe technology, a termination consisting of tantalum resistors is designed. High-frequency power, which can for example be coupled out of the signal path under test via a directional coupler (Fig. 9b), is fed into the termination and dissipated. The subsequent rise in temperature is measured by a bipolar differential temperature sensor placed below the resistors. Because the tantalum resistors have a low temperature coefficient, the termination's return loss is stable even for high input powers.

Instead of using a temperature stable resistor, [94] investigates several resistive layers in a standard SiGe technology for one with a particularly high thermal coefficient. Silicided polysilicon is identified as being suitable for the implementation of 50 Ω thermistors that can handle the expected output power of 15 dBm coming from a 77 GHz automotive radar PA. The designed thermistor is then used at the output of a PA in a reference channel with the goal to establish an absolute power reference measurement. This reference can be used to calibrate the diode/transistor-based power detectors used in the actual transmitter channels of the radar IC. Fig. 21 illustrates the concept: The PA output is fed to the thermistor. A quarterwave transformer together with the shorting capacitor C_s ensures that the DC pad is fully isolated from the PA output. Using this pad and a ground pad, the resistance change of the thermistor can be measured. The method is further refined in [95], reporting a dynamic range of 18 dB with an uncertainty of 0.5 dB at 77 GHz.

As we can see from the examples above, temperature effects are a viable option for power measurement in the context of millimeter-wave BIST. However, existing literature still lacks practical demonstration that these sensors can scale to larger circuits and systems. The impact of thermal coupling on the accuracy has to be characterized. A potential solution lies in the proposal put forth in [94] and [95]. As explained above, these studies suggest utilizing thermal sensors exclusively as calibrators for other power detectors. Further investigation is necessary to quantify the accuracy improvements achievable with this strategy.

VI. CONCLUSION AND OUTLOOK

Over the past decade, driven largely by the success of automotive radar, specific millimeter-wave self-test features have become the de facto standard, as evidenced by the preceding discussion. These features primarily pertain to output power monitoring of PAs to ensure compliance with regulations. Additionally, receiver test components are now commonplace in many transceivers. However, a significant challenge for millimeter-wave BIST lies in identifying a universally applicable "golden" test system concept that can be employed across a majority of transceiver circuits. Currently, the multitude of diverse concepts, often customized for specific CUT scenarios by experienced designers, results in substantial design overhead when integrating self-test functionality. To address this situation, one potential approach involves leveraging electronic design automation (EDA), which is already standard practice in digital circuits. For instance, software-assisted design could automatically size optimal directional couplers based on the metal stack and performance requirements.

Our exploration of components, signal generation, injection, and measurement has revealed that all essential circuit blocks for successful millimeter-wave BIST are currently available, at least up to D-band frequencies (110 GHz – 170 GHz). Naturally, future research should try to cover the rest of the millimeter-wave frequency range up to 300 GHz. Beyond merely pushing for higher frequencies, the research focus must shift toward enhancing the accuracy and repeatability of integrated high-frequency test. Unfortunately, many test concepts are published today without a rigorous analysis of how much the BIST improves the circuit performance, and how robust the approach is to variation. We remain hopeful that this will change in the coming years.

The test and calibration of phased arrays constitute a crucial topic, warranting a dedicated review article. Phased arrays commonly suffer from both static and time-dependent amplitude and phase deviations [96], necessitating precise calibration for optimal performance. Numerous research groups have contributed a wealth of approaches to phased array BIST and calibration, as evidenced by works such

as [48], [56], [57], [96], [97], [98], [99], [100], and [101]. However, a systematic consolidation of these diverse approaches remains absent in the current literature.

ACKNOWLEDGMENT

The authors would like to thank the late Ralf Reuter for setting them on the path that would lead to this article many years ago.

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