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RESEARCH ARTICLE

Novel Double Slope Frequency Shift Chirp Symbol

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ABSTRACT One of the most significant concerns in serial digital communication is the synchronization of data bits between the transmitter and receiver. Therefore, the preferred coding symbols should contain an inherited clock signal. The cyclic-shift chirp, which is primarily used in long-range systems, employs a single slope in a symbol, which contains few information for synchronization. Hence, two new forms of cyclic-shift chirp symbols are proposed herein. The associated coding schemes are based on the use of a dual slope within one symbol. Synchronization is inherited in the coding symbol using a dual slope. Additionally, both proposed coding schemes utilize the same decoding technique. The decoded chirp symbol is in the form of a pulse width modulation signal, which can be used for synchronization and retrieving data bits from their duty cycle. The simulation results show that the coding and decoding processes of the proposed coding schemes align with those of a theoretical framework. The error performance analysis for the proposed detection scheme is given and the results of error probability analysis are consistent with the simulation results. Moreover, under a Rayleigh fading channel, the proposed coding schemes provide superior performance compared with other comparable coding schemes.

INDEX TERMS Chirp signal, chirp symbol, cyclic-shift chirp modulation and demodulation, non-coherent, frequency shift chirp, chirp spread spectrum.

I. INTRODUCTION

In 1945 (i.e. during World War II), a linear frequency modulating signal or chirp signal was invented for radar operations. Subsequently, it appeared in a patent as "Pulse Transmission" in 1954, which was proposed by Darlington and Summit [1]. In this patent, linear-frequency modulation for pulse transmission was proposed to overcome the limitations of a power amplifier that cannot release high power in a short period. Namely, a high-power signal is spread out in the time domain in the form of a linear modulating signal. Therefore, a high-power signal occurring in a short time can be transmitted using a low-power amplifier. Subsequently, these signals are combined to achieve high power (or high signal strength) in a short time by a receiver, providing noise immunity to the signal.

The principle of chirp signals has been applied in many modern radar systems. A chirp radar is similar to a frequency-modulated continuous-wave (FMCW) radar [2], which can be referred to as a linear FMCW; however, the main difference between them is the processing technique. For the FMCW radar, the slope of the linear frequency variation is used to determine the duration of round-trip travel. By contrast, a chirp radar determines the time required for traveling by delaying the chirp signal to obtain a pulse. The position of the time at which this pulse occurs corresponds to the duration of the round-trip travel [3]. A chirp signal possesses dominant properties, such as low power consumption and high immunity to fading noise, owing to the inherent frequency and time information of the signal.

Several researchers have proposed the use of chirp signals for data encoding. In 2009, Slats [4] proposed a technique for the low-power wireless transmission of data obtained from household meters (electric, gas, and water) and applied linear frequency modulation in radar for digital data transmission.

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Subsequently, the chirp signal appeared as a category of spread spectrum modulation known as the ''chirp spread spectrum'' [5]. In chirp-spread spectrum modulation, data bits are encoded using up-chirp and down-chirp signals. In 2004, Hiscock [6] invented cyclic-shift chirp coding, which features the same beginning and ending frequencies for one symbol. Currently, cyclic-shift chirp coding is widely used in long-range technology. The decoding process of chirp modulation generally relies on a coherent technique that requires synchronization between chirp symbol and inverse chirp symbol [7]. The non-synchronization of these signals render data decoding errors inevitable.

In this study, two novel types of encoding based on the dual slopes of chirp signals are proposed: the double-slope frequency shift chirp-down chirp start zero (DSFSC-DCSZ) and the double-slope frequency shift chirp down chirp stop minimum frequency (DSFSC-DCSMF). The main advantage of these coding techniques is that each coding symbol contains both positive and negative slopes, thus implying that synchronized information is inherent in the encoded signal. Therefore, an inverse chirp is not required in the decoding process. Data bits can be decoded using noncoherent techniques [8], [9], [10], and [11]. Additionally, compared to the schemes in [6] and [7], the proposed techniques achieve 2 dB better fading noise performance, leveraging the clock signal inherent in the codes. The non-coherent detection scheme for the two proposed coding will be presented. The remainder of this paper is organized as follows: Section I provides a brief introduction of this study. Section II presents the principles of chirp modulation and cyclic shift chirp signals. Section III describes the methods used to generate the proposed chirp symbols, namely, DSFSC-DCSZ and DSFSC-DCSMF, including their decoding processes. In addition, this section presents an error analysis of the proposed coding signal. Section IV presents the simulation results to confirm the proposed coding schemes. Finally, the conclusions are presented in Section V.

II. PRINCIPLE OF ENCODING AND DECODING PROPOSED DSFSC-DCSZ AND DSFSC-DCSMF

A. CHIRP MODULATION

Compressed high-intensity radar pulse (CHIRP) modulation is a modulation technique that provides the spread spectrum of the modulated signal. In up-chirp and down-chirp modulations, the chirp signals are frequency-modulated signals whose frequency increases and decreases linearly, respectively. The up-chirp and down-chirp symbol can be mathematically expressed as:

$$\left.\begin{array}{ll} v_{up}(t) = a(t - t_0) & ;\ t_0 < t \le t_0 + T_s \\ v_{down}(t) = -a(t - t_0) + V_{\max} & ;\ t_0 < t \le t_0 + T_s \end{array}\right\}, \quad (1)$$

where $v_{up}(t)$, $v_{down}(t)$ is an up-chirp and down-chirp symbol in the time domain, a is the slope of a chirp symbol (V/s), $V_{\max}$ is the maximum voltage level (V), t_0 is the starting time of a chirp symbol (s), and T_s is the period of a chirp symbol (s). When an up-chirp symbol or down-chirp symbol is input into a voltage control oscillator, the chirp signal is obtained as follows:

$$c(t) = A\cos\left(\omega_c t + \frac{1}{2}\mu t^2\right), \quad (2)$$

where $c(t)$ is the chirp signal in the time domain (V), A is the peak amplitude of the chirp signal (V), ω_c is the angular frequency of the carrier signal (rad/s), μ is the chirp rate, defined as a k_{VCO} (rad/s^2), and k_{VCO} is the constant of a VCO (rad/V·s or 2πHz/V). The instantaneous frequency of the chirp signal $\omega_i(t)$ which is the derivative of the angle with respect to time, can be expressed as

$$\omega_i(t) = \omega_c + \mu t. \quad (3)$$

For $\mu > 0$, the frequency of a chirp signal increases linearly, whereas for $\mu < 0$, the frequency of a chirp signal decreases linearly, as illustrated in Fig. 1 which shows examples of up-chirp and down-chirp signals. Examples of a digital signal(data), the corresponding chirp symbol, and the corresponding chirp signal are shown in Fig. 2.

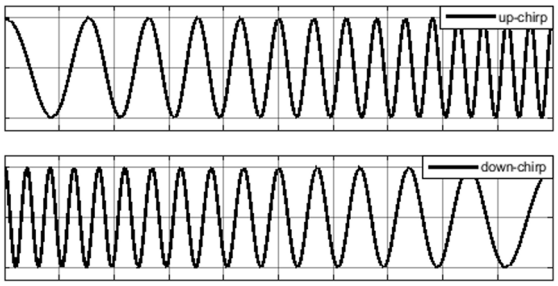

FIGURE 1. Examples of chirp signals.

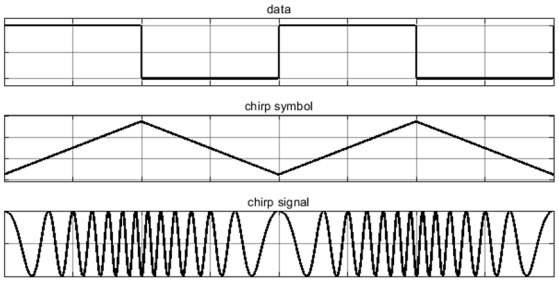

FIGURE 2. Example of chirp modulation.

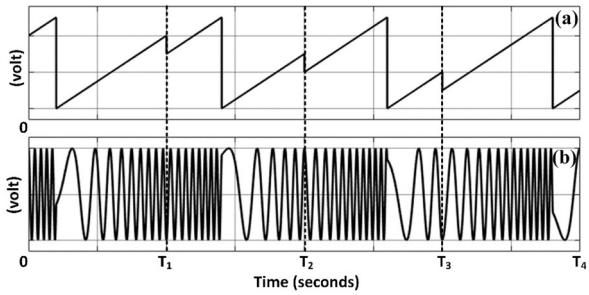

FIGURE 3. Relationship between (a) cyclic-shift chirp symbols and (b) cyclic-shift chirp signals.

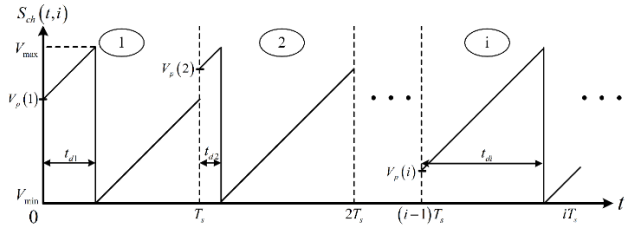

FIGURE 4. General plot of cyclic-shift chirp symbols.

B. CYCLIC SHIFT CHIRP MODULATION [6]

Cyclic shift chirp modulation is a form of chirp modulation in which the initial and final frequencies within one symbol are the same. Similarly, from the perspective of the cyclic-shift chirp symbol, the initial and final amplitudes within one symbol are identical. Examples of cyclic shift chirp symbols and cyclic-shift chirp signals are shown in Fig. 3.

The cyclic-shift chirp symbol can be plotted as a general graph, as shown in Fig.4, and can be expressed mathematically as

$$S_{ch}(t,i) = \begin{cases} \frac{V_{\max}-V_{\min}}{T_s}(t-(i-1)T_s)+V_p(i) \\ \qquad ;(i-1)T_s \le t \le (i-1)T_s + t_{di} \\ \frac{V_{\max}-V_{\min}}{T_s}(t-iT_s)+V_p(i) \\ \qquad ;(i-1)T_s + t_{di} \le t \le iT_s \end{cases} \tag{4}$$

where $V_p(i)$ is the amplitude level of a phase (V), which serves as the input for phase modulation using a sawtooth wave as a carrier signal; $V_{\max}$ is the maximum amplitude of a cyclic-shift chirp symbol (V); T_s is the period of a cyclic shift chirp symbol (s); and t_{di} is the duration of the first interval of a sawtooth signal (s).

III. PRINCIPLES OF PROPOSED DOUBLE-SLOPE CHIRP SYMBOLS

A. DOUBLE-SLOPE FREQUENCY SHIFT CHIRP (DSFSC) SYMBOLS

The single-slope cyclic-shift chirp signal cannot be decoded using a noncoherent technique [8], [9], [10], [11] and requires a reference symbol for decoding [13]. Hence, two forms of frequency shift chirp symbols based on a dual-slope frequency shift chirp are proposed herein. In both coding forms, the up-chirp and down-chirp are contained in one symbol, where the up-chirp increases linearly and proportionally to an information signal. Two types of down-chirps exist: one type begins at zero, whereas the other type ends at the minimum frequency, and they are abbreviated as DSFSC-DCSZ and DSFSC-DCSMF, respectively. Details pertaining to each coding format are provided below.

1) DSFSC-DCSZ SYMBOL

For the DSFSC-DCSZ symbol, the up-chirp has an initial amplitude related to the analog level of the i^{th} data set,, which increases linearly with the slope S_L, where the interval is

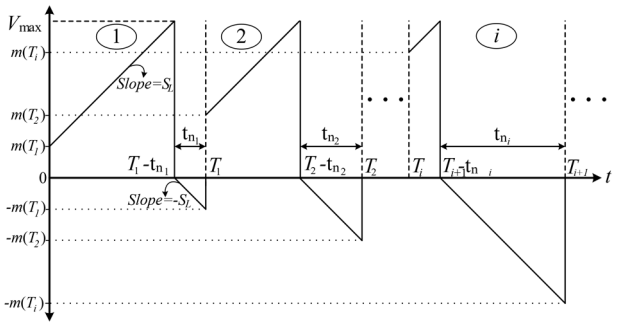

FIGURE 5. Plot of DSFSC-DCSZ symbols.

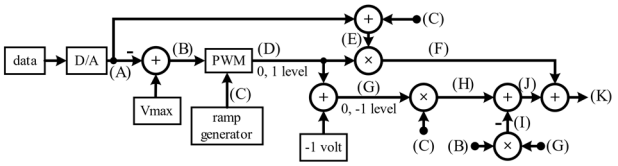

FIGURE 6. Block diagram showing generation of proposed DSFSC-DCSZ symbols.

proportional to this analog signal. By contrast, the down-chirp begins at zero decreases linearly with the slope - S_L and ends at -$m(T_i)$. A plot of the DSFSC-DCSZ symbols is shown in Fig. 5.

For the i^{th} symbol, a DSFSC-DCSZ symbol can be expressed as

$$v_{1i}(t) = \begin{cases} s_L \times (t - T_i) + m(T_i) \\ \qquad ; \quad T_i \le t < T_{i+1} - t_{n_i} \\ -s_L \times \left(t - \left(T_{i+1} - t_{n_i}\right)\right) \\ \qquad ; \quad T_{i+1} - t_{n_i} \le t \le T_{i+1} \end{cases} \tag{5}$$

where s_L is the slope (V/s), T_{i-1} is the beginning time of the i^{th} symbol, t_{n_i} is the down-chirp duration (s), $T_s = T_i - T_{i-1}$ is the duration of one symbol (s), and $m(T_i)$ is the analog level of the i^{th} data set. The process of generating the proposed DSFSC-DCSZ symbols is illustrated in Fig. 6. It comprises two processes, i.e., up-chirp and down-chirp generation processes.

In the generation process, the data bit is first converted to an analog signal $m(t)$. As an example, if one symbol represents two bits of data containing four codewords 00, 01, 10, and 11, then four possible analog levels exist as shown in Fig.7 (A). Each analog level is subtracted from the DC level $V_{\max}$(see Fig. 7 (B)). The analog-level $m(t)$ of digital-to-analog converter must be positive and less than $V_{\max}$. Subsequently, the signal at point (B) is modulated with a ramp signal (see Fig. 7 (C)) to generate a pulse width modulation (PWM) signal, as shown in Fig. 7 (D). The PWM signal is designed to exhibit minimum and maximum voltages of 0 and 1 V, respectively. In the up-chirp generation process, the combination of the analog signal (A) and ramp signal (C) as shown in Fig. 7 (E) is multiplied by the PWM signal (D). The obtained output is an up-chirp signal as shown in Fig. 7 (F). For down-chirp generation, the PWM signal at point (D)

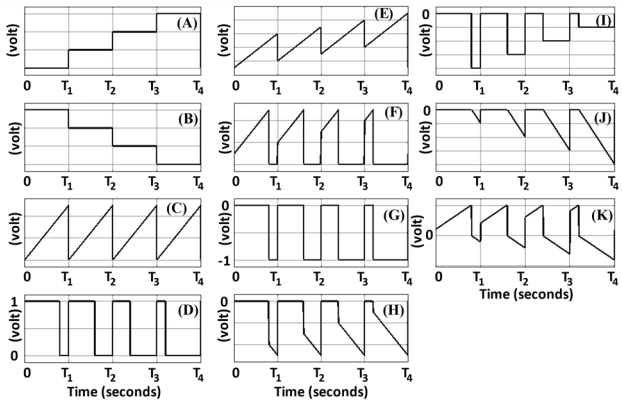

FIGURE 7. Trends of signals associated with generation of DSFSC-DCSZ symbols.

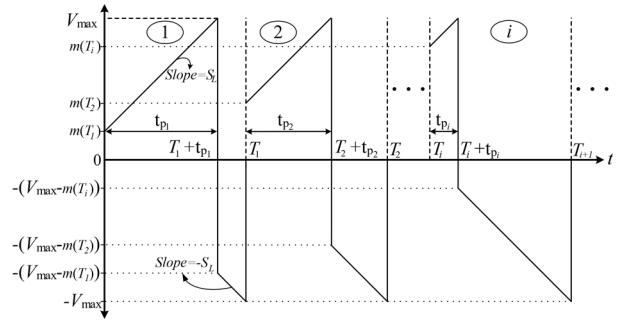

FIGURE 8. Example of plot for DSFSC-DCSMF symbols.

is inverted by summing it with the DC −1V level, as shown in Fig. 7 (G). The inverted PWM signal (G) is multiplied by the ramp signal (C), which results in the signal shown in Fig. 7 (H). Subsequently, the signal at point (H) is subtracted from the signal at point (I), which is the product of the signals at points (B) and (G). The resulting signal shown in Fig. 7 (J), is a down-chirp signal. Combining the up-chirp signal (F) and down-chirp signal (J) yields a complete waveform for the DSFSC-DCSZ symbol, as shown in Fig. 7 (K).

2) DSFSC-DCSMF SYMBOL

For the DSFSC-DCSMF symbol, the up-chirp portion is similar to that of the DSFSC-DCSZ symbol; however, the down-chirp portion ends at the minimum voltage of $-V_{max}$ within each symbol. An example of a plot for DSFSC-DCSZ symbols is shown in Fig. 8.

A DSFSC-DCSMF symbol can be expressed as

$$v_{2i}(t) = \begin{cases} s_L \times (t - T_i) + m(T_i) & ; \ T_i \le t < T_i + t_{p_i} \\ -s_L \times (t - T_i) & ; \ T_i + t_{p_i} \le t \le T_{i+1} \end{cases} \tag{6}$$

where s_L is the slope (V/s), T_{i-1} is the beginning time of the i^{th} symbol, t_{p_i} is the up-chirp duration (s), $T_s = T_i - T_{i-1}$ is the duration of one symbol (s), and $m(T_i)$ is the analog level of the i^{th} data set. The process of generating the proposed DSFSC-DCSMF symbols is shown in Fig. 9.

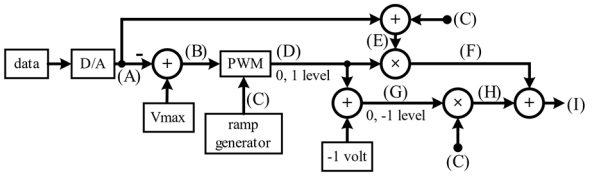

FIGURE 9. Block diagram showing generation of proposed DSFSC-DCSMF symbols.

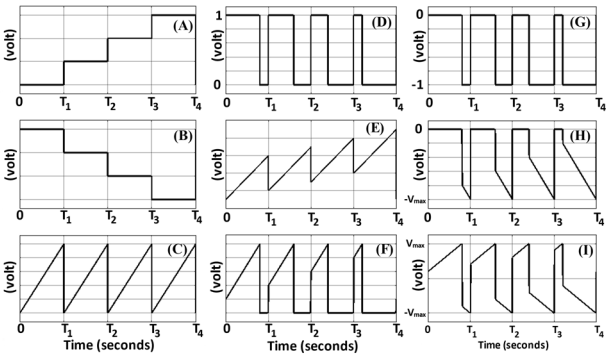

FIGURE 10. Trends of signals associated with generation of DSFSC-DCSMF symbols.

Because the up-chirp-generation process is the same as that of the DSFSC-DCSZ, only the down-chirp generation process is discussed herein. The difference between the generation of the down-chirp signal in the DSFSC-DCSMF and that in the DSFSC-DCSZ is that the obtained signal at point (H), which is the product of the inverted PWM signal (G) and ramp signal (C), represents the down-chirp portion. No further processing is required, and the combination of the up-chirp signal (F) and down-chirp signal (H) provides the complete waveform for the DSFSC-DCSMF symbol (I). A plot of the signals points at (A)–(I) is shown in Fig.10.

The techniques to generate the proposed chirp symbols: DSFSC-DCSZ and DSFSC-DCSMF which are discussed in section I) and II), respectively, show that both symbols contain dual slopes, namely positive and negative slopes with a single symbol. The advantage of dual slopes is the inherent synchronization of the signal within the symbol. When these symbols are modulated into frequency-shift chirp signals, a noncoherent demodulation technique can be applied to retrieve the data bit. In the next section, the decoding of the proposed double-slope frequency-shift chirp symbols is discussed.

It is noted that in designing the DSFSC symbol, it should be designed to distinguish as much as possible between upper level of positive slope and negative slope signal for easy comparison by the decoder.

B. DECODING PROCESS OF PROPOSED DSFSC

In this section, the decoding process of the proposed double slope frequency-shift chirp symbols (for both the DSFSC-DCSZ and DSFSC-DCSMF) as depicted in Fig. 11 is discussed. After demodulation, the DSFSC symbols are

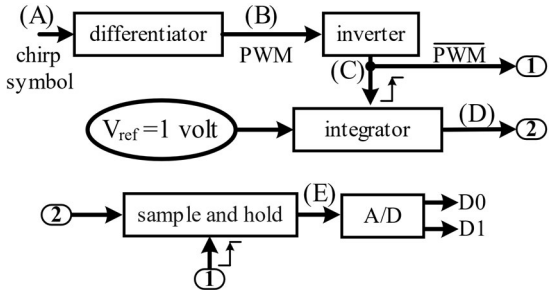

FIGURE 11. Block diagram of DSFSC decoding process.

recovered (A). By differentiating these symbols, the resulting signals become PWM signals (B). It is noted that after differentiating, the signal is clipped and filtered out. The period of the PWM signals is constant, which indicates that the clock signal is embedded in the PWM signal. Therefore, the DSFSC symbols can be decoded using a noncoherent decoding technique.

The obtained PWM signal is inverted (C) and used to control the integrator sample and hold circuit. The integrator has a reference voltage of 1V and an initial voltage of 0V. The output of the integrator is an analog signal (D) whose amplitude is directly proportional to the duty cycle of the PWM signal. This analog signal is converted into a digital signal (E) that corresponds to the transmitting site. Finally, the data bits (D0 and D1) are recovered. However, a delay occurs, where; the data bits are delayed by one symbol-time. The relationship between the signals at points (A)–(E) in Fig. 11 is shown in Fig. 12. Notably, the DSFSC-DCSZ symbols are used as examples.

C. ERROR PERFORMANCE ANALYSIS FOR OPTIMUM SYNCHRONOUS AND PROPOSED ASYNCHRONOUS DETECTION OF DSFSC-DCSZ AND DSFSC-DCSMF

Error performance analysis of the data bit transmission based on the modulation of the DSFSC symbols, i.e., $s_i(t)$ and $s_j(t)$ (where i, j are 1, 2, 3, and 4), the analysis method presented in [13] is utilized as a reference. The normalized correlation among the four signals ($\rho(s_i, s_j)$) is expressed as

$$\rho\left(s_i, s_j\right) = \frac{1}{E_s} \int_0^{T_s} s_i\left(t\right) s_j\left(t\right) dt \tag{7}$$

for the four signals in 2-bit encoding, E_s is the energy of the chirp signal and T_s is the period of one symbol.

1) GAUSSIAN NOISE OPTIMUM ERROR PERFORMANCE ANALYSIS FOR DSFSC-DCSZ SYMBOL

For the DSFSC-DCSZ symbol, by denoting $v_{1i}(t)$ for i =1, 2, 3, and 4 as four possible symbols of the 2-bit encoding, as expressed in (5) and shown in the plot in Fig. 5, the normalized correlation among these four symbols ($\rho(v_{1i}, v_{1j})$) of the DSFSC-DCSZ coding contains six pairs of ($\rho(v_{1i}, v_{1j})$), $i \neq j$ for i, j = 1, 2, 3, and 4. The values of these normalized correlations are used to determine the squared Euclidean distance $D^2(v_{1i}, v_{1j})$ as follows:

$$D^2\left(v_{1i}, v_{1j}\right) = 2E_s\left(1 - \rho\left(v_{1i}, v_{1j}\right)\right) \tag{8}$$

The minimum value of the normalized squared Euclidean distance was 0.35, which was employed to determine the maximum error performance of the 2-bit DSFSC-DCSZ coding system which is expressed as

$$\begin{aligned} P_e &\simeq Q\left(\sqrt{\frac{\min\left\{D^2\left(v_{1i}, v_{1j}\right)\right\}}{2N_0}}\right) \\ &\simeq Q\left(\sqrt{\frac{(2E_s\,(0.35))}{2N_0}}\right) \\ &\simeq Q\left(\sqrt{\frac{(0.35E_s)}{N_0}}\right). \end{aligned} \tag{9}$$

N_0 is the power density Gaussian noise.

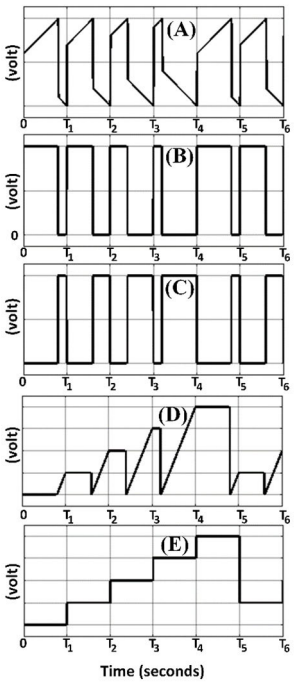

FIGURE 12. Trends of signals associated with DSFSC decoding process.

2) GAUSSIAN NOISE ERROR PERFORMANCE ANALYSIS FOR DSCFC-DCSMF SYMBOL

Similarly, for the DSFSC-DCSMF symbol, by denoting $v_{2i}(t)$ for i =1, 2, 3 and 4 to represent the four possible symbols of the 2-bit encoding, as expressed in (6) and shown in the plot in Fig. 8, the normalized correlation among these four symbols ($\rho(v_{2i}, v_{2j})$) of the DSFSC-DCSZ coding contains six pairs of ($\rho(v_{2i}, v_{2j})$), $i \neq j$ for i, j = 1, 2, 3, and 4. Subsequently, the values of these normalized correlations are used to determine the squared Euclidean distance $D^2(v_{2i}, v_{2j})$ as follows:

$$D^2\left(v_{2i}, v_{2j}\right) = 2E_s\left(1 - \rho\left(v_{2i}, v_{2j}\right)\right) \tag{10}$$

The minimum value of the normalized squared Euclidean distance was 0.33, which was employed to determine the maximum error performance of the 2-bit DSFSC-DCSZ coding system which is expressed as

$$P_e \simeq Q\left(\sqrt{\frac{\min\left\{D^2\left(v_{2i}, v_{2j}\right)\right\}}{2N_0}}\right) \simeq Q\left(\sqrt{\frac{(2E_s\,(0.33))}{2N_0}}\right) \simeq Q\left(\sqrt{\frac{(0.33E_s)}{N_0}}\right) \tag{11}$$

3) RAYLEIGH FADING CHANNEL ANALYSIS FOR OPTIMUM DETECTION DSFSC SYMBOLS

In general, to determine the average error probability, the integrand of the product the probability density function of Rayleigh fading and Gaussian (AWGN), as shown in (12), is evaluated [14], [15], [16].

$$P_e = \int_0^{\infty} p_\gamma\,(\gamma)\,P_e\,(\gamma)\,d\gamma \tag{12}$$

where $p_\gamma(\gamma)$ and $P_e(\gamma)$ are the probability density functions for the Rayleigh fading and Gaussian Q-function of the proposed technique, respectively which are expressed as

$$p_\gamma\,(\gamma) = \frac{1}{\bar{\gamma}} e^{\left(-\frac{\gamma}{\bar{\gamma}}\right)}, \quad \gamma \geq 0 \tag{13}$$

$$P_e\,(\gamma) = Q\left[\sqrt{\frac{E_s}{N_0}\,(1-\rho\,(i,j))}\right] \tag{14}$$

Based on [15], the Q-function is expressed as

$$Q\,(x)\,\frac{1}{\sqrt{2\pi}} \int_x^{\infty} e^{-\frac{t^2}{2}}\,dt = \frac{1}{\pi}\int_0^{\pi/2} e^{\left(-\frac{x^2}{2\sin^2(\theta)}\right)}\,d\theta, \tag{15}$$

By evaluating the Q-function using (14), the Gaussian probability density function of the proposed technique is

$$P_e\,(\gamma) = \frac{1}{\pi}\int_0^{\pi/2} e^{\left(-\frac{\left(\sqrt{\frac{E_s}{N_0}(1-\rho(i,j))}\right)^2}{2\sin^2(\theta)}\right)}\,d\theta = \frac{1}{\pi}\int_0^{\pi/2} e^{\left(-\frac{\frac{E_s}{N_0}(1-\rho(i,j))}{2\sin^2(\theta)}\right)}\,d\theta \tag{16}$$

where $\gamma = \alpha^2\frac{E_s}{N_0}$, $\bar{\gamma} = E\left[\alpha^2\right]\frac{E_s}{N_0}$, α is the channel fading amplitude, and N_0 is the power density Gaussian noise. Based on (12), it can be rewritten as

$$P_e = \int_0^{\infty} \frac{1}{\bar{\gamma}} e^{\left(-\frac{\gamma}{\bar{\gamma}}\right)} \frac{1}{\pi}\int_0^{\pi/2} e^{\left(-\frac{\frac{E_s}{N_0}(1-\rho(i,j))}{2\sin^2(\theta)}\right)}\,d\theta\,d\gamma$$

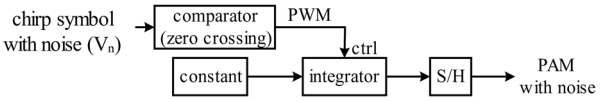

FIGURE 13. Block diagram of decoding algorithm for error performance analysis.

$$P_e = \frac{1}{\pi\bar{\gamma}}\int_0^{\frac{\pi}{2}}\int_0^{\infty} e^{\left(-\frac{(1-\rho(i,j))\gamma}{2\alpha^2\sin^2(\theta)}-\frac{\gamma}{\bar{\gamma}}\right)}\,d\gamma\,d\theta \tag{17}$$

Evaluating $\int_0^{\infty} e^{\left(-\frac{(1-\rho(i,j))\gamma}{2\alpha^2\sin^2(\theta)}-\frac{\gamma}{\bar{\gamma}}\right)}\,d\gamma$ and substituting the result into (17) yields

$$P_e = \frac{1}{\pi}\int_0^{\frac{\pi}{2}} \frac{2\alpha^2\sin^2(\theta)}{\bar{\gamma}\,(1-\rho\,(i,j)) + 2\alpha^2\sin^2(\theta)}\,d\theta = \frac{1}{\pi}\int_0^{\frac{\pi}{2}} \frac{2\alpha^2\sin^2(\theta)}{\Omega\frac{E_s}{N_0}\,(1-\rho\,(i,j)) + 2\alpha^2\sin^2(\theta)}\,d\theta = \frac{1}{\pi}\int_0^{\frac{\pi}{2}} \frac{2\alpha^2\sin^2(\theta)}{E\left[\alpha^2\right]\frac{E_s}{N_0}\,(1-\rho\,(i,j)) + 2\alpha^2\sin^2(\theta)}\,d\theta \tag{18}$$

In this study, the maximum fading error probability P_{emax} is expressed as

$$P_{e\max} = \frac{1}{\pi}\int_0^{\frac{\pi}{2}} \frac{2\alpha^2\sin^2(\theta)}{E\left[\alpha^2\right]\frac{E_s}{N_0}\,(1-\rho_{\max}\,(i,j)) + 2\alpha^2\sin^2(\theta)}\,d\theta, \tag{19}$$

where in the case of a frequency-nonselective, gradually fading channel, $E\left[\alpha^2\right] \approx \alpha^2$. Therefore,

$$P_{e\max} = \frac{1}{\pi}\int_0^{\frac{\pi}{2}} \frac{2\sin^2(\theta)}{\frac{E_s}{N_0}\,(1-\rho_{\max}\,(i,j)) + 2\sin^2(\theta)}\,d\theta = \frac{1}{\pi}\int_0^{\frac{\pi}{2}} \frac{\sin^2(\theta)}{\frac{E_s}{2N_0}\,(1-\rho_{\max}\,(i,j)) + \sin^2(\theta)}\,d\theta \tag{20}$$

4) ERROR PERFORMANCE ANALYSIS FOR PROPOSED ASYNCHRONOUS DETECTION

For the decoding process as shown in Fig. 11, it is known that the differentiator generates noise unpractical. Hence, the zero-crossing technique is applied to avoid corrupted noise. The block diagram of decoding is given in Fig. 13. The error performance analysis is analyzed using this decoding structure is given as follows.

Let the probability density function of AWGN $f\,(V_n)$ contributed to the timing deviation (jitter) of the comparator be

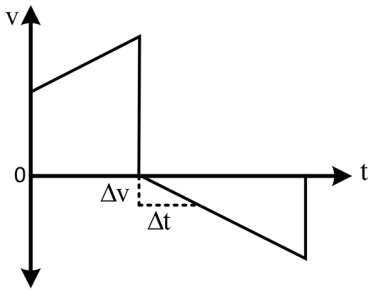

FIGURE 14. The proposed chirp symbol.

given by

$$f\left(V_n\right) = \frac{1}{\sqrt{2\pi V_{nRMS}^2}} e^{-\frac{(V_n)^2}{2V_{nRMS}^2}} \tag{21}$$

where V_n is noise amplitude and $V_{nRMS}^2 = \sigma^2$ is noise variance.

By considering the slope S_i of the ith chirp symbol (see Fig. 14) as $\Delta V_i = S_i \Delta t$, therefore, (21) is rewritten as

$$f\left(\Delta t\right) = \frac{1}{\sqrt{2\pi V_{nRMS}^2}} e^{-\frac{(S_i \Delta t)^2}{2V_{nRMS}^2}} \tag{22}$$

It is seen that (22) is the probability density function of the timing jitter Δt. In the proposed scheme, the parameter of time (in the form of PWM) is changed into voltage (in the form of PAM) therefore, the deviation of output amplitude ΔV_o related to the timing jitter Δt of the jth chirp symbol is $\Delta V_o = S_j \Delta t$ or $\Delta t = \frac{\Delta V_o}{S_j}$. Since every symbol has equally slope, the probability function of the noise amplitude $V_n = \Delta V_o$ contributed to the amplitude of the recovered PAM signal is given by

$$f\left(\Delta V_o\right) = \frac{1}{\sqrt{2\pi V_{nRMS}^2}} e^{-\frac{(\Delta V_o)^2}{2V_{nRMS}^2}} \tag{23}$$

It is seen from (23) that the noise effect is similar to the AWGN that affects the amplitude of the signal. Hence, the proposed demodulation scheme is equivalent to the unipolar PAM signal affected by noise signal as shown in Fig. 13.

The error performance analysis starts with determining the average energy per bit. Referring to (3.2-4 and 3.2-5) of [14], for $m = 1, 2, 3, \ldots, M$ and M is number of amplitude levels of unipolar PAM signal, the average energy per bit is given by

$$E_{bavg} = \frac{E_p}{M} \sum_{m=1}^{M} A_m^2 = \frac{E_p \left(M+1\right)\left(2M+1\right)}{6 \log_2 M} \tag{24}$$

where E_p is the energy of a pulse and A_m is the mth amplitude level. Based on adapting determination analysis of the Euclidean distance of bipolar PAM given in [14], the minimum value of the normalized squared Euclidean distance

TABLE 1. Relationships among data bit, analog level, and initial phase of 2-bit coding.

2-bit data	Initial phase (radians)	$V_p\left(i\right)$ (Volt)
00	$2\pi/5$	1
01	$4\pi/5$	2
10	$6\pi/5$	3
11	$8\pi/5$	4

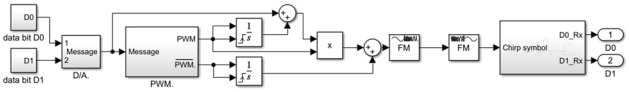

FIGURE 15. Block diagram of modulation and demodulation of 2-bit DSFSC-DCSZ symbol.

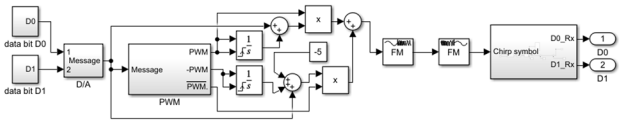

FIGURE 16. Block diagram of modulation and demodulation of 2-bit DSFSC-DCSMF symbol.

between the ith pulse P_i and the jth pulse P_j, $\min\left\{D^2\left(p_i, p_j\right)\right\}$, of the proposed unipolar PAM detection is

$$\min\left\{D^2\left(p_i, p_j\right)\right\} = E_p \tag{25}$$

By substituting (24) into (25), it yields

$$\min\left\{D^2\left(p_i, p_j\right)\right\} = \frac{6E_{bavg} \log_2 M}{\left(M+1\right)\left(2M+1\right)} \tag{26}$$

Therefore, the maximum error performance of the proposed asynchronous detection is given by

$$\begin{aligned} P_e &\simeq Q\left(\sqrt{\frac{\min\left\{D^2\left(p_i, p_j\right)\right\}}{2N_0}}\right) \\ &\simeq Q\left(\sqrt{\frac{6E_{bavg} \log_2 M}{2N_0\left(M+1\right)\left(2M+1\right)}}\right) \end{aligned} \tag{27}$$

For M = 4, the error performance of the DSFSC-DCSZ based on the proposed asynchronous detection is

$$P_e \simeq Q\left(\sqrt{0.133 \frac{E_{bavg}}{N_0}}\right) \tag{28}$$

By considering (20) and (28), the maximum fading error probability P_{error} of the DSFSC-DCSZ is given by

$$P_{e\max} = \frac{1}{\pi} \int_0^{\frac{\pi}{2}} \frac{2\sin^2\left(\theta\right)}{\frac{E_s}{N_0}\left(0.133\right) + 2\sin^2\left(\theta\right)} d\theta \tag{29}$$

For the DSFSC-DCSMF, the error performance in AWGN and fading noise, based on the proposed asynchronous

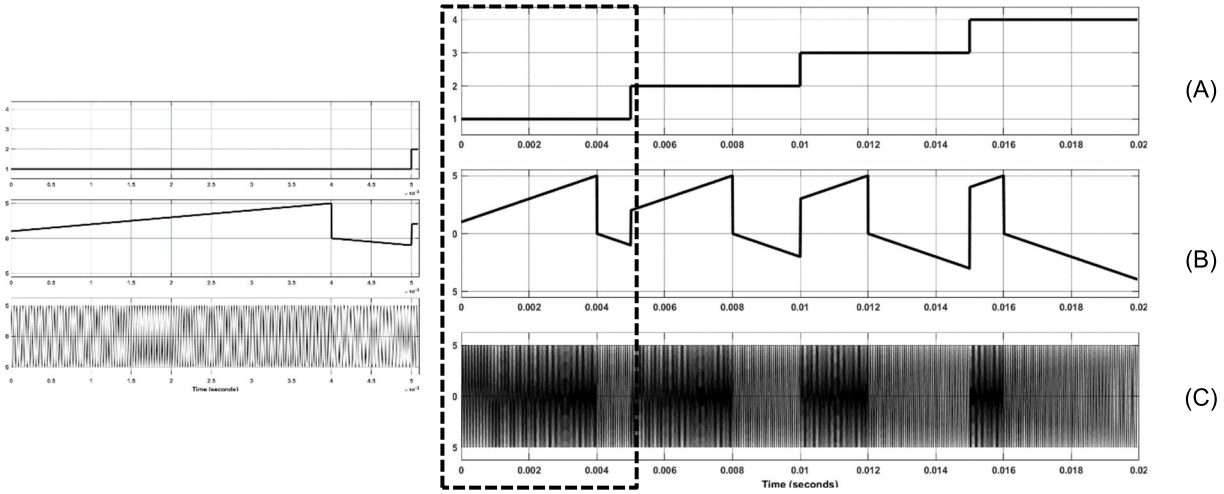

FIGURE 17. Simulation results for modulation of 2-bit DSFSC-DCSZ symbol: (A) data analog signal, (B) waveform of DSFSC-DCSZ symbol, and (C) modulated DSFSC-DCSZ signal.

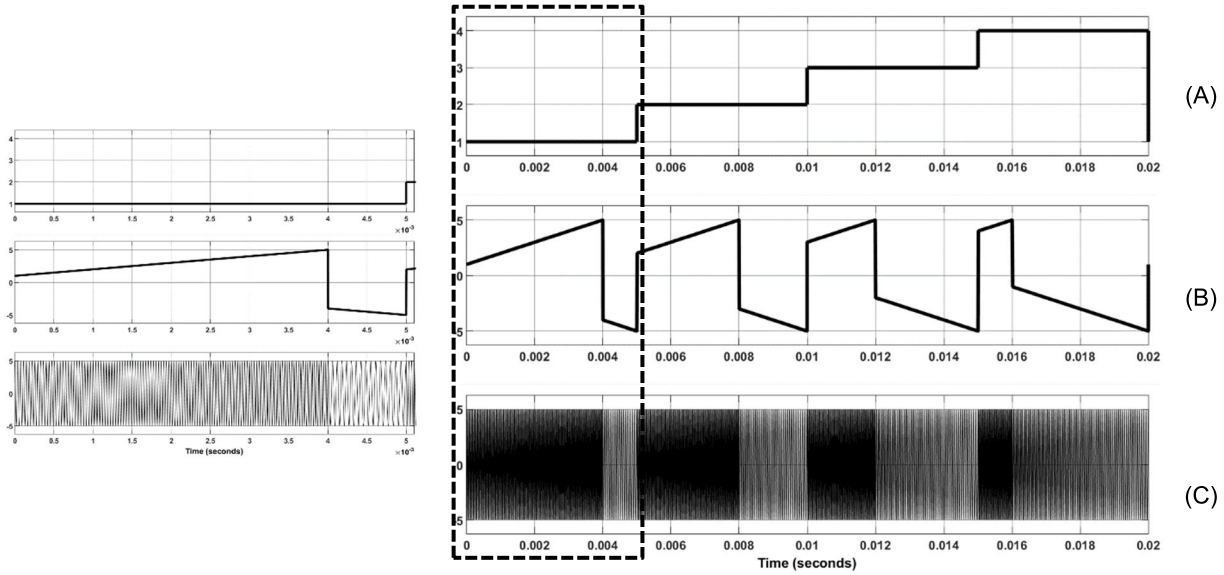

FIGURE 18. Simulation results for modulation of 2-bit DSFSC-DCSMF symbol: (A) data analog signal, (B) waveform of DSFSC-DCSZ symbol, and (C) modulated DSFSC-DCSZ signal.

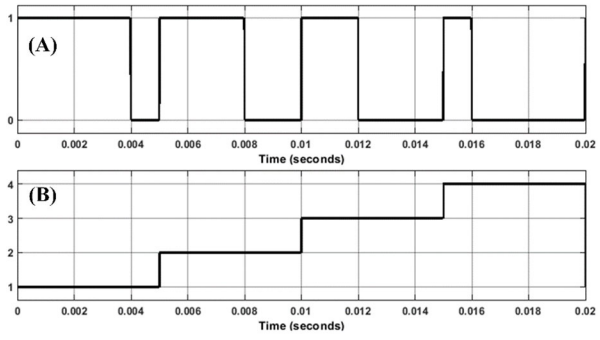

FIGURE 19. Simulation results for demodulation of 2-bit DSFSC symbol: (A) decoded chirp signal, (B) recovered data analog signal.

detection, can be determined using similar analysis as described for the DSFSC-DCSZ. The difference between the DSFSC-DCSMF and the DSFSC-DCSZ lies in the fact that the average energy per bit for DSFSC-DCSMF is times that of the average energy per bit for DSFSC-DCSZ. The error performance and the maximum fading error probability of the DSFSC-DCSMF respectively are

$$P_e \simeq Q\left(\sqrt{0.133\sqrt{2}\frac{E_{bavg}}{N_0}}\right) \tag{30}$$

$$P_{e\max} = \frac{1}{\pi}\int_0^{\frac{\pi}{2}} \frac{2\sin^2(\theta)}{\frac{E_s}{N_0}\left(0.133\sqrt{2}\right) + 2\sin^2(\theta)} d\theta \tag{31}$$

IV. SIMULATION RESULTS

A. DSFSC MODULATION AND DEMODULATION

In this section, the theories of the proposed DSFSC-DCSZ and DSFSC-DCSMF coding are verified via computer

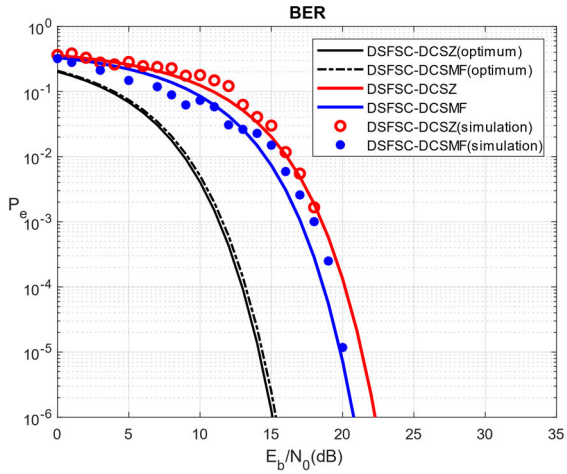

FIGURE 20. Bit error rate performance of proposed coding schemes.

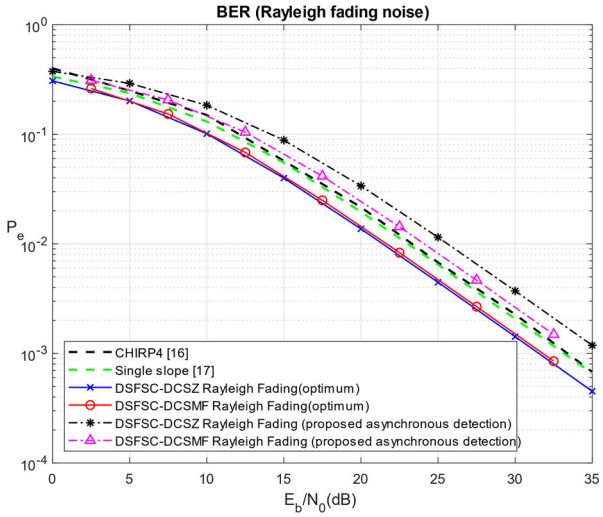

FIGURE 21. Bit error rate Rayleigh Fading performance of proposed coding schemes.

simulation using MATLAB. A 2-bit coding scheme was utilized in the simulation, and the relationships among the data bit, analog level, and initial phase of the four symbols are listed in Table 1. During the modulation process, the VCO was configured with a constant (k_f) of 2 kHz/V, and the minimum frequency ($f_{\min}$) and maximum frequency ($f_{\max}$) of the VCO were set at 15 and 35 kHz, respectively.

The block diagram used to modulate and demodulate the 2-bit DSFSC-DCSZ symbol and 2-bit DSFSC-DCSMF symbol are depicted in Figs. 15 and 16, respectively. The simulation results for the DSFSC-DCSZ and DSFSC-DCSMF cases are presented in Figs. 17 and 18, respectively.

The chirp signals of the DSFSC-DCSZ shown in Fig. 17 (C) and those of the DSFSC-DCSMF shown in Fig. 18 (C) indicate that the frequency of the chirp signal increases linearly and is proportional to the amplitude of the DSFSC symbol as shown in Figs. 17 (B) and 18 (B), respectively. In the demodulation process, the chirp signal is frequency demodulated and the retrieved chirp symbol is then decoded. The simulation results for both cases are the same since the energy per one chirp symbol is equal, as shown in Fig. 17(C) and 18(C). The decoded chirp signal, which is in the form of a PWM signal, is shown in Fig. 19 (A). The recovered analog signal after decoding is shown in Fig. 19 (B).

B. BIT ERROR RATE (BER)

Based on the mathematical analysis presented in Section III-C., the error performances of the proposed coding schemes were examined and the results are shown in Fig. 21. The BER under various power levels of the AWGN for the DSFSC-DCSZ (optimum detection) and DSFSC-DCSMF (optimum detection) coding schemes are predicted using (9) (shown by ——) and (11) (shown by – – – –), for DSFSC-DCSZ (proposed asynchronous detection) (28a) (shown by ——) and DSFSC-DCSMF (proposed asynchronous detection) (28b) (shown by ——), DSFSC-DCSZ (proposed asynchronous detection simulation) (shown by o) and DSFSC-DCSMF (proposed asynchronous detection simulation) (shown by •) respectively.

Additionally, under Rayleigh fading noise (optimum detection) conditions, the BER of both proposed coding schemes shown in Fig. 21, (DSFSC-DCSZ (optimum detection) (shown by —×—) and DSFSC-DCSMF (optimum detection) (shown by —o—)) are similar. When compared with other 2-bit coding schemes, the BER for both the proposed coding schemes outperformed the CHIRP4 scheme [16] (shown by – – –) and the single-slope coding technique [17] (shown by – – –) while —·✱·— and —·△·— are DSFSC-DCSZ and DSFSC-DCSMF (proposed asynchronous detection) respectively.

V. CONCLUSION

In this study, a new cyclic-shift chirp coding method based on a double slope was proposed. Using a double slope within a single symbol offers an inherited clock signal. Therefore, the decoding process can be accomplished via noncoherent decoding. Two forms of DSFSC coding classified based on the down-chirp characteristics, which were abbreviated as DSFSC-DCSZ and DSFSC-DCSMF, were presented herein. Both coding schemes can be decoded using the same noncoherent decoder. Simulation results obtained using MATLAB for the proposed coding schemes indicated that the decoded chirp symbol appeared in the form of a PWM signal. The analog level corresponding to the data bits was retrieved from the width of the PWM signal, and the data bits were then decoded. The error performance analysis for the proposed detection scheme is also presented, demonstrating that the theoretical analysis aligns with the simulation results. Additionally, the Bit Error Rates (BERs) at various noise power levels under a Rayleigh fading channel show that the proposed coding schemes exhibited better BER performance than other comparable coding schemes with optimum detection.

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