IEEE Access
Multidisciplinary ⋮ Rapid Review ⋮ Open Access Journal

Received 3 May 2024, accepted 19 May 2024, date of publication 27 May 2024, date of current version 3 June 2024.

Digital Object Identifier 10.1109/ACCESS.2024.3405624

RESEARCH ARTICLE

A 164-dBΩ Transimpedance Amplifier for Monolithic CMOS-MEMS Oscillators in Biosensing Applications

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This work was supported in part by MCIN/AEI/10.13039/501100011033 "ERDF a way of making Europe" under Project PID2021-122460OB-I00, and in part by the Health Research Institute of the Balearic Islands (IdISBa) and co-funded by European Union under Project PRI22-01.

ABSTRACT This article presents a fully differential tunable high-gain transimpedance amplifier (TIA) conceived as a front-end circuit for monolithic CMOS-MEMS resonators operating in self-sustained oscillation mode. The proposed solution is based on a capacitive-feedback network topology by means of a varactor for gain control. The design is specifically oriented to CMOS-MEMS biosensing applications that require post-CMOS MEMS processing since the adoption of a TIA solution provides robustness against one of such processing steps (i.e., oxygen plasma activation) and a 10× improvement in feedthrough signal elimination compared to a single-ended alternative. The ASIC was fabricated using a 0.35-μm commercial CMOS technology from Austria Microsystems featuring a maximum transimpedance gain of 164 dBΩ with a 10-dB tuning range. It operates at frequencies up to 10 MHz with an input-referred current noise density as low as 13 fA·Hz$^{-1/2}$ providing an exceptional high-performance sensing. With a 3.3 V supply voltage, it exhibits a 1.6 mW power consumption. The TIA was integrated on-chip with various MEMS resonator topologies, either oriented to volatile organic compounds (VOCs) detection or to microfluidics integration for Lab-on-Chip (LoC) systems, corroborating self-sustained oscillation with a 135-ppb measured Allan deviation and 1.1 V output voltage swing.

INDEX TERMS CMOS-MEMS oscillator, transimpedance amplifier (TIA), Lab-on-Chip (LoC), ASIC.

I. INTRODUCTION

The continuous advances achieved by the microelectronics industry have brought robust, precise, and high-performance devices and systems thanks to a sustained miniaturization trend dictated by the well-known Moore's law [1]. These advances provide improved performance at the cost of increased power consumption and still drive business growth within the More Moore framework. More recently, exhaustive research provided a significant functional diversification under the More than Moore paradigm incorporating non-digital traditional functions within Systems-on-Chip (SoC) such as analog/RF, sensing, high power, etc., offering added value by including functionalities based on silicon technologies that do not necessarily scale with Moore's law [2]. One of such domains integrates microelectromechanical systems (MEMS) resonators, as frequency-determining element, in oscillator applications operating either as clock reference generators or sensors thanks to their compatibility and easy integration with CMOS technologies, maintaining nanoscale miniaturization capabilities [3]. Redirecting the More Moore capabilities from a CMOS mature technology to the More than Moore requirements offers key advantages for MEMS like fast turnaround, small footprint, monolithic integration, minimized parasitics, low cost, batch production and well-established design tools [4].

The associate editor coordinating the review of this manuscript and approving it for publication was Norbert Herencsar.

TABLE 1. List of abbreviations and acronyms used in this work.

Abbreviation	Definition	Abbreviation	Definition	Abbreviation	Definition
CMOS	Complementary Metal Oxide Semiconductor	**MEMS**	Micro Electro Mechanical Systems	**TIA**	Transimpedance Amplifier
ASIC	Application Specific Integrated Circuit	**VOC**	Volatile Organic Compound	**LoC**	Lab-on-Chip
SoC	System-on-Chip	**PDMS**	Polydimethylsiloxane	**CC-Beam**	Clamped-Clamped Beam
PMOS	P-Channel Metal Oxide Semiconductor	**NMOS**	N-Channel Metal Oxide Semiconductor	**AMS-035**	Austria Microsystems 0.35-µm CMOS technology
AGC	Automatic Gain Control	**DIP**	Dual In-Line Package	**IC**	Integrated Circuit
RF	Radio Frequency	**FoM**	Figure-of-Merit	**ppb**	Part-per-billion

CMOS-MEMS oscillators for timing applications present impressive performance [5] and have already met mobile phone reference-clock demands [6]. Also, MEMS resonators constitute excellent sensors transducing chemical/physical magnitudes to frequency changes [7], [8] for a straightforward readout that, when coupled to a supporting amplifier, provides self-sustained oscillator operation for real-time frequency tracking with quasi-digital output [9]. In this line, technological trends in MEMS resonators are driven by: (i) nanoscale miniaturization seeking for extremely high sensitivity with challenging electromechanical transduction [10], and (ii) monolithic SoC integration requiring a transduction mechanism integrated on-chip [11].

However, the many advantages provided by the CMOS-MEMS technology involves also enormous efforts to convert the analog MEMS readout signal to the digital domain in a straightforward manner, while implementing a high-performance oscillator [12]. Two well-known readout schemes to build an oscillator with a MEMS resonator are the transimpedance amplifier (TIA) [13] and the modified Pierce topology [14].

The materials available in CMOS technologies to construct high-Q resonators are limited [15], and the mechanical structures' geometry must fulfill the technology design rules constraining their electromechanical performance [16]. As an example, regarding capacitive transduction, typical resonator motional resistances are in the order of MΩ and above [17]. In addition, MEMS scaling-down further reduces capacitive coupling providing very low signal currents, while the resonance frequency increases [18]. Therefore, the on-chip front-end amplifier required to convert such small currents to voltage must achieve very large gain at the operating frequency, while the input-referred current noise is kept at a minimum to guarantee high-performance timing and high-resolution [19]. Power consumption and chip area [20] should be also reduced as required for portable Lab-on-Chip (LoC) applications.

One of the MEMS domains experiencing a huge interest is the one of Bio-MEMS [21], consisting of systems that perform biological and biomedical-related functions [22] by adopting already-existing MEMS knowledge [23] to include bio-compatible materials (PDMS is an example) and in some cases including microfluidic platforms for fluid handling and dispensing. This requires adopting non-standard CMOS fabrication techniques like MEMS surface chemical functionalization for gas sensing [24], or microfluidics integration for micro-calorimetric operation [25]. These two cases, for example, require the adoption of oxygen plasma activation and cleaning steps, that must guarantee no damage induction to the electronic circuitry integrated for signal conditioning and readout. MEMS interfacing with fluidic samples for thermal evaluation require increased interaction area, impacting the resonator feedthrough capacitance, thus degrading the resonator frequency response and compromising the resulting phase shift for Barkhausen criteria completion. All these requirements related to biosensing applications increase the operating constraints on the integrated TIA design.

Given the aforementioned restrictions regarding commercial CMOS compatibility and post-fabrication steps, the objective of this work is focused on the development of a front-end circuitry fulfilling all the electronic, technological and functional constraints described. In this sense, we present the design and experimental results of a fabricated TIA achieving outstanding performance for CMOS-MEMS oscillator operation while fulfilling the robustness requirements related to post-CMOS plasma activation steps, required for biosensing applications. The proposed solution is based on the capacitive feedback topology presented in [26], implemented considering a fully differential scheme to compensate for the large MEMS resonator feedthrough capacitance. This is achieved by connecting both an active and a dummy MEMS resonator as shown in Figure 1. The ASIC was fabricated using a commercial 0.35-μm CMOS technology from Austria Microsystems and incorporates a 10-dB variable gain thanks to integrating a varactor element pair. The amplifier circuit drains 1.6 mW from a 3.3 V power supply and features a maximum transimpedance gain of 164 dBΩ, 10-MHz bandwidth and an input-referred current noise as low as 13 fA·Hz$^{-1/2}$, while occupying a total area of 0.03 mm^2. The system is demonstrated to operate in self-sustained

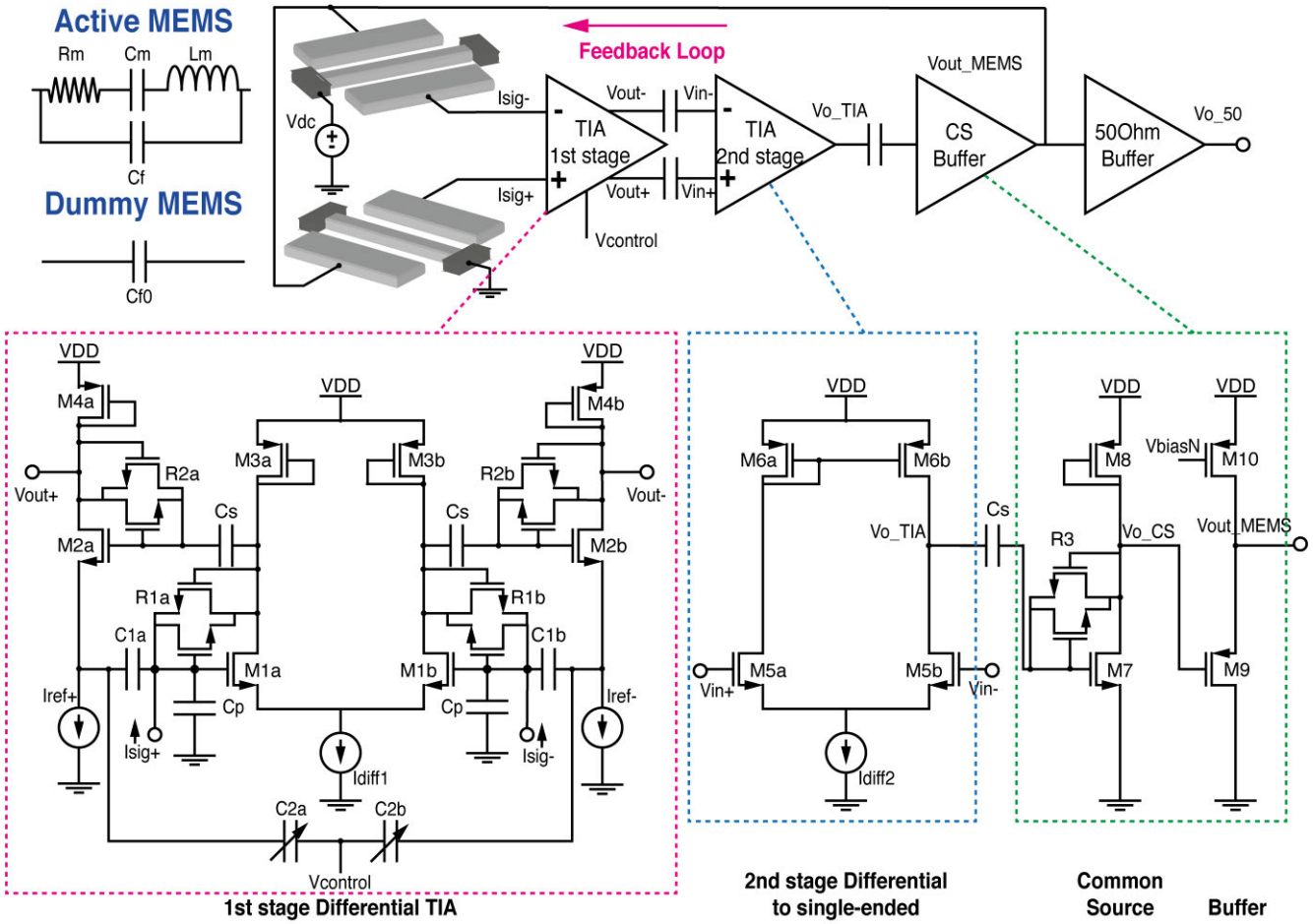

FIGURE 1. Functional diagram of the proposed fully differential gain-controlled TIA operating in self-sustained oscillation mode with detailed transistor-level schematic of each stage. The active (DC biased) and dummy (grounded) MEMS resonators are depicted together with their equivalent RLC lumped model. An additional 50-Ω output buffer is included for benchtop equipment connection and testing purposes. Transistor dimensions in μm: M1 = 4(2.5/0.5), M2 = 4(5.0/0.5), M3 = 2(0.5/0.5), M4 = 2(0.5/0.5), R1 = 1.0/0.5, R2 = 1.0/0.5, R3 = 1.0/0.5 M5 = 4(2.5/0.5), M6 = 2(0.75/0.5), M7 = 2(1.0/0.5), M8 = 2(0.5/0.5), M9 = 20 (8.0/0.5), M10 = 5(6.0/0.5). Capacitances: C_1 = 180 fF, C_2 (max) = 8 pF, C_s = 500 fF. Biasing currents: I_{ref} = 16.2 μA, $I_{diff\,1}$ = 62.9 μA, $I_{diff\,2}$ = 124 μA. V_{DD} = 3.3 V. V_{biasN} = 2.25 V, obtained from a biasing cell. All the elements referred to as Xa and Xb are assumed to be equivalent given the differential nature of the scheme but labelled so for clarification purposes.

oscillating mode when monolithically integrated with two different CMOS-MEMS resonator topologies: (i) a 4-anchored plate resonator for volatile organic compounds (VOCs) sensing with improved linearity that shows an output peak-to-peak voltage of 0.95 V and an Allan deviation of 135 ppb and, (ii) a CC-Beam resonator oriented to micro-calorimetric sensing with 10× improved resonance peak excursion and 1.1 V peak-to-peak output voltage.

The content of this paper is organized as follows. First, the proposed TIA topology is described, and the post-layout simulation results are presented. Second, the plasma effect immunity of such architecture is demonstrated by experimental data, as well as the feedthrough capacitance compensation thanks to a differential topology. Next, measured data of the amplifier noise is shown together with open-loop and closed-loop characterization of the full CMOS-MEMS oscillator system for the two resonators. Finally, a comparison table with state-of-the-art works in the literature is given and the main conclusions summarized.

II. PROPOSED TIA ARCHITECTURE

The first stage (i) is a capacitive-feedback TIA based on the topology reported in [26]. As depicted in Figure 1, the original architecture was extended to a fully differential input for feedthrough signal cancelation [13] while C_2 was replaced by a varactor pair with common node for gain tuning through a control voltage ($V_{control}$). Feedthrough cancellation is achieved by using an active MEMS resonator, i.e. DC-biased, which sources both motional and feedthrough currents and a twin dummy resonator, i.e. grounded, that only sources the feedthrough signal (see Figure 1). This scheme was chosen because, compared to the modified Pierce topology used in previous works (which uses the MEMS resonator and adjacent metal tracks parasitic capacitance (C_p in Figure 1) to integrate the motional current [27]), the presented TIA shows independence of the open-loop transimpedance gain against such parasitic capacitance [12]. Even though the Pierce topology can attain a larger transimpedance gain and superior oscillator noise rejection thanks to a high input impedance

provided by a noiseless capacitive element, the TIA reported here meets the gain demands of resonators working in the sub-10-MHz range and achieves an input-referred current noise below most state-of-the-art works for high-performance oscillators.

The overall transimpedance amplifier is also composed by (ii) a second stage as a differential pair to convert the differential signal to a single-ended one, followed by (iii) a common-source stage amplifier with diode-connected PMOS load to give an extra open-loop gain and a PMOS-based source follower buffer to feed the MEMS resonator actuation electrode in self-oscillation mode. Additionally, a 50-Ω buffer is included to drive 50-Ω loads. The biasing currents are obtained from a standard current mirror scheme and the voltage V_{biasN} from a highly stable biasing network. The transistors sizes chosen for this design are given in Figure 1, as well as the biasing currents value and capacitances; all transistors feature a channel length of 0.5 μm.

A. CAPACITIVE-FEEDBACK CURRENT AMPLIFIER

The proposed circuit first stage (Figure1) consists of a NMOS differential pair amplifier, namely M1a-M1b loaded by M3a-M3b, with a sufficient voltage gain while keeping a balanced voltage at its inputs. This leads to a differential current amplifier that integrates the current through C_1 generating a voltage drop through C_2 and, consequently, proportionally amplifying the current according to the capacitance ratio. Such current is converted to a voltage thanks to loading the drains of M2a-M2b with an active resistor, implemented with a diode-connected PMOS load for maximum AC gain. The resulting transimpedance gain of the first stage is given by [13]

$$\frac{\Delta V_{out}}{\Delta I_{sig}} = \left(1 + \frac{1}{2}\frac{C_2}{C_1}\right)\frac{1}{g_{m,M4}}, \tag{1}$$

being $g_{m,M4}$ the transconductance of M4. The DC biasing point is set by a highly resistive antiparallel NMOS transistor pair (R_1) operating in the sub-threshold region which exhibits an equivalent resistance in the order of GΩ and plays a negligible role on the operating frequency [28]. Subsequent stages are AC-coupled to avoid DC offset effects, allowing for independent stage biasing. Gain control was implemented using two varying capacitors, i.e. a varactor element, as C_2, given that the transimpedance gain is directly proportional to such value and can be voltage tuned. The on-chip integrated varactors were implemented by a MOS structure with terminals connected to the gate and N+ contacts inside a N-well [29], respectively, that were already available within the AMS-C35 technology design kit. The control voltage was applied to the N+ contact side and changed the equivalent MOS capacitance when ranging from 0 to 3.3V, being at its maximum when $V_{control}$ was set to 0 V. The fully differential topology requires including two varactors in series, for which the transimpedance gain is half the value of C_2, with the control voltage applied at the common node (see Figure 1).

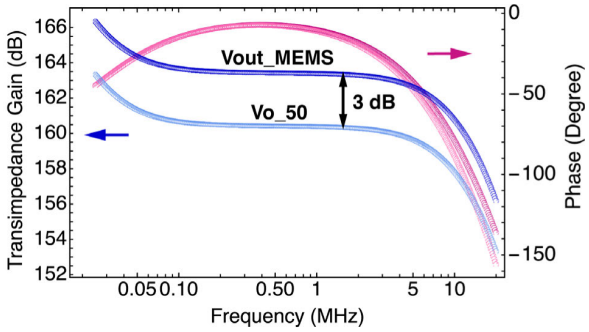

FIGURE 2. Post-layout simulation Bode plot for V_{out_MEMS} and V_{o_50} nodes, respectively. The results have been obtained for a parasitic capacitance of 20 fF at the input node and a control voltage of 0 V (maximum gain).

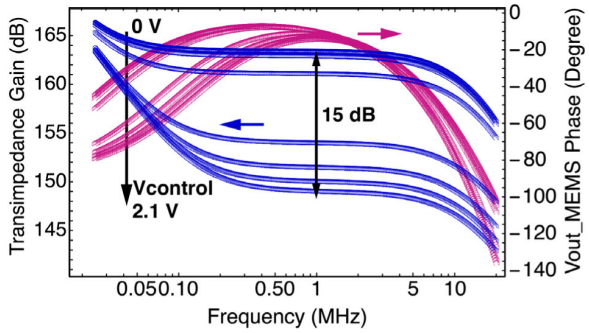

FIGURE 3. Post-layout simulation Bode plot for the V_{out_MEMS} node as a function of the control voltage from 0 V to 2.1 V, obtaining an overall 15 dB gain excursion. The results have been obtained for a parasitic capacitance of 20 fF at the input node.

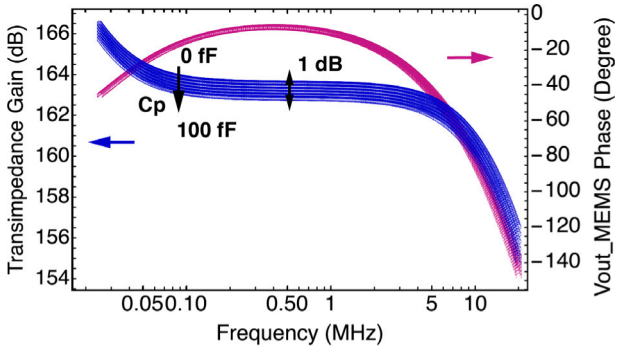

FIGURE 4. Post-layout simulation Bode plot for the V_{out_MEMS} node as a function of the parasitic capacitance (Cp) at the input node ranging from 0 fF to 100 fF. The results have been obtained for a control voltage of 0 V.

The proposed topology exhibits several advantages for MEMS applications compared to a resistive-feedback TIA [13]: it has enhanced noise performance since the gain is provided by a noiseless capacitive network and also provides superior gain because it is set through a capacitance ratio rather than a resistor. The on-chip integrated capacitances present some limitations given that a minimum value is set by the technology Poly-Poly capacitor module and its maximum value is set by the varactor element, leading to a design trade-off that balances variability, gain and area. The overall area plays a minor role since the circuit footprint bottleneck should also consider the MEMS element dimensions together with the readout amplifier.

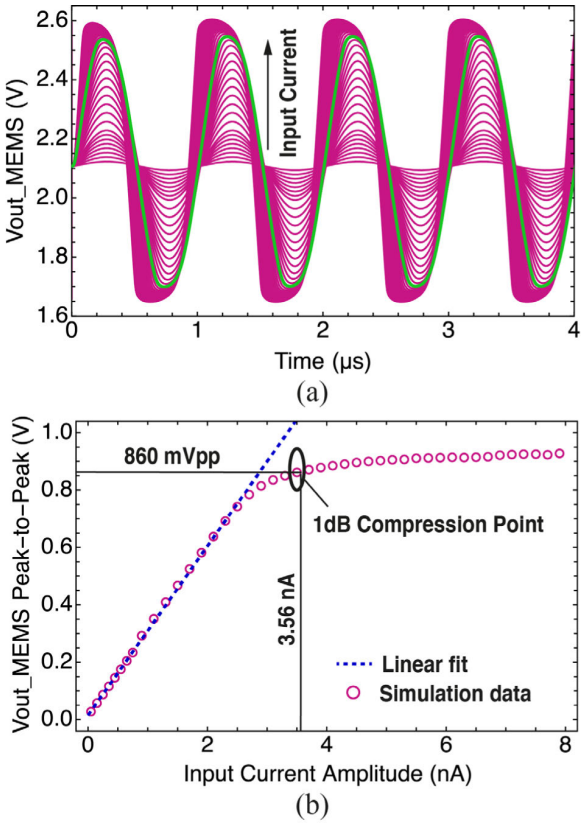

FIGURE 5. Post-layout transient simulation analysis to study the linearity of the TIA. (a) Voltage waveform at the V_{out_MEMS} node for varying input current amplitude ranging from 100 pA to 8 nA at a frequency of 1 MHz. The waveform corresponding to the 1-dB compression point is highlighted in green. (b) Peak-to-peak voltage at the given node vs. input current simulation results; the blue dashed line follows a linear fit at small current amplitude resulting into a 1-dB compression point of 860 mVpp.

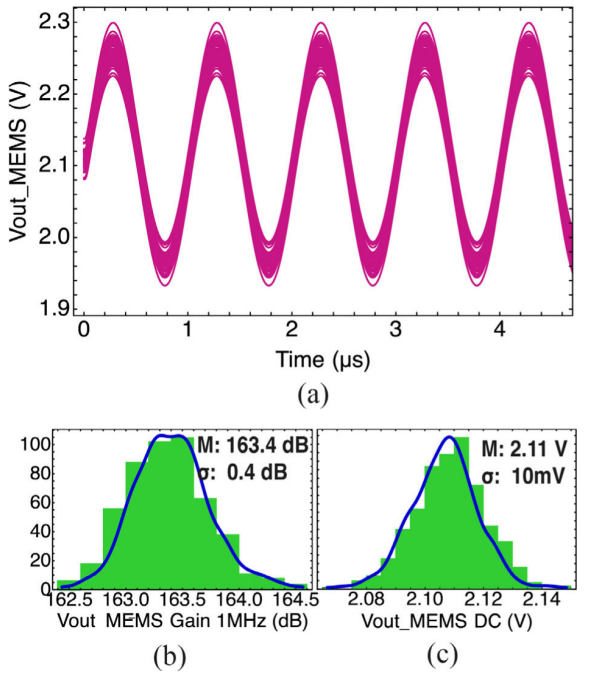

FIGURE 6. Post-layout Monte Carlo simulation results for 500 iterations. (a) Voltage waveform plot at the V_{out_MEMS} node for an input current amplitude of 1 nA and frequency of 1 MHz. (b) Histogram plot of the AC gain at a 1 MHz frequency for a control voltage of 0 V. (c) Histogram plot of the DC voltage value at such node.

Accounting for the differential nature of the topology, all elements, either transistors or capacitors, that come in pairs were laid out following the standard common-centroid guidelines to minor mismatch fabrication variability ending up with an optimal design. This led to implementing all paired capacitors as two parallel elements each with half the value of the target capacitance.

B. POST-LAYOUT SIMULATION RESULTS

Extensive simulation analyses were carried out to confirm the expected circuit operation at the post-layout level to account for parasitic components. For simulation purposes, the resulting MEMS resonator current was mimicked via a current source between the two input nodes. Figure 2 depicts the Bode plot for the resulting transfer function, i.e. voltage over input current, at the V_{out_MEMS} and V_{o_50} nodes under AC analysis, to show a 3-dB drop in the open loop magnitude due to the 50-Ω output buffer attenuation. Simulation results in Figure 2 show a maximum transimpedance gain of 164 dBΩ within the operating bandwidth for $V_{control}$ 0 V. Figure 3 represents the resulting transimpedance gain at the TIA output as a function of the control voltage resulting into a simulated gain tuning range of 15 dB, while the phase is kept roughly constant within the operation bandwidth being a paramount advantage for automatic gain control (AGC) topologies. Notice that $V_{control}$ was raised up to 2.1 V given that experimental characterization showed no further reduction at this value. The transimpedance gain Bode plot was also obtained for values of the MEMS parasitic capacitance to confirm the topology mitigation to such input loading. Figure 4 demonstrates only a 1-dB drop and a constant phase plot after raising C_p up to 100 fF when a typical value for MEMS resonators for this technology is safely assumed below 50 fF. This advantage of the TIA reported in this article is crucial for plasma tolerance as further detailed next.

We also completed transient simulations to ensure proper operation and to characterize the TIA linearity and output voltage swing. Figure 5a plots the resulting voltage waveform at V_{out_MEMS} when the input test current source was set to a 1-MHz frequency while sweeping the amplitude from 100 pA to 8 nA. The voltage swing obtained approached 1 Vpp and a linear operation was ensured up to 860 mVpp where the 1-dB compression point was found (see Fig. 5b). The voltage waveform flattened and deviated from sinusoidal in a symmetrical way, i.e. both at the upper and lower non-linear boundaries.

Monte Carlo simulations (500 iterations) confirmed the proposed design robustness to variability and mismatch as demonstrated in Figure 6. The subsequent voltage waveforms depicted in Figure 6a for an input current amplitude of 1 nA within the linear range largely falls within safety margins of DC biasing point and resulting amplitude. This was further

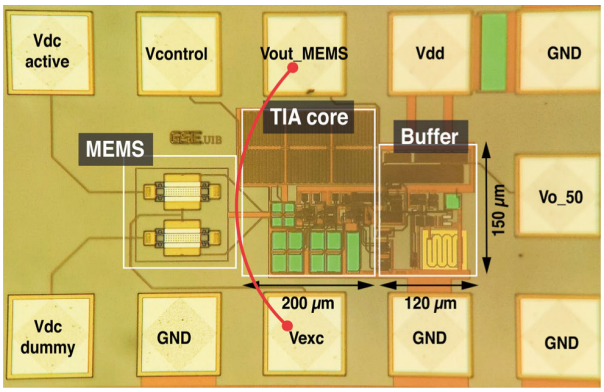

FIGURE 7. Optical image of the CMOS-MEMS oscillator IC fabricated in a CMOS 0.35-μm commercial technology from Austria Microsystems (AMS-035). The MEMS resonator region is highlighted in a dashed-line area and so does the TIA core, output buffer and biasing network. The closed-loop bonding for self-sustained operation is drawn as well.

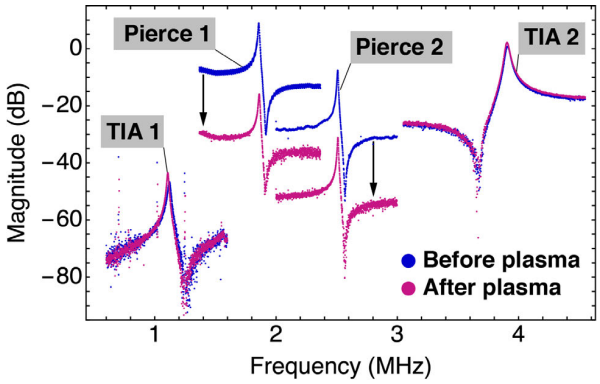

FIGURE 8. Plasma effect characterization. Experimental open-loop electromechanical transmission coefficient measured before and after 2-min oxygen plasma activation for various MEMS resonator structures monolithically integrated with a TIA and a Pierce amplifier, respectively. It is clearly stated that the TIA topology shows a much-improved tolerance. TIA2 refers to the topology presented here, TIA1 refers to [12], Pierce1 to [14] and Pierce2 to [9].

confirmed in Figure 6b and Figure 6c where the DC voltage obtained was 2.11 V with a deviation of 10 mV (0.5 %). The transimpedance gain was 163.4 dB with a deviation of 0.37 dB (0.2%).

III. CMOS-MEMS INTEGRATION

The CMOS-MEMS IC was fabricated in a 0.35-μm commercial CMOS technology (AMS-C35) constituting a mature technology, offering low fabrication cost and fast turnaround. This technology is supplied at 3.3 V and comprises a four-metal-layer stack interconnected by tungsten VIAs and a two-polysilicon-layer capacitor module. The MEMS resonators were constructed using one of the metal layers for which a post-CMOS wet-etching step was required to remove the sacrificial oxide and release the mechanical moving parts. This step was completed at our lab facilities, after having received the dies from the foundry, by using a commercial etchant (Silox Vapox III from Transene Company, Inc.); further details on the fabrication process can be found in [14] and [17]. This fabrication approach allows for a co-fabrication of the MEMS resonators and the readout circuit. After post-processing, the CMOS dies were attached, and wire bonded to a standard DIP chip carrier and mounted on a PCB.

Figure 7 is an optical image of the fabricated chip with the MEMS resonator pair monolithically integrated with the TIA circuit together with the 50-Ω buffer and the biasing circuitry. The circuit was designed to operate both in open- and closed-loop mode by performing a wire bond between the MEMS actuation voltage (V_{exc}) and the TIA output (V_{out_MEMS}). The dummy MEMS was typically biased to GND to eliminate its motional capacitive current even though the design allows some flexibility by routing it to a bonding PAD different from GND.

IV. PERFORMANCE IN CMOS-MEMS BIOSENSORS

A. ROBUSTNESS TO PLASMA

(i) The development of VOCs sensing systems requires to activate the MEMS resonator surface prior to functionalization [30] and, (ii) the integration of a micro-calorimeter within a microfluidics platform requires a plasma activation for the PDMS layer to be properly bonded to the IC passivation layer, sealing the micro-channels. Then, the CMOS IC undergoes such cleaning/activation steps in both applications for which robustness to plasma must be ensured for the on-chip readout circuit.

After several experimental evidence from various IC generations and amplifier topologies, we observed that the Pierce topology was damaged during the plasma process experiencing an important reduction of the open-loop transimpedance gain. However, the TIA alternative presented here remained resistant to such plasma process as shown in Figure 8. We measured the open-loop transmission coefficient of a MEMS-TIA pair right after post-CMOS wet-etching, and then applied an oxygen plasma cleaning step (Harrick Plasma PDC-002) for 2 minutes at maximum power to measure again the open-loop response. We repeated this same procedure for four amplifier topologies: (i) single-ended TIA as reported in [12], (ii) differential TIA in this article, (iii) single-ended Pierce [14], and (iv) differential Pierce [9]. Figure 8 depicts the measured data showing that the Pierce topology suffered an important -20dB gain degradation after the plasma treatment that the TIA version did not. In the case of the Pierce topologies, the gain reduction prevented the CMOS-MEMS oscillator to meet the Barkhausen criteria for self-sustained oscillation, being critical for the overall system operation. Sample evaluation revealed that the damage over the CMOS circuit was not directly related to the semiconductor active elements operation, but to the amplifier working principle as described next.

The oxygen plasma is a partially ionized gas that contains electrons and ions resulting from applying an RF AC electric field together with low-pressure operation. This leads to the well-known antenna effect in CMOS fabrication [31] for which the exposed metals collect ions from the environment that, if finding a direct path to ground, result in no further

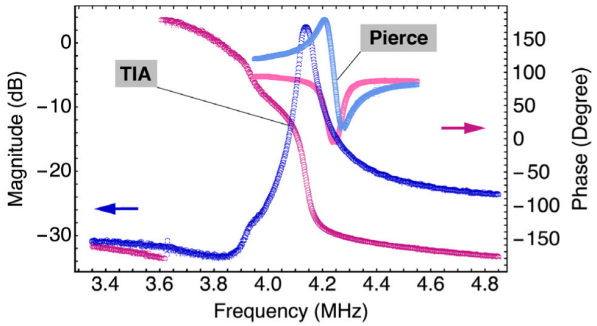

FIGURE 9. Experimental open-loop characterization depicting the electromechanical transmission coefficient Bode plot for the same MEMS CC-Beam resonator oriented to micro-calorimetric operation comparing the differential TIA and single-ended Pierce amplifiers performance, respectively. Due to the differential nature of the TIA architecture, the feedthrough capacitance is mostly cancelled out for which a much larger resonance peak is achieved, as well as a larger frequency shift compared to the Pierce topology.

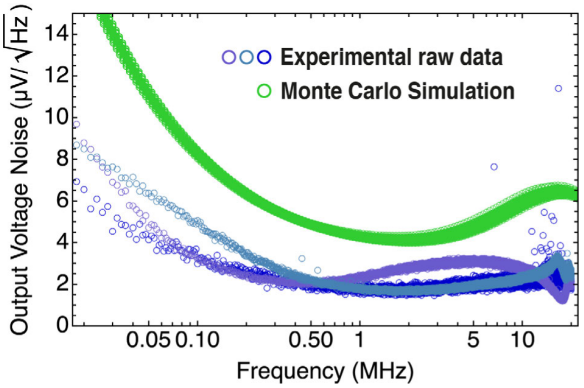

FIGURE 10. Output voltage noise spectrum at the V_{o_50} node obtained from post-layout simulations (green circles) and experimental raw data from the fabricated TIA (blue circles) for three different dies. The experimental data was captured using the Noise Marker function from a Rode&Schwartz FSVA4 spectrum analyzer, which is specifically oriented to measure the noise density spectrum from noise-like signals.

damage. However, if these ions hit the transistor gate oxide, they may cause breakdown or remain trapped. The Pierce amplifier topology integrates a current through the input capacitance at the node where the readout electrode feeds the sensing current (very high impedance node). This node has an exposed metal, the MEMS readout electrode, that can collect the charges generated by the plasma and cannot be driven to ground. Therefore, the parasitic capacitance increases and the overall transimpedance gain is degraded. On the contrary, the TIA open-loop gain depends on the ratio of two integrated capacitances and not on the intrinsic parasitic capacitance. Despite the same charge trapping process could occur, the amplifier topology mitigates any further degradation and becomes robust to plasma activation.

B. FEEDTHROUGH SIGNAL CANCELATION

The micro-calorimeter-oriented design reported in [25] uses a buried-metal fabrication approach in which the CC-Beam resonator was defined at the MET2 level while MET3-MET4 were reserved for a two-level covering grid with regularly spaced holes for zero-level packaging and PDMS adhesion compatibility [32]. Moreover, this fabrication strategy was demonstrated to noticeably improve the wet-etching release reliability thanks to a controlled diffusion mechanism [33]. Yet, this fabrication strategy inevitably leads to an enlarged feedthrough capacitance that overshadows the motional sensing signal and limits the self-oscillation abilities even to the extent of not completing the Barkhausen criteria due to a moderate phase shift. This picture can be directly made extensive to other geometries that, although not using the same fabrication strategy, exhibit an important feedthrough capacitance. The proposed fully differential TIA topology mostly cancels the feedthrough signals compared to a single-ended alternative.

Figure 9 demonstrates for the same CMOS-MEMS CC-Beam resonator, via open-loop experimental data, how a single-ended Pierce topology suffers from signal loss due to the feedthrough capacitance: the achieved phase shift and resonance peak excursion are minored. On the contrary, the reported fully differential TIA improves the peak excursion by 10-times and so does the open-loop phase shift.

V. EXPERIMENTAL RESULTS AND COMPARISON

The fabricated IC integrating the designed TIA and a CMOS-MEMS resonator pair was experimentally characterized under several conditions. First, the output voltage noise was measured. Then, two integrated resonator topologies, i.e., one oriented to VOCs sensing and another to micro-calorimetric operation, were measured both in open- and closed-loop configurations as detailed in the following sub-sections. The DC voltages, either the CMOS supply, the MEMS biasing, and the control voltage were powered by a source measure unit (Keysight B2900). The transmission coefficient in open-loop mode was measured using a network analyzer (Keysight ENA 5061B) and the oscillation frequency recorded via a frequency counter (Pendulum CNT-91). The noise spectrum was recorded using a spectrum analyzer (Rhode&Schwartz FSVA4).

A. TIA OUTPUT VOLTAGE NOISE

Figure 10 plots the experimentally measured voltage noise spectral density at V_{o_50} for the TIA from three dies (depicted in different blue scale) to illustrate process variability and compares it to the post-layout Monte Carlo simulation outcomes (in green), being all of them in good agreement. This measurement was performed by setting the MEMS excitation voltage and its DC biasing to GND to isolate the TIA noise contribution. The acquired data provided a voltage noise of 1.44 μV·Hz$^{-1/2}$ at 2 MHz, directly related to an input-referred current noise of 13 fA·Hz$^{-1/2}$ accounting for the transimpedance gain.

B. MEMS PLATE RESONATOR FOR VOCS

One MEMS structure integrated with the sustaining TIA was a plate resonator equivalent to the one reported previously [34], implemented as a pair for fully differential

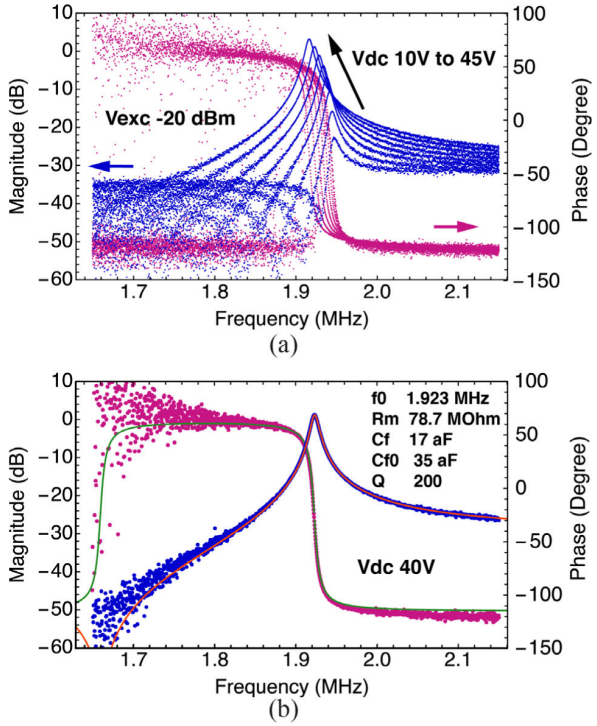

FIGURE 11. Open-loop experimental characterization of the MEMS plate resonator for VOCs sensing integrated on-chip with the readout TIA. (a) Electromechanical transmission coefficient Bode plot for Vdc ranging from 10 V to 45 V and an input power of – 20dBm. (b) RLC model fit for Vdc 40 V to obtain an accurate estimation of the MEMS plate resonator parameters thanks to the TIA capabilities, i.e. transimpedance gain almost insensitive to varying input parasitic capacitance.

operation, specifically oriented for VOCs monitoring. An open-loop characterization was done to obtain the transmission coefficient magnitude and phase, as depicted in Figure 11a, checking for Barkhausen criteria completion. Results demonstrate a clean phase transition with large shift and a resonance peak 35 dB above remaining feedthrough signal level thanks to the differential topology. Figure 11b illustrates the RLC model (see Figure 1) characterization of the integrated MEMS resonator provided that the TIA gain roughly depends on the structure parasitic capacitance and offers accurate values to be used in subsequent design stages. The resulting derived motional resistance was 78.7 MΩ, a good match for the theoretically predicted 59 MΩ [32]. The varactor-based gain tuning mechanism was confirmed experimentally: Figure 12 demonstrates a 10 dB tuning range for V_{o_50} being swept from 0 V to 2.1 V when plotting the open-loop transmission coefficient at a fixed MEMS DC bias of 40 V. A relevant aspect is that the phase curves overlap each other showing no influence of the control voltage on such characteristic, an important advance for AGC solutions since no extra phase distortion is included.

Self-sustained oscillation was verified by closing the feedback loop obtaining the output voltage waveform depicted in Figure 13a. The peak-to-peak voltage measured was 675 mV_{pp} at V_{o_50} which leads to a 950 mV_{pp} voltage excursion at V_{out_MEMS}, the node at which the signal is fed

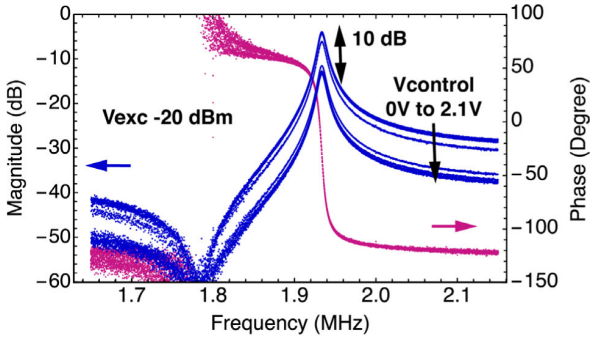

FIGURE 12. Experimentally measured open-loop electromechanical transmission coefficient Bode plot for a MEMS plate resonator vs. the control voltage ranging from 0 V to 2.1 V. The MEMS DC bias voltage is set to 40 V. The designed and fabricated TIA gives a gain tuning range of 10 dB from experimental data.

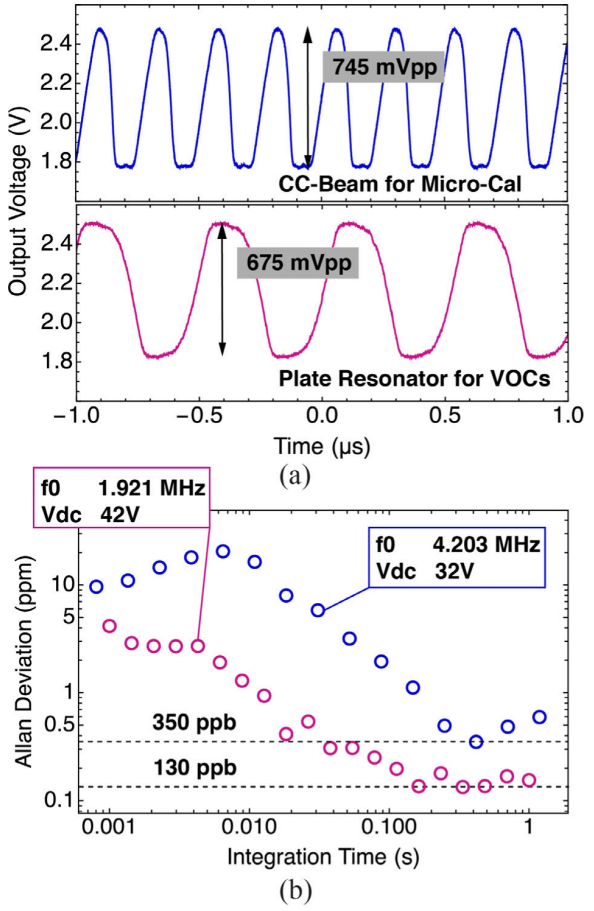

FIGURE 13. Self-sustained CMOS-MEMS oscillator experimental characterization for the integrated MEMS resonators: (i) CC-Beam for Micro-Cal and Plate Resonator for VOCs. (a) V_{o_50} voltage waveform with a measured peak-to-peak voltage of 745 mVpp and 675 mVpp, respectively. (b) Measured Allan deviation versus the integration time for a biasing voltage of 32 V and 42 V, showing an optimum frequency stability of 350 ppb and 130 ppb, respectively.

back to the MEMS resonator actuation electrode. The signal linearity was kept in good conditions given a highly linear MEMS structure and, as earlier stated from simulations, maintains a symmetrical behavior. These facts, together with a high-performance noise density, leads to a measured Allan

TABLE 2. CMOS-MEMS integrated TIAs summary and performance comparison with state-of-the-art.

	GSE-UIB This work	GSE-UIB [12]	NTHU [36]	NUS [37]	Stanford [13]	Geor. Tech [35]	ETS Mont. [38]	Stanford [39]	TU Delft [28]
CMOS Technology	0.35-µm AMS	0.35-µm AMS	0.35-µm TSMC	0.35-µm	0.18-µm	0.35-µm TSMC	65-nm TSMC	0.35-µm	0.18-µm
Topology	Differential	Single-ended	Single-ended	Differential	Differential	Single-ended	Differential	Single-ended	Single-ended
Results	Measured	Measured	Measured	Measured	Measured	Measured	Measured	Measured	Measured
Supply (V)	3.3	3.3	2.5	1.5	1.8	3.3	1.0	2.5	1.8
Area (μm^2)	200 × 150	100 × 200	140 × 400	-	280 × 180	25 × 55	130 × 225	300 × 500	400 × 400
Power (mW)	1.6	0.91	0.15	0.58	0.44	0.80	0.9	6.9	5.2
Output Swing (V_{pp})	1.1	0.38	1.5	-	-	-	-	-	-
Max. Gain (dBΩ)	164	121	138	153	155	106	98	97	107
Gain tuning range (dB)	10	10	-	-	-	-	15	15	33
Frequency (MHz)	10	50	1.2	0.21	1.8	10	140	20	7.0
In. Noise ($fA/Hz^{1/2}$)	13	190	25	6.7	65	310	15000	2400	1700
Out. Noise ($\mu V/Hz^{1/2}$)	2.0	0.23	0.20	0.30	3.6	0.062	1.2	0.16	0.38
FoM	1.6×10^{24}	3.1×10^{23}	6.6×10^{22}	1.9×10^{22}	7.3×10^{21}	5.4×10^{21}	4.1×10^{20}	4.3×10^{19}	1.4×10^{19}

deviation of 130 ppb in Figure 13b for a biasing voltage of 42 V and an operating frequency of 1.92 MHz.

C. MEMS CC-BEAM RESONATOR FOR MICRO-CALORIMETER

The second MEMS structure integrated with the sustaining amplifier was a CC-Beam resonator, previously reported in [25], oriented to microfluidics integration and micro-calorimetric sensing in biological, chemical and biomedical applications. The open-loop characterization is given in Figure 9 showing again a 35-dB resonance peak excursion and large phase shift suited for self-sustained oscillator operation. It was corroborated (see Figure 13a and Figure 13b) with a voltage excursion of 1.1 V_{pp} at V_{out_MEMS} and a measured Allan deviation of 350 ppb, a larger value compared to the VOCs-oriented MEMS platform attributed to the MEMS CC-Beam larger non-linear behavior, the voltage waveform in Fig. 13a shows such non-linearity.

D. COMPARISON WITH THE STATE-OF-THE-ART

The TIA reported in this work, besides the advantages already highlighted like C_p-independent gain, plasma robustness and feedthrough signal cancelation, offers performance figures that positively compare to most prior art described alternatives. Table 2 summarizes the most prominent TIA amplifiers found in the literature and compares their design, implementation and performance. A typical Figure-of-Merit (FoM) is defined as

$$FoM = \frac{k_B T}{V_{on}^2} \frac{f_0^2 R_M^2}{P}, \tag{2}$$

where V_{on} stands for the output voltage noise density, f_0 refers to the −3dB bandwidth or the given operating frequency if the first fails to be included, R_M to the transimpedance gain, and P to the TIA core power consumption. Among all works in the literature, only this work and three others implemented a differential topology. The presented circuit occupies the smallest area, except for a solution from Georgia Tech [35] at the cost of a much lower transimpedance gain. In terms of power consumption, our solution presents the highest value, even only facing a 4× increase [13], among the differential topologies because of featuring the best gain-bandwidth-noise trade-off. This fact is entirely supported by achieving a very promising FoM of 1.6×10^{24}, almost one order of magnitude superior to our previous single-ended work [12] and 20-times larger than a high-performance circuit from NTHU [36]. Moreover, the higher transimpedance gain, 164 dBΩ, is attained by our solution and only followed 10-dB behind by a work from Stanford [13]. In this line, the gain tuning range is comparable to its counterparts, except for the work in [28] that achieves an experimental 33-dB tuning range thanks to a complex and area-hungry capacitive ladder feedback network. Finally, a paramount figure for CMOS-MEMS oscillators like the input-referred current noise is found to be also in the top, i.e. 13 $fA{\cdot}Hz^{-1/2}$, only surpassed by an alternative operating at a 210-kHz frequency [37].

The circuit presented in this work, compared to existing solutions reviewed in Table 2, attains great potential for signal readout in CMOS-MEMS biosensing oscillators, which highlights the prominence of the results reported. Such experimental outcomes demonstrate part-per-billion frequency resolution in oscillator closed-loop topology aligned with high-resolution sensing. It provides an optimal differential topology for feedthrough reduction in large-area resonators, offers an excellent noise level for ultra-stable frequency resolution and offers compatibility with post-processing steps required for a variety of applications in the biomedical domain. Also, featuring the largest gain in Table 2 is a paramount advantage to interface high-performance MEMS resonators. To the extent of the author's knowledge, limited counterparts have been proposed to fulfill all highlighted strengths.

VI. CONCLUSION AND FUTURE WORK

We designed, simulated, and experimentally characterized a fully differential TIA for CMOS-MEMS monolithic integrated oscillators using a capacitive feedback network topology with a varactor-based variable-gain strategy. The proposed architecture is specifically suited for biosensing applications thanks to its robustness against plasma activation processes and signal feedthrough cancellation. The overall performance was evaluated to offer a high transimpedance gain of 164 dBΩ with 10-dB tuning range, 10-MHz operating frequency and a low current noise of 13 fA·Hz$^{-1/2}$ revealing as the best alternative in the reviewed state-of-the-art literature with a FoM of 1.6×10^{24}.

The circuit design was sustained by extensive post-layout simulations, including Monte Carlo analysis, and positively compared to the experimental data in terms of output voltage noise density. The plasma robustness and feedthrough cancellation were experimentally confirmed, together with the CMOS-MEMS self-sustained operation when co-integrated with a MEMS plate resonator for VOCs sensing and a CC-Beam for micro-calorimetric operation. The resulting oscillation figures demonstrated a measured Allan deviation parameter of 135 ppb and a voltage output swing at the feedback node of 1.1 V. Overall, this design represents a promising solution for high-sensitive CMOS-MEMS oscillators in Lab-on-Chip systems oriented to biosensing applications.

The present work opens a wide range of future research directions as it represents a generic solution for CMOS-MEMS oscillators. Exploitation of this topology in Lab-on-Chip systems oriented to biosensing applications will enable the development of an integrated CMOS-MEMS microcalorimeter or the differential readout in functionally-active VOCs resonators over a non-active reference.

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