IEEE Access
Multidisciplinary | Rapid Review | Open Access Journal

Received 9 May 2024, accepted 21 May 2024, date of publication 27 May 2024, date of current version 3 June 2024.

Digital Object Identifier 10.1109/ACCESS.2024.3405533

RESEARCH ARTICLE

Experimental Investigations on Photovoltaic Interface Neutral Point Clamped Multilevel Inverter-Based Shunt Active Power Filter to Enhance Grid Power Quality

RAJENDRAN BOOPATHI AND VAIRAVASUNDARAM INDRAGANDHI
School of Electrical Engineering, Vellore Institute of Technology, Vellore 632014, India
Corresponding author: Vairavasundaram Indragandhi (indragandhi.v@vit.ac.in)

ABSTRACT In this research study, a photovoltaic (PV) interface three-level Neutral Point clamped (NPC) voltage source inverter-based three-phase Shunt Active Power Filter (SAPF) has been proposed. Initially, the major power quality issues, such as compensating for reactive power, minimizing Total Harmonic Distortion (THD) of source current, improving power factor, and injecting the PV system's energy into the electrical power system, are discussed. Later, a multilevel NPC inverter-based SAPF was developed to address power quality concerns by utilizing the Synchronous Reference Frame Theory (SRF) and Adaptive Neuro Fuzzy Inference System (ANFIS) algorithm. The reference current required for the compensation is calculated using the SRF theory, and the ANFIS algorithm is implemented to generate a smooth DC link voltage. In addition, a Hysteresis Current Controller (HCC) is employed to provide the required switching pulses for the neutral point clamped voltage source inverter, thereby reducing the THD produced by Nonlinear (NL) loads, which can be balanced or unbalanced. The SAPF efficiently utilizes the active power generated by PV arrays. It employs an Enhanced Incremental Conductance (EINC) based MPPT controller to maximize power extraction of PV arrays into the power grid. Additionally, it supports load-reactive power demand and improves grid power quality by eliminating harmonics. The performance of the proposed system is validated using both hardware and MATLAB simulation. From the experimental results, it is observed that the proposed system exhibits better performance by minimizing the harmonics and maintaining the DC link voltage constant under balanced and unbalanced NL load conditions.

INDEX TERMS Neutral point clamped converter, FPGA, power quality, photovoltaic system, ANFIS, shunt active power filter.

I. INTRODUCTION

The availability of current centralized electric energy generation is inadequate to meet the increasing demand for electricity. Energy production is a crucial area of study that has a significant impact on global economic progress. It encompasses a wide range of technologies and approaches and is a topic of great interest and concern for governments, businesses, and individuals alike [1], [2]. The field demands innovative solutions and continuous research to meet the challenge of generating energy safely, efficiently, and sustainably. Numerous countries and private industries allocate substantial funds to fulfill the growing demand for electricity, predominantly through the utilization of customary sources that use coal, diesel turbines, or gas turbines. However, due to their exorbitant pricing, inefficiency, and detrimental influence on the environment, the adoption of these energy sources is gradually restricted. It is widely acknowledged that extensive industrial production results in a surge of carbon dioxide emissions, global warming, and ecological harm.

The associate editor coordinating the review of this manuscript and approving it for publication was Jorge Esteban Rodas Benítez.

This phenomenon leads to a depletion of natural resources, which poses a threat to future energy generation. Hence, various governments have resorted to utilizing renewable energy technologies or green energy technologies, which are naturally replenishing. The aforementioned energy sources are deemed as non-contributory to the phenomenon of global warming and are regarded as environmentally favorable [3], [4], [5], [6].

Among the various renewable energy technologies, the potential of photovoltaic (PV) system-based distributed energy resources is a promising renewable energy technology. PV systems are highly reliable, efficient, and capable of generating unlimited quantities of energy in most regions around the world [7]. They have proven to be particularly useful in providing a continuous energy supply to isolated villages and regions. They also help non-oil-producing countries decrease the expenses associated with importing energy and production, leading to lower consumption bills. Additionally, PV systems exhibit environmental friendliness by virtue of their lack of pollutant emissions, hence prompting researchers to enhance the production methods of superior PV systems. Advancements in technology have the potential to make PV systems a major contributor towards fulfilling the world's energy requirements while simultaneously reducing environmental harm [8].

An essential challenge in integrating photovoltaic systems with the electrical network is the issue of power quality, resulting from the increasing presence of non-linear loads linked with the electrical network. These loads are contributing to several issues, such as current harmonics, voltage harmonics, power factor, reactive power, and a growing need for active power [9], [10], [11]. In order to address these problems, grid-connected PV systems use components such as a PV panel, power converter (DC-DC), DC-link energy storage, a three-level SAPF, a grid-connected filter, and the controller circuit. Integrating SAPF into the electric power producing system leads to substantial enhancement in power and current quality, and the requirement for regular equipment maintenance is avoided, leading to cost reduction. In recent times, the energy and power sector has witnessed a significant advancement, leading to the introduction of a multitude of NL loads. However, this has considerably affected the quality of power. A number of approaches have been developed to reduce to mitigate the impact of such NL loads on power quality. These techniques include passive filters, series, parallel, and hybrid active power filters [12], [13].

In high-power industrial applications, AC and DC drives are commonly employed, but they have been found to produce undesired harmonics. Due to the reverse rating limits of the switches employed, two-level active power filters cannot be employed to mitigate the harmonics generated by high-power NLs. A major challenge in integrating solar panel power into the grid is minimizing the THD, which is a crucial concern when supplying electricity to the grid through solar panels. The SAPF is an effective method for removing harmonics and balancing reactive power, implemented using two-level inverters [14].

However, this approach is typically used for medium power range NLs, as the higher switching frequency of the two-level inverter might cause issues while controlling enhanced NLs power. This is because static switches in inverters exhibit significant switch currents, which may require several inverter switches to minimize switched currents at a certain power level, leading to an elevation in switch voltage [15]. In order to address this limitation, a viable solution is to link the photovoltaic system with the electrical system through a multilevel inverter. It has numerous benefits, including decreased harmonic rates, reduced switching losses, and enhanced electromagnetic compatibility [16], [17], [18], [19]. As explained in [20], the use of NPC-based inverter design is extensive in architecture and is widely utilized in high and medium-power applications to compensate for reactive power and eliminate harmonics in power lines. These inverters provide numerous positive aspects, including decreasing the amount of output voltage harmonics, an improvement in source current harmonics, a reduction in voltage stress on power semiconductors, a reduction in switching losses, and the possibility of overcoming challenges that have been linked to SAPF-based two-level inverters. The effectiveness of SAPF employing three-level NPC inverters is influenced by specific techniques for producing reference current harmonics with excellent tracking quality, dynamic DC bus voltage management, dynamic and stable injected currents, and robust and accurate creation of gate-switching pulses. Several studies have looked into how the frequency at which switches are changed and the pulses used to switch gates impact the efficacy of three-level NPC inverters. In the process of compensation, the reference current is extracted while the DC bus voltage is regulated. The SRF theory is frequently employed to control the reference current generation in SAPF. The Instantaneous Reactive Power Theory (IRPT) is also used, but it is suboptimal for dynamic load fluctuations, has a slow response time, and demands significant processing power. The literature favors the use of SRF theory to describe PV-based distributed static compensator, which enhances power quality [21].

The management of the capacitor voltage on the inverter DC side is a crucial component that determines the workings of any Active Power Filter (APF). Employing Proportional Integral (PI) controllers for regulating the voltage on the inverter DC side has been a traditional approach. However, the use of PI controllers requires an accurate model, which is difficult to obtain for a system with considerable nonlinearity. Therefore, a variety of intelligent controllers have been explored in the literature that do not require precise models. These controllers include Particle Swarm Optimization (PSO)-based controllers, Genetic Algorithm (GA), Fuzzy Logic Control (FLC), Artificial Neural Network (ANN)-based controls, and others. Benchouia et al. designed an FLC that adjusts to voltage error fluctuations, which was validated experimentally using DSPACE-1104 [22].

Mahajan et al. [23] developed a simulation and constructed an ANN current controller-based multilayer harmonic filter. This filter includes an FLC to regulate the voltage on the DC-link side of the inverter [24]. However, one of FLC's disadvantages is that it must manage various fuzzy sets and rules in relation to load fluctuations. In order to overcome these limitations, an Adaptive Neuro-Fuzzy Inference System controller is implemented to regulate for inverter DC side capacitor voltage regulation. This controller combines the benefits of FLC and ANN controllers with the ability to adjust to changes in the system [25], [26]. A basic three-level hysteresis current controller (HCC) is utilized to create triggering pulses for the Multi-Level Inverter (MLI) employed in parallel APF. The system's operation is validated using MATLAB and proto-type hardware. The proposed approach aims to enhance system stability by effectively managing load changes, in contrast to traditional linear control strategies that rely on a PI controller.

The principal contributions of this work include:

1) The Enhanced Incremental Conductance (EINC) based MPPT controller accurately tracks and attains the maximum power point from the PV module.
2) The propose an EINC-based PV interconnection through a three-level NPC voltage source inverter SAPF to supply active power from the PV system and support load reactive power demand.
3) An ANFIS controller to maintain constant DC-link capacitor voltage and optimize PV-SAPF performances in varying load scenarios. On the other hand, the HCC is employed to generate the gating signals more effectively.
4) The performance of both the ANFIS controller and the conventional PI controller in SAPF will be analyzed and compared to validate the ability of the ANFIS controller.
5) The ANFIS controller, combining SRF theory and HCC, effectively improves power quality by mitigating harmonics and reducing source current THD, meeting IEEE 519 standards, thereby enhancing overall system performance.

The remaining portion of the article structure is as follows: Section II reviews the Modelling and description of systems of PV-based three-level NPC inverters with the SAPF system given. In the same section, it discussed the Photovoltaic array used in the system, extraction of harmonics utilizing SRF theory, and an ANFIS controller implemented for controlling DC link voltage. In section III, Simulation Results and discussion under balanced/unbalanced under NL load conditions. PV based three level NPC inverter with SAPF is tested under varied loading conditions of hardware results and presented in Section IV. Finally, in Section V, the paper is the conclusion of the research work.

II. MODELLING AND DESCRIPTION OF SYSTEMS

The PV-based multilevel inverter-based SAPF system proposed for this study is shown in Figure 1. This system

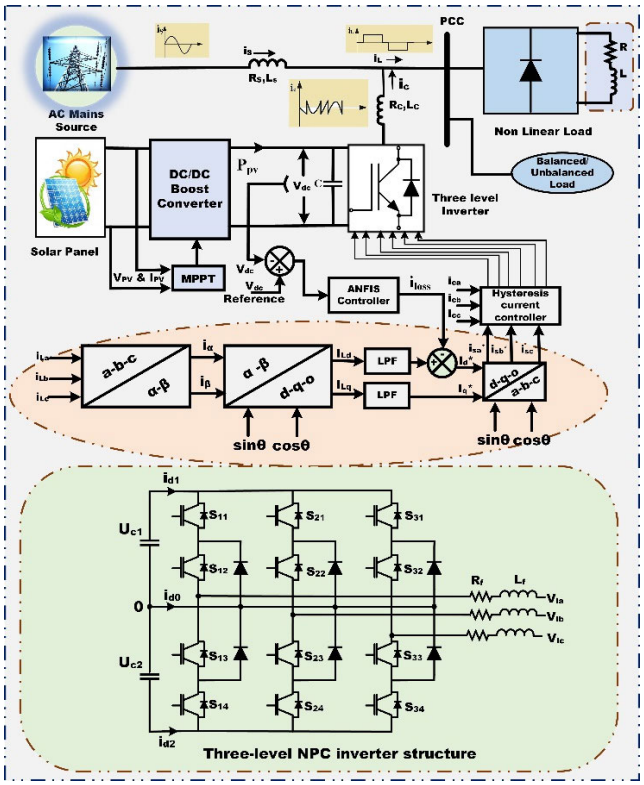

FIGURE 1. Power circuit of diagram of integrated three-level NPC inverter-based PV-SAPF.

incorporates a PV module, a DC-DC step up converter, a multilevel inverter-based SAPF, and loads that are connected together. A three-phase, three-level SAPF DC-link obtains the output of a DC-DC step up converter and adjusts its duty cycle accordingly to achieve MPP under all operating conditions. Interfacing inductors are utilized to connect the SAPF network at the PCC to smooth grid currents. A three-phase uncontrolled rectifier is coupled to an inductive load in order to get a load with non-linear behaviour. A multilevel inverter-based SAPF is employed, with switching pulses provided by a three-level HCC. This system has the ability to enhance power factor, minimize harmonic distortion, support reactive power demand as well as deliver active power from a PV system to a load or distribution system simultaneously. Below are brief descriptions of the other components.

The three-level NPC inverters include two capacitors (U_{C1}, U_{C2}) linked to the DC bus in order to create a link with the reference point (o) and acquire a medium voltage, in addition to the anti-parallel arrangement of the transistors and diodes. Each arm of the inverter contains four bidirectional switches. The differential equations below can be used to explain the interaction, with SAPF being regarded as the source of current from the PCC [11], [27].

$$\begin{cases} L_f \dfrac{di_{fd}}{dt} = -R_f i_{fd} - L_f \omega i_{fq} + V_{sd} - V_{fd} \\ L_f \dfrac{di_{fq}}{dt} = -R_f i_{fq} - L_f \omega i_{fd} + V_{sq} - V_{fq} \\ C \dfrac{di_{fq}}{dt} = i_{fd} V_{fd} + i_{fq} V_{fq} \end{cases} \tag{1}$$

TABLE 1. Three level inverter switching state.

Voltage	States	Current State of Switching Devices (M=1,2,3) (0=OFF,1=ON)			
		S_{M1}	S_{M2}	S_{M3}	S_{M4}
$V_{dc}/2$	P	1	1	0	0
0	O	0	1	1	0
$-V_{dc}/2$	N	0	0	1	1

The source current in the PCC point is composed of two components, filter currents (I_F) and load currents (I_L), according to Kirchhoff's current law, which can be expressed as $I_S = I_F + I_L$. In this instance, the parallel SAPF acts like a current generator that limits the harmonics in the load current, which consists of a combination of reactive and active components. In this particular scenario, the parallel SAPF functions as a current generator to mitigate the presence of harmonics in the load current, which consists of both active and reactive components. The system is designed to inject harmonic currents into the electrical network with the same amplitude as those absorbed by the load but in the opposite phase.

In the switching S_{MX}, the modes of operation are represented by the numbers '−1', '0', and '1'. These values indicate that the corresponding arm is linked to the positive, negative, or neutral points of the DC-link capacitor, respectively. M = a, b, c, and X = 1, 2, 3, 4 are the values that are shown in Table. 1. lists the relationships between operations and the associated output voltages.

A. PHOTOVOLTAIC ARRAY

As seen in Figure 2, the PV cell's non-linear V-I characteristics vary with temperature and solar radiation. As a result, monitoring the array's maximum power output is crucial. The MPPT controller regulates the boost converter operation by taking into account several inputs, including PV array parameters (V_{oc}, I_{sc}), solar radiation, temperature, and output parameters such as DC link voltage. When the MPP fluctuates and when irradiance conditions rapidly change, conventional incremental and conductance MPPT techniques perform less well. For the purpose of addressing these challenges, an enhanced INC MPPT has been developed. This technique controls the duty cycle of a step-up converter to efficiently extract maximum power. The details of this development are extensively addressed in the reference article [28], [29], [30] discussed in detail. The EINC MPPT technique is shown in Figure 3. The DC-DC step-up converter receives the output from the PV array. The SAPF's DC bus is where the boost converter's output is attached. The PV array produces an output voltage of 305.6 V, which is increased to 750 V using a step-up converter. Equations. (2), (3) provide the PV module's diode and load currents, as shown below.

$$I_d = I_{sat}\left(e^{\frac{QV_{oc}}{AKT}} - 1\right) \tag{2}$$

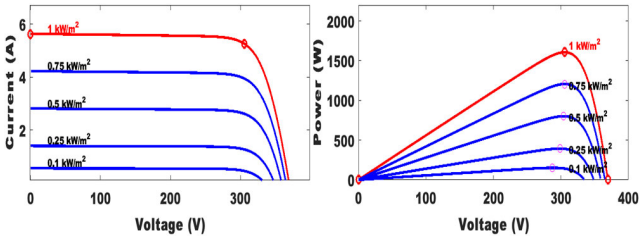

FIGURE 2. Trina solar TM-200DA01A; PV curve for solar PV array voltage vs. and power and voltage vs. current characteristics.

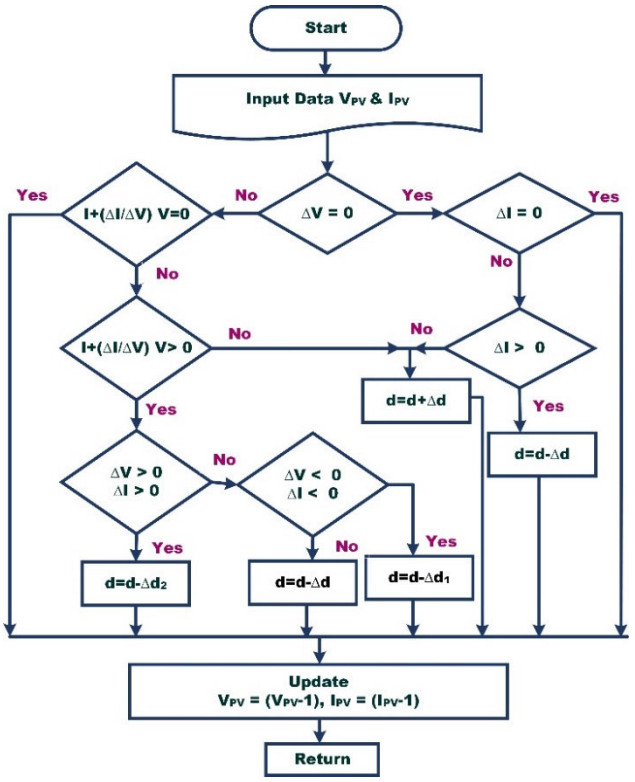

FIGURE 3. EINC MPPT technique.

$$I = I_L - I_{sat}\left(e^{\frac{QV_{oc}}{AKT}} - 1\right) - \frac{V_{oc}}{R_{sh}} \tag{3}$$

When I = 0, the maximum PV voltage is attained during open circuit conditions and is provided by Equation (4)

$$V_{oc} = \frac{AKT}{Q} log_n\left(\frac{I_L}{I_{sat}} + 1\right) \tag{4}$$

The system is implemented using an Array type of Trina Solar TSM-200DA01A solar PV module for sun power.

In Figure 4, a comparison is presented between the EINC and INC MPPT techniques in extracting maximum power output from photovoltaic systems while taking into account variations in irradiance and temperature. The EINC algorithm outperforms the conventional INC algorithm, particularly in terms of dynamic response. The conventional method is less effective than the new approach in situations where solar irradiation is decreasing and even less efficient when radiation

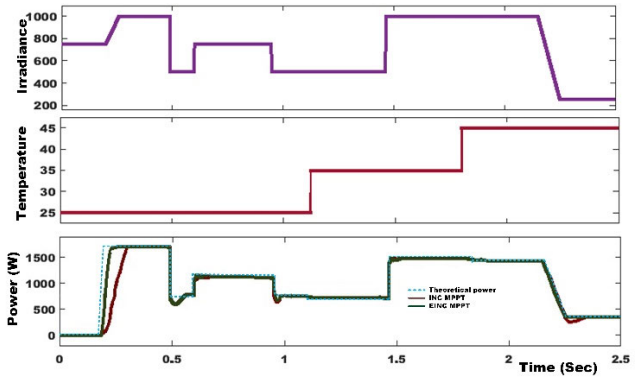

FIGURE 4. Characteristics of MPPT techniques and their effectiveness in extracting maximum PV output power under changing irradiance and temperature conditions.

is increasing. Based on these results, the proposed approach ensures superior dynamic response when solar irradiation changes rapidly in either direction. Regarding temperature, the PV output power (P_{PV}) waveforms are inversely proportional to changes in temperature, and P_{PV} power is only minimally affected.

B. SRF THEORY-ANFIS CONTROLLER

Several methods are available for providing harmonic compensation, including the IRPT, SRF, and the Direct Current (DC) link voltage regulation approach implemented in the SAPF. However, the SRF theory has been selected for this study due to its faster transient response. The system design presented below depends on the SRF theory.

Figure 1 illustrates the block diagram for the control method based on SRF. The feedback signals obtained from the load currents (i_{La}, i_{Lb}, and i_{Lc}) are transformed to Park transformation for obtaining d-q-0 coordinates as in Equation (5).

$$\begin{bmatrix} i_{Ld} \\ i_{Lq} \\ i_{L0} \end{bmatrix} = \frac{2}{3} \begin{bmatrix} \cos\theta & -\sin\theta & \frac{1}{2} \\ \cos\left(\theta-\frac{2\pi}{3}\right) & -\sin\left(\theta-\frac{2\pi}{3}\right) & \frac{1}{2} \\ \cos\left(\theta+\frac{2\pi}{3}\right) & \sin\left(\theta+\frac{2\pi}{3}\right) & \frac{1}{2} \end{bmatrix} \begin{bmatrix} i_{La} \\ i_{Lb} \\ i_{Lc} \end{bmatrix} \tag{5}$$

Phase locked loops (PLLs) are used to extract phase information from signals, synchronizing them with points of common coupling. These transformations generate pure sine and cosine waves synchronized to grid voltage. A low pass filter is employed to filter components like i_d and i_q, which are DC components of the d-axis and q-axis currents. The fundamental and harmonic segments of the i_d and i_q are illustrated in Equations (6, 7).

$$i_{Ld} = i_{dDC} + i_{dAC} \tag{6}$$
$$i_{Lq} = i_{qDC} + i_{qAC} \tag{7}$$

These two-phase reference source i_d, i_q currents are then transformed into three-phase references compensating i^*_{sa}, i^*_{sb}, and i^*_{sc} currents using the abc transformation in Equations. (8), (9), and (10).

$$i^*_{sa} = \frac{\sqrt{2}}{3}\left[i_{d,AC}\cos(\omega t) - i_q\sin(\omega t)\right] \tag{8}$$
$$i^*_{sb} = \frac{\sqrt{2}}{3}\left[i_{d,AC}\cos(\omega t - \frac{2\pi}{3}) - i_q\sin(\omega t - \frac{2\pi}{3})\right] \tag{9}$$
$$i^*_{sc} = \frac{\sqrt{2}}{3}\left[i_{d,AC}\cos(\omega t + \frac{2\pi}{3}) - i_q\sin(\omega t + \frac{2\pi}{3})\right] \tag{10}$$

The ANFIS controller maintains a stable DC-link voltage by producing active current by comparing reference DC-link voltage ($V_{dc\,ref}$) and actual DC-link capacitor voltage ($V_{dc\,Act}$). The reference filter current is produced by comparing the actual load current with the reference source current. The resulting error is then sent to the hysteresis current controller, which generates the necessary pulses to turn the SAPF ON or OFF.

C. ANFIS BASED DC-LINK CAPACITOR VOLTAGE CONTROL ALGORITHM

ANFIS has proven to be a very intelligent system, capable of handling the uncertainty of the ANN and Sugeno-type Fuzzy Inference System (FIS). ANFIS generates a fuzzy inference system depending on the provided available input and output by optimizing membership functions using the ANN's learning capabilities. The neural network block receives the computed data and trains the data using the backpropagation (BP) learning technique. The developed data set is inputted through the fuzzy interference system, which generates the fuzzy control rules. The article evaluated the system with fuzzy MF rules such as 3*3, 5*5, and 7*7; nevertheless, the THD and settling time were the same for each rule. Because they require less computing burden, 3*3 rules are selected in this case to enhance power quality. Triangular MF was used in this article's fuzzification process to improve ANFIS performance. The rule base of the ANFIS controller is made up of two fuzzy if-then rules of the first order Sugeno type. The controller is equipped with two inputs and a single output. After the neural network produces its output, a defuzzifier is used to convert linguistic variables into crisp variables. The VSI is then controlled by the SAPF controller using the crisp variable. Sugeno Takagi Figure 5 illustrates the five-layered structure of FIS, which is implemented here utilizing ANFIS. The first hidden layer fuzzifies the input variable, and the second hidden layer receives T-standard operators to calculate the rule. Rule strengths are standardized by the third and fourth hidden layers, which also establish the rule's subsequent parameters. Summing together all of the incoming signals allows the fifth layer to compute all of the input. Table. 2 details the functions of each layer, highlighting that the ANFIS controller layers fulfill specific responsibilities.

Training of ANFIS Controller to Control DC-Link Capacitor Voltage:

Initially, the data for training the ANFIS controller is generated from the PI controller by considering $K_p = 0.18$ and

TABLE 2. Responsibilities carried out by the ANFIS controller layer.

Name of the Layer		The Layer Outputs
Layer-1:	Fuzzification Layer	It employs the Sugeno fuzzy rule to translate input physical variables into linguistic variables, demonstrating the adaptive nature of each node (U and V). The work uses error voltage (Er) and change in error voltage (ΔEr) as input variables, denoted by e_1 and e2. The result of this layer, as provided by $L_i^1 = \mu_{V1} E_r$ (11) $L_j^1 = \mu_{V2} \nabla E_r$ (12)
Layer-2:	Product Layer	calculates the degree of applied fuzzy rule by multiplying inputs at each node with a fixed type nature. $L_i^2 = d_i = (\mu_{Ui} E_r) \times (\mu_{Vi} \Delta E_r)$ (13)
Layer-3:	Normalized layer	In this layer's {labeled (N)} nodes are all the fixed nature types. This layer is employed to complete the IF portion of the fuzzy rule and normalize the input degree. The result of this layer is provided by $L_i^3 = \bar{d}_i = \frac{d_i}{\sum_{k=1}^{2} d_k}$ (14)
Layer-4:	Defuzzifier Layer	The fourth layer of the ANFIS architecture features square-shaped, adaptable nodes, each producing MF output based on learning principles. $L_i^4 = d_2 \times f_i = \left(\bar{d}_i \times (x_i \times E_r + y_i \times \Delta E_r + z_i)\right)$ (15)
Layer-5:	Output Layer	This layer, consisting of a fixed nature type exit node labeled by a summation sign, provides the final part of the fuzzy rule. $L_i^5 = \sum_i (\bar{d}_i \times f_j) = \frac{\sum_i (d_i \times f_i)}{\sum_i^d}$ (16)
Here, the nodes i and j employ the input variables Er and ΔEr.		

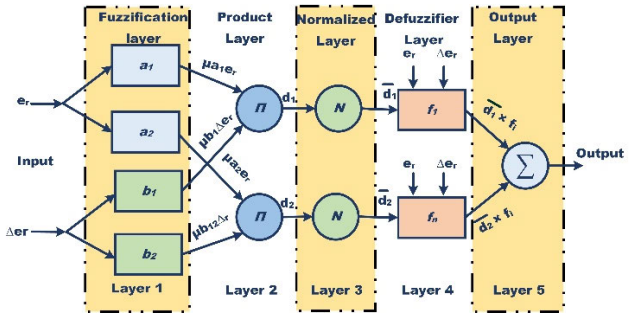

FIGURE 5. ANFIS controller structure.

$K_i = 0.48$. The PI controller is simulated in a MATLAB workspace under different load conditions to generate training data when coupled to a SAPF controller. In the second stage, an ANFIS model is developed using MFs, Sugeno fuzzy rules, one output variable, and two input variables (error and change in error). An ANFIS model with a 3*3 MF is created with a triangular function. In the third stage, the ANFIS model-based learning process involves training the backpropagation algorithm with 55 epochs in order to precisely determine the training error. The training process is continued until the error between the target data and the ANFIS output is reduced to its minimum. The ANFIS fuzzified variable is finally converted to a crisp variable, which the SAPF controller subsequently utilizes to reduce THD and enhance PQ. The flow chart for the ANFIS algorithm-based SAPF tuning based on PQ improvement is shown in Figure 6(a). The epochs and training errors of the ANFIS controller employed by SAPF are displayed in Figure 6(b), and the estimated ANFIS model's RMSE has been obtained to be 0.065982.

III. SIMULATION RESULTS AND DISCUSSION

In the MATLAB environment, a proposed simulation model of PV-SAPF is built on various load conditions. The model consists of a PV panel, NL loads, a control unit, a coupling inductance, a three-level inverter, and a three-phase AC source. Table.3 shows the design and the parameters of the simulation. The investigation shows the operation of a combined PV-SAPF system by examining its effects on balanced, unbalanced, and NL loads.

A. CONTROL PERFORMANCE DURING BALANCED AND NLS CONDITIONS

A balanced and NLs is connected to the PCC of the distribution system. Figure 7. depicts grid voltage, grid voltage

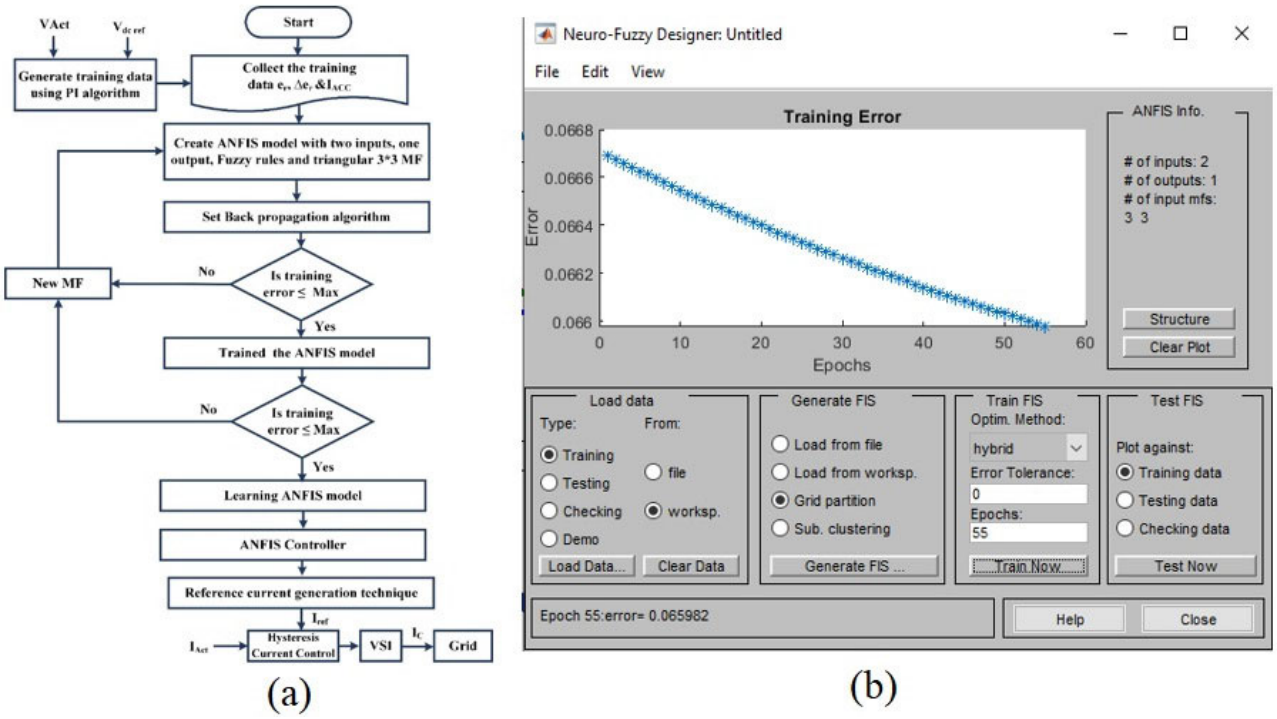

FIGURE 6. (a) Flowchart depicting the functioning SAPF using ANFIS algorithm (b) epochs and training errors of ANFIS controller.

TABLE 3. Design the parameters of the simulation.

Components	Parameter	Value
Grid	Source voltage (Phase voltage)	230 V,50 Hz
PV Boost converter	PV Module	P_{PV}=200.9W; I_{sc}=5.62 A; V_{oc}=46.2 V; V_m=38.2 V; I_m=5.26 V.
	Boost Converter	L=68.5 mH; C_{in}= 100 µF; V_{pv}=V_{in}=305.6 V; V_{dc}=750 V
Filter	Inductance	5 mH
DC-link voltage	Capacitor	2200µF
Nonlinear load	Resistor and inductor	R=81Ω and L=12mH
Balanced load	Resistive load	R_1= R_2= R_3=110Ω
	Inductive load	160mH
Unbalanced load	Resistive load	R_1=110Ω; R_2=75Ω; R_3=50Ω
Note: V_m , I_m and P_{PV} are maximum power voltage, current and power of PV; Voc and Isc are open-circuit voltage and Short-circuit current.		

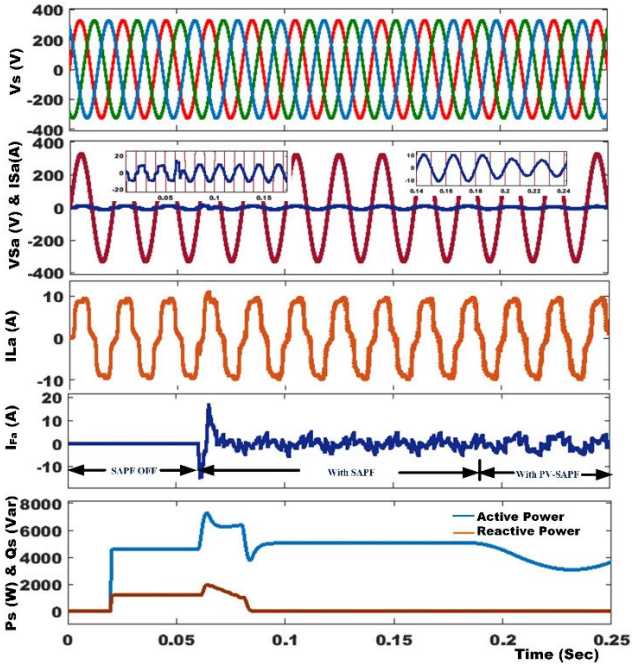

FIGURE 7. System performance of system (a) grid voltage (b) grid voltage and current (c) Load current (d) Filter current (f) Source active and reactive power waveforms.

and current, load current, filter current, and active and reactive power. When the system operates without a SAPF, the signatures of both the source and load currents are similar. However, once the SAPF is enabled at t=0:06s, it injects a harmonic current in the opposite direction to reduce the presence of harmonics in the source current, irrespective of the load's characteristics. The average power flow at the point of common coupling (PCC) is measured both with and without the functioning of the grid controller. The SAPF mode starts injecting power at t=0:06s, which eliminates

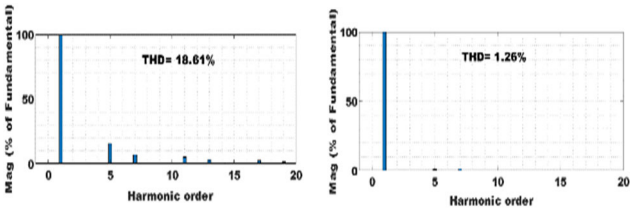

FIGURE 8. Harmonic spectrum: before and after compensation of phase A source current.

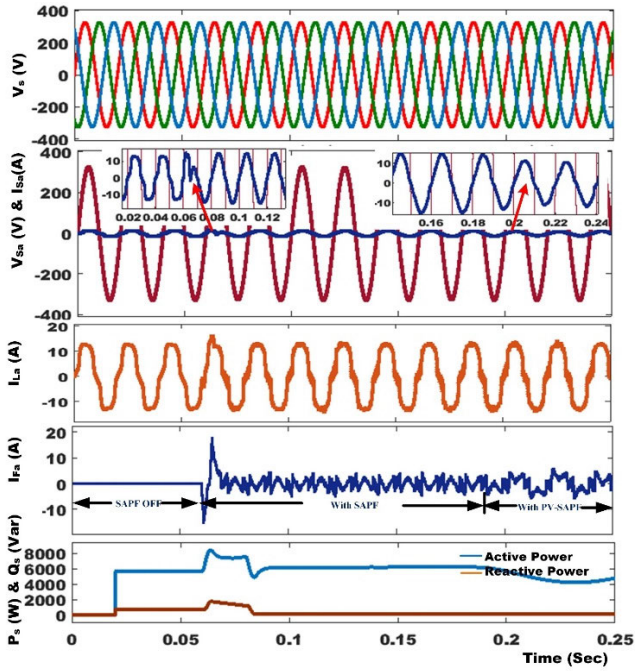

FIGURE 9. System performance of system (a) grid voltage (b) grid voltage and current (c) Load current (d) Filter current (f) Source active and reactive power waveforms.

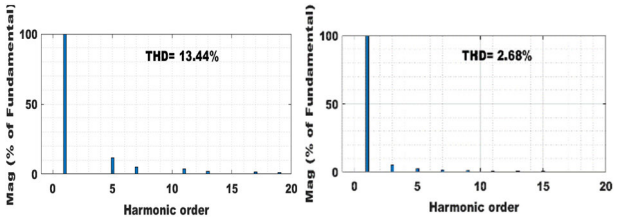

FIGURE 10. Harmonic spectrum: before and after compensation of phase A source current.

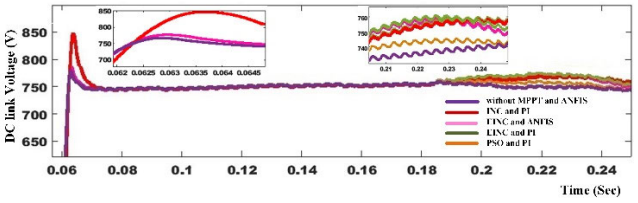

FIGURE 11. DC-link voltage transient response of different control algorithms.

TABLE 4. Performance of DC link voltage in SAPF with different control algorithms.

Case	Before compensation	After Compensation	
		PI controller with SAPF	ANFIS controller with SAPF
Maximum overshoot(volt)	--	846	768
Transient settling time(sec)	--	0.075	0.064
%THD	26.16	3.28	1.36

reactive power from the source. The addressed source currents are synchronized with the source voltage to ensure a power factor of unity. At t=0:18s, Photovoltaic (PV) is combined with SAPF real power fed into the system's load to mitigate harmonics and decrease reactive power demand. The harmonic spectrums of before and after compensation of source currents are shown in Figures.8, respectively. The THD of the source current has been minimized to 1.26% from 18.61%.

B. CONTROL PERFORMANCE DURING UNBALANCED AND NLS CONDITIONS

An unbalanced and NLs is connected to the PCC of the distribution system. Figure 9 depicts grid voltage, grid voltage and current, load current, filter current, and active and reactive power. Source current THD has been minimized from 13.44% to 2.68%, as shown in the Figures.10, respectively, in the harmonic spectrum. The DC-link voltage control approaches of the integrated system with step up converter are depicted in Figure 11. i) ANFIS in PV-SAPF and without MPPT; ii) PI in SAPF and INC for MPPT; (iii) ANFIS in PV-SAPF and EINC for MPPT; (iv) PI in PV-SAPF and EINC for MPPT; V) PI in PV-SAPF and PSO for MPPT. Table. 4 displays the performance of the DC link voltage in SAPF using various control techniques. It shows that the EINC MPPT with the ANFIS-based PV-SAPF method settles faster than the PI-based method, providing a better transient response with lower overshoots and DC-link voltage changes.

IV. HARDWARE RESULTS AND DISCUSSION

Appropriate control circuits, DC bus capacitors, source and filter inductors, voltage source inverter, and other components need to be carefully designed and selected in order to construct a SAPF for harmonic reduction and reactive power compensation. The selection of processor speed, interface circuits, and sensor components affects the SAPF's performance. The SAPF system design parameters used the experimental validation shown in the Table. 5.

The Vivado 2023.2- Artix-7 DSP FPGA controller executes a synchronous reference frame-based algorithm

TABLE 5. Design parameters of the experimental validation.

Components	Parameter	Value
Grid	Source voltage (Phase voltage)	230 V,50 Hz
Filter	Inductance	5 mH
DC-link voltage	Capacitor	2200μF
Nonlinear load	Resistor and inductor	R=81Ω and L=12mH
Load	Resistive load	0.5KW to 1.5KW
	Inductive load	80mH to 160mH
Chromo PV simulator (model-62050H-600S)	Open circuit voltage, V_{OC} Short circuit current, I_{SC}	600V 6A

contributing to the SAPF system. The Hall Effect current sensor (HE100T01) and voltage sensor (IC 7840) are used to sense each phase's load voltages and currents, respectively. In addition, these transducers are employed to achieve isolation between the control and power circuits. Using a signal conditioning circuit, the signals from the sensors are transformed into a range of 0 to 5 V to be properly utilized with the FPGA's analogue channels. These circuits' outputs connect to 12-bit bipolar Analog to Digital (A/D) converters (IC AD7366), and IO lines deliver the digital data to the FPGA processor. The Programme is utilized to construct the switching signals for IGBTs, developed from the synchronous reference theory. The minimum current needed for the drive function must be maintained by the driver circuit (TLP 250 IC). Four driver circuits are required to create switching pulses for the IGBT modules (SKM100GB12T4) SEMITRANS 2 fast IGBT Module uses the three-level diode-clamped inverter, which is utilized to realize SAPF. The SAPF prototype model is demonstrated in Figure 12.

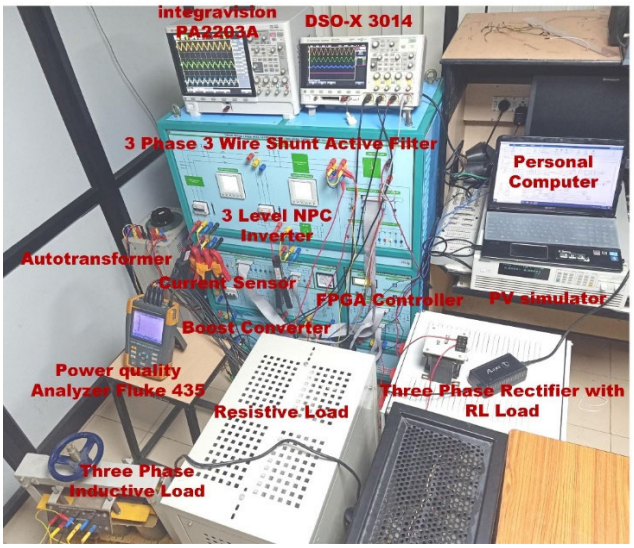

FIGURE 12. The SAPF was implemented using the SRF technique on the laboratory's experimental setup.

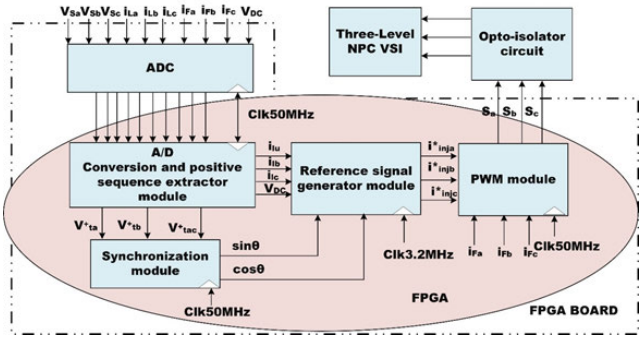

FIGURE 13. Control strategy development implemented on FPGA.

A. FPGA IMPLEMENTATION OF SRF THEORY

The proposed research utilizes FPGA to implement the SRF control strategy of SAPF in a modular manner, continuously monitoring control performance. Specifically, an Artix-7 DSP FPGA has been used to fully develop the controller. Reference signal generation, synchronization, A/D conversion and positive sequence extractor module, and switching pulses (PWM) module are the four modules needed to accomplish all of the controller operations, according to the overall schematic displayed in Figure. 13 illustrating the modular design of the control strategies.

1) ANALOG TO THE DIGITAL CONVERSION MODULE

This module performs the A/D conversions by obtaining sequential bits via an external ADC channel. The system handles the synchronization between the external ADC and the FPGA and then transfers the resulting 12-bit bipolar analog-to-digital converters (IC AD7366) to the subsequent module. This module executes ten conversions, including 3φ supply voltage (V_{sabc}), load current (I_{Labc}, injection filter current (I_{Fabc}), and DC link voltage (V_{dc}). Moreover, this module implements the technique outlined in reference to separate the 3φ positive sequence component of PCC voltage from the 3φ PCC voltage.

2) SYNCHRONIZATION MODULE

This module obtains a 3φ positive sequence PCC voltage, and it uses the input voltages to determine the synchronizing angle. After applying Equation (5) to transform the 3φ voltages (V_{sa}, V_{sb}, and V_{sc}) into 2φ voltages (V_α and V_β), the grid synchronizing angles sin θ and cos θ were determined as follows:

$$\sin\theta = \frac{V_\alpha}{\sqrt{V_\alpha^2+V_\beta^2}}; \cos\theta = \frac{V_\beta}{\sqrt{V_\alpha^2+V_\beta^2}} \tag{17}$$

3) REFERENCE SIGNAL GENERATION MODULE

The SAPF reference signal is computed in this module based on the inputs of grid synchronization angles and load current

(I_{La}, I_{Lb}, and I_{Lc}). This module includes the PI controller, abc–dq block, LPF, and dq–abc block. The abc-dq block outputs id and iq, and id is then processed through a digital LPF to produce the dc component. Moreover, a discrete PI controller that employs several registers to hold the prior values processes the error that results from comparing the actual DC voltage with its reference. The reference d-axis current is obtained by combining the oscillating portion of the i_d with the ANFIS algorithm, which employs the PI ($K_p = 0.1$, $K_i = 0.01$) method by collecting training data. The ANFIS model is trained using error and its change as input, with the corrected active component current as the output variable. The ANFIS controller's output represents the power loss (I_{loss}). The reference compensator current $i^*_{c(abc)}$ for SAPF is then obtained by translating the reference d-axis current l^*_d and i_{lq} to an a-b-c frame utilizing reverse Park's and Clarke's transformations.

4) PWM MODULE HCC MODULE

The most common current controller is the hysteresis current controller because of its enhanced dynamic performance and simple operation. An MLI-based voltage source inverter uses multilevel hysteresis currents with inner and outside hysteresis bands. The hysteresis band's interior consists of a lower negative value (y_{neg}) and an upper positive value (y_{pos}). The voltages V_{ao}, V_{bo}, and V_{co} generate two positive phase voltage levels, 0 and $V_{dc}/2$. To reduce compensated current, select $V_{dc}/2$. Voltage level 0 is utilized to amplify the compensated current. Additionally, during the negative half-cycle of phase voltage, two voltage levels are formed on the AC side voltage of the inverter. During the negative half-cycle of the phase voltage, the inverter generates voltage levels of $-V_{dc}/2$ and 0 on the AC side. A voltage level of $-V_{dc}/2$ is generated in order to amplify the corrected current. Conversely, a high level of 0 is produced to reduce the compensated current in the negative phase voltage. As gating signals for the switching S_{A1} and S_{A2} of the H-bridge connected in phase A, the output Q_1 and its inverted output $\bar{Q}_1$ are provided. The outer hysteresis band, similarly, has a lower negative value and an upper positive value. The SR flip-flop 1 receives the current error that is made by subtracting the actual current from the reference current. It then compares these outputs to the positive and negative inner hysteresis band limits. The gating pulses for the other two switches, S_{A3} and S_{A4}, are generated by comparing this current error with the outer hysteresis band limits, positive and negative, and using another SR flip-flop 2. In order to generate switching signals, the following process of logic has been utilized.

B. PERFORMANCE OF SAPF UNDER NL LOADS IN THE STEADY STATE ANALYSIS

Three-phase SAPF's compensating characteristics are demonstrated experimentally by connecting it to a diode bridge rectifier with RL load. Figure 14 depicts the non-sinusoidal nature of the load current, encompassing the

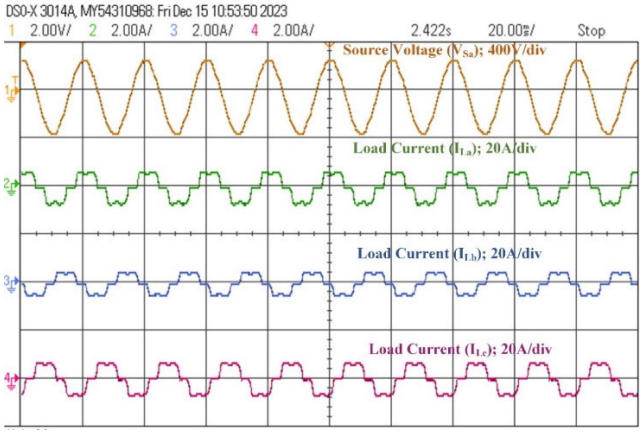

FIGURE 14. Phase A voltage with RL load with diode rectifier three-phase load currents: (a) A-phase load current (amperes); (b) B-phase load current (amperes); (c) C-phase load current (amperes).

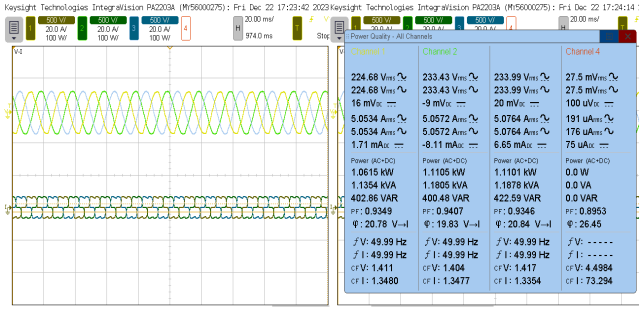

FIGURE 15. Steady-state response of before compensation of three phase source voltage and current, and power quality analysis of (real, reactive and apparent power, power factor).

fundamental component and the significant harmonic component at the point of common coupling.

Fig. 15 shows the steady-state behavior of three-phase source voltage and current, examining power quality metrics, real, reactive, and apparent power, and power factor characteristics. DSO-X3014A and Keysight technologies integravision PA2203A high-performance power analyzer were used to record these signals. The source currents measured total harmonic distortion (THD) is 26.0%, much higher than the harmonic current distortion limits specified by IEEE 519. The requirement of opposite harmonic current produced through the FPGA is depicted in Figure 16. This current is observed to be changing rapidly according to the harmonic signals. The SAPF output is directly coupled to the PCC, utilizing the 5mH coupling reactance. As a result, the three-level NPC-based SAPF enables reactive power compensation, minimizes harmonics in source current for NL loads, and the source side maintains unity power factor, as shown in Figure 17.

Figure. 18 demonstrates the switching performances of the SAPF. The SAPF system feeds the requirement of reactive power of NL loads and harmonics within four microseconds at the PCC, causing the supply current to become

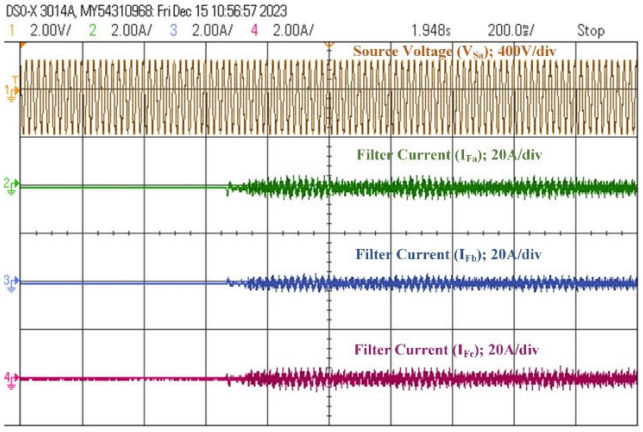

FIGURE 16. Phase A voltage with the compensation of three phase filter currents in SAPF.

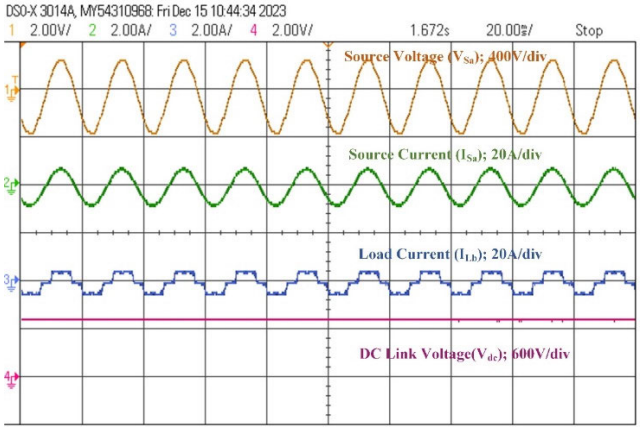

FIGURE 17. SAPF steady-state response (phase-A).

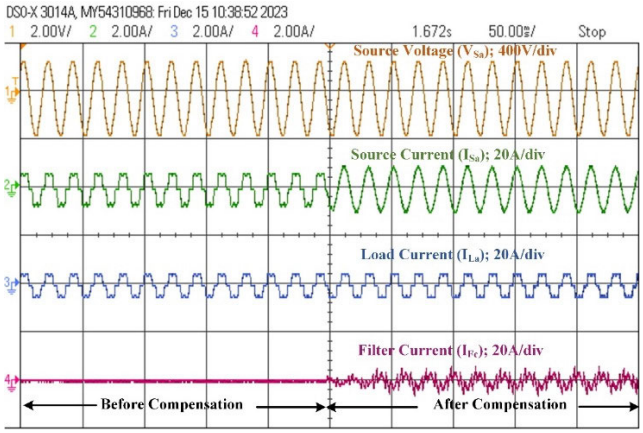

FIGURE 18. SAPF steady-state switching response (Phase-A).

sinusoidal due to NL loads' harmonics. The shunt active filter operates with sinusoidal and unity power factor steady-state balanced supply currents in all three phases. The power quality analysis shows the steady-state behavior of three-phase source voltage and source current and examines power

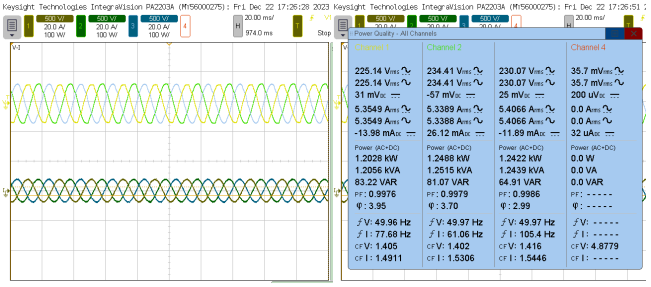

FIGURE 19. Steady-state response of after compensation of three phase source voltage, source current, and power quality analysis of (real, reactive and apparent power, power factor).

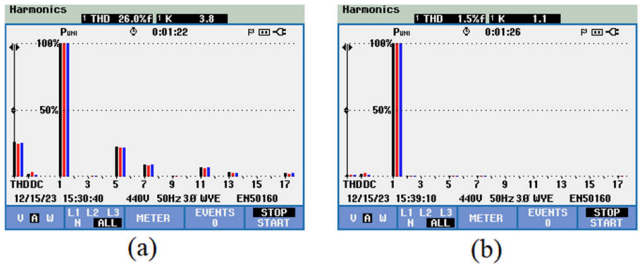

FIGURE 20. % THD of source current: (a) Before compensation, (b) After compensation.

quality metrics, real, reactive, and apparent power, and power factor characteristics, which are shown in Figure 19. Furthermore, Figures 20 (a) and (b) indicate the source current of before and after compensation. THD has minimized from 26.0% to 1.5%.

The PLL and the DC voltage regulators are two of the outputs that are stable during steady-state operation. The FPGA-based architecture's controllers operate concurrently and independently because of parallelism. The quick ADC to the hysteresis current control module generates the gate pulses in this scenario. Once the harmonic signals are acquired, the expected time to produce the PWM signals for VSI to provide compensatory current is four microseconds.

C. PERFORMANCE OF SAPF UNDER LINEAR AND NL LOADS IN THE STEADY STATE ANALYSIS CASE

Compensation for reactive power and harmonics connected with parallel linear (R = 0.5KW and L = 160mH) and NL loads in this scenario is considered, and SAPF performance is examined. The supply side power factor improved from 0.82 to 0.99 lag before compensation to after compensation, shown in Figures 21 and 22, and the supply reactive power decreased from 959.80 VAr to 80.30 VAr, resulting in a power factor-maintained unity at the source. It is clear that the suggested approach measures reference current precisely and compensates for the load's harmonic and reactive power. Furthermore, Figures. 23 (a) and (b) indicate that the source current's THD has decreased from 14.74% to 1.49%.

The study analyzed configurations with varying inductance values from 83 mH to 160 mH and resistance levels spanning

TABLE 6. Performance of the varying linear load condition SAPF performance.

		L=83 mH			L=100 mH			L=120 mH			L=140 mH			L=160 mH		
		R=0.5 KW	R=1 KW	R=1.5 KW	R=0.5 KW	R=1 KW	R=1.5 KW	R=0.5 KW	R=1 KW	R=1.5K W	R=0.5 KW	R=1 KW	R=1.5 KW	R=0.5 KW	R=1 KW	R=1.5 KW
Before compensation of SAPF	P (KW)	1.3497	1.7854	2.1401	1.4093	1.7913	2.0783	1.4255	1.7778	2.1761	1.3921	1.7043	1.9762	1.4372	1.8212	2.1825
	S (KVA)	2.0482	2..4305	2.7544	1.9744	2.3083	2.5671	1.8669	2.1704	2.5415	1.7321	2.0108	2.2585	1.7278	2.0930	2.4359
	Q (Kvar)	1.5405	1.6492	1.7339	1.3828	1.4559	1.5070	1.2055	1.2450	1.3129	1.0291	1.0672	1.0933	0.958	1.0314	1.0819
	PF	0.6590	0.7346	0.7770	0.7138	0.7760	0.8096	0.7636	0.8191	0.8562	0.8041	0.8476	0.8750	0.8318	0.8702	0.8960
	% of THD	10.21	8.521	7.638	11.846	9.961	8.985	12.855	11.005	9.641	13.986	11.728	10.656	14.740	12.463	11.07
After compensation of SAPF	P (KW)	1.7841	2.3043	2.7118	1.8070	2.2475	2.7401	1.7479	2.1789	2.6121	1.6960	2.0120	2.3636	1.7513	2.1973	2.5395
	S (KVA)	1.7873	2.3078	2.7171	1.8117	2.2507	2.7453	1.7502	2.1819	2.6158	1.6990	2.0143	2.3654	1.7531	2.1998	2.5419
	Q (Var)	106.74	128.18	- 168.44	129.53	120.92	-169.93	89.81	114.17	-139.10	101.45	96.61	-92.57	80.30	103.56	-111.09
	PF	0.9982	0.9985	0.9981	0.9975	0.9986	0.9981	0.99	0.9986	0.9986	0.9982	0.9988	0.9992	0.9990	0.9989	0.9990
	% of THD	1.408	1.390	1.531	1.729	1.520	1.532	1.453	1.625	1.519	1.625	1.482	1.293	1.492	1.439	1.351
P= Active power; S=Apparent power; Q= Reactive power; PF= Power factor; THD= Total Harmonic Distortion																

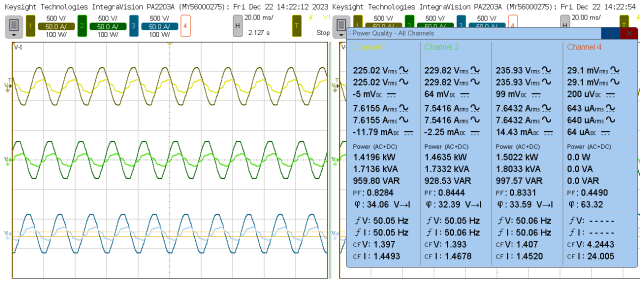

FIGURE 21. Steady-state response of before compensation of three phase source voltage, current, and power quality analysis of (real, reactive and apparent power, power factor).

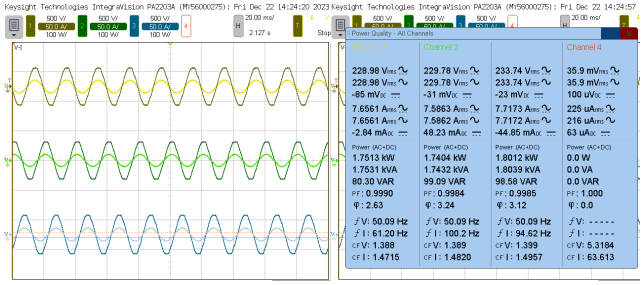

FIGURE 22. Steady-state response of after compensation of three phase source voltage, current, and power quality analysis of (real, reactive and apparent power, power factor).

0.5 KW to 1.5 KW, aiming to evaluate the effectiveness of SAPF in improving system parameters based on a meticulous examination.

The study found that even under fluctuating load circumstances, the injected current accurately tracked the reference current, and there was a reduction in reactive power delivered from the source, anc from the source, and an improved power factor. This indicates that the proposed approach operates efficiently. The findings are summarized in Table. 6.

D. PERFORMANCE OF SAPF UNDER DYNAMIC LOADING

The study examines the dynamic responsiveness of a developed FPGA-based SAPF system under transients resulting from sudden fluctuations in load. The source current increases quickly within twenty milliseconds when the load value increases from 0.5 KW to 1 KW, where time t_1 and DC link voltage reached steady state at time t_2 and t_2 to t_3 are the steady state durations. Again, the load increased from 1 KW to 1.5 KW at time t_3 and reached a steady state response at time t_4, as shown in Figure 24, where t_1-t_2 and t_3-t_4 are the transient length and t_2-t_3 are the steady state durations. Similarly, load decreased from 1.5 KW to 1 KW and 1 KW to 0.5 KW at t_1 and t_3, as shown in Figure 25, where t_1-t_2 and t_3-t_4 are the transient length and t_2-$t_3$are the steady state durations. The efficient control of DC-link voltages, ensuring continuous maintenance of a fixed voltage and Source currents become sinusoidal and balanced, and the current waveform is seen to stabilize afterwards within around a single repetition of the fundamental frequency at load-variating conditions.

E. PERFORMANCE ANALYSIS OF TWO LEVEL BASED SAPF AND THREE LEVEL INVERTERS BASED SAPF

The performance discoveries for two- and three-level SAPF are presented in this section. The filter currents and voltages are smoothed, filter operating stress is decreased, and

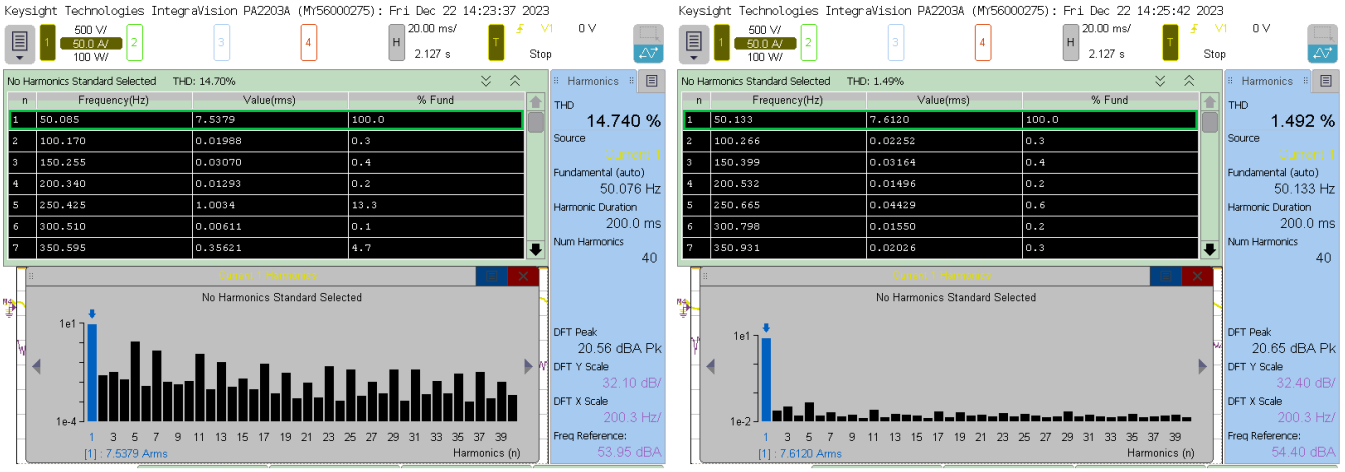

FIGURE 23. % THD of source current: (a) Before compensation, (b) After compensation.

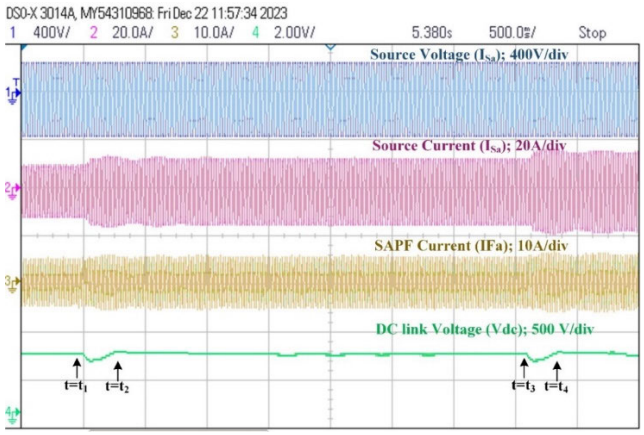

FIGURE 24. Dynamic loading of change from 0.5 KW to 1.5 KW load condition response of SAPF (Phase-A).

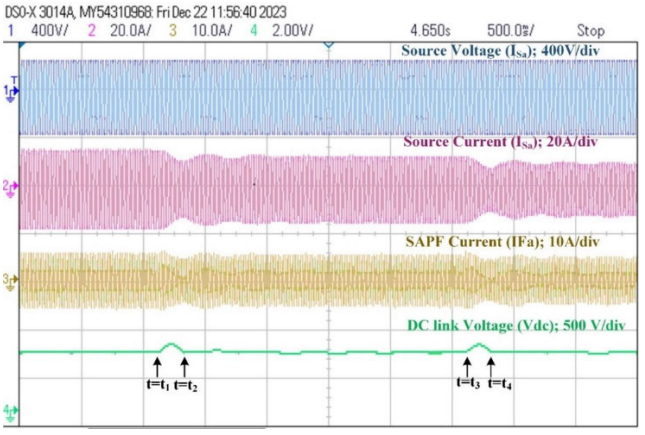

FIGURE 25. Dynamic Loading of change from 1.5 KW to 0.5 KW load condition response of SAPF (Phase-A).

harmonic distortion in both load and source currents is improved by the three-level APF. The two-level inverter compensates for harmonics and creates a sinusoidal source current by injecting three-phase currents and filter voltages. These show that, compared to three-level SAPF, the filter voltages have large step sizes, and the filter currents have a significant amount of harmonics. As a result, they increase the burden on SAPF, which causes losses for the converter. Using two-level and NPC-based three-level inverter SAPF, the percentage of source current THD is reduced from 26% to 4.3% for two-level inverter SAPF, as shown in Figure 26 (a) and (b), and three-level-based SAPF is reduced from 26% to 1.5%, as shown in Figures 20 (a) and (b).

F. PERFORMANCE OF PV BASED SAPF UNDER NL LOADS

In the initial condition, the PV current at the output remained zero, while the grid remained entirely responsible for the diode bridge RL load; When total real power is transferred from the power source to the load during the operation, it is shown in Figures 14, 15, 16 and 17. It compensates for reactive power demand and NL load to generate harmonic current. THD is reduced from 26.00% to 1.5%, and source current is improved from 5.05A to 5.35A.

In the second condition, both the boost converter and NPC inverter are turned on, PV power is received, and the converter current maintains its set value. The dc-link capacitor voltage (V_{dc}) reaches the desired value. PV is interconnected with the SAPF part of active power delivered from PV-SAPF to load; steady-state operation implies that the dual-purpose inverter delivers actual power from the photovoltaic array into the PCC while supplying the reactive and harmonic components of the NL load current. This ensures that the grid current remains in phase with the a-phase PCC voltage. Figure 27 illustrates the source voltage and current, load current, and filter current. Figure. 29(a) shows that the THD of the source current is reduced from 26.0% to 2.7%.

TABLE 7. Comparison of source power, phase angle, power factor, and percentage of THD under SAPF and PV- SAPF conditions using experimental testing.

	Source Power				φ	Power Factor	% THD
	V_{ph} (V)	I_{ph} (A)	P_{total} (W)	Q_{total} (VAR)			
SAPF OFF state	230	5.05	3260.025	1237.065	20.78°	0.93	26.0%
SAPF ON state	230	5.35	3689.851↑	192.731↓	2.99°	0.99	1.5%
PV-SAPF (1500W)	230	3.176	2188.070↓	121.48↓	3.17°	0.99	2.7%
PV-SAPF (3600W)	230	-2.04	-1401.831↓	-122.64↓	175°	-0.99	3.2%

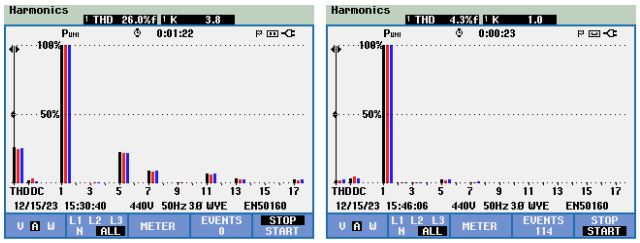

FIGURE 26. % THD of source current: (a) Before compensation, (b) After compensation.

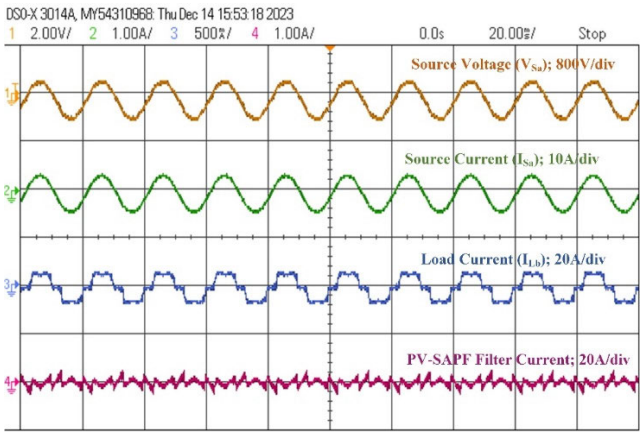

FIGURE 27. PV interconnected with SAPF net power supply from the PCC to load.

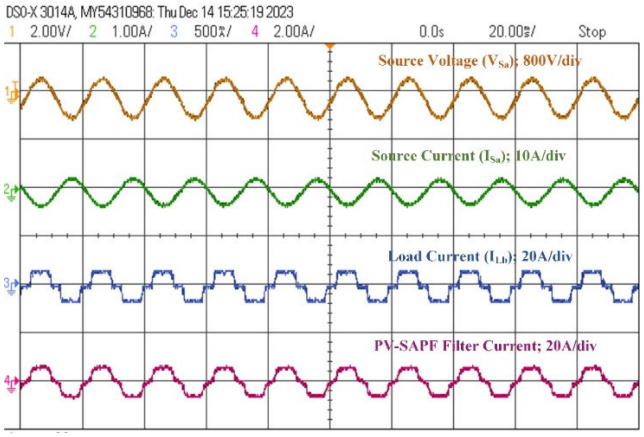

FIGURE 28. PV interconnected with SAPF net power supply from the PCC to the grid and load.

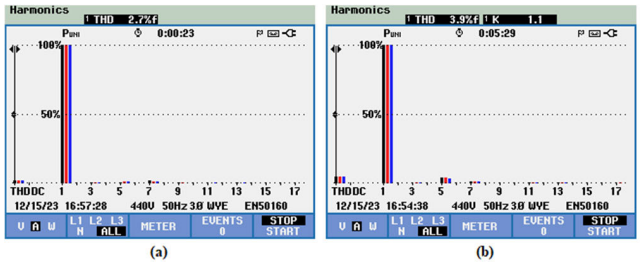

FIGURE 29. After compensation of source current %THD: (a) Active power delivered from PV-SAPF to load (b) Active power delivered from PV-SAPF to load and grid.

The third condition, the PV power generated, exceeds the load's actual power. The extra electricity is observed feeding the grid with a unity power factor. Figure. 28 depicts the source voltage and current, load current, and filter current steady-state operation. THD is reduced from 26.0% to 3.9%, as shown in Figure. 29(b). The comparison of source power, phase angle, power factor, and percentage of THD under SAPF and PV-SAPF conditions using experimental testing is depicted in Table 7.

G. ANALYSIS OF POWER LOSSES AND EFFICIENCY

This section examines an in-depth analysis of the losses associated with the proposed topology and highlights the crucial role played by key parameters, including switching frequency and load value, in determining conversion efficiency. It is imperative to take into account the interplay between these parameters for achieving optimal system performance. The majority of the loss occurs during the conversion stage in semiconductor devices, with three distinct types: conduction loss, switching loss, and OFF-state loss [31], [32], [33]. Conduction loss arises from the ON-state voltage and ON-state resistance in the IGBT devices as the load currents flow through them. Figure 30 illustrates the overall inverter loss between two-level and three-level inverters. To compare the switch losses of the two inverters, we used the device

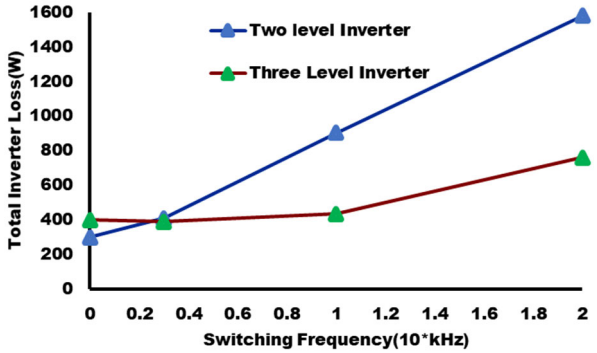

FIGURE 30. Comparative analysis of the overall losses between two-level and three-level inverters at different switching frequencies.

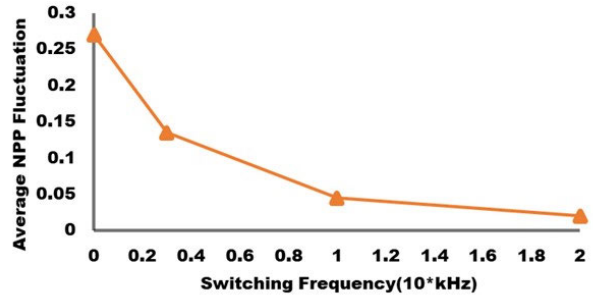

FIGURE 31. Two capacitor voltages vary with three level inverter switching frequency.

characteristics of (SKM100GB12T4) SEMITRANS 2, which operates at 1200.0 V. The DC-bus voltage was set at 750.0 V, and each capacitor had a capacitance value of 2200μF for the DC-link. The implementation of the control strategy resulted in a significant reduction in overall inverter loss. Now, the total loss from the inverter has been reduced to just 60% compared to the two-level inverter, and it's approximately 54% less than the loss observed in the scheme with higher switching frequencies.

Figure 31. graphically demonstrates the variations in the average neutral point potential, as delineated by Equation 18, in reaction to changes in the modulation index. It becomes apparent that the topology predicated on high-switching losses manifests a voltage variation that is approximately half of that observed in the architecture based on low-switching losses. This alteration in duty cycle occurs within the switching cycles, predicated upon the disparity in capacitor voltage.

$$\mathbf{V_{dc\ CapDiff}} = \frac{\mathbf{V_{dc\ Cap\ upper}} - \mathbf{V_{dc\ Cap\ lower}}}{\mathbf{V_{dc}}} \tag{18}$$

In Figure 32 (a) and (b) depict the conduction and switching losses of two-level inverters and three-level inverters, along with the loss distribution of IGBTs and diodes. The upper and lower halves of the inverter leg in a two-level inverter exhibit symmetrical loss distribution. However, the loss distribution of a three-level inverter is not precisely equal. This is due to the frequent alteration of the switching

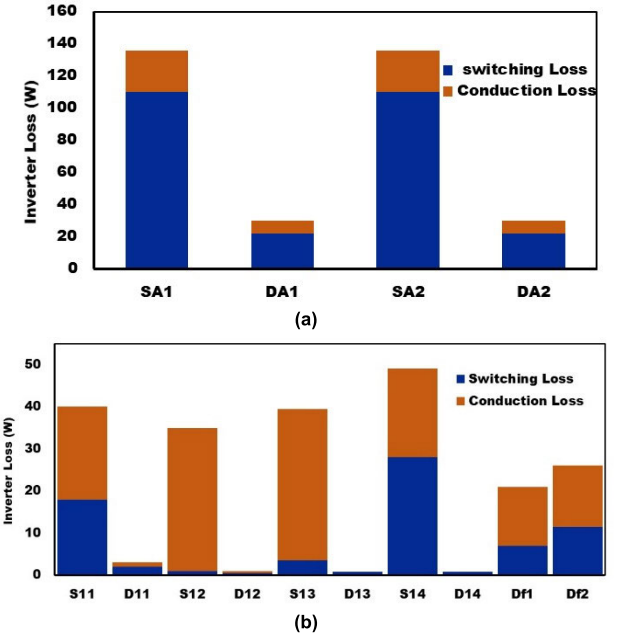

FIGURE 32. Conduction and switching losses of (a) Two-level inverter and (b) Three-level inverter.

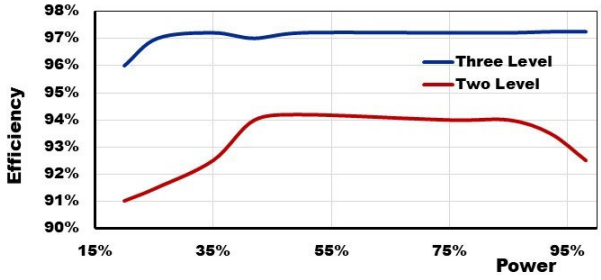

FIGURE 33. Comparison of efficiencies: Three level NPC inverter and Two-level inverter.

sequence to maintain equivalent voltages between the two DC-link capacitors. Additionally, the inner IGBT switches have longer conduction times compared to the outer switches. Furthermore, antiparallel diode losses are nearly insignificant when the modulation index is high. This is because NPC diodes provide increased power sharing, allowing the load current to flow while the main power switches, such as S_{11} and S_{14}, are switched off. It is clear that in the case of a three-level inverter, conduction losses are the primary factor, whereas in a two-level inverter, switching losses take precedence.

The efficiency of the system is clearly illustrated in Figure 33, wherein three-level NPC multilevel inverters are demonstrated to possess a superior efficiency compared to conventional inverters, primarily attributable to reduced switching losses. Comparative analysis indicates that the three-level Neutral Point Clamped inverter outperforms the two-level inverter, showing a performance improvement of 4%. It achieves an efficiency rate of 97.5% across a wide range of load conditions.

V. CONCLUSION

This paper proposed a photovoltaic (PV) interface three-level Neutral Point clamped voltage source inverter-based three-phase Shunt Active Power Filter for reactive power compensation and minimization of harmonics in the presence of both balanced and unbalanced nonlinear load. To enhance the performance of the SAPF, SRF theory and ANFIS algorithm-based controller are incorporated. The reference current for compensation is generated using SRF theory, and the control for the maintenance of smooth DC link voltage is provided by the ANFIS controller. The model is demonstrated in both hardware and simulation environments. Under balanced and unbalanced NL loads, the proposed SAPF provides satisfactory results in terms of eliminating harmonics, balancing loads, and regulating voltage. Furthermore, it does not exhibit any frequency variations at PCC. The experimental results show that it generates a THD of 26.0% before the compensation, which is reduced to 1.5% after compensation in case of loads being nonlinear. During the evaluation of the performance of the proposed system under balanced linear load conditions, numerous observations are made and tabulated by varying the linear loads. In the case of R = 0.5 KW and L = 160mH, the THD obtained before compensation is 14.740 % which gets reduced to 1.492% after compensation. In addition, the performance of the proposed system under dynamic load conditions is also analyzed, and the obtained results are satisfactory. Further, the analysis is carried out for the generation of active power using PV, and the results are verified under different supply conditions. The obtained current THD satisfies IEEE 519-1992 harmonic boundaries, and a near unity power factor is attained after compensation.

ACKNOWLEDGMENT

The authors would like to acknowledge the support from the School of Electrical Engineering, Vellore Institute of Technology, Vellore, India. They would also like to thank the Management of Vellore Institute of Technology, Vellore for the facilities provided during the execution of this work.

REFERENCES

[1] E. Koutroulis and F. Blaabjerg, "A new technique for tracking the global maximum power point of PV arrays operating under partial-shading conditions," *IEEE J. Photovolt.*, vol. 2, no. 2, pp. 184–190, Apr. 2012, doi: 10.1109/JPHOTOV.2012.2183578.

[2] J. Ahmed and Z. Salam, "A critical evaluation on maximum power point tracking methods for partial shading in PV systems," *Renew. Sustain. Energy Rev.*, vol. 47, pp. 933–953, Jul. 2015, doi: 10.1016/j.rser.2015.03.080.

[3] O. Pinzón-Quintero, D. Gaviria-Ospina, A. Parrado-Duque, R. Rodríguez-Velásquez, and G. Osma-Pinto, "Assessment of power quality parameters and indicators at the point of common coupling in a low voltage power grid with photovoltaic generation emulated," *Electr. Power Syst. Res.*, vol. 203, Feb. 2022, Art. no. 107679, doi: 10.1016/j.epsr.2021.107679.

[4] W. U. Rehman, A. R. Bhatti, A. B. Awan, I. A. Sajjad, A. A. Khan, R. Bo, S. S. Haroon, S. Amin, I. Tlili, and O. Oboreh-Snapps, "The penetration of renewable and sustainable energy in asia: A State-of-the-Art review on net-metering," *IEEE Access*, vol. 8, pp. 170364–170388, 2020, doi: 10.1109/ACCESS.2020.3022738.

[5] M. M. V. Cantarero, "Of renewable energy, energy democracy, and sustainable development: A roadmap to accelerate the energy transition in developing countries," *Energy Res. Social Sci.*, vol. 70, Dec. 2020, Art. no. 101716, doi: 10.1016/j.erss.2020.101716.

[6] S. J. Pinto, G. Panda, and R. Peesapati, "An implementation of hybrid control strategy for distributed generation system interface using Xilinx system generator," *IEEE Trans. Ind. Informat.*, vol. 13, no. 5, pp. 2735–2745, Oct. 2017, doi: 10.1109/TII.2017.2723434.

[7] S. Echalih, A. Abouloifa, I. Lachkar, A. E. Aroudi, Z. Hekss, F. Giri, and M. S. Al-Numay, "A cascaded controller for a grid-tied photovoltaic system with three-phase half-bridge interleaved buck shunt active power filter: Hybrid control strategy and fuzzy logic approach," *IEEE J. Emerg. Sel. Topics Circuits Syst.*, vol. 12, no. 1, pp. 320–330, Mar. 2022, doi: 10.1109/JETCAS.2022.3152535.

[8] X. Liang and C. Andalib-Bin-Karim, "Harmonics and mitigation techniques through advanced control in grid-connected renewable energy sources: A review," *IEEE Trans. Ind. Appl.*, vol. 54, no. 4, pp. 3100–3111, Jul. 2018, doi: 10.1109/TIA.2018.2823680.

[9] S. Senguttuvan and M. Vijayakumar, "Solar photovoltaic system interfaced shunt active power filter for enhancement of power quality in three-phase distribution system," *J. Circuits, Syst. Comput.*, vol. 27, no. 11, Oct. 2018, Art. no. 1850166, doi: 10.1142/s0218126618501669.

[10] W. Yuan, X. Yuan, L. Xu, C. Zhang, and X. Ma, "Harmonic loss analysis of low-voltage distribution network integrated with distributed photovoltaic," *Sustainability*, vol. 15, no. 5, p. 4334, Feb. 2023, doi: 10.3390/su15054334.

[11] N. Debdouche, B. Deffaf, H. Benbouhenni, Z. Laid, and M. I. Mosaad, "Direct power control for three-level multifunctional voltage source inverter of PV systems using a simplified super-twisting algorithm," *Energies*, vol. 16, no. 10, p. 4103, May 2023, doi: 10.3390/en16104103.

[12] R. Boopathi and V. Indragandhi, "Comparative analysis of control techniques using a PV-based SAPF integrated grid system to enhance power quality," *e-Prime Adv. Electr. Eng., Electron. Energy*, vol. 5, Sep. 2023, Art. no. 100222, doi: 10.1016/j.prime.2023.100222.

[13] T. M. T. Thentral, K. Vijayakumar, S. Usha, R. Palanisamy, T. S. Babu, H. H. Alhelou, and A. Al-Hinai, "Development of control techniques using modified fuzzy based SAPF for power quality enhancement," *IEEE Access*, vol. 9, pp. 68396–68413, 2021, doi: 10.1109/ACCESS.2021.3077450.

[14] A. A. Imam, R. S. Kumar, and Y. A. Al-Turki, "Modeling and simulation of a PI controlled shunt active power filter for power quality enhancement based on P-Q theory," *Electronics*, vol. 9, no. 4, p. 637, Apr. 2020, doi: 10.3390/electronics9040637.

[15] A. Bielecka and D. Wojciechowski, "Stability analysis of shunt active power filter with predictive closed-loop control of supply current," *Energies*, vol. 14, no. 8, p. 2208, Apr. 2021, doi: 10.3390/en14082208.

[16] S. Nyamathulla, D. Chittathuru, and S. M. Muyeen, "An overview of multilevel inverters lifetime assessment for grid-connected solar photovoltaic applications," *Electronics*, vol. 12, no. 8, p. 1944, Apr. 2023, doi: 10.3390/electronics12081944.

[17] U.-M. Choi, J.-S. Lee, F. Blaabjerg, and K.-B. Lee, "Open-circuit fault diagnosis and fault-tolerant control for a grid-connected NPC inverter," *IEEE Trans. Power Electron.*, vol. 31, no. 10, pp. 7234–7247, Oct. 2016, doi: 10.1109/TPEL.2015.2510224.

[18] N. V. Kurdkandi, M. G. Marangalu, S. Mohammadsalehian, H. Tarzamni, Y. P. Siwakoti, Md. R. Islam, and K. M. Muttaqi, "A new six-level transformer-less grid-connected solar photovoltaic inverter with less leakage current," *IEEE Access*, vol. 10, pp. 63736–63753, 2022, doi: 10.1109/ACCESS.2022.3182240.

[19] N. V. Kurdkandi, M. G. Marangalu, O. Husev, A. Aghaie, M. R. Islam, Y. P. Siwakoti, K. M. Muttaqi, and S. H. Hosseini, "A new seven-level transformer-less grid-tied inverter with leakage current limitation and voltage boosting feature," *IEEE J. Emerg. Sel. Topics Ind. Electron.*, vol. 4, no. 1, pp. 228–241, Jan. 2023, doi: 10.1109/JESTIE.2022.3205546.

[20] J.-S. Lee, R. Kwak, and K.-B. Lee, "Novel discontinuous PWM method for a single-phase three-level neutral point clamped inverter with efficiency improvement and harmonic reduction," *IEEE Trans. Power Electron.*, vol. 33, no. 11, pp. 9253–9266, Nov. 2018, doi: 10.1109/TPEL.2018.2794547.

[21] V. Kamatchi Kannan and N. Rengarajan, "Photovoltaic based distribution static compensator for power quality improvement," *Int. J. Electr. Power Energy Syst.*, vol. 42, no. 1, pp. 685–692, Nov. 2012, doi: 10.1016/j.ijepes.2012.04.061.

[22] M. T. Benchouia, I. Ghadbane, A. Golea, K. Srairi, and M. E. H. Benbouzid, "Implementation of adaptive fuzzy logic and PI controllers to regulate the DC bus voltage of shunt active power filter," *Appl. Soft Comput.*, vol. 28, pp. 125–131, Mar. 2015, doi: 10.1016/j.asoc.2014.10.043.
[23] V. Mahajan, P. Agarwal, and H. O. Gupta, "An artificial intelligence based controller for multilevel harmonic filter," *Int. J. Electr. Power Energy Syst.*, vol. 58, pp. 170–180, Jun. 2014, doi: 10.1016/j.ijepes.2014.01.020.
[24] A. K. Panda and R. Patel, "Adaptive hysteresis and fuzzy logic controlled-based shunt active power filter resistant to shoot-through phenomenon," *IET Power Electron.*, vol. 8, no. 10, pp. 1963–1977, Oct. 2015, doi: 10.1049/iet-pel.2014.0680.
[25] U. R. Babu, V. V. K. Reddy, and S. T. Kalyani, "SVC and DSTATCOM comparison for voltage improvement in RDS using ANFIS," *Int. J. Electron. Commun. Eng.*, vol. 9, no. 8, pp. 1019–1023, 2016.
[26] R. Kumar and H. O. Bansal, "Real-time implementation of adaptive PV-integrated SAPF to enhance power quality," *Int. Trans. Electr. Energy Syst.*, vol. 29, no. 5, May 2019, Art. no. e12004, doi: 10.1002/2050-7038.12004.
[27] B. Deffaf, H. Farid, H. Benbouhenni, S. Medjmadj, and N. Debdouche, "Synergetic control for three-level voltage source inverter-based shunt active power filter to improve power quality," *Energy Rep.*, vol. 10, pp. 1013–1027, Nov. 2023, doi: 10.1016/j.egyr.2023.07.051.
[28] D. Prasad and C. Dhanamjayulu, "Solar PV integrated dynamic voltage restorer for enhancing the power quality under distorted grid conditions," *Electr. Power Syst. Res.*, vol. 213, Dec. 2022, Art. no. 108746, doi: 10.1016/j.epsr.2022.108746.
[29] R. Boopathi and V. Indragandhi, "Solar photovoltaic-interfaced shunt active power filter implementation for power quality enhancement in grid-connected systems," *Int. J. Circuit Theory Appl.*, vol. 51, no. 11, pp. 5305–5323, Nov. 2023, doi: 10.1002/cta.3710.
[30] A. Belkaid, I. Colak, and O. Isik, "Photovoltaic maximum power point tracking under fast varying of solar radiation," *Appl. Energy*, vol. 179, pp. 523–530, Oct. 2016, doi: 10.1016/j.apenergy.2016.07.034.
[31] C. Dhanamjayulu, G. Arunkumar, B. J. Pandian, and S. Padmanaban, "Design and implementation of a novel asymmetrical multilevel inverter optimal hardware components," *Int. Trans. Electr. Energy Syst.*, vol. 30, no. 2, pp. 1–28, Feb. 2020, doi: 10.1002/2050-7038.12201.
[32] A. Salem, H. Van Khang, and K. G. Robbersmyr, "Four-level three-phase inverter with reduced component count for low and medium voltage applications," *IEEE Access*, vol. 9, pp. 35151–35163, 2021, doi: 10.1109/ACCESS.2021.3062110.
[33] S.-A. Amamra, K. Meghriche, A. Cherifi, and B. Francois, "Multi-level inverter topology for renewable energy grid integration," *IEEE Trans. Ind. Electron.*, vol. 64, no. 11, pp. 8855–8866, Nov. 2017, doi: 10.1109/TIE.2016.2645887.

RAJENDRAN BOOPATHI received the B.E. degree in electrical and electronics engineering and the M.E. degree in power electronics and drives from Anna University, Chennai, in 2010 and 2013, respectively. He is currently a Research Scholar with the School of Electrical Engineering, Vellore Institute of Technology (VIT), Vellore, Tamil Nadu. His research interests include photovoltaic systems, power converters, artificial intelligence, power quality, and grid integration of energy systems.

VAIRAVASUNDARAM INDRAGANDHI received the B.E. degree in electrical and electronics engineering from Bharathidasan University, in 2004, the M.E. degree in power electronics and drives from Anna University, Chennai, India, and the Doctor of Philosophy degree. She accomplished the thesis for the Ph.D. entitled "Analysis and Modeling of Multi-Port DC-DC Boost Converter for Hybrid Power Generation System" with Anna University. She is currently a Professor with the School of Electrical Engineering, VIT University, Vellore, Tamil Nadu. She has been engaged in research work for the past 15 years in the area of power electronics, drives and renewable energy systems. Her research interests include power converters, artificial intelligence, and power quality. She was awarded the Gold Medal for the achievement of university first rank.