IEEE Access
Multidisciplinary | Rapid Review | Open Access Journal

Received 17 May 2024, accepted 21 May 2024, date of publication 24 May 2024, date of current version 5 June 2024.

Digital Object Identifier 10.1109/ACCESS.2024.3405373

TOPICAL REVIEW

COTS Devices for Space Missions in LEO

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ABSTRACT In the framework of the NewSpace revolution, time–to–market and budget constraints drive the development of small and medium–sized satellites in Low Earth Orbit (LEO) orbit. The adoption of Commercial Off–the–Shelf (COTS) components represents the current trend to fulfill the NewSpace goals, given their low cost, wide product availability, small time–to–market, and the ability to integrate the most recent advancements in space applications. However, migrating from radiation-hardened (rad–hard) devices to COTS ones requires ensuring comparable reliability levels. To this end, an ''up–screening'' of the COTS devices and systems should be performed in compliance with widely adopted standard regulations, such as those used by ESA or NASA. In this paper, we review COTS components and systems, such as diodes, Bipolar Junction Transistors (BJTs), Field Effect Transistors (FETs), Operational Amplifiers (OPAMPs), memories, and Field Programmable Gate Arrays (FPGAs), proven–flight or ad–hoc tested for compliance with standard regulations. In conclusion, the most promising devices in terms of cost and radiation tolerances are identified, providing useful benchmarks for space engineers developing COTS–based innovative systems.

INDEX TERMS COTS, radiation effects, radiation tests, space avionics.

I. INTRODUCTION

The 21st century marked the beginning of the NewSpace era, characterized by a strong commercialization of space activities, once the exclusive domain of government agencies. The availability of cheaper components and the rise of ride–sharing opportunities are some of the factors that contributed to gradually cutting the costs of manufacturing and launching satellites, allowing startups, universities, and even individual citizens to access space with very small budgets. This led to a substantial increase in the number of payloads launched into orbit, which sextupled over the past four years [1]. The emergence of private companies in the space market has prompted the exploration of new business models, essentially driven by budget and time–to–market constraints. Traditional missions, which were primarily devoted to space communications purposes, often involved large complex satellites designed for 10–15 years lifetimes and launched in expensive–to–reach orbits, such as the Geostationary Earth Orbit (GEO). With the advent of NewSpace, a range of new–generation missions have taken hold, characterized by a series of cost–cutting choices ranging from the orbital target to the electronic components.

Spacecraft sizes and complexity have scaled down, with an increasing exploitation of micro and nanosatellites, such as the popular Cubesats. The orbital target has shifted more toward the LEO, due to its lower launch costs [2], [3]. Launching a kilogram in LEO can cost about $1,400, while it is about twenty times higher for GEO [4]. The interest in LEO also stems from its growing opportunities for low–latency, high–speed, high–bandwidth communications, and high–resolution imaging. Moreover, NewSpace missions are designed to have shorter orbital lifetimes, often with durations of months instead of years [5]. Historically, given the very high launch costs, designers sought to prolong the mission lifetime as much as possible to maximize the exploitation of each satellite [6]. This usually involved more extensive mission assurance procedures and the use of redundant elements, at the expense of increased mass and costs. The NewSpace approach of reducing mission length allows smaller, cheaper components to be used and speeds up testing phases.

In this context, the selection of Electrical, Electronic, and Electromechanical (EEE) parts has increasingly leaned towards COTS components [7]. Unlike their space–qualified

The associate editor coordinating the review of this manuscript and approving it for publication was Derek Abbott.

counterparts, which are specifically designed for space environments, these components are readily available on the market and more cost–effective. However, their vulnerability to radiation poses significant challenges. Satellites are constantly hit by harmful radiation during their lifetime, which can result in malfunctions and failures of the onboard electronics [8]. Traditional space–grade devices are rad–hard by design and extensively tested, to ensure particularly high radiation tolerance. However, this process is quite expensive and time–consuming [9], often resulting in devices with outdated performance to the state–of–the–art. Furthermore, the limited availability of rad–hard components, due to their specialized nature and low production volumes, leads to increased costs compared to their commercial equivalents. The price for a batch of typical rad–hard Metal–Oxide Semiconductor Field–Effect Transistors (MOSFETs) can be on the order of several thousand euros [10], while its automotive–grade counterpart can be found on the market for a few tens of euros [11]. Despite these drawbacks, rad–hard components represent the only adequate solution for satellites expected to undergo intensive radiation doses during their lifetime and for missions where reliability cannot be compromised. As the probability of radiation–induced failures increases with mission altitude and duration, rad–hard devices are therefore essential for missions outside LEO or lasting for many years. On the other hand, for all short–duration missions in LEO typical of the NewSpace age, radiation risks may be so low that rad–hard components result in being overqualified for the purpose. Rad–hard parts can withstand up to 300 times, and occasionally even higher, than the total radiation exposure a typical satellite in LEO experiences over a year [12]. In those cases, the COTS approach offers a viable alternative that can dramatically reduce costs and increase performance.

Since COTS components are designed with little regard for radiation effects, uncertainty on their in–orbit reliability arises. To mitigate this issue, space engineers have adopted up–screening techniques over the years, which involve subjecting the components to rigorous testing to assess their suitability for space missions. This approach has been employed by the National Aeronautics and Space Administration (NASA) since the 1990s when they began introducing combinations of COTS and rad–hard devices on space platforms. Although up–screening does not provide the same assurances as rad–hard devices, it provides a better understanding of device failure modes and causes, thus increasing the confidence level of designers considering their use [13]. As more and more companies want to leverage low–cost technologies to access space and provide services at competitive costs, there is a growing demand for quantifying radiation risks and the performance of available commercial devices.

This paper presents an in–depth analysis of the most promising up–screened COTS components for space applications. A wide range of EEE parts is examined, including diodes, BJTs, FETs, OPAMPs, memories, and FPGAs. Only recently up–screened devices have been considered, particularly starting from 2015. Radiation tests include procedures to evaluate Total Ionizing Dose (TID) effects or device–specific Enhanced Low–Dose Rate Sensitivity (ELDRS) using high–energy photons and particle exposure, Displacement Damage (DD) by proton and neutron irradiation, and Single Event Effects (SEE) through Heavy Ions (HIs) or particles beams. In the realm of testing procedures for commercial–grade electronic components, an array of methods has been proposed and utilized by researchers and manufacturers over the years. This methodological diversity reflects the dynamic nature of the field but also results in variations in test outcomes. Such variability is a critical issue in fields where reliability is non–non-negotiable, like space applications. This study specifically examines electronics that have been tested in compliance with several key standards: the Military Standards (MIL–STDs) from the U.S. Department of Defense, the European Space Components Coordination (ESCC) specifications, and the standards from the Joint Electron Device Engineering Council (JEDEC). These documents include the most widely adopted standards for radiation testing of space EEE parts and are in use at major space agencies, such as NASA and ESA. Test results have been primarily retrieved from two comprehensive sources: ESA's Radiation Test Database [14] and a set of published compendiums that summarize radiation tests performed by NASA Goddard Space Flight Center [15].

II. SPACE RADIATION ENVIRONMENT

Outer space is permeated by radiation that, while imperceptible by human means, poses significant risks to satellites' electronics, potentially leading to several adverse effects ranging from minor dysfunctions to catastrophic mission failures. In 1994, NASA's Clementine spacecraft was launched to test some components during extended exposure to the space environment and to study the Moon and an asteroid [16]. The mission succeeded in its lunar mapping objective, but after four months the central systems sent an unintentional command that caused a thruster to fire and use up all propellant. The mission terminated and NASA declared that the malfunction was caused by a Single Event Upset (SEU), one of the most common effects of cosmic radiation on electronics [17].

Radiations can be classified according to the energy released during the interaction with the matter, their source, and their penetration depth [18]. Based on energy level, the first distinction is made between non–ionizing (low-energy) and ionizing (high-energy) radiation. The non–ionizing one can only increase the energy state of electrons within atoms and molecules, so it can be easily shielded. Instead, ionizing particles have sufficient energy to remove electrons from atoms, so they represent a main concern for spacecraft instrumentation. Ionizing radiation can be further classified based on whether it carries an electrical charge, such as in α and β radiation, or is neutral, such as in γ-rays. The former directly ionizes atoms upon interaction, while the latter causes indirect ionization inside a material by setting a chain of events along its path and generally has a greater penetration depth.

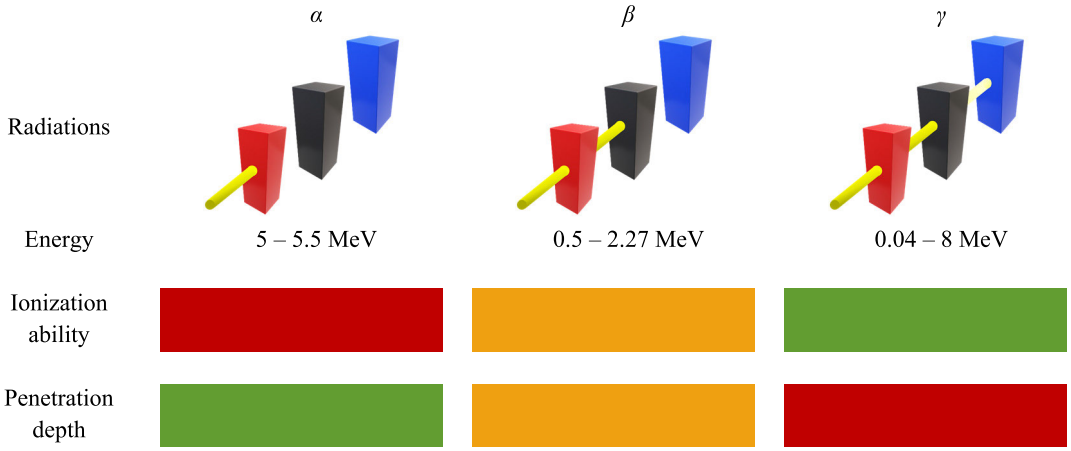

FIGURE 1. Main properties of α, β, and γ radiations. Legend: green: high, orange: medium, red: low.

Fig. 1 summarizes the main properties of the α, β, and γ radiations, which are the most common in space.

α particles consist of Helium (He) nuclei emitted by high atomic number (Z) isotopes [19]. They are heavy and characterized by a strong ionization power. Because of their mass, they quickly interact with atoms and molecules when traversing matter, releasing their energy in short paths. Hence, they have a high rate of energy deposition, and they can be shielded even with thin sheets of paper.

β particles are high–energy electrons or positrons spontaneously emitted by unstable atoms. Since they are smaller and faster than α particles, they can travel farther inside materials. However, they too are easily stoppable using light shielding around sensitive components. Unlike the previous particles, γ-rays are massless electromagnetic waves and have the greatest power of penetration, which makes them the most difficult type of radiation to shield and thus the most concerning for operational spacecraft [20].

As illustrated in Fig. 2, the sources of ionizing radiation in space are mainly three: trapped particles inside Earth's magnetosphere, Galactic Cosmic Rays (GCRs) [21], and particles emitted from the Sun during solar flares and coronal mass ejections, called Solar Energetic Particles (SEPs) [22]. Trapped radiation consists of different types of particles captured by the geomagnetic field and forced into two torus–shaped regions surrounding the Earth, called Van Allen belts. The inner belt, with spanning altitudes of approximately 1,500 to 12,000 km, mainly hosts highly energetic protons in the 10 – 100 MeV range that originate from collisions between GCRs and atoms of the Earth's upper atmosphere [23].

These particles travel with a spiral motion along the field lines of the geomagnetic field, and when they get closer to a magnetic pole, the stronger magnetic force slows them down and eventually bounces them back toward the equator. Instead, the outer belt occupies a much larger region extending from roughly 15,000 km above the Earth to 65,000 km, and contains less energetic protons along with electrons and various ions, with energies ranging from 10 keV to 10 MeV [24]. While the inner belt is largely stable, the outer belt is subject to considerable variations in terms of size and particle concentration, which change in response to geomagnetic storms driven by the Sun.

During solar storms, large amounts of charged particles are captured by the belts, and the particles themselves are much more energetic. However, the relationship between solar events and the size and shape of the belts is still poorly understood, which makes them even more threatening for space operations. Another problem with the Van Allen belts arises from their symmetry to the geomagnetic field, whose approximate dipole axis is inclined by about 11° to Earth's rotational axis and is offset by roughly 450 km to Earth's center [25]. This results in a lower strength of the magnetic field in a region above South America and the Atlantic Ocean, which causes the innermost part of the Van Allen belts to be unusually close to Earth's surface. This region is known as the South Atlantic Anomaly and is one of the most dangerous near–Earth zones for satellites [26]. Because of the increased radiation flux that satellites experience when passing through this region, different precautionary measures are taken, such as the interruption of nominal operations.

GCRs originate from outside the solar system and consist of highly charged and high kinetic energy particles, of which approximately 85% are protons, 14% are α particles and 1% are High Z and Energy (HZE) ions [27]. Although they are fewer in percentage, HZE ions are the most concerning component for the onboard electronics since individual particles can reach energies of up to 10^{12} MeV, potentially causing severe damage. The flux of GCRs in interplanetary space changes according to the solar magnetic activity, which has a nearly periodic nature with cycles of 11 years. During periods of peak solar activity, also called solar maxima, GCRs have a harder time entering the solar system as they are deflected by the Sun's magnetic field. Conversely, during periods of solar minima, the shielding effect of the heliosphere is milder, allowing for the increased flux of GCRs [28].

The last source of harmful radiation directly originates at the Sun, which constantly emits a stream of charged particles into space collectively known as solar wind [29]. As the solar wind flows towards the Earth, it also carries some of the Sun's magnetic field. Occasionally, localized fluctuations in the Sun's magnetic field cause strong bursts that discharge billions of tons of Sun's matter from its upper atmosphere into a particular direction. These events are termed Coronal Mass Ejections (CMEs) and release large amounts of SEPs, of which protons are the dominant constituent. At one Astronomical Unit (AU), these particles travel at speeds of roughly 375 km/s. When these enhanced flows of SEPs reach the Earth, geomagnetic storms occur, which are temporary disturbances of the Earth's magnetic field that cause issues to any satellite in orbit [30]. A well–known adverse effect is that the atmosphere heats up and expands upward upon interaction with these storms because of an exchange of energy. This significantly increases the density of the upper layers of the atmosphere, where most satellites orbit, exposing them to an increased drag force. On February 4, 2022, SpaceX launched 49 ''Starlink'' satellites in Very LEO (VLEO), where they encountered an unexpected drag resistance due to a geomagnetic storm. This caused most satellites to re–enter and burn up in the atmosphere a few days later [31]. Geomagnetic storms are also responsible for GNSS positioning errors and, in some cases, for interruptions of satellite communications [32]. Moreover, during these events, the magnetosphere experiences an increased flux of high–energy electrons, which penetrate spacecraft shielding and accumulate within the electronics. The buildup of electrons can eventually cause discharge and permanent damage to critical electronic components. Even during mild storms, penetrating radiation or charged particles can affect the output signal from electronics [33]. Besides CMEs, bursts of radiation coming from the Sun can also originate from solar flares, which are among the most energetic events of the Solar System and are often accompanied by CMEs and SEP events. The hazard posed by these phenomena is compounded by the impossibility of reliably predicting their occurrence and giving adequate warning before their onset. However, solar activity is monitored by the National Oceanic and Atmospheric Administration (NOAA), which regularly reports about a variety of geophysical phenomena that could directly or indirectly affect satellite performance [34].

III. RADIATION EFFECTS

The interaction of radiation with EEE devices can lead to several various consequences.

When particles and highly energetic photons traverse a device's materials, they deposit energy through ionizing and non–ionizing processes. This results in two primary effects: the generation of electron–hole pairs, so-called ionization process, and the displacement of atoms, so-called DD. Fig. 3 illustrates the factors that contribute to these effects and the mechanisms by which they affect the operation of

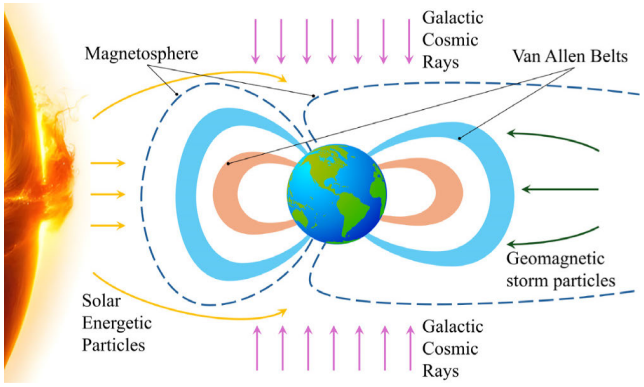

FIGURE 2. Space radiation environment.

electronic devices.When considering the time scale of the radiation–induced effects, a distinction can be made between the nearly instantaneous deviations from the nominal operation, known as SEEs, and the gradual effects resulting from prolonged radiation exposure, referred to as TID effects [35]. SEEs are stochastic events occurring in short time intervals ($\approx 10^{-9}$ s) due to charge deposition induced by a single particle striking a device's sensitive area. The TID arises from the cumulative build-up of electron-hole pairs in semiconductors, which can affect their electrical properties. On the other hand, the DD refers to the material's structural changes at the atomic level due to the passage of energetic particles, which consists of a cumulative process that worsens with time. The DD often correlates with TID effects, especially through charge trapping and changes modifications in interface states [36]. While the DD does not directly cause SEEs, it can modify the material properties that, in turn, affect the likelihood and severity of SEEs [37].

This section introduces and explains the key physical reference quantities essential to understanding radiation effects on EEE devices. Then, it systematically explores SEEs, TID effects, and DD in dedicated subsections, providing a clear and detailed understanding of these phenomena.

A. PHYSICAL REFERENCE QUANTITIES

To accurately characterize radiation environments, some dosimetric quantities that describe the distribution of particles, and their energies have to be defined. Two primary scalar measures used are particles number N and radiant energy R [38]. N is the total number of particles passing through a given area, while R is their energy, excluding rest mass. Therefore, for a beam of particles with average energy$E$:

$$R = N \cdot E \tag{1}$$

where E and R are measured in Joules (J). Both N and R can be quantified per unit area of the traversed material. The fluence (Φ) measures particle count per unit area and is calculated as:

$$\Phi = \frac{dN}{da} \tag{2}$$

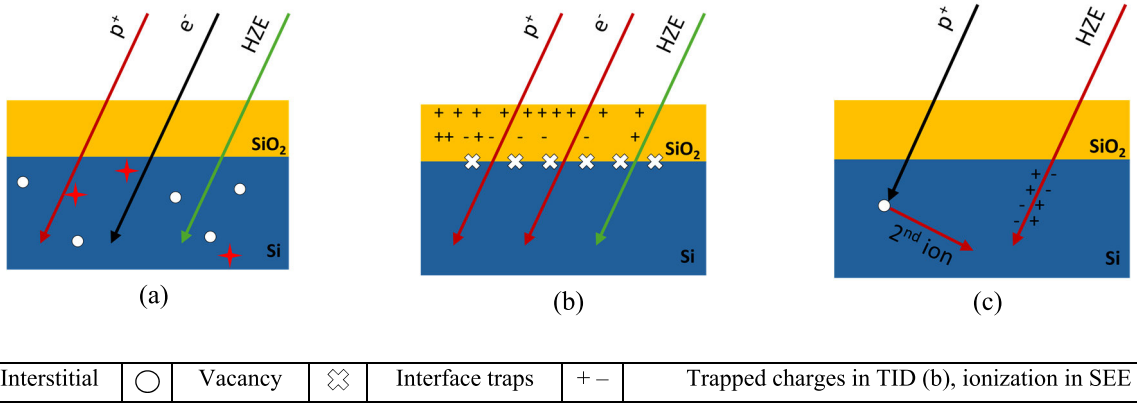

FIGURE 3. The relative impact of electrons (e^-), protons (p^+), and HZE on semiconductor structures, with resulting DD (a), TID (b), and SEE (c) effects, respectively. Protons are the primary cause of DD and have a significant role in TID effects, as shown by the red arrows. Electrons exhibit a major role in TID (red arrow) and a moderate role in DD (black arrow). HZE particles have a minor impact on DD and TID (green arrow) but are the main contributors to SEEs (red arrow).

where (dN) is the infinitesimal particle number and da is the infinitesimal area. Similarly, energy fluence (Ψ) quantifies the radiant energy per unit area. It is defined as:

$$\Psi = \frac{dR}{da} \tag{3}$$

where dR is the infinitesimal radiant energy, and it is expressed in is $J{\cdot}cm^{-2}$.

Another related quantity is the flux, or fluence rate, which describes the rate at which particles or energy pass through a unit area. Particularly, particles flux (φ) is defined as the infinitesimal rate of change of particle fluence over an infinitesimal amount of time (dt):

$$\varphi = \frac{d\Phi}{dt} \tag{4}$$

and it is measured in $cm^{-2}{\cdot}s^{-1}$. Similarly, the radiant flux (ϕ) quantifies the rate at which radiant energy passes through a unit area.

As radiation traverses matter, it may interact with the material with a resulting alteration of energy and trajectory of the incoming or impacted particles, or it might even generate new secondary particles. The specific probability of these interactions is quantified by coefficients that depend on the type and energy of the radiation, the composition of the target, and the nature of the interaction process. The fundamental interaction coefficient is the cross-section (σ), which reflects the total sensitive region within the device that can lead to a SEE when traversed by a particle. For a specific particle and target, σ is defined as the ratio of the number of SEEs (N_{SEE}) to the fluence (Φ):

$$\sigma = \frac{N}{\Phi} \tag{5}$$

The dimensions of σ correspond to an area. However, in practice, units such as $cm^2{\cdot}\ bit^{-1}$ or $cm^2{\cdot}\ devices^{-1}$ are often used, depending on whether SEEs affect a single bit or the entire device's operation, respectively. The sensitive areas within a component are often distributed non–uniformly across its three–dimensional volume. A larger σ indicates higher SEE susceptibility, as it indicates a greater probability of incident particles depositing sufficient energy to disrupt the component's operation. The value of σ depends on the device's materials, architecture, and biasing, and also on the species, energy, and angle of incidence of the particles. By measuring σ across different radiation parameters, the vulnerability of a component to SEE and its failure modes can be thoroughly characterized. Understanding σ facilitates predicting SEE rates in specific operational environments, enabling quantitative SEE risk assessments, development of hardening approaches, and system-level rate predictions [17].

The net energy deposition (ϵ) by a radiation field inside a volume V of material can be calculated as the total radiant energy entering the volume (R_{in}), plus the sum of all internal energy changes within the volume (ΣQ), such as energy released from nuclear reactions, minus the radiant energy leaving the volume (R_{out}):

$$\epsilon = R_{\text{in}} + \Sigma Q - R_{\text{out}} \tag{6}$$

The absorbed dose (D) measures the energy absorbed from radiation per unit mass of a specified material. It is defined as the differential quotient of the net energy deposition ($d\varepsilon$) over an infinitesimal amount of mass (dm) of the target material:

$$D = \frac{d\epsilon}{dm} \tag{7}$$

The SI unit used for D is the gray (Gy), equivalent to 1 J per kg. An alternative unit often used in engineering contexts is the rad (radiation absorbed dose), where 1 rad corresponds to 10^{-2} Gy. Since D varies according to the elemental composition and density of the target material, it is common practice to specify the material of interest next to the unit. In the realm of semiconductor devices, Silicon is the primary material used; hence, the unit rad(Si) is commonly employed to relay information specifically relevant to Silicon-based damage assessment. The dose rate $\dot{D}$ indicates the rate at which energy is deposited per unit mass in a material. It is

defined as the time derivative of D:

$$\dot{D} = \frac{dD}{dt} \tag{8}$$

The dose rate is an important metric for quantifying radiation exposure over time and its potential damage to materials. The effects of a high dose delivered quickly over a short duration can differ significantly from the same dose applied gradually over a prolonged period, even if the total absorbed dose remains constant. $\dot{D}$ is expressed in Gy/s or rad/s.

Similar considerations may be applied to the TID, which is the cumulative energy, per unit mass, transferred to a material through ionization processes. Absorbed dose and TID are similar concepts that mainly differ in their application: the former is a general term used in fields like medicine and radiological protection to quantify radiation exposure, while the latter is specific to the electronics industry, assessing the long-term effects of ionizing radiation on electronic components.

Another important concept in the context of radiation effects on electronic devices is the Linear Energy Transfer (LET). To properly describe the LET, it is necessary to first introduce the concept of linear electronic stopping power (S_{el}), defined as the ratio of the mean energy (dE) lost by charged particles – resulting from ionization or excitation interactions with atomic electrons – to the distance (dl) traveled in a material:

$$S_{el} = \frac{dE}{dl} \tag{9}$$

The "restricted" LET (L_Δ) [39] is defined as the average energy lost by charged particles per unit length due to electronic interactions, minus the sum of kinetic energies exceeding a given cutoff value Δ, which are carried away by secondary electrons, denoted as $dE_{ke,\Delta}$:

$$L_\Delta = S_{el} - \frac{dE_{ke,\Delta}}{dl} \tag{10}$$

which is expressed as keV/μm. Importantly, L_Δ describes the local energy deposition along a particle's track, excluding energy removed by secondary electrons above the Δ threshold. When no energy cutoff is specified, the quantity in Eq. (10) – now referred to as unrestricted LET and denoted with L – simply equals the S_{el}. Rigorously, using the unrestricted LET is only justified when a material encounters a single radiation type. In practical situations, especially in environments like LEO, electronic components are exposed to a variety of radiation types (e.g., protons, electrons, and heavier ions), each with its energy distribution. Moreover, charged particles can undergo processes like energy loss straggling, namely variations in the amount of energy they lose, and nuclear reactions, which produce secondary particles. These factors complicate the radiation field, making it a mix of different particles with a broad range of energies. To accurately represent this complex radiation scenario with a single measure, an averaged LET is used, which takes into account the variety of particles and their energies in the radiation field. Historically, two averaging approaches have been widely utilized: track averaging (LET_t), which sums across all particle tracks, and dose averaging (LET_d), which gives greater weight to higher–LET particles. The inclusion of secondary particles generated during ion interactions also considerably influences LET calculations. Without clearly detailing the averaging approach and specific radiation environment, assessing radiation effects and comparing study results becomes challenging. Since energy loss correlates with material density, it is practical to normalize the LET by the material's density. This density-adjusted value, often expressed in MeV·cm^2·mg^{-1}, is simply referred to as LET [40].

A few final reference quantities are introduced that specifically pertain to DD effects. In this context, the Non-Ionizing Energy Loss (NIEL) is defined as the fraction of energy lost by a radiation particle through non-ionizing processes, which causes atoms in the semiconductor lattice to be displaced. In a generic radiation field, the NIEL depends on the energy of the incident particles, with higher energies typically resulting in greater DD potential. The unit for NIEL is typically given in MeV·cm^2/g. Another important quantity is the Displacement Damage Dose (DDD), which quantifies the cumulative non–ionizing energy deposited in a material by radiation. It is calculated by integrating the NIEL, as a function of the particle's energy, across the particle fluence spectrum [41], with the resulting value typically expressed in units of MeV/g. One last metric is the Displacement Damage Equivalent Particle Fluence (DDEF). This quantity enables the comparison of DD from different types of radiation by normalizing their effects to a standard reference, typically 1 MeV neutrons. The DDEF is derived by adjusting the fluence of each particle type to match the DD that would be caused by these reference neutrons, facilitating a unified assessment of DD across diverse radiation environments.

B. SINGLE EVENT EFFECTS

The SEEs are typically induced by interactions between high–energy particles and the sensitive areas of semiconductor devices. The most concerning are HIs, which cause direct ionization, and protons or neutrons, which lead to indirect ionization through secondary particles released in nuclear reactions following a collision. High–energy photons, such as γ–rays, can also contribute indirectly to SEEs, albeit to a lesser extent, by generating secondary particles during interactions with matter. For instance, γ–rays interacting with atomic nuclei in semiconductors can produce recoil nuclei or secondary particles like protons or neutrons through photon–neutron reactions or other nuclear processes. These secondary particles, in turn, can cause SEEs by interacting with the electrons of the semiconductor material of the device [42], generating ionized atoms. Specifically, this occurs because of electrons moving from the valence band to the conduction band, creating electron–hole pairs. When the LET of the incident particle, or that of secondary particles

from nuclear reactions, exceeds the threshold LET (LET_{th}), changes in device operation may be observed [43].

According to ESCC Basic Specification No. 25100 [44], SEEs can be classified based on the effects on the device's operation including Single Event Upset or Soft Error (SEU), Single Event Transient (SET), Single–Event Functional Interrupt (SEFI), Single Event Latch–up (SEL), Single Event Hard Error or Stuck Bit (SEHE), Single Event Gate Rupture (SEGR), and Single Event Burnout (SEB) [44].

SEUs consist of an inversion in the state of a logic cell, categorized as soft errors because normal functioning is restored after a reset or rewrite. HIs are a primary source of SEUs, often being the initial form of impact from GCRs on spacecraft electronics, causing these SEE–inducing events. SETs are temporary voltage spikes at a circuit node, triggered by a single energetic particle hit. SEFIs refer to malfunctions in complex devices such as memory, processors, FPGAs, or mixed-signal chips. These require a reset or power cycle for functionality restoration and may lead to data loss. SELs occur due to the activation of a parasitic thyristor structure in an integrated circuit, creating a low–impedance, high–current state. This state can be destructive if sustained, potentially causing irreversible device damage. However, if permanent damage is averted, reinitializing the device through power cycling is necessary to resume normal operations. SEHEs signify permanent or semi–permanent operational changes in a memory cell, such as a memory bit becoming stuck. SEBs result from the activation of a parasitic bipolar structure in a power transistor, which can lead to a destructive high current flow unless adequately safeguarded, as highlighted in [45]. SEGRs are characterized by the destructive physical rupture of a gate oxide or another dielectric layer in an integrated circuit, leading to bias–dependent leakage currents.

Destructive events is a collective term encompassing various SEEs that can lead to irreversible operational failure of a device, rendering it non-functional without replacement. This category includes unaddressed SEBs in power transistors, SEGRs, and SELs that are not promptly resolved. Additionally, a large accumulation of SEHEs or stuck bits, exceeding error correction capabilities, is also considered an irreversible effect.

C. TOTAL IONIZING DOSE EFFECTS

The cumulative impact of ionizing radiation on electronic components over an extended period influences the performance of electronic devices through a variety of physical mechanisms, including charge buildup, interface state generation, mobility degradation, oxide breakdown, and enhanced susceptibility to SEEs [46].

Ionizing radiation primarily ionizes atoms in semiconductors, generating electron–hole pairs that alter the material's electrical properties. In diodes, charge accumulation affects the depletion region width, altering bias characteristics. For BJTs, this buildup influences minority carrier recombination, impacting current gain and frequency response. Accumulated charges in FETs lead to threshold voltage shifts, affecting the voltage required to turn the device on or off. In digital circuits, threshold voltage shifts and leakage currents can lead to timing variations, affecting the reliability of the circuit [47].

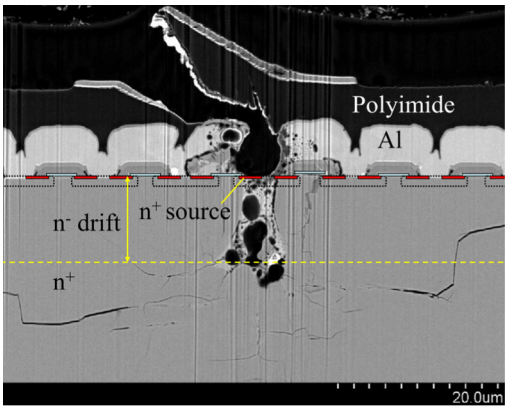

FIGURE 4. Cross–sectional scanning electron microscopy image of SEB damage in a SiC power MOSFET [45]. Reprinted from Microelectronics Reliability, Volume 55, Issues 9–10, Tomoyuki Shoji, Shuichi Nishida, Kimimori Hamada, Hiroshi Tadano, Analysis of neutron-induced single-event burnout in SiC power MOSFETs, Pages 1517-1521, Copyright (2015), with permission from Elsevier.

The semiconductor bandgap, defining the energy required for electrons to move from the valence to the conduction band, determines the material's electrical conduction and radiation response. Electrons in the valence band require a specific minimum amount of energy, characteristic of the material, to be promoted to the conduction band. This transition enables the conduction of electric current through the crystal lattice. Interface states within the bandgap directly affect charge carriers formation and so the device's electrical response. The existence of interface states is determined by the presence of defects in the bulk of the SiO_2, called oxide traps, or at the Si–SiO_2 interface, called interface traps [48].

Both charge buildup and the formation of new interface states can lead to increased charge carrier scattering. This occurs as the carriers collide with trapped charges, impurities, or defects, losing momentum and changing direction, resulting in reduced mobility. Regarding PN devices, reduced mobility may result in slower response times for diodes and reduced gain or switching speeds for BJTs. In MOS devices, reduced mobility can lead to slower switching speeds and a reduction in drive current capability in MOSFETs. Overall, the reduced mobility perpetually leads to slower device operation device. For digital circuits, this can manifest as decreased processing speeds and longer response times to input signals, potentially leading to timing errors where the circuit may misinterpret signals or fail to synchronize properly, resulting in higher error rates. For analog circuits, the effects of reduced mobility include increased noise or distortion [49].

In semiconductor devices, oxide layers are typically composed of SiO_2 and serve as insulators or dielectrics. Particularly, the thin gate oxide in MOSFETs separates the gate terminal from the underlying semiconductor channel, while in capacitors, oxide layers are used as dielectrics to

increase capacitance without increasing the physical size. Long–term radiation exposure to these layers leads to the accumulation of defects, reducing their ability to withstand electric fields and eventually causing dielectric breakdown, where the loss of insulating properties renders the material conductive. In MOSFETs, dielectric breakdown of the gate oxide can cause a short circuit between the gate and the channel or substrate, leading to permanent device failure. This disruption in the controlled charge flow renders the transistor non–functional. In integrated circuits using oxide layers for insulation between different components, a breakdown could lead to shorts between circuit elements, thereby disrupting the circuit's overall functionality [50].

Finally, TID effects include modifications in a device's sensitivity to SEEs. Trapped charges and TID–induced alterations in material properties may reduce the amount of charge required from a single ionizing particle to initiate an SEE, enabling particles with previously insufficient energy to trigger such events. Trapped charges can modify the internal electric fields of a device, influencing the collection of charges generated by ionizing particles and thus increasing the probability of an SEE. In diodes and BJTs, modifications at the junctions can heighten their vulnerability to ionizing particles, potentially leading to a rise in SET occurrences. In FETs, especially MOSFETs, the gate oxide may become more prone to ionizing events due to TID–induced trapping, elevating the risk of gate oxide breakdown or other SEE–induced malfunctions [51].

D. DISPLACEMENT DAMAGE

DD in semiconductor materials is caused by non–ionizing interactions, where energetic particles physically displace atoms from their lattice sites, resulting in the creation of point defects such as vacancies and interstitials. The mechanism involves the transfer of kinetic energy from the energetic particle to the semiconductor's atoms through a scattering process, whose characteristics vary based on the particle's type and energy. The first atom struck in this process is known as the Primary Knock–on Atom (PKA). When this collision occurs, the PKA gains energy from the incoming particle and can be displaced from its lattice position, which can lead to additional collisions with neighbouring atoms and eventually a chain reaction of further displacements. The subsequently displaced atoms are called ''recoils'' and their energy distribution, or ''PKA spectrum'', is influenced by the collision kinematics, as illustrated in Fig. 5.

For instance, in Silicon, electrons and photons around 1 MeV typically undergo a Rutherford or Coulomb scattering, governed solely by the static electric potential, leading to isolated point defects scattered within the lattice. In contrast, a neutron of comparable energy can create a dense cluster of defects due to its significant energy transfer to the PKA, causing widespread displacement of neighboring atoms and creating a highly disordered region. This interaction is known as nuclear elastic scattering, where the incident particle's kinetic energy is transferred to the PKA

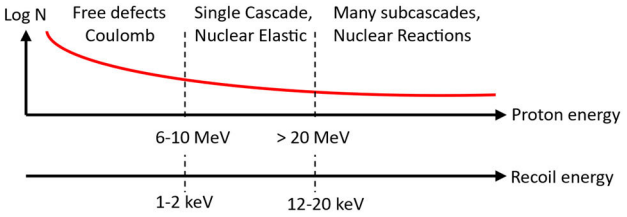

FIGURE 5. Correlation between the energy of PKAs and the resultant defect configurations in Silicon. The logarithmic scale indicates the number of interactions (N) as a function of the incident proton's energy [52].

via elastic interaction. At higher particle energies, nuclear interactions become more likely, leading to nuclear inelastic scattering. In this scenario, the energy imparted to the PKA can destabilize its nucleus, emitting secondary particles and generating multiple sub–cascades. The affected regions, referred to as terminal subclusters, exhibit significantly higher defect densities compared to those impacted by Rutherford scattering [36].

The primary lattice defects initially formed consist of vacancies and interstitials. A vacancy is created when an atom is knocked out of its lattice position, leaving behind an empty spot. The displaced atom may then occupy a position not normally part of the lattice structure, becoming an interstitial. Together, a vacancy and its associated interstitial form a so–called Frenkel pair or *I-V* pair, which is illustrated in Fig. 6. In Silicon, more complex structures such as divacancies, namely larger clusters of vacancies, can also form. When these defects interact with impurity atoms, they form defect–impurity complexes such as the vacancy–phosphorus pair. The threshold energy required to displace an atom in Silicon is about 21 eV. Since a 1 MeV neutron typically produces recoil energy around 50 keV, it is easy for EEE devices to accumulate DD in a radiation–intense environment such as the LEO [53].

An important note is that the type and initial energy of the incident particle are not a reliable indicator of the concentration of defects produced. The number of *I-V* pairs produced is proportional to the PKA energy, which in turn depends on the NIEL, the small fraction of total energy loss that effectively causes atomic displacements. In other words, while the number of cascades and sub–cascades created during scattering processes increases with incident particle energy, the nature of the damage in these areas remains consistent [54]. According to the Shockley–Read–Hall theory, the electrical effects are proportional to the concentration of defects through a damage constant that depends on the specific device and the measured parameters [55], [56]. Therefore, the NIEL is an important parameter in analyzing DD effects on EEE devices.

DD often leads to the creation of new energy levels within the semiconductor's bandgap. These defect states can significantly alter the electrical and optical behavior of semiconductor materials and devices. Several physical effects influence the charge carrier transport from the valence band to the conduction band, including (a) thermal generation

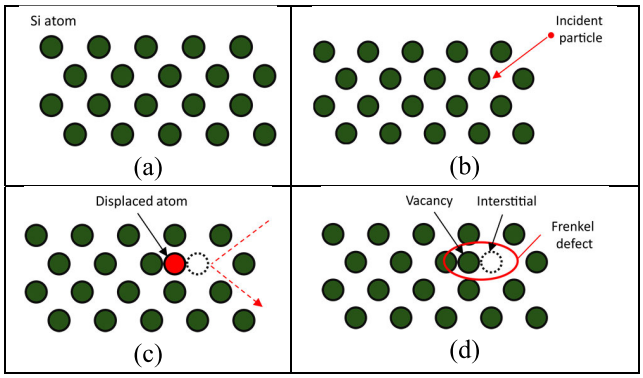

FIGURE 6. Illustration of DD in Silicon: (a) a pristine Silicon lattice; an incident particle striking the lattice and displacing a Silicon atom; (c) the displaced atom moving away from its original lattice position, creating a vacancy; (d) formation of a Frenkel defect, characterized by the newly created vacancy and the displaced atom in an interstitial position (d) [42].

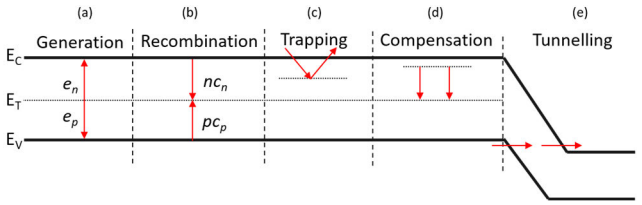

FIGURE 7. Conceptual diagram of the effects of DD within the band structure of a semiconductor and its influence on electronic properties. In (a), thermal generation of carriers from a deep level (ET) to the conduction band (EC) or valence band (EV) occurs at rates e_n and e_p, respectively. In (b), carrier capture by ET from EC or EV can proceed at rates nc_n and pc_p. In (c), carrier trapping is depicted when ET predominantly interacts with either EC or EV. In (d), compensation is illustrated by ET counterbalancing the doping levels, influencing the material's conductivity. In (e), ET facilitates carrier tunneling under a substantial electric field, enabling charge transition from EV to EC [57].

of electron–hole pairs, (b) recombination of electron–hole pairs, (c) carrier trapping, (d) compensation of donors or acceptors, and (e) defect–assisted tunneling, as shown in Fig. 7. The presence of defect levels near the midgap significantly contributes to the thermal generation of electron–hole pairs, a mechanism that inadvertently increases leakage current in devices. This leakage is a byproduct of the thermally excited electrons transitioning from the valence to the conduction band, creating holes that contribute to the unintended current flow. Concurrently, recombination centers may form in correspondence due to radiation–induced impurities, where electrons and holes prematurely recode, decreasing carriers' lifetime. This effect is particularly detrimental to bipolar transistors, where it leads to gain reduction. Additionally, defect centers can temporarily trap carriers, introducing inefficiencies in the charge transfer in devices such as Charge–Coupled Devices (CCDs). This trapping can cause delays or errors in the signal processing functions of CCDs, affecting their overall performance. Another relevant effect is the compensation of donors or acceptors by radiation–induced centers, which neutralizes free electrons or holes, thereby altering the carrier concentration within the material. Such alterations can remarkably affect device characteristics, including the resistance encountered in a transistor's collector region. The last DD effect is defect–assisted tunneling, where radiation–induced defects provide a pathway for carriers to tunnel through potential barriers.

This mechanism can lead to an increase in device currents, notably affecting the reverse current in diode structures, which can have implications for the diode's reverse–bias behavior and overall efficiency. In diodes, these effects can manifest as changes in the *I-V* characteristics, increased leakage currents, and altered breakdown voltages. In BJTs, DD primarily impacts the gain and frequency response, while in FETs, it can cause threshold voltage shifts and mobility changes [36]. After their formation, these defects tend to reorganize themselves into more stable configurations, a process that is influenced by temperature and is known as thermal annealing. This typically reduces the severity and quantity of the damage. However, in certain cases, this reordering process can result in the formation of more problematic defects, a phenomenon called reverse annealing. For example, during short, intense radiation bursts at room temperature, defects are created almost instantaneously. These defects then migrate and reorder, generally resulting in a reduction of the damage's impact, known as forward annealing. This process can be quite rapid, often completed within seconds to minutes, according to the type and energy of the incident particle. Following this initial phase is long–term annealing, which can continue for years at room temperature. The rate and extent of annealing can be accelerated by raising the temperature or by increasing the carrier's injection level [58].

IV. STANDARD FOR RADIATION TESTING

Several existing standards for testing and qualification of electronic parts against radiations have been proposed in the literature [40], [44], [59], [60], [61]. Three sources have been considered in this survey: ESCC standards [44], [59], developed collaboratively by the ESA member States, MIL standards [62], [63], issued by the U.S. DoD, and JEDEC Standard Documents (JESD), from the JEDEC association. All devices discussed in this paper have been tested according to these tests, which have been referred by NASA as the "key space radiation test standard" [64]. Each standard provides a framework for evaluating the radiation hardness and reliability of EEE parts in demanding and challenging environments, such as those encountered in military or space operations. While they all serve the same general purpose, there are differences in terms of their focus, requirements, and testing methodologies. MIL standards tend to be particularly stringent, while the JESD ones are less comprehensive and recommended for use in conjunction with other standards.

A. MIL-STD-750-1

The test methods described by the MIL–STD–750–1A standard [65] apply to semiconductor devices, specifically to transistors, diodes, tunnel diodes, rectifiers, voltage regulators, and other related parts.

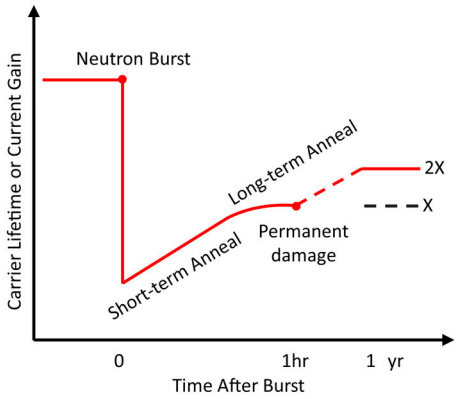

FIGURE 8. Temporal evolution of bulk Si parameters after a neutron burst. The immediate drop following the burst indicates the onset of damage. The subsequent upward trend represents the short–term annealing phase, marked by a partial recovery of properties, yet stabilizing at a level indicative of permanent damage, as shown by the asymptotic trend towards the dashed line labeled 'X'. The line marked '2X' denotes a potential doubling of this asymptotic value, hinting at further recovery achievable through long–term annealing. [36].

1) METHOD 1017.1 – NEUTRON IRRADIATION

Method 1017.1 aims to determine the responsiveness of semiconductor devices to neutron irradiation. In particular, the goal is to measure the degradation of critical device electrical parameters as a function of neutron fluence. The test sample shall include a minimum of 10 randomly selected parts.

The test is destructive and consists of three steps: 1) electrical tests on the device to record the pre–exposure levels of the critical parameters, 2) exposure of the devices to neutron irradiation, and 3) post–irradiation electrical tests to assess if the critical parameters are within specified limits. The radiation exposure levels, the electrical parameters to be measured and the criteria for pass/fail the devices after irradiation are defined before the test.

The neutron source shall be a TRIGA Reactor or a Fast Burst Reactor with a well–characterized energy spectrum, and operations may be in either pulse or steady–state pulse conditions. Starting from the known energy spectrum, the neutron fluence shall be calculated by measuring the amount of radioactivity induced in a fast–neutron threshold activation foil such as ^{32}S, ^{54}Fe, or ^{58}Ni, which is irradiated simultaneously to the devices. The conversion from induced radioactivity to neutron fluence shall be performed according to standards ASTM E263 [66], ASTM E264 [67], and ASTM E265 [68]. The irradiation and the electrical tests shall be made at a controlled room temperature of 20°C ± 10°C. If a measure of the radiation absorbed is needed, CaF_2 thermoluminescence dosimeters shall be used in accordance with the ASTM E668 [69] standard.

2) METHOD 1019.5 – STEADY–STATE TOTAL DOSE IRRADIATION PROCEDURE

The purpose of Method 1019.5 is to evaluate the degradation of critical electrical parameters in semiconductor devices exposed to ionizing radiation. The method includes three tests, a standard test to be performed in every case and two additional ones to be performed under certain conditions.

The standard test consists of three steps: 1) electrical tests on the device to record the pre–exposure parameter levels, 2) steady–state irradiation of the device with a ^{60}Co γ–ray source, and 3) post–exposure electrical tests to assess if the critical parameters are within specified limits. The radiation levels, the electrical parameters to be measured and the criteria for pass/fail the devices after irradiation are defined before the test. The test requires the devices to be enclosed in a Pb/Al container, made of an outer Pb shield at least 1.5 mm thick and an inner Al shield of at least 0.7 mm, to minimize dose enhancement effects caused by low–energy scattered radiation [70]. If necessary, electrical tests may also be performed during the exposure to avoid variations introduced by post–irradiation time-dependent effects. The radiation field produced by the ^{60}Co source shall be uniform within 10% inside the irradiated volume, as verified with proper dosimetry instruments. The radiation is chosen according to one of the following conditions: 1) dose rate in the range 50–300 rad(Si)/s (standard test condition). If multiple exposures at different radiation levels are performed, the dose rate shall not vary by more than 10% between each irradiation; 2) for MOS devices only, the dose rate can be equal to or greater than the maximum dose rate of the intended application, if this is lower than 50 rad(Si)/s; 3) the test may be performed at the dose rate of the intended application if agreed by the involved parties.

The above standard test conditions might lead to excessively conservative results for devices whose intended application is characterized by very low dose rates, such as in space missions, where the flux of particles varies over a wide range, as demonstrated in [71]. In these cases, an extended room temperature anneal test may be performed after carrying out the standard procedure, if the device failed it. This test is appropriate for MOS devices only and has the effect of simulating the device performance under very low dose rate environments, even though the standard test was performed at high dose rates. The procedure requires subjecting the device to a room temperature anneal for enough time to allow the device parameters that have exceeded their specification limits to return to within specification. However, the total time span of the temperature anneal shall not exceed the ratio between the TID and the maximum dose rate of the intended application. The room temperature shall be such as to ensure that the case of the device will have a temperature within the range of 24°C ± 6°C. After this extended annealing test, the device parameters are measured again through electrical tests and, if they fall within the specification limits, the device can be considered suitable for applications in very low dose rate environments.

After carrying out the above procedure, an additional accelerated annealing test shall be performed for MOS devices only, which might exhibit severe time–dependent effects for low dose rate ionizing radiations. The test involves 1) irradiating the device following the standard procedure

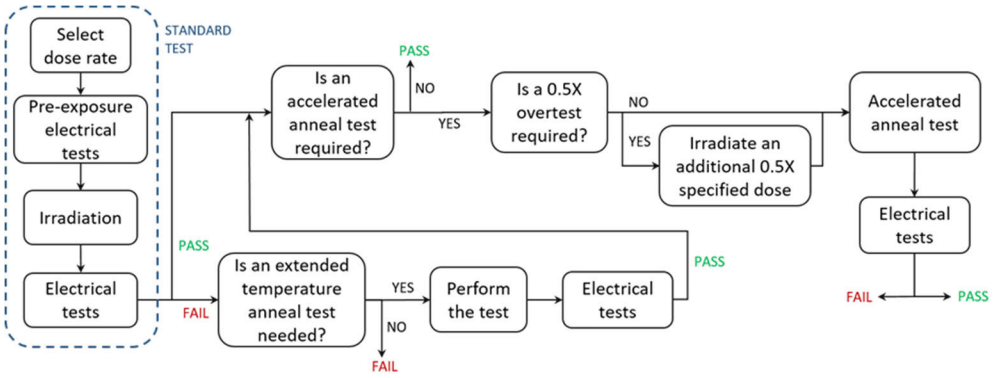

FIGURE 9. Test method 1019.5 from MIL–STD–750–1.

but using a 0.5 overtest factor, i.e. half of the dose previously used, and 2) heating the device inside an environmental chamber and using its worst–case static bias conditions. The heating step shall be carried out according to one of the following conditions: 1) at 100°C ± 5°C for 168 ± 12 hours; 2) at an alternate temperature/time profile that has been demonstrated to cause equal or greater degradation in the device parameters as that caused by the previous condition; 3) at an alternate temperature/time profile that has been demonstrated to cause trapped hole annealing of greater than 60% and interface state annealing of less than 10%.

After these steps, electrical tests are performed again for a final assessment of the parameters degradation. Fig. 9 summarizes all the steps of this test method.

3) METHOD 1019.5 – SINGLE–EVENT BURNOUT AND SINGLE–EVENT GATE RUPTURE

Method 1080.1 describes a standard approach for the characterization and verification of planar vertical power MOSFET semiconductor devices to SEB and SEGR.

The described tests can be used for lot acceptance and qualification of those devices. The main required instrumentations for the tests include an HZE particle source, a dosimetry system, proper instrumentation for applying test conditions and measuring electrical parameters of interest, test circuit boards, and, in some cases, a vacuum chamber system. The source of HI, typically a cyclotron or a Van de Graaff generator, must be capable of providing a flux $> 1{\cdot}10^5$ ions/cm$^2{\cdot}$s and shall ensure a beam uniformity of ± 15% over the die area.The ion range is not uniquely specified by the document, but it should be picked to ensure a proper penetration depth to induce a SEB and SEGR response [46].

The required resolution to the electrical measurement system should be sufficient to resolve gate currents < 10 nA and drain currents < 100 nA. The vacuum chamber system, if required, must be capable of evacuating the chamber to less than 0.13 Pa within approximately 15 to 20 minutes.

The method includes two kinds of tests, characterization and verification. The characterization tests produce SEB cross–sectional area curves or SEB and SEGR failure threshold curves. They are typically performed before verification tests to establish the worst-case operating conditions of the device or to identify the sensitive die area. These tests require that the devices be irradiated while in off–state bias conditions. The verification tests involve irradiating the device under specified test conditions, e.g., ion beam and bias conditions. This kind of test is useful for hardness assurance, qualification tests, and acceptance tests of MOSFET to determine their suitability at the specified test conditions.

B. MIL-PRF–19500 – JAN QUALIFIED COMPONENTS

The MIL–PRF–19500 specification provides general performance requirements and associated verification methods for semiconductor devices intended for use within military and/or space applications. Such components require particularly extensive tests, as they must guarantee high reliability and they need to operate under very demanding conditions, such as wide temperature ranges and strong vibration loads. In addition to radiation requirements, the document includes a broad range of other requirements that devices must fulfill to comply with the specification. All test methods and conditions required by MIL–PRF–19500 specification follow the test methods described by MIL–STD–750 specification [72]. MIL–PRF, which stands for *Military Performance Specification*, is a subcategory of MIL–STD, which sets out more specific performance requirements for individual components and systems. More specifically, while MIL–STD standards provide a broad overview of requirements, MIL–PRF standards are more specific and set out more rigorous performance requirements for particular components and systems.

Electronic components that are tested and proven to conform to MIL–PRF–19500 are marked with a Joint Army Navy (JAN) label. Besides the basic JAN certification, MIL–PRF–19500 provides additional designations to identify higher quality levels that reflect the amount of testing and screening a device has undergone and successfully passed.

For hermetic encapsulated semiconductor devices, the quality levels are in ascending order: JANTX, JANTXV, and JANS. The 'TX' suffix, which stands for "*Testing Extra*", means that a device has gone through screening tests, which are not required for the JAN level. JANTXV devices must pass all screening tests of the JANTX level, plus an additional visual inspection to enable further elimination of defective

parts. The highest quality level is JANS, where the suffix 'S' indicates that the device is qualified for space applications. JANS components require all the tests of the previous levels plus additional processes, such as a failure analysis and a Particle Impact Noise Detection (PIND) test. In addition, these devices offer serialization and traceability to a single wafer lot.

For non–hermetic encapsulated devices, three quality levels are provided by the specification, identified by the common JANP mark plus additional TX or TXV modifiers, as applicable. JANP, JANPTX and JANPTXV require similar lot acceptance testing and requirements of the JAN/JANTX/JANTXV devices, respectively.

For unencapsulated semiconductor devices (die), two quality levels are provided differentiated by the labels JANHC and JANKC. The suffixes 'HC' and 'KC' reflect similar quality levels to those of JANTXV and JANS levels, respectively.

Regarding radiation tests, they are only prescribed for JANTXV, JANS, JANTPTX, JANHC and JANKC devices, which are the only ones that may qualify for Radiation Hardness Assurance (RHA) [73]. Testing procedures are in accordance with test methods number 1017, 1019, 1080 and 3478 from the MIL–STD–750 specifications. For radiation-hardened devices, eleven additional designations differentiated by the suffixes 'E', 'K', 'U', 'M', 'D', 'P', 'L', 'R', 'F', 'G' and 'H' are provided to indicate their RHA level. The designators specifically indicate the TID to which the devices have been subjected following Test Method 1019. Letters 'E', 'K' and 'U' refer to low dose rate levels and indicate a TID of $3{\cdot}10^4$ rad(Si), $5{\cdot}10^4$ rad(Si), and $1{\cdot}10^5$ rad(Si), respectively. Letters 'M' to 'H' refer to high dose rate levels, with 'M' indicating the lowest TID ($3{\cdot}10^3$ rad(Si)) and 'H' indicating the highest ($1{\cdot}10^6$ rad(Si)).

C. MIL–STD–882 – 1

The test methods described by the MIL–STD–883–1 standard apply to microcircuits, microcircuit arrays, and the individual elements of which circuits and arrays are made of. While MIL–STD–750 applied to generic EEE parts for military applications, MIL–STD–883 is a more specific standard targeted at microelectronic components. When these parts are involved, MIL–STD–883 is often considered more rigorous than MIL–STD–750, because of its more detailed and focused testing requirements and procedures [74]. The test procedure for method 1019.9 is reported in Fig. 10.

1) METHOD 1017.3 – NEUTRON IRRADIATION

This test aims to determine the NIEL degradation of semiconductor devices caused by neutron irradiation. In addition to microcircuits, this test is also applicable to transistors and diodes. The test procedure is equivalent to that described in MIL–STD–750–1A, Method 1017.1, with only a few minor differences. In this case, the employed neutron source shall produce a broad energy spectrum, through either a TRIGA reactor or a Fast Burst reactor, or a monoenergetic spectrum.

As this test focuses on the NIEL effects, some measures shall be taken to avoid generating TID effects. The amount of ionizing radiation produced by the neutron source per unit of neutron fluence shall be determined before the test and shall not be higher than 500 rad(Si) per $1{\cdot}10^{12}$ n/cm^3. The neutron fluence associated with the radiation source shall not cause the devices to receive a TID more than 10% of its rated value. If necessary, shielding may be used to reduce the TID exposure.

2) METHOD 1019.9 – IONIZING RADIATION

The purpose of Method 1019.9 is to evaluate the degradation of critical electrical parameters in packaged semiconductor integrated circuits exposed to ionizing radiation. As for Method 1019.5 in MIL–STD–750–1A, the radiation source shall be a ^{60}Co gamma ray and the devices shall be enclosed in a Pb/Al container during irradiation.

Two different procedures can be distinguished depending on whether the device–under–test belongs to one of these classes: 1) MOS and digital bipolar devices, or 2) bipolar (or BiCMOS) linear or mixed–signal devices. In the first case, the testing procedure is the same as that described by Method 1019.5 in MIL–STD–750–1A (see Fig. 9), with only minor changes. For example, all devices intended for cryogenic temperature applications shall be irradiated and characterized at cryogenic temperature.

A different procedure shall be followed for bipolar or BiCMOS devices, whose flow chart is illustrated in Fig. 10. A specific testing is required in this case for parts that can be affected by ELDRS effects, which cannot be simulated through the same tests designed for MOS parts. If a part is not known whether it is ELDRS susceptible, it shall be subjected to an ELDRS characterization test (see [75] for more details). Devices that do not contain bipolar transistors or linear circuit functions, or have been demonstrated not to exhibit concerning ELDRS effects via the characterization test, can be tested following the standard test conditions described in Method 1019.5 in MIL–STD–750–1A (i.e., irradiation at 50–300 rad(Si)/s and electrical tests at room temperature, without post–irradiation annealing test). All devices not meeting the previous criteria shall be tested according to one of the following conditions: 1) standard test conditions using a prescribed dose rate agreed by the involved parties; 2) standard test conditions using a dose rate < 10 mrad(Si)/s and applying an over test factor of 1.5 to the radiation level, i.e. the device shall be irradiated with a radiation level 1.5 times the specification dose; 3) accelerated test conditions. This test may be performed according to one of the following methods: a) a room temperature irradiation at a dose rate > 10 mrad(Si)/s, b) an elevated temperature irradiation, c) combinations of high dose rate tests and elevated temperature anneals, d) switched dose rates, or e) other. In any case, the test requires the application of additional parameters, such as an overtest factor, whose values shall be determined before the test following a detailed characterization test.

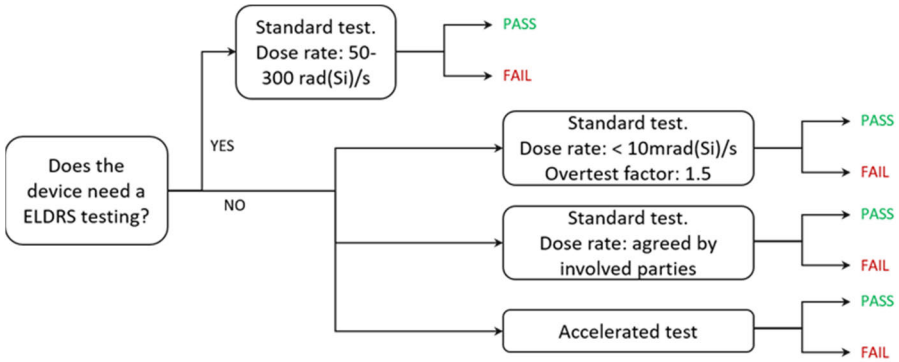

FIGURE 10. Test method 1019.9 from MIL–STD–883–1.

D. ESCC 22900 – TOTAL DOSE STEADY–STATE IRRADIATION TEST METHOD

The ESCC 22900 standard defines the testing requirements and procedures to simulate TID effects on integrated circuits and discrete semiconductors. The specification provides two distinct test sequences for whether the test objective is the technology evaluation or the qualification and lot acceptance of the devices under consideration. The former is used to assess the radiation–induced effects on the devices, while the latter aims to determine the devices' tolerance to radiation. In each case, a steady-state ^{60}Co gamma-ray source or an electron accelerator beam is required as the radiation source.

For technology evaluation testing, the procedure starts with the selection and serialization of a minimum of 20 sample devices taken from a minimum of two different wafer lots. Electrical tests at room temperature are performed before irradiation to record the pre-exposure levels of critical electrical parameters. An irradiation step follows, characterized by a minimum of five exposures to increasing radiation dose, until the prescribed dose is reached, or a functional failure occurs. The total radiation dose, the dose rate level, the device bias conditions, the electrical parameters of interest and their allowable post-irradiation limits must be specified in a Test Plan before the test. Testing conditions shall include both biased and unbiased devices. Subsequent exposures shall be performed less than 2 hours apart and electrical characterization should be performed within 1 hour after each exposure. The radiation source is then shut down for the next 168 hours, called the annealing step, to examine the device response in the absence of radiation. The final stage involves baking the devices at $+100 \pm 5$°C for another 168 hours and performing final electrical measurements. This last stage is considered destructive for the devices.

Regarding dose rate, the specification provides two possible windows to choose from: a) *Standard Rate*, ranging from 0.36 to 180 krad(Si)/hour, and b) *Low Rate*, ranging from 36 to 360 rad(Si)/hour. The latter should be used when time dependent or ELDRS effects might be relevant to the devices under test. These cases apply, for example, to devices containing generic MOS elements or bipolar transistors.

The testing sequence for qualification and lot acceptance is like that for technology evaluation, with some differences mainly in the irradiation phase. Each device shall be exposed to a minimum of three different radiation doses of increasing intensity, as detailed in the specification. As an example, if the prescribed TID is 50 krad(Si), the specification requires the device to be irradiated consecutively with 25 krad(Si), 50 krad(Si) and 75 krad(Si). Whenever a device fails the post–irradiation electrical test, its corresponding lot is rejected.

For standard temperature tests, the temperature range shall be 20°C ± 10°C.

E. ESCC 25100 – SINGLE EVENT EFFECTS TEST METHOD AND GUIDELINES

The ESCC 25100 standard defines requirements and procedures for testing integrated circuits and discrete semiconductors under HZE and proton irradiation. The objective is to evaluate the sensitivity of the devices under test to a wide range of SEE effects, such as SEL, SEU, SEGR, and others. For non–destructive tests (e.g., SEU, SEFI, SET), a minimum sample size of two is required, while at least three devices shall be used for destructive tests (e.g., SEL, SEGR, SEB). However, more pieces should be used for the statistical determination of failure events. The radiation source shall be a particle accelerator. For HI testing, the use of a vacuum chamber is suggested unless the accelerator allows extraction of the beam in air.

The test involves irradiating the devices according to prescribed particle fluence and energy and performing post–exposure electrical tests to assess the number of SEE events occurred. The ion specie and charge state, its energy and, for HIs only, its LET must be described in a Test Plan before all activities. Test equipment and electrical measurements depend on the specific SEEs under investigation. For example, for SEB and SEGR test of power MOSFETs, test hardware and software shall be designed in accordance with Test Method 1080 from MIL–STD–750 specification. Device

test conditions and particle beam properties should also be selected according to the SEE of interest. In general, all conditions are established to ensure worst–case device response.

A device susceptibility to a particular SEE is determined by evaluating the cross–section σ, namely the ratio between the number of events occurred and the particle fluence. For HI testing only, the beam might be tilted of an angle θ with respect to the normal to the device surface. In this case, the calculation of the cross–section shall consider the effective fluence as follows σ = number of events / effective fluence = number of events / (fluence·cos(θ)). Tested devices shall be equipped with dosimeters to constantly monitor the flux and measure the fluence throughout the tests.

F. JESD57 - STANDARD

JEDEC Standard No. 57A is a guideline document that establishes requirements for conducting HI ($Z > 1$) SEE tests in analog and/or digital discrete semiconductor devices and integrated circuits. This method is specifically designed for use with Van de Graaff or cyclotron accelerators, which provide a continuous beam of particles ideal for SEE testing. Sealed radioactive sources, despite offering continuous irradiation, are excluded as well due to their inability to provide the level of controlled and directed beam delivery that particle accelerators offer.

The document outlines three distinct procedures aimed at evaluating different aspects of a device's response to SEEs: collecting data for SEE cross-section curves, determining the safe operation areas for SEGR and SEB, and characterizing SET in analog and digital circuits. Before conducting these tests, some preparatory steps are described that can be divided into three phases, including performing beam dosimetry, detailing a test plan and part preparation.

The first phase involves measuring the energy and purity of the beam, especially if not known a priori. The beam should consist solely of one ion species, with a tight energy distribution. The usage of a surface barrier detector is prescribed for these assessments, with additional details provided in the document. The standard advises ensuring that the beam's energy conforms to within 10% of the targeted level and the impurity level is maintained below 1%.

The test plan should detail the device information, ensure a large and uniform sample size, and describe the comprehensive test setup including the equipment and capabilities for various SEE types. It should specify test conditions in a matrix format, covering device operation, program parameters, and beam characteristics like incidence angles. Tests shall be performed under application–specific conditions or worst-case conditions for the device type, which should be articulated in the test plan. Some guidelines are provided to establish worst-case operating conditions, however, it is recommended to ascertain the failure modes for each device type due to possible competing mechanisms. The plan shall establish a flux range to isolate single ion effects and determine particle fluence levels to confidently assess all sensitive areas for rare event likelihood. As suggested, a typical ion flux range is $1{\cdot}10^3$ ions/cm^2 to $1{\cdot}10^5$ ions/cm^2, while a fluence value that resulted historically adequate is $1{\cdot}10^7$ ions/cm^2.

The objective of the part preparation is to make sure that the beam will reach the sensitive part of the DUT. Devices must be decapsulated to allow beam access unless specific coatings are used for protection, which must be characterized to ensure they do not affect the test. The electrical performance of the DUT should be verified both before and after decapsulation. If the device is flip–chip packaged or has extensive metallization, die thinning may be necessary to ensure uniform ion penetration for reliable SEE testing. Finally, validation of the entire test setup, including checks on all software, hardware, fixtures, and interfaces to ensure accurate data capture and prevent mechanical stress or interference during the test setup.

Following the pretest activities, irradiation can be performed. As anticipated, three radiation tests are described in the standard, aiming at characterizing different aspects of the device's response to SEEs. In particular, for the collection of SEE cross-section curve data, the operating conditions of the DUT should be kept steady while modifying the beam conditions to gather data on SEE cross-section versus LET. The standard suggests acquiring at least six data points to facilitate a Weibull distribution fit, with particular attention to gathering data up to double the LET necessary for cross-section saturation, or a minimum of 80 MeV·cm^2/mg. The standard includes additional options for follow–on tests depending on whether SEEs are initially detected or not. These involve varying flux, angle, and operational parameters in the former case, or increasing fluence and varying conditions in the latter case. For SEGR/SEB safe operation data collection, the operating conditions of the DUT should be varied against a constant beam setting, to determine the SEGR/SEB susceptibility.

The bias voltage and stress conditions should be systematically modified to outline the DUT's operational limits, complemented by post-exposure evaluations to ensure device integrity. Adequate data collection across different bias levels should be ensured to define failure threshold curves, and the DUT operation should be monitored during irradiation to verify performance and note any degradation or failure. For SET characterization in analog circuits, device conditions need to be maintained constants while varying beam characteristics, or vice versa, to categorize and plot SET signatures. It is recommended to capture about 100 pulses to define SET response envelopes and construct a cross-section versus LET curve for rate determination. The process should be repeated across various samples and conditions outlined in the test plan, adjusting the testing environment to prevent pulse overlap and to collect a substantial number of events for a robust analysis.

As for the other standards, the document ends with instructions for creating a final report. This should include all test data, descriptions of the products tested, details of the test setup and methods, a summary of the results, and the conclusions reached from the tests.

G. JESD234 - STANDARD

Similarly to the JESD57A standard, JESD234 covers procedures for SEE testing of electronic devices. The difference is in the radiation source addressed, which here is the moderate energy protons, specifically in the range of 40 to 500 MeV. Although protons are capable of causing SEEs through both direct and indirect ionization, the latter is the predominant mechanism at this energy range. This allows close replicating of the conditions experienced by semiconductors in space, where proton–induced SEEs are mainly caused by nuclear reaction byproducts rather than direct proton ionization. It is noted that irradiation across the whole energy spectrum is discretionary, contingent on the expected environmental conditions for the specific space application.

The prescribed test facility is a proton accelerator capable of delivering energies within 40–500 MeV. The standard primarily covers SEU, SET, SEFI, and SEL tests, for which the end goal is a graph of the cross-section versus proton energy. Instead, for SEB and SEGR effects, the document suggests referring to the procedure reported by MIL–STD–750, TM 1080, whose objective is to establish the safe operational limits of the device.

As noted by the standard, unwanted TID and DD effects can interfere with the proton irradiation of SEEs. For example, SEU occurrence in some devices exhibits a dependence on the total dose absorbed. This can be accounted for by using the maximum system total dose level as the worst-case condition for the SEU sensitivity test. Although possible DD effects are acknowledged, no specific guidance is given to account for them during testing. For SEU testing, proton energies above 200 MeV are usually not necessary due to their rarity in space. Instead, for SEL testing, where even a small cross-section is unacceptable, energies between 40–500 MeV might be required. Direct ionization is noted to occur at energies below 5 MeV, but evidence suggests significant effects at up to 25 MeV at certain angles. If data shows an increase in cross-section with decreasing proton energy, further analysis is needed to understand the implications for technology. However, testing at such low-energy levels is not accounted for in this standard.

The document outlines pretest activities, including beam dosimetry and part preparation, with similar requirements as those found in the JESD57A standard, such as achieving a $\pm 10\%$ beam uniformity. However, a few key differences are found in the methods. Instead of a surface barrier detector, dosimetry systems for measuring proton beam characteristics are typically provided by the accelerator's facility. The mentioned possibilities are scintillators, secondary electron monitors, and Faraday cups for determining beam energy, flux, and uniformity. The beam's energy is primarily set by the machine's tune, but degraders can be inserted to spread the energy to achieve a specific range necessary for testing. The recommended proton flux is between 10^5 and 10^9 protons/cm^2·s. Selecting the total fluence must trade-off the need to ensure that all sensitive areas of the DUT receive adequate exposure against the device's tolerance to TID to prevent damage. Generally, a target of at least 100 significant events is aimed for to draw confident conclusions, although this may not be feasible for rare event occurrences. Since protons are very penetrating, test samples usually do not need to be decided, as opposed to HI testing. Moreover, DUT are tested in open air, as vacuum testing is typically used for energies < 10 MeV. Concerning the sample size, a minimum of five devices is advised for homogeneous lots, such as those from a single wafer, to ensure statistical reliability. When dealing with non–homogeneous lots with parts coming from various production runs, the number of test samples should be increased to ensure adequate diversity representation across the lot.

For the destructive tests involving latch-up, burnout, and SEFI, the process involves setting the DUT in the fixture under maximum supply and temperature conditions, then beginning proton exposure while monitoring for SEL rates to match testing capabilities. The goal is to expose the DUT until a specific number of latch events are observed or a maximum fluence, specified as 10^{10} protons/cm^2, is reached. If destructive events occur, options include adjusting flux or beam angles to continue testing without damaging the equipment or the DUT. If no events are detected, various parameters like fluence, supply voltage, or operating conditions may be modified to induce events, including testing at different angles or selecting a higher energy level.

For non–destructive tests focusing on upsets and transients, the DUT should be placed in its fixture and set to minimum supply levels at room temperature. After verifying the DUT operation, proton exposure can be initiated, aiming for an error rate as specified in the test plan. The test continues until reaching either the set number of errors or the maximum fluence, typically aiming for at least 100 upsets or a fluence of 10^{10} protons/cm^2. The test conditions should be adjusted based on initial outcomes, and involve varying the flux, beam angle, operating parameters, or temperature.

The test finally foresees writing a final report summarizing test results.

V. RADIATION EFFECTS ON COTS DEVICES

This section includes six subsections, each of which is devoted to a particular classification of devices, such as diodes, BJTs, FETs, OPAMPs, memory modules, and FPGAs. Each subsection begins with an introduction on the device type, highlighting its main applications in space missions, before delving into a comprehensive review and discussion of test outcomes. These tests draw from radiation experiments performed by NASA's Radiation Effects & Analysis Group and Space Radiation Physics Office [76], as well as data sourced from the ESA Radiation Test Database [77], spanning the period from 2017 to the present. This temporal range encompasses reported findings of notable significance within the literature. The outcomes of these tests are reported in the Supplementary Material, where they are organized into

separate tables associated with different device types. For each device, two tables are provided: one reporting results for immediate effects of radiation (SEE tests) and the other for accumulated dose effects (TID/DD), as their test procedures differ significantly. Moreover, a table listing all devices involved in the tests is supplied, along with relevant information such as part types and electrical characteristics. The main goal is to provide an accessible and comprehensive repository that can practically help in the decision-making process of designing electronic systems for space applications. Therefore, it is intended as a resource for engineers and mission planners, allowing them to make well-informed decisions on the utilization of COTS devices in space. The SEE tests include experiments using HI, with the specific ion type noted where data is available. Additionally, tests have been conducted using protons (p^+), electrons (e^-), and laser–induced stimulations to replicate the effects of high–energy particles. For TID and DD effects, tests are categorized based on both radiation type, including gamma rays (γ), protons, and neutrons (n_0), and dose rate, distinguishing between High Dose Rate (HDR) and Low Dose Rate (LDR) conditions. Testing facilities are situated both in the United States and in Europe. U.S. facilities include: the Texas A&M University (TAMU) [78], the Lawrence Berkeley National Laboratory (LBNL) [79], the Brookhaven National Laboratory's NASA Space Radiation Laboratory (NSRL) [80], the University of California at Davis Crocker Nuclear Laboratory (UCDCNL) [81], the Ohio State University Nuclear Reactor Laboratory (OSU) [82], the Naval Research Laboratory (NRL) [83], the Massachusetts General Francis H. Burr Proton Therapy (MGH) [84], the Provision Center for Proton Therapy (PROV) [85], and NASA's Goddard Space Flight Center (GSFC) [15]. In Europe, tests have been conducted at the Université Catholique de Louvain (UCL) in Belgium [86], the JÜLICH Injector Cyclotron (JULIC) in Germany [87], the Grand Accélérateur National d'Ions Lourds (GANIL) in France [88], the CERN Super–Proton–Synchrotron North Area (SPS–NA) [89], [90], the CERN H8 beam line (H8) [91], [92], which straddles the Franco–Swiss border, ESTEC's ^{60}Co Facility in the Netherlands (ESTEC) [93], the ^{60}Co gamma irradiators at Fraunhofer INT (TK100, TK1000A, TK1000B) [94], the GSI Helmholtz Centre for Heavy Ion Research (GSI) [95], the ^{60}Co facility at Physikalisch–Technische Bundesanstalt (PTB) in Germany [96], the TRAD's ^{60}Co source in France (GAMRAY) [97], the cyclotron facility at the University of Jyväskylä (RADEF) in Finland [98], the PROSCAN project at the Paul Scherrer Institute (PIF) in Switzerland [99], and the ALTER's ^{60}Co irradiator (RADLAB) in Spain [100].

A. DIODES

Diodes play a critical role in various subsystems of space systems, offering essential functionalities for the overall reliability and performance of spacecraft. One of the primary functions of diodes in space systems is as rectifiers in power supply circuits. Diodes are used to convert alternating current (AC) to direct current (DC), ensuring a stable and consistent power supply to vital components such as communication systems, guidance systems, and scientific instruments onboard spacecraft. Additionally, diodes serve as protection devices against reverse current flow, overvoltage, and voltage spikes. In this capacity, they protect sensitive electronic components from potential damage due to transient events such as solar flares, electromagnetic interference, or radiation–induced glitches. Moreover, diodes are integral components in temperature sensing and control systems. By exploiting the temperature–dependent characteristics of diodes, engineers can accurately measure and regulate the thermal conditions within spacecraft, mitigating the risk of overheating or temperature fluctuations that could compromise the mission objectives. Furthermore, diodes find application in signal conditioning and filtering circuits, where they facilitate the manipulation and conditioning of analog and digital signals for data transmission, processing, and control purposes. In addition to their fundamental roles in power supply, protection, temperature sensing, and signal conditioning, diodes are extensively utilized in various specialized subsystems within space systems. For instance, they are crucial components in radiation monitoring and mitigation systems. Specifically, diodes are employed in radiation monitoring circuits to detect and quantify the intensity of radiation exposure that spacecraft experience in space, providing valuable data for assessing the health and longevity of critical components. Furthermore, diodes are integral to propulsion systems, where they serve in pulse–forming networks for generating precise timing signals required for the controlled ignition of thrusters or the deployment of solar sails. Moreover, diodes are employed in telemetry and telecommand subsystems for data transmission between spacecraft and ground stations. They enable the modulation, demodulation, and encoding of telemetry data, ensuring reliable communication links over vast distances in the harsh space environment. Additionally, diodes play a role in attitude control systems, aiding in the precise orientation and stabilization of spacecraft by providing accurate reference voltages for attitude sensors and actuators.

Among the various types of diodes utilized in space applications, silicon diodes stand out for their extensive usage in rectifying AC to DC power, as well as in clipping and clamping circuits, reverse current protection, logic gates, and voltage multiplication. In early space missions, Si–diodes were chosen for their ability to achieve medium–high dropout voltages (< 1 V) and handle small currents (hundreds of mA) in standard configurations. Schottky diodes, with very low dropout voltages (< 0.5 V), were favoured for reverse protection and rectification tasks. Zener diodes were relied upon for their stable high reverse breakdown voltages, serving as voltage references and limiters. Switching diodes, known for their high–frequency operation, found applications in several circuits. Due to their extensive use in space missions, significant literature addresses the radiation hardness of Si–diodes. Theoretical studies on silicon p-n diodes have revealed that

low doses of carbon ion radiation increase forward current due to damage, whereas high doses reduce forward current, attributed to charge compensation and the development of a partially depleted intrinsic junction region [101]. Moreover, radiation causes a substantial reduction in minority carrier lifetime and diffusion length within Si–based power diodes, resulting in increased forward voltage [102]. Radiation type, fluence, and energy strongly influence these outcomes. Low-energy protons (fluence of $1.45{\cdot}10^{14}$ cm^{-2}) lead to the complete degradation of silicon power diodes, similar to the effects of much higher γ–ray fluences ($4.25{\cdot}10^{20}$ cm^{-2}). Experiments have shown that electron and neutron radiations are less harmful than protons and γ–rays [102], although with some vulnerability, such as the case of the Infineon^{TM} BAR64–05 E6327 RF PIN diode [103]. In summary, in terms of fluence, diode failure typically occurs around $1{\cdot}10^{14}$ cm^{-2} for 1 MeV protons, roughly $1{\cdot}10^{17}$ cm^{-2} for 100 MeV protons, and over $1{\cdot}10^{20}$ cm^{-2} for γ–rays [104]. Another radiation–induced effect in Si–diodes is the creation of recombination centers in the silicon, which shortens minority carrier lifetime and creates deep–level traps in the bandgap. This contributes to carrier recombination and thermal electron–hole pair generation, leading in turn to an increase in diode leakage current under reverse bias conditions [105]. Structural changes can be observed by using high neutron fluences ($> 10^{13}$ n_0/cm^2), which cause unique conduction mechanisms when combined with very low operating temperatures (< 20 K). Finally, the freeze–out of carriers results in a sharp increase in the forward turn–on voltage, reaching over 400 V from approximately 1.1 V (for a non–irradiated diode) at a neutron fluence of $5.9{\cdot}10^{14}$ n_0/cm^2.

Besides silicon, alternative materials have been investigated to enhance radiation robustness. Diodes based on 4H–SiC displays excellent stability against γ–radiation doses up to 1 Mrad(Si), although with increased interface charge impacting reliability [106]. Similarly, experimental TID tests on SiC Schottky rectifiers (such as Wolfspeed^{TM} C4D40120D and Semelab^{TM} SML020DH12) demonstrated their outstanding radiation tolerance – exceeding 1 Mrad(Si) – with minimal impacts on forward voltage and only moderate increases in leakage current [107], [108].

GaAs Schottky diodes have also been investigated due to their remarkable robustness against various radiation types, including proton, neutron, and gamma radiation. This resilience stems from the inherent properties of GaAs, a compound semiconductor known for its high electron mobility and radiation tolerance. GaAs Schottky diodes are relatively resistant to proton radiation damage due to the strong covalent bonds within the crystal lattice, which helps mitigate the creation of defect states. GaAs Schottky diodes maintain their integrity well against neutron radiation due to the material's high atomic number and the absence of neutron–capture isotopes. Nevertheless, GaAs Schottky diodes are known for their resilience to gamma radiation owing to the efficient recombination of radiation–induced defects and the superior charge transport properties of the material [109].

Radiation tests data collected from the literature are summarized in Tab. S1–S3 of the Supplementary Material, revealing distinct trends in diode performance under radiation exposure. In terms of TID effects, SiC Schottky rectifiers, such as Wolfspeed^{TM} C4D40120D and Semelab^{TM} SML020DH12, demonstrate excellent tolerance exceeding 1 Mrad(Si). Notably, Wolfspeed^{TM} C4D40120D SiC Schottky diode maintains a consistent forward voltage of around 1.65V even when irradiated with up to 1 Mrad(Si) under both biased and unbiased conditions. The reverse leakage current experiences moderate increases, rising from an initial 0.4 μA to around 60 μA for biased samples at 1 Mrad(Si), and to a lesser extent (15 μA) for unbiased samples. Slight recovery occurs after 168 hours of 100 °C annealing [107]. The Semelab^{TM} SML020DH12 exhibits similar resilience, with less than a 1% increase in forward voltage and less than one order of magnitude rise in reverse leakage current after 1 Mrad(Si) [108]. Importantly, these SiC Schottky diodes show saturation in radiation–induced defect generation and no continued annealing effects, highlighting their robustness for TID exceeding mega–rad levels.

In contrast, SEE testing reveals vulnerabilities in certain diode types. While many devices exhibit no SEE occurrence, including high–speed switching diodes such as the onsemi^{TM} MMBD1501A and the NXP^{TM} BAS16,215, as well as some Schottky types like the onsemi^{TM} NSR0140P2T5G, others degrade during testing, such as the Infineon^{TM} BAR64–05 E6327 RF PIN diode [103]. This indicates varying levels of susceptibility and highlights the need for protective measures. SEE testing on SiC Schottky diodes like the CREE^{TM} C4D40120D suggests high radiation vulnerability, particularly at higher LET values, with failures occurring far below rated voltage levels. Discrepancies in radiation tolerance are observed across test facilities and manufacturing lots [110]. Remarkably high failure cross–sections are documented, such as with the Semelab^{TM} SML020DH12 under chromium ion irradiation [111].

Additional SEE testing on other diode types including the Infineon^{TM} HFB16HY20CC, NXP^{TM} BAS70–05–7–F, onsemi^{TM} NSR0140P2T5G, has demonstrated strong resilience, with no catastrophic failures or parametric degradation up to maximum LET levels [103]. However, some exceptions remain: while Zener diodes such as the BZX84 series from NXP^{TM} experiences degradation when biased at 100% Zener voltage, their parameters remain within specification following irradiation [112].

In summary, test outcomes for diodes reveal a broad spectrum of susceptibility influenced by factors like material and architectural design. Still, it is possible to identify components that are more suitable for applications in the space radiation environment. Regarding power rectification applications, such as power supplies and high-power converters, Wolfspeed^{TM} C4D40120D and Semelab^{TM} SML020DH12 diodes exhibit minimal changes in forward voltage and moderate increases in reverse leakage current under 1 Mrad(Si) TID conditions. For protection from reverse

current, overvoltage, and voltage spikes, it must be considered that the onsemi™ NSR0140P2T5G demonstrated no catastrophic failures or parametric degradation up to maximum LET levels in SEE testing, while the NXP™ BZX84 Series, although it experiences degradation when biased at 100% Zener voltage, it remains within specification following irradiation. For high-frequency operations, such as signal conditioning and filtering circuits, onsemi™ MMBD1501A and NXP™ BAS16,215 diodes exhibits strong resilience with no SEE occurrence. However, rigorous testing is critical for quantifying failure thresholds and understanding safe operational conditions within radioactive environments. Because of such performance variability, it is essential to extensively qualify parts intended for high–radiation usage.

B. BJTs AND HBTs

Bipolar Junction Transistors (BJTs) serve as key components for various spacecraft subsystems. In communication subsystems, BJTs play a critical role in RF transmitters and receivers, enabling the amplification of weak signals received from distant spacecraft or ground stations and ensuring reliable data transmission across vast interstellar distances. Their high–frequency performance and low noise characteristics make them ideal for amplifying signals in both uplink and downlink communications, facilitating command and telemetry operations essential for spacecraft control and monitoring. A NewSpace application of commercial BJTs involves their use as Low-Noise Amplifiers (LNAs) in the implementation of space-aerial-terrestrial integrated 5G networks. Since LNAs are positioned at the front end of receiver systems, evaluating their radiation tolerance levels is crucial to ensure reliable RF links [113].

BJTs are also extensively employed in satellites' power management subsystems. Their ability to handle high–power levels efficiently makes them well-suited for voltage regulation, power distribution, and energy conversion tasks. They are commonly utilized in power converters, voltage regulators, and battery charge controllers, ensuring the optimal utilization of energy resources onboard spacecraft and maintaining stable power supplies for critical systems and payloads. Additionally, BJTs contribute to the fault protection mechanisms of power distribution systems, safeguarding sensitive electronic components from overcurrent and overvoltage conditions that may arise during spacecraft operations.

In navigation and guidance subsystems, BJTs find application in precision control circuits and attitude determination systems. These transistors facilitate the implementation of feedback control algorithms for spacecraft stabilization, trajectory correction maneuvers, and orientation control. By modulating thruster-firing sequences or adjusting solar panel orientations, BJTs assist in maintaining the desired attitude and trajectory of spacecraft, enabling precise navigation and alignment with target destinations or orbital parameters. Their reliability and radiation tolerance are particularly advantageous in this context, where uninterrupted operation is essential for mission success.

BJTs are also integral to the data processing and computing subsystems of spacecraft, often referred to as Command and Data Handling (C&DH). Within onboard computers and digital signal processors, BJTs are utilized in logic gates, memory circuits, and arithmetic units, enabling real–time data processing, scientific computations, and autonomous decision–making capabilities. Their high–speed operation and low power consumption are essential for executing complex algorithms, image processing tasks, and sensor data fusion operations onboard spacecraft, supporting a wide range of scientific experiments, remote sensing applications, and Earth observation missions.

HBTs, on the other hand, are a variant of BJTs that uses differing semiconductor materials for the emitter and base regions, creating a heterojunction. This allows for improved performance over BJTs, including higher speed and efficiency, due to better electron mobility and energy band alignment. HBTs are particularly useful in high–frequency applications, such as RF and microwave circuits, where they offer superior performance in terms of speed and power efficiency compared to traditional BJTs. For these reasons, there has been a shift towards using HBTs in space applications, driven by the need for higher performance in terms of speed and efficiency. HBTs, especially those based on compound semiconductors like GaAs or nP, can operate at much higher frequencies than silicon–based BJTs.

Concerning radiation–induced effects, DD in bipolar devices typically results in an increased recombination rate of minority carriers, which consequently shortens their lifetime. This reduction in minority–carrier lifetime causes a decreased device gain. It should be noted that the degradation of gain in bipolar devices can be attributed to both ionizing effects and DD. Generally, p-n-p devices exhibit a greater sensitivity to DD compared to n-p-n devices. Moreover, the utilization of low–power devices that can handle high collector currents is advisable to mitigate such degradation. The impact of degradation observed in discrete bipolar devices is equally applicable to bipolar integrated circuits, such as comparators, OPAMPs, and voltage regulators.

The decrease in current gain is the main harmful effect of the radiation on the BJTs. This effect is strictly correlated to the trapping of charges at the Si/SiO_2 base interface, with a resulting increase of the base current and then a decrease of the gain. As reported in [114], the base current increases as the TID increases, with an increment in the surface state generation–recombination current and a resulting decrease of the lifetime of the minority charges and then the collector current. In particular, the generation current matches with recombination within the base–emitter junction in the absence of radiation. The radiation leads to an imbalance of the two velocities, due to the charges trapping on, or near, the surfaces of insulating layers, with a resulting decrease of recombination velocity and the surface potential at the $Si - SiO_2$ interfaces. The gain degradation dispersions, which

vary with the collector–emitter breakdown voltage, are larger for low-bias current levels. This effect is emphasized for small dose rate values ($<$ 1 rad/s), caused by the space–charge effect in the oxide. It produces a higher oxide-trapped charge density at a low dose rate, also with the formation of interface traps, determining the high susceptibility of the BJTs to radiations at low dose rates [70]. The susceptibility to low dose rates is expressed as Low Dose Rate Enhancement Factor (LDR EF). The n-p-n BJT shows considerably higher mean LDRs than the p-n-p counterpart, which is due to their different polarity. In particular, in the p-n-p BJT, the positive charges induced by the radiation in the oxide extend the surface depletion region at the emitter. However, the emitter is heavily doped and only a small change in the depletion layer arises. On the other hand, the depletion layer in the n-p-n device can spread significantly within the low–doped base. This effect combined with the interface traps leads to a large degradation in n-p-n transistors.

The hardness of BJTs to HIs irradiation as SEEs test is difficult to estimate. HIs cause defects in the silicon base, but since most BJTs are large devices, spanning up to 1 m^2 in surface area with a base thickness of several μm, the number of introduced defects is much smaller than the number of atoms present, rendering negligible the generated recombination (leakage) current. Titus et al. [115] first demonstrated SEB effects in BJTs in devices with a lightly doped epitaxial configuration, enabling the avalanche mechanism characteristic of SEB. They measured SEB voltage thresholds below the breakdown voltage, with collector–emitter and base open. To mitigate SEB effects, strategies such as employing narrow stripes and increasing base doping have been proposed to improve SEB burnout performance while lowering the base–emitter voltage drop. As can be seen from Tab. S4–S5 of the Supplementary Material, the n-p-n power transistor Microchip^{TM} 2N5154U3 exhibits considerable gain degradation at a dose rate of 50 mrad/s when biased at 80 V [116]. This is indicative of the impact radiation can have on devices designed to handle higher power levels. Conversely, the p-n-p signal transistor 2N2907AUB from the same manufacturer also experiences gain degradation, but at a lower dose rate of 10 mrad/s, highlighting the variation in radiation sensitivity across different types of BJTs [117].

Interestingly, general–purpose n-p-n transistors such as the 2N2222AUB and 2N2369A from Microchip^{TM}, demonstrate minimal LDR sensitivity despite their broad operational ranges, suggesting a certain resilience in standard applications [116]. This behaviour contrasts with power BJTs like the Semelab^{TM} BUL54A, which displays both gain degradation and breakdown voltage reduction at HDR conditions, emphasizing the need for careful consideration when employing these components in radiation environments [118].

Data also reveals that power BJTs, particularly p-n-p types such as the Microsemi^{TM} 2N7371, show no effects under specific LDR conditions [119]. This suggests that, with proper management, these devices can maintain their performance characteristics in certain radiation environments. However, the gain reduction, particularly evident at lower collector currents in HDR conditions for devices such as the Infineon^{TM} BC817K, signifies that even signal BJTs are susceptible to the cumulative effects of radiation [120].

During the last decades, SiGe HBTs have generated significant interest in the space community for their superior radiation tolerance compared to traditional silicon–based transistors, as well as for their aforementioned high–speed, high integration levels within BiCMOS platforms, and cost–effectiveness. This resilience is due to the presence of germanium, whose lattice arrangement helps to reduce the impact of radiation–induced defects. n-p-n HBTs in the 250 nm CMOS platform and dual–gate versions in the 130 nm CMOS platform (7HP and 8HP, 2nd and 3rd generation) have been widely investigated by ESA for new Space missions starting in 2021. SiGe HBTs exhibit classical bipolar TID damage, as the increase in off–state input (base) current, which is attributed to the creation of generation/recombination traps along the emitter–base spacer oxide interface. SiGe HBTs have demonstrated the ability to withstand radiation doses ranging from hundreds of krad to several Mrad without experiencing failure. Specifically, they maintain satisfactory performance even when exposed to a total γ–radiation dose of tens Mrads(Si), however significant damage is observed at 50 Mrads(Si).

The TID response of high-voltage SiGe HBTs from five different technologies (0.35 to 0.13 μm nodes) has been investigated in [50], showing wide variability in threshold voltage shifts correlated with gate oxide thickness, while leakage currents show no systematic correlation. Despite limited V_{th} shifts at high TID, significant leakage occurs above 100 krad(Si). High particle fluence causes serious electrical degradation, with on-resistance increasing above $5{\cdot}10^{14}$ p/cm^2 and output characteristic deformations. Nonetheless, COTS components like the IHP SGB25VGOD could be suitable for various space applications. As for the 4th generation, namely 9HP BiCMOS technology, statistical analyses have been performed by considering flux rates of 50 rad(SiO_2)/s and 10 mrad(SiO_2)/s for high and low dose rates, respectively. Several devices experience a change of 15% to the base current up to 80 krad(SiO_2).

Finally, the inner structure of SiGe HBTs makes them resilient to ELDRS [121]. In particular, the incorporation of a strained SiGe alloy within an epitaxially grown base and a thin emitter–base space within the heavily doped base region results in numerous benefits to the TID exposure, such as the suppression of the current leakage correlated to Si interface traps. Unlike lateral or substrate p-n-p devices, SiGe HBTs show a vertical structure wherein carrier transport can be strongly attenuated by using shallow trench isolations. Concerning DD, several ions strongly affect gain degradation. In smaller devices, the relative number of defects is relatively higher compared to larger counterparts, causing a small increase of the current recombination that is largely

unpredictable due to its strong dependency on fabrication steps. For SEEs, a moderate 6% decrease is observed for both cutoff (f_t) and maximum (f_{max}) frequencies, well within the measurement error of the setup, while the gain (β) at the peak f_t experiences less than a 0.3% reduction with 63.3 MeV proton fluences ranging from $1{\cdot}10^{12}$ p/cm^2 to $5{\cdot}10^{13}$ p/cm^2. For the 3rd and 4th generation devices, both forward and inverse base–current leakage are significantly lower than those of previous technology nodes, where the increased radiation–induced base–current leakage had previously been attributed to the increased electric field in the emitter-base at the device periphery, and associated with the higher local doping associated with the vertical and later scaling [122]. The improved radiation tolerance of the 3rd and 4th generations is due to the ''raised extrinsic base'' configurations, resulting in emitter–base and collector–base junctions physically further removed from the shallow trench isolation edges [123]. The effective trap density near both junctions is such that there is less carrier combination and reduced variation with respect to no irradiation. For satellite applications, SiGe HBTs can be considered for LNAs in space-aerial-terrestrial integrated 5G networks and other RF applications, voltage regulation, power distribution, and energy conversion tasks, onboard computers, and digital signal processors due to their radiation tolerance, high-frequency performance, and efficiency. The Microchip^{TM} 2N2222AUB and 2N2369A, which demonstrate minimal LDR sensitivity, are suitable for general purpose applications and memory circuits in C&DH subsystems. Microsemi^{TM} 2N7371 diodes have shown resilience under harsh radiation conditions and are suitable for high-power tasks in space environments.

C. FETs

FETs are three-terminal active semiconductor components that utilize the electric field induced by an input voltage to modulate the output current. Unlike their bipolar counterparts, FETs only employ electrons or holes as charge carriers, whereby they are classified as unipolar transistors. Thanks to their compact size and low power needs, FETs find ubiquitous applications in integrated circuits. Two main FET categories are considered in this paragraph, namely junction FETs (JFETs) and metal–oxide–semiconductor FETs (MOSFETs), the latter also known as insulated gate FETs (IGFETs). Within the MOSFET classification, two main types exist – enhancement mode MOSFETs and depletion mode MOSFETs. While JFETs represent the simpler FET structure, relying on a semiconductor junction to control current flow, MOSFETs incorporate an insulated gate electrode to modulate conductivity in the underlying channel.

One of the primary applications of MOSFETs lies in power management systems, where they serve as key components in power converters and regulators. In signal processing subsystems, they enable precise amplification, filtering, and modulation of communication signals. These transistors are often integrated into RF amplifiers, transmitters, and receivers. MOSFETs also find extensive use in attitude control and propulsion systems, where they contribute to the modulation of thrust and propulsion mechanisms. In propulsion systems, MOSFETs are employed in electronic valves and motor control circuits, enabling the efficient operation of propulsion thrusters and reaction wheels.

The effects induced by radiation exposure in MOS devices originate from diverse physical mechanisms, occurring on very different timescales, with different dependences on the applied electric field and temperature. Therefore, the overall radiation response of a MOS component or circuit can be extremely intricate.

Four types of physical processes occur in MOSFETs under radiation exposure: the creation of electron–hole pairs, transport of holes through bulk SiO_2, holes trapping near the Si/SiO_2 interface, and accumulation of induced radiation at the Si/SiO_2 interface [46]. When radiation passes through the gate oxide, electron–hole pairs are created from the deposited energy, which follows the flow of the impacted particles. The creation of an electron–hole pair requires approximately 3.6 eV of energy at a temperature of 300 K in Si, whereas in SiO_2, it is roughly 17 eV. The number of electron–hole pairs is proportional to the deposited energy, resulting in an intrinsic correlation with the total damage caused by the TID. Holes trapping at the $Si–SiO_2$ interface results in both fixed oxide charge and interface traps, causing shifts in the device's parameters such as threshold voltage. V_{TH} shifts exhibit a nonlinear trend with respect to the oxide thickness, with sensitivity increasing between t_{ox} of 0.1 μm to 2.0 μm. Similarly, carrier mobility, subthreshold swing, and low–frequency noise degrade after irradiation. Post–irradiation fading effects are characterized by minimal short–term fading beyond 60 seconds and a fading time constant of approximately 1 week [124].

In SiO_2, electrons exhibit much higher mobility compared to holes, so they escape the oxide in relatively short time frames, typically within 10^{-12} s [125], [126], [127], [128]. Despite these high velocities, a fraction of electrons, depending on the incident particles' energy and type and also influenced by the strength of the electric field, recombine with the holes. The remaining uncombined holes are referred to as charge yield. Since holes remain relatively immobile and close to their point of generation, there is a negative shift in the threshold voltage V_{TH} of the MOS, which is proportional to the charge yield.

In the presence of an electric field, holes migrate toward the Si/SiO_2 interface or Si/gate interface when the MOS is polarized with a positive or negative gate voltage, respectively. This phenomenon, known as hopping transport, leads to a short–term recovery of the V_{TH}. This phase is characterized by high dispersion, occurring within a few tenths of a second and potentially lasting for decades. The hopping transport of radiation–induced holes in MOS oxides is largely affected by the applied electric field, with greater fields accelerating the transport. Temperatures above 140 K cause a thermal activation of the transport process. Differences in defect densities

depending on the oxide processing affect the hole trapping and hopping.

As the holes arrive at the interface, some of them fall into relatively deep traps. This trapping occurs because there are more lattice imperfections at the interface compared to the deeper internal zones, which leads to a negative variation in V_{TH} that can persist for hours or even years.

The last but most important response to irradiation is the trapping of induced radiation right at the Si/SiO_2 interface. The transport of hydrogen ions plays a key role in the formation of interface traps localized within the Si bandgap dependent on the Fermi level, which results in a shift of the V_{TH}. Specifically, when holes migrate into the oxide layer, they can interact with Si–H in the bulk material, resulting in the release of hydrogen ions. As previously mentioned, under positive bias voltage, these ions may reach the Si/SiO_2 interface, where they react with the Si–H bonds. This results in the formation of H_2 molecules and Si dangling bonds, namely a Si atom bonded with other three Si atoms, and an unpaired electron [129], [130]. Instead, under negative bias voltage, H^+ ions reach the Si/gate interface, where the low density of Si–H makes this scenario less critical. This differential behaviour makes the p-channel MOS more robust to the buildup of interface traps compared to n-channel MOS. Additionally, the occurrence of interface traps is strictly correlated with the temperature [131]. The rate of change in V_{TH} decreases if thermal annealing is performed. Moreover, the electric field amplifies the dispersive transport of holes in amorphous SiO_2 through a mechanism involving small polaron hopping [132]. As demonstrated in [133], the density of the interface traps depends on the oxide thickness and can be mitigated by using a thin gate oxide (thickness $\ll$ 10 nm) [134], [135].

The trapped charge in the oxide, which is always positive, is responsible for the change in the threshold voltage $\Delta V_{ot} = -q\Delta N_o/C_{ox}$, where q is the elemental charge, $C_{ox} = \varepsilon_{ox}/t_{ox}$ is the specific capacitance of the MOSFET with ε_{ox} dielectric constant and t_{ox} gate oxide thickness, and ΔN_o is the density of trapped holes in the oxide per unit area. The trapped charge at the interface depends on the type of MOSFET and can be positive, negative, or neutral, and is responsible for the variation of the threshold voltage given by $\Delta V_{it} = -\Delta Q_{it}/C_{ox}$, where ΔQ_{it} is the trapped charge at the interface. The total threshold change ΔV_{tot} is given by the sum of the two components $\Delta V_{tot} = \Delta V_{ot} + \Delta V_{it} = -(\Delta Q_{ot} + \Delta Q_{it})/C_{ox}$.

Specific radiation–induced effects have been observed and described in literature, in various types of FETs, including SiC power MOSFETs, SiC JFETs, and advanced III-V FETs. In SiC power MOSFETs, latent gate oxide damage from HIs occurs for LET $>$ $\sim$10 MeV·cm^2·mg^{-1}, even at very low drain–source voltages ($<$10% of rated breakdown voltage). This oxide damage can cause gate rupture when applying gate stress post–irradiation. Furthermore, drain–gate leakage current degradation at higher drain–source voltages is tied to a device's drain neck width, resulting in variations between parts and potential failures in post–irradiation gate stress tests. Additionally, all SiC power MOSFETs exhibit elevated drain–source leakage current at around 350–400V (irrespective of voltage ratings), resulting from damage in the p-n junction region. Catastrophic single–event burnout is observed across all SiC MOSFETs tested, occurring around 50% of rated voltage.

SiC JFETs, including three normally–off and one normally–on vertical trench, exhibited drain–gate leakage current degradation during exposure to argon ions with 11 MeV·cm^2·mg^{-1} LET. One JFET experienced non–catastrophic drain–source current degradation while catastrophic failure (without preceding degradation) occurred at LETs below 40% of rated voltage. The specific origin of failure – whether it stemmed from drain–gate or drain–source burnout – remains undetermined [136].

While InGaAs n-channel MOSFETs and InGaSb p-channel MOSFETs with sub–10 nm dimensions experience hole trapping in the gate dielectric after being exposed to 10 keV X–rays, hole trapping levels vary based on the gate bias during irradiation. These advanced III-V FETs also exhibit several radiation–related effects. For example, InGaAs FinFETs display charge enhancement factors of up to $\times$14 due to shunting and parasitic bipolar interactions. InGaAs MOSFETs manifest signals with long temporal tails triggered by oxygen ion strikes. Finally, the width of the fin impacts both the peak SET current and the collected charge, with wider fins demonstrating a more pronounced response [137].

Tabs. S6–S8 of the Supplementary Material gather test results from several experiments conducted by NASA and ESA on FET devices, revealing valuable insights into their radiation response. Experiments from [138] indicate that the 150 V n-channel MOSFETs onsemi^{TM} NVBLS4D0N15MC, with potential applications in power tools and battery-operated vacuums, exhibit no Destructive SEE (DSEE) up to a surface LET of 9.3 MeV·cm^2·mg^{-1} at a fluence of 5.0·10^5 ions/cm^2. However, SEGR and SEB are observed at LET levels of 17.0 MeV·cm^2·mg^{-1} and above, with fluences greater than or equal to 2.8·10^5 ions/cm^2. Similar tests on the 900 V SiC n-channel FETs SSDI^{TM} SFC85N9051, optimized for power applications, reveal higher resistance to DSEE. No effects are observed up to LET of 37 MeV·cm^2·mg^{-1} with fluences of 5.0·10^5 ions/cm^2 for drain–source voltages (V_{DS}) of 45 V. Micro SEGR events occur at higher V_{DS} (90 V), followed by full SEGR at LETs of 28.6 and 37 MeV·cm^2·mg^{-1}. Destructive effects are also noted at low V_{DS} = 12 V. Other SiC FETs considered in the NASA tests are the 200 V SSDI^{TM} SFF80N20S1 and 100 V SSDI^{TM} SFF120N10S1, ideal for fast switching tasks, and the 60 V n-channel MOSFETs Vishay^{TM} SQP120N06–06, suited for power-intensive applications. These devices only exhibit DSEE at elevated LET and bias conditions. Importantly, SiC FETs generally fare better against destructive radiation effects compared to Si MOSFETs of comparable ratings. However, all FET

types demonstrate destructive responses beyond certain LET thresholds, with susceptibility decreasing with increasing biasing conditions.

JFET amplifiers such as Linear Systems™ LSK389–UT and LSK489–UT exhibit degradation immunity to TID up to 25 krad(Si) and to HI with high LET (48 MeV·cm^2·mg^{-1}), making them ideal for low-noise signal processing. Similarly, the NXP Semiconductor™ BF862 n-channel JFET offers exceptional resilience, showing no destructive effects during HI tests with LET up to 85.8 MeV·cm^2·mg^{-1} under operating voltages (up to 20 V drain–source, -15 V gate–source). This makes it well-suited for particle detection instruments or for precise navigation in Inertial Measurement Units (IMUs). The ON Semiconductor™ BSS123 n-channel FET appears to be more vulnerable, with SEGR occurring at HI ion LET of 48 MeV·cm^2·mg^{-1} under drain–source voltages of 25–30 V.

Testing on power MOSFETs indicates varying levels of resistance to TID, SEB, and SEGR [139]. Results from [103] reveal further details about the hardness to radiation of trench power MOSFETs, which exhibit SEBs with variation in failure thresholds even between identical parts. Data in the tables highlight specific examples of this variability, indicating the effect of LET levels and V_{DS} conditions on failure points. Notably, both SEB and TID effects (threshold voltage shifts, increases in drain–source leakage current) occur even with zero V_{DS} bias.

SiC MOSFETs such as the Wolfspeed™ C2M0080120D show sensitivity to ionizing radiation even at low doses. The main effects include significant increases in off–state leakage current and on–state resistance as well as threshold voltage shifts. Performance does not fully recover after annealing. Similarly, SEE tests on these same SiC MOSFETs [140] find high SEE vulnerability including destructive failures of SEB and SEGR, even at very low LETs. Safe operating voltages have to be severely reduced compared to rated specifications, heavily constraining their operational use [141]. Concerning SiC JFETs, such as the Infineon Technologies™ IJW120R100T1, TID test results [142] are more positive, demonstrating resistance up to 1 Mrad(Si) with modest shifts that anneal out after the exposure. However, as it occurs for the SiC MOSFETs, SEE results are more concerning [143], with failure risks due to SEB and SEGR even at low LET and fluence levels. Therefore, JFETs are deemed unsuitable for most applications without major restrictions or shielding.

TID and SEE effects of another SiC MOSFET, STMicroelectronics™ SCT20N120, have been investigated in [142] and [143]. TID testing causes degradation, particularly in terms of leakage currents, threshold voltage shifts, increased on–resistance, and higher diode forward voltage. Although annealing improves these responses, full recovery is not achieved. SEE testing on this device has highlighted its vulnerability to both SEB and SEGR at surprisingly low LET levels with HIs. Proton exposures induce failures too, despite at a much lower cross-section. Significant variability appeared between device lots in SEE testing.

Overall, these studies demonstrate that DSEE remains a concern for FETs operating in radiation environments. SiC FETs generally exhibit greater resistance to destructive effects compared to silicon MOSFETs of similar ratings, but destructive responses occur for all FET types beyond certain LET and bias parameters. Importantly, these studies show that device–to–device variation exists even within identical FET models, making individual testing and derating of components essential for mission–critical applications in space.

D. OPAMPs

One of the primary functions of OPAMPs in space systems is signal conditioning. Signals collected from sensors and other components often require amplification, filtering, or other processing before they can be effectively utilized by the system. OPAMPs provide precise and configurable amplification capabilities, allowing engineers to tailor the signal to meet specific requirements. Feedback loops also employ OPAMPs to stabilize and control system parameters such as voltage levels, currents, and frequencies. This is particularly crucial in space systems where environmental conditions can vary drastically, and precise control is necessary for reliable operation.

Furthermore, OPAMPs are integral components in analog–to–digital (ADC) and digital–to–analog (DAC) converters. They are also utilized in power management subsystems to regulate and distribute power efficiently across various components of the spacecraft. This includes voltage regulation, current limiting, and voltage/current monitoring functionalities. In communication subsystems, OPAMPs are employed in the design of RF amplifiers, filters, and modulators/demodulators. They enable precise control of signal gain, frequency response, and modulation/demodulation processes, ensuring optimal performance of the communication link under varying conditions such as signal attenuation, interference, and Doppler shifts. OPAMPs also contribute significantly to the reliability and longevity of the mission through fault detection and mitigation. They are often integrated into fault detection circuits, where they monitor critical parameters such as temperature, voltage levels, and current consumption. In the event of anomalies or deviations from nominal values, these circuits can trigger appropriate responses such as activating redundant systems, reconfiguring operating modes, or implementing corrective measures to prevent catastrophic failures. In attitude control and navigation subsystems, OPAMP–based sensor interfaces and feedback loops enable the acquisition, processing, and interpretation of data from gyroscopes, accelerometers, star trackers, and other sensors used for attitude determination and navigation. Finally, OPAMPs are integral to scientific instrumentation payloads. Whether it is measuring atmospheric composition, monitoring radiation levels, or conducting experiments in microgravity environments, OPAMPs are employed in sensor readout circuits, signal conditioning modules, and data acquisition systems. Specifically, they enable the amplification, filtering, and digitization of sensor outputs.

CMOS, bipolar, and BiCMOS OPAMPs all display susceptibility to radiation effects, though specific responses vary by architecture and radiation type, as can be noticed from Tab. S9 – S11 of the Supplementary Material. From a general point–of–view, CMOS OPAMPs, such as the Analog Devices™ AD8572, demonstrate surprising resilience, maintaining function up to 50 krad(Si) with initial gain–bandwidth reduction followed by recovery during annealing [144]. This finding resonates with the HDR resilience and good TID tolerance (up to 49 krad(Si)) observed in the Analog Devices™ AD8021 OPAMP [145], [146]. Similarly, bipolar OPAMPs such as Texas Instruments™ LM6144 remain functional through 50 krad(Si) irradiation but undergo steady gain–bandwidth decline. BiCMOS OPAMPs, such as the Analog Devices™ AD627, exhibit earlier failure points (7.84 krad(Si)) without subsequent recovery during annealing [144]. However, BiCMOS devices, such as the Texas Instruments™ OPA855 and Texas Instruments™ OPA856, demonstrate enhanced robustness in various radiation environments [147]. TID exposure in CMOS OPAMPs can reduce gain–bandwidth, potentially increasing susceptibility to high–frequency distortion as seen in 0.5 μm CMOS devices with pMOS input differential pairs. Improved radiation hardness is observed in architectures using nMOS–input stages, which show better linearity, resilience to threshold voltage shifts, and less performance degradation overall [148]. These radiation–induced limitations on bandwidth are also observed in bipolar OPAMPs, e.g. the Texas Instruments™ μA741, with impacts on both their gain–bandwidth product and slew rate [149]. Furthermore, recent studies highlight dose–dependent degradation in input offset voltage, quiescent current, output voltage swings, and open–loop gain under TID conditions [150]. Modern fabrication processes might allow CMOS OPAMPs to offer better radiation tolerance than previously assumed, as highlighted by unexpected trends in noise voltage behaviour. Noise voltage is found to decrease following high–dose exposure in both CMOS and bipolar OPAMPs, while offset voltage is minimally affected in CMOS and slightly increased in bipolar OPAMPs. Additionally, bipolar OPAMPs demonstrate unexpected variability in total harmonic distortion [144]. Some bipolar devices, like the Analog Devices™ OP484FSZ, show particular neutron sensitivity leading to degradation in input offset current and voltage [145]. Further complexities arise when TID and analog SETs are combined. Experiments on the Texas Instruments™ LM124 using dose rate switching (DRS) demonstrate degradation in supply current, slew rate, and open–loop gain, mirroring effects of LDR exposure. Additionally, high dose rate X–ray flash testing indicates an increase of over 50% in analog SET width as a synergistic result of TID exposure, consistent across LDR and DRS experimental results [151].

As emerged by the aforementioned examples and other data in Tab. S9 and S10 of the Supplementary Material, OPAMP devices feature varying radiation tolerance, underscoring the importance of careful device selection for the needs of space applications. The Analog Devices™ AD8021, a low–noise, high–speed BiCMOS OPAMP, demonstrates continued functionality without apparent degradation under HDR gamma conditions, highlighting its superior radiation response [145]. The Analog Devices™ AD8021ARZ demonstrates good tolerance to TID up to at least 49 krad(Si), with only minor changes in parameters such as input offset voltage, input bias currents, open–loop gain, and common–mode rejection ratio [146]. However, other devices exhibit different vulnerabilities. The Linear Technology™ LTC2054HV, while offering high voltage gain, experiences degradation in offset voltage and quiescent current under LDR gamma conditions. This sensitivity could potentially compromise precision in certain applications [150]. Similarly, the Analog Devices™ OP484FSZ is susceptible to input offset current and voltage degradation under neutron exposure, highlighting a known weakness of bipolar devices to this type of radiation. Studies on the Linear Technology™ LTC2054HVMP highlight the effects of TID on specific device parameters. Exposed to gamma radiation at a low dose rate of 10 mrad(Si)/s up to 100 krad(Si), pronounced degradation occurs in input offset voltage (V_{OS}) under biased conditions, exceeding datasheet specifications between 80–90 krad(Si). Similarly, polarization current (IQ) exceeds specifications between 90–100 krad(Si). Importantly, V_{OS}, output voltage swings ($V_{OUT\text{-}HIGH}$/$V_{OUT\text{-}LOW}$), and IQ demonstrate statistically significant correlations between parameter degradation and accumulated radiation dose. While open–loop gain stays within specifications until 100 krad(Si), other electrical parameters show varying degrees of degradation. Irradiation under an unbiased state causes less severe degradation, with no parameters exceeding datasheet specifications up to 100 krad(Si). This bipolar OPAMP appears to remain functional up to 100 krad(Si), with performance limits exceeded between 80–100 krad(Si).

Tests focused on the Analog Devices™ AD620SQ/883B revealed specific radiation–induced effects and dose thresholds. Key degradations were observed in parameters like bias currents ($+I_B$, $-I_B$), input offset current (I_{IO}), gain error, and power supply rejection ratios (PSRR) at doses ranging from 3 krad(Si) to 14 krad(Si). Notably, positive bias current ($+I_B$) degrades beyond specification limits after a dose of 5.411 krad(Si), with the average dose to failure being 8.464 krad(Si) for biased parts and 11.408 krad(Si) for unbiased parts. Other parameters exhibit failures within this dose range as well. Annealing is found to provide partial recovery for some parameters like I_B, I_{IO}, and PSRR, but not to pre–radiation levels in most cases. Probability analysis suggests consideration of additional shielding to reduce failure risk due to radiation effects on this OPAMP [152].

The BiCMOS technology used in devices like the Texas Instruments™ OPA855 and OPA856 demonstrates robustness in various radiation environments, providing promising options for radiation–hardened designs. High–output devices

such as the Apex^{TM} PA02 offer substantial output voltage swings but also exhibit resilience against a range of irradiation conditions.

Results from HIs testing reported in Tab. S11 of the Supplementary Material for multiple OPAMPs provide important insights into their susceptibility to SEEs. The Linear Technology^{TM} LTC6268–10 is found to be susceptible to SETs, with cross-sections ranging from approximately $1{\cdot}10^{-5}$ cm^2 at 2.5 MeV·cm^2·mg^{-1} to $1{\cdot}10^{-3}$ cm^2 at 80 MeV·cm^2·mg^{-1}. However, no other SEEs are observed up to a LET of 85.6 MeV·cm^2·mg^{-1}. While some SETs occur, most appear to last less than 7 μs. Estimated on–orbit SET rates for this device are of a few events per device year under typical space conditions. Test data for the Analog Devices^{TM} AD8021 evidence good SEL immunity up to an effective LET of 81.6 MeV·cm^2·mg^{-1} at a junction temperature of 85°C. SET testing at a LET of 10 MeV·cm^2·mg^{-1} has resulted in a measured SET cross-section of $3.5{\cdot}10^{-6}$ cm^2, with SETs manifesting as voltage transients on the output and a threshold of 270 mV. Overall, data show that the Analog Devices^{TM} AD8021 has a good SEL immunity but presents SET susceptibility. The Texas Instruments^{TM} OPA691, a current feedback OPAMP, exhibits a SET threshold $<$ 69.9 MeV·cm^2·mg^{-1} with a maximum SET cross-section of approximately 10^{-4} cm^2 at 69.9 MeV·cm^2·mg^{-1}. Maximum observed SET amplitudes are $\pm$1.25 V on the output, with maximum durations lower than 0.2 μs. Similarly, a range of low–noise OPAMPs (Texas Instruments^{TM} OPA842, OPA847, OPA855, and OPA856) demonstrate SET thresholds below 69.9 MeV·cm^2·mg^{-1}. Maximum SET cross-sections for these devices are in the order of 10^{-4} to 10^{-5} cm^2, with amplitudes up to $\pm$2.5 V on the output and durations less than 0.2 μs [147]. Importantly, the Analog Devices^{TM} AD620SQ/883B experiences degradation in several parameters when irradiated to 25 krad(Si) at 10 mrad(Si)/s. Input offset current exceeds specification at 3.3 krad(Si), while positive and bias currents do it at 5.4 krad(Si) and 8.5 krad(Si), respectively. In contrast, all parameters of the Texas Instruments^{TM} OP484 remain within specification up to 50 krad(Si) when irradiated at 10 mrad(Si)/s. However, the $V_{\text{OUT-HIGH}}$ drops below the minimum specification at a total dose of 75 krad(Si). Annealing effects are observed on the Analog Devices^{TM} AD620SQ/883B after irradiation. After 212 hours of annealing, parameters appear to return near or within specification levels. For example, the input offset current has improved from ~20,000 nA during irradiation to 13 nA after the 212-hour annealing.

In summary, the different OPAMPs tested revealed degradation starting at different TID levels, indicating variability in radiation tolerance across devices. The Analog Devices^{TM} AD8572, due to its ultralow offset, drift, and bias current, is indicated for precision current sensing and thermocouple amplification, having demonstrated resilience up to 50 krad(Si). Another suitable component, which showed tolerance up to 49 krad(Si), is the Analog Devices^{TM} AD8021, a high-speed, voltage feedback amplifier with low voltage and low current noise. It is well-suited for applications such as ADC preamps and drivers, and instrumentation preamps. For applications requiring high gain bandwidth and low input voltage noise, such as optical time domain reflectometry and laser distance measurement, the Texas Instruments^{TM} OPA855 and OPA856 are excellent choices that exhibit enhanced robustness in harsh radiation environments. The Texas Instruments^{TM} OP484 is particularly well-suited for battery-powered instrumentation and power supply control and protection. It offers wide bandwidth, low noise, and rail-to-rail input and output. The OP484 maintains all parameters within specification up to 50 krad(Si) when irradiated at a rate of 10 mrad(Si)/s. Key parameters that degrade across OPAMPs include input bias and offset currents, output voltages, and power supply rejection ratios. These could be highlighted as particularly sensitive parameters for OPAMPs under radiation exposure. Additionally, test results indicate part–to–part variability, with parameters in a given OPAMP exceeding specifications at slightly different dose levels. This highlights the importance of testing multiple samples to characterize device responses fully. Many OPAMPs tested exhibit SETs when exposed to HIs, with cross-sections in the order of 10^{-4} – 10^{-5} cm^2. SETs manifest as transient disturbances on the output voltages, with amplitudes up to $\pm$2.5 V and durations less than 0.2 μs. No destructive SEL effects are observed up to the maximum LET used during testing of 69.9 MeV·cm^2·mg^{-1} [116]. Certain design factors appear to significantly affect radiation tolerance, such as process technology (CMOS, bipolar, BiCMOS) and circuit architecture. While shielding strategies may help mitigate device–specific sensitivity, careful TID and SEE testing are ultimately needed to accurately evaluate expected performance in a space environment.

E. MEMORIES

Memories are integral components of space missions that are utilized to store mission–critical data, including telemetry, command sequences, scientific observations, and operational parameters. They are also essential for buffering and caching data during communication between different subsystems or with ground stations, ensuring smooth data transmission and reception. In satellite communication systems, memories serve as temporary storage for data packets during transmission, allowing for efficient flow control and error correction mechanisms.

Additionally, memories are utilized in fault-tolerant systems, where redundant data storage schemes are implemented to mitigate the effects of radiation–induced errors or hardware failures. This redundancy ensures the integrity of critical data and allows uninterrupted system operations even in the presence of faults. Memories are also employed in the execution of onboard software, storing program instructions, and temporary data during computation processes. Advanced onboard computers in spacecraft often utilize memories with fast access times and large storage capacities

to support real-time processing of sensor data, navigation algorithms, and autonomous decision-making. Memories also store configuration data for reconfigurable hardware elements such as Field–Programmable Gate Arrays (FPGAs) or Application–Specific Integrated Circuits (ASICs), allowing for in–flight reprogramming or reconfiguration of system functionalities. In long–duration missions, memories play a vital role in supporting extended mission durations and autonomous operation. They are utilized for storing historical mission data, software updates, and diagnostic logs, facilitating post–mission analysis and troubleshooting. Moreover, memories enable software-defined functionalities, allowing for flexible mission planning and adaptation to changing mission requirements or environmental conditions.

Research has extensively explored the effects of radiation on nonvolatile memories (NVMs), offering guidelines for testing and outlining specific phenomena and failure modes [153], [154], [155], [156]. HI testing at various angles is essential due to the potential for particle strikes in space. Indeed, peripheral control circuits demonstrate particular susceptibility to functional failures from HIs, often affecting data integrity [153]. This vulnerability is confirmed by the collected test data (see Tab. S12 – S15 of the Supplementary Material), where SEFIs manifest across NAND and NOR flash devices during active modes [147], [157], [158], [159], [160].

Proton testing has evidenced that TID effects are the primary radiation concern, with secondary ions generated by nuclear interactions responsible for observed proton–induced SEEs [153]. Interestingly, SEUs even without observable SEFIs or SELs are seen during proton testing, for example in the Macronix^{TM} MX30LF4G18AC NAND flash, highlighting the complex nature of the response of these devices to proton irradiation [147], [157].

TID testing causes threshold voltage shifts that can induce bit errors, primarily failing control logic. There are potential TID impacts on retention and reliability, and concerns are raised due to micro–dose effects causing retention failures [153]. Data in Tab. S12 – S15 of the Supplementary Material underscore this effect, showing data instability of memories over time after TID exposure with increased errors across 16/64 Gb SLC NAND flash, and complete functional failures for doses between 30–60 krad [161], [162]. Data collected on NAND flash devices also indicate a compromise in charge storage from TID, and SEUs even occurring during the powered–off state (e.g., see Kioxia America^{TM} TC58NVG2S0HTAI0) [147], [157].

For CMOS NVMs, the DD results are less significant, since error correction codes can mitigate single and double–bit errors in several cases. Specific results highlight the occurrence of bit errors in 8.3 nm flash tunnel oxide arrays at TID levels beyond 100 krad(Si), with a noted correlation between reduced charge pump voltage (from $\sim$20 V to $<$ 10 V) and functional failures. However, the overheating step at 100 °C, which followed the first TID exposure in accordance with the test procedure, did not yield significant results. This is the case, for example, for the Samsung^{TM} 8 Gb flash device, where further irradiations drastically increased the retention errors in data storage (20$\times$ with a 4$\times$ dosage increase) [153].

Radiation effects on commercially dominant Floating Gate (FG) flash memories have also been analyzed. TID induces FG charge injection, trapping within the tunnel oxide, or electrons gaining enough energy to escape, thus altering the stored charge, shifting V_{TH} distributions, and causing bit errors. TID failures typically manifest within peripheral circuits, such as charge pumps integral to program/erase cycles. In terms of SEEs, HIs create secondary V_{TH} distribution peaks by discharging FGs. The mean V_{TH} shift demonstrates a linear correlation with particle LET and oxide electric field strength. Additionally, MBUs propagate throughout columns. Notably, lower energy ions generate larger shifts, attributed to their smaller track sizes that enhance tunnelling efficiency [154]. Consequently, higher LET particles induce both more frequent SEUs and MBUs in NAND and NOR devices, as evidenced by the collected test data [147], [157], [158], [159], [160].

For the specific devices reviewed, several important trends and sensitivities emerge. HI irradiation consistently causes SEUs in NAND flash devices, such as the Macronix^{TM} MX30LF4G18AC, where individual bits are flipped. The likelihood of SEUs increases with higher LET particles. MBUs, affecting several bits within a word, begin to occur at LETs over 10 MeV$\cdot$cm$^2\cdot$mg^{-1}, while SEFIs, impacting larger scales of operation, arise during active modes like Read or Erase/Write. Moreover, devices may also experience SELs, requiring power cycling. The severity of these effects is strongly correlated with both the LET and operating mode of the device.

NOR flash devices, like Micron^{TM} PC28F00AM29EW and Macronix^{TM} MX68GL1G0G, demonstrate similar responses. SEUs and MBUs are observed, with increasing frequency for higher LET particles. Importantly, SEFIs, causing interruptions like buffer write/read errors or extended erase delays, occur during dynamic testing. Some NOR flash devices also demonstrate vulnerability to SELs, resulting in high leakage currents, and requiring power cycles [147], [157], [158], [159], [160]

Proton irradiation testing yields varied results. The Micron^{TM} PC28F00AM29EW NOR flash memory shows exceptional resilience, exhibiting no latchups or ruptures even under extreme test conditions and low error rates, such as limited erase block or write buffer timing errors. Its susceptibility appears confined to the internal high–voltage generation circuitry during erase/write operations.

The Macronix^{TM} MX30LF4G18AC NAND flash does not experience SELs during proton testing. SEUs are observed, mainly in terms of single-bit flips, but with no clear dependence on proton energy. Notably, SEU sensitivity varies across blocks and SEU rate increases non–linearly with proton fluence, suggesting a cumulative process wherein sensitive cells gradually lose charge.

The Avalanche^{TM} AS216MA1G2B–ASC MRAM demonstrates susceptibility to SELs withing the range of 21.1 < LET_{th} < 58.8 MeV·cm^2·mg^{-1}, with SEL occurrence even observed via laser testing [147], [157], [163], [164]. However, it shows remarkable resilience to TID, enduring up to 1 Mrad(Si) without observable degradation [147], [157], [161], [162].

Samples of Micron Technology^{TM} MT29F series SLC NAND flash devices, both in the 16 Gb and 64 Gb versions, demonstrate post–irradiation data instability following TID tests. Bit errors increase steadily over time after exposures from 10–60 krad, indicating degradation in data retention. Complete functional failures occur between 30–60 krad. Importantly, higher bit density devices generally show greater initial errors at lower doses. TID testing for the Micron^{TM} MT29F4T08CTHBBM5 and Hynix^{TM} H25QFT8F4A9R 3D NAND devices resulted in functional impairment. Error rates vary between SLC and MLC modes, with the Micron^{TM} device experiencing failures in erase circuitry at relatively low doses.

In summary, COTS memory devices exhibit a complex spectrum of sensitivities to radiation. NAND flash reveals clear patterns of SEEs under HIs, with more severity in dynamic modes and at higher LETs. TID leads to data loss and potential device failure across flash devices, with sensitivity tied to device density. NOR flash displays SEUs, MBUs, and SELs under HIs, with error rates correlated with the LET. Lastly, while some MRAM types show encouraging TID resistance, SEL risks emerge as a key concern. These findings underscore the need for shielding and/or error correction strategies for COTS memories to achieve reliable operation in space environments.

F. FPGAs

FPGAs are semiconductor devices containing configurable logic blocks and reprogrammable interconnects. They are utilized for tasks such as image processing, signal modulation and demodulation, error correction coding, and sensor interfacing. Their reconfigurable nature allows for real–time adaptation to changing mission requirements and environments.

Since the 1990s, several studies have examined the various ways in which radiation can affect FPGAs. Antifuse FPGAs feature varying susceptibility to radiation effects, with HI–induced ruptures occurring at LET thresholds above 37 MeV·cm^2·mg^{-1}, while in SRAM–based FPGAs, configuration upsets occur even at low LET thresholds of 4–5 MeV·cm^2·mg^{-1}, resulting in driver conflicts, bus fights, and I/O errors [165]. These outcomes reflect also on recent high configuration memory (CRAM) SEU sensitivity, such as the Xilinx^{TM} FPGAs [166]. Moreover, CMOS processes in the range of 0.6–0.8 μm exhibit increased proton SEE susceptibility compared to older technologies, although design techniques like the balanced storage cells can provide improvement. In terms of latchup behaviour, performance is strictly tied to fabrication details, with thresholds ranging from < 10 MeV·cm^2·mg^{-1} in some bulk CMOS to > 80 MeV·cm^2·mg^{-1} in optimized epitaxial processes). Similarly, TID tolerance varies significantly, ranging from < 3 krad(Si) in scaled commercial models to > 300 krad(Si) in hardened antifuse FPGAs. Generally, CMOS scaling below 1 μm tends to increase susceptibility to TID effects [165].

Concerning TID effects, antifuse, Flash, and SRAM FPGAs demonstrate unique behaviour. In antifuse FPGAs, power supply current (I_{cc}) and propagation delay increase, with functional failures noted around 30 krad, potentially due to radiation–induced charge pump degradation. Hardening methods can extend tolerance beyond 70 krad. In Flash FPGAs, anomalies linked to floating gate switch disruption emerge, accompanied by increasing I_{cc} and delays for doses up to 500 krad. SRAM FPGAs may encounter power–up failures around 50 krad, although the root cause is unclear and could potentially originate from TID effects within SRAM configuration cells.

SEEs also vary among different FPGA technologies. While antifuse devices may experience clock and control logic upsets, such as JTAG, these effects have known causes and can be mitigated through design approaches. In this context, interesting performance is achieved by the Microsemi^{TM} RTG4 FPGA, which exhibits high SEE resistance in configuration logic but presents unprotected shift registers as areas of vulnerability. For Flash FPGAs, sensitivity to clock upsets is observed above 18–20 MeV·cm^2·mg^{-1}, without SEEs occurring in Flash cells. In SRAM FPGAs, configuration bit SEUs are the primary concern, since nearly 10% of functional interrupts are attributable to uncorrected bit upsets [167].

Investigating in quantitative details, data collected from ESA and NASA SEE and TID tests are summarized in Tab. S16 – S18 of the Supplementary Material. As expected, SEEs noticeably impact FPGAs, with sensitivities depending on device architecture, memory type, and angle of incident radiation. CRAM (configuration memory) appears especially prone to upsets, and both single–bit and multi–bit/cell upsets appear in these devices. Mitigation strategies like selectively shielding or isolating essential configuration bits appear warranted. BRAMs often show high SEU rates, while Flip–flops and SRLs have more varied responses. Notably, SEFI rates remain relatively low within many of the FPGAs studied. For example, in the Xilinx^{TM} Zynq–7000 FPGA, CRAM cross-sections range from $1.62{\cdot}10^{-9}$ cm^2/bit to $2.09{\cdot}10^{-9}$ cm^2/bit for different incident angles. Isolating essential CRAM bits yields values of $0.82{\cdot}10^{-9}$ cm^2/bit and $1.13{\cdot}10^{-9}$ cm^2/bit. BRAM cross-sections are higher: $7.13{\cdot}10^{-9}$ cm^2/bit (0 degrees) and $14.15{\cdot}10^{-9}$ cm^2/bit (45 degrees). Interestingly, 1K to 3K bits within a BRAM block could be affected together in distinct patterns. SEU cross–sections for Flip–flops (FFs) come in at $8.11{\cdot}10^{-9}$ cm^2/bit (0 degrees) and $12.06{\cdot}10^{-9}$ cm^2/bit (45 degrees), while shift registers in SRLs are lower at $3.87{\cdot}10^{-9}$ cm^2/bit (0 degrees) and $5.13{\cdot}10^{-9}$ cm^2/bit (45 degrees). SET events sometimes involve groups of FFs and SRL bits. Upsets could be single (SBUs) or involve multiple cells/bits (MBUs & MCUs), sometimes spanning

frames in patterns dependent on memory type. The likelihood of transitions from 0 to 1 or from 1 to 0 is approximately equal in CRAM/SRLs, but different biases occur in FFs and BRAMs. SEFIs that require power cycling or software reset are minimal during readback and verification [168], [169].

The characterization of Xilinx^{TM} Kintex–7 FPGA provides further SEU insights. CRAM totals fall within $2.49{\cdot}10^{-10}$ cm^2/bit, dropping even more ($1.23{\cdot}10^{-10}$ cm^2/bit) for essential bits. BRAM SEU rates come in around $6.05{\cdot}10^{-10}$ cm^2/bit, FFs around $7.89{\cdot}10^{-10}$ cm^2/bit, and SRLs with the highest sensitivity at $8.37{\cdot}10^{-10}$ cm^2/bit. Notably, essential CRAM bits show the lowest sensitivity, while SRLs are the highest. Most CRAM upsets are SBUs, but MCUs (often 2–bit upsets per frame) do not occur, with patterns seemingly tie to bit interleaving. Configuration register errors leading to SEFIs are not seen in this device, by using 230 MeV/u iron ions at an effective LET of 2.29 MeV·cm^2·mg^{-1}, and a dosage of $3.58{\cdot}10^5$ ions/cm^2 [166].

As expected, flash–based FPGAs reveal differing characteristics regarding SEEs. Configuration logic often demonstrates high resistance. However, unprotected shift registers appear susceptible. Microsemi^{TM} RTG4 devices demonstrate these different responses. Their configuration logic appears much radiation–resistant, with zero configuration SEUs under high LET testing (reaching 86.6 MeV·cm^2·mg^{-1}). On the other hand, shift registers lacking mitigation have noticeable SEU impacts at a LET of 20 MeV·cm^2·mg^{-1} and 100 MHz, ranging from $1{\cdot}10^{-4}$ to $4{\cdot}10^{-3}$ cm^2/bit [170].

For the Microsemi^{TM} PolarFire FPGA, SEUs affect shift registers, counters, and SRAM. Cross-sections increase with higher LET values. Shift registers have mostly single–bit upsets that reset after one clock cycle and potential clock/reset SET–induced burst errors. While single counter-upsets do not cause critical disruption, SRAM upsets indicate that SECDED error correction would be beneficial [171].

In the Xilinx^{TM} XC7Z045–2FFG900C with 0° to 85°C operational temperature range, resilience to SEUs is observed at an LET threshold of 2.29 MeV·cm^2·mg^{-1}, with a cross-section below $8.37{\cdot}10^{-10}$ cm^2/device. However, proton exposure induces SEUs, SEFIs, and system crashes, showing heightened susceptibility at lower energies [168], [169].

The Microsemi^{TM} A3PE3000–1PQG208I, designed for a wider −40 to 100°C temperature range, may indicate optimizations for harsh environments. It underwent application–specific SEE characterization at LBNL and TAMU, highlighting the value of targeted testing [147].

Devices tested specifically at LBNL, such as the Xilinx^{TM} XCKU040–2FFVA1156E, have shown that Triple Modular Redundancy (TMR) can significantly reduce SEU cross–section, standing as a promising mitigation strategy against radiation [157].

Concerning TID effects, certain components within COTS FPGAs may exhibit early failures, with JTAGs appearing of heightened concern. On the other hand, various FPGA resources exhibit high tolerance, potentially exceeding mission requirements. In this direction, the Lattice Semiconductor^{TM} LIFCL–40–8BG400C successfully passes TID tests up to 200 krad(Si) for all embedded designs and components on four devices, including shift registers, PLLs, DSPs, SERDES, and ADCs. However, the first failure – linked to the JTAG – arises at a dose level of 250 krad(Si), highlighting a specific vulnerability within the design [147], [172].

Diverging outcomes emerge from TID tests on the Xilinx^{TM} Zynq–7000 FPGA with proton bombardment (30–200 MeV). Here, CRAM proves exceptionally sensitive, with a cross-section around $6{\cdot}10^{-15}$ cm^2/bit. Flip–flops, LUT RAMs (SRL and DRAM) display approximately one order of magnitude higher cross-sections at $1{\cdot}10^{-14}$ cm^2/bit, indicating higher vulnerability in the user logic. CRAM MCUs have complex cross–frame boundary patterns, with 4–6% defying error correction provided by the Xilinx^{TM} SEM IP. Conversely, Block RAMs (BRAMs) demonstrated notably higher resilience with substantially lower cross-sections. Application–level testing on ARM cores reveal increasing silent data corruptions (SDCs) alongside cache reduction, proving as a valuable mitigation tool. Without any cache, SDCs are observed at a rate of $\sim$1–$3{\cdot}10^{-13}$ cm^2/bit, roughly double the raw bit failure rate. This is due to an intrinsic functionality of the processor, which can internally mask some errors. Surprisingly, the observed overall system crashes are low, around 1–$3{\cdot}10^{-15}$ cm^2/bit, due to inherent architectural strengths [169].

In summary, this data collection emphasizes the complexity of using COTS FPGAs in radiation–rich environments typical of space applications. Device, component, and architecture–level effects, coupled with varied SEU and TID responses, make generalization highly challenging. Careful tailoring of radiation mitigation strategies based on specific device selection and mission parameters is essential to ensure COTS FPGA reliability and success in space. Key takeaways lie in the greater sensitivity of user logic/memory over configuration bits, cache value in processor resilience, complex MCU patterns specific to CRAM, and the relative advantages of BRAMs and the processor architecture in managing radiation.

VI. CONCLUSION

The advent of the NewSpace era has led to a proliferation of small satellite missions employing COTS electronics rather than costly radiation–hardened aerospace parts. However, utilizing COTS devices in hazardous space radiation environments poses reliability risks necessitating careful evaluation. In this paper, recent radiation test results have been reviewed per established standards to facilitate informed component selection across critical categories of semiconductor devices.

Multiple facilities executed the presented radiation experiments following recognized testing standards. Proton and HI single–event effect tests complied with ESCC 25100 guidelines, administered via cyclotrons and particle accelerators. TID and DD evaluations adhered to ESCC 22900 protocols,

utilizing ^{60}Co gamma sources and particle accelerators like the Jyväskylä RADEF cyclotron. These standardized procedures lend credibility regarding the validity of gathered data and provide application–specific performance insights unavailable from data sheet parameters alone.

Examining response trends across device types reveals that certain COTS technologies have exhibited promising radiation tolerance under standardized test conditions.

Regarding diodes, onsemi^{TM} MMBD1501A ultrafast switching diodes demonstrated immunity to destructive single–event effects during multiple HI exposure tests, with no events observed up to LET thresholds above 64 MeV cm^2/mg. However, the Infineon^{TM} BAR64–05 RF PIN diode exhibited both increased leakage current and single–event burnout susceptibility during HI strikes. These results highlight that while certain diodes suit NewSpace applications from a radiation perspective, failure mechanisms in other diodes could undermine reliability if not addressed through appropriate derating, redundancy, or shielding.

Likewise, for BJTs, parametric shifts were observed in heavy–duty power transistors like Semelab^{TM} BUL54A when subjected to gamma irradiation, with substantial gain degradation and collector–emitter breakdown voltages impacts occurring beyond 1 Mrad(Si). Thus hardening techniques may prove advisable for demanding space applications. Conversely, general–purpose small–signal devices like Onsemi^{TM} 2N2222A showed far lower sensitivity to ionizing dose rates up to 300 rad(Si)/s, maintaining adequate gain for typical voltage amplifier or interface circuits without supplemental hardening.

SiC power MOSFETs like CREE^{TM} CPM2–1200–0025B showed no measured degradation effects when subjected to high gamma dose rates at GSFC and Ohio State University facilities, indicating suitability for space systems requiring resilience to ionizing radiation exposure over long durations.

Additionally, Magnetoresistive RAM (MRAM) devices such as Avalanche's AS216MA1G2B–ASC maintained full functionality without parametric degradation across multiple test sites administering TID up to 250 krad(Si)). Such remarkable radiation hardness underscores MRAM's prospect for usage in future space assets demanding extreme resilience to cumulative ionizing damage.

Conversely, the presented data also reveals potential weaknesses in certain COTS devices that could undermine reliable performance in radiation environments. For instance, SiGe HBT ICs including n-p-n transistors in 250 nm CMOS platform showed current gain degradation when subjected to gamma radiation, with failures occurring at doses as low as 800 krad(Si) under certain bias conditions. Thus, SiGe HBTs may require shielding or redundancy techniques when employed in nanosatellites expecting multi–year operational lifetimes despite maintaining frequency performance within specifications.

Additionally, GaN HEMTs like EPC Corporation's EPC2019 exhibited channel resistance increases when subjected to high fluence neutron irradiation. Although tolerant to administered ionizing dose levels, neutron–induced lattice defects impacted conductivity characteristics in these devices. Such parametric shifts over prolonged durations in orbit could ultimately threaten amplifier gain margins or voltage conversion ratios in spacecraft power circuits.

In summary, modern COTS radiation tolerance varies widely across semiconductor technologies and specific components must be certified through application–specific testing to qualify for usage in electronics intended for deployment in hazardous radiation regions like outer space. The information presented herein aims to assist electrical engineers in discriminating between candidate devices through actual performance benchmarking under standardized conditions replicating key aspects of the space environment. By combining strategic component selection, rigorous validation, and targeted hardening measures, the expanding NewSpace industry may continue augmenting small spacecraft capabilities toward levels formerly only attainable via costly legacy solutions. However, as mission durations lengthen along with distance from Earth's protective envelope, qualification processes must keep pace through comprehensive testing that fully characterizes modern COTS radiation susceptibilities before deployment to realize the full economic and exploratory potential promised by high–capability nanosatellites over their entire operational lifetimes.

ACKNOWLEDGMENT

(Giuseppe Brunetti and Giulio Campiti are co-first authors.)

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Open Access funding provided by 'Politecnico di Bari' within the CRUI CARE Agreement