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RESEARCH ARTICLE

A Single-Ended-to-Differential Low-Noise Amplifier With Transformer-Based Feedback Network for 3–5 GHz UWB Applications

ICKHYUN SONG[1], (Member, IEEE), SANG GYUN KIM[2], (Member, IEEE), SEUNG HWAN JUNG[2], (Member, IEEE), AND MOON-KYU CHO[3], (Member, IEEE)

[1]Department of Electronic Engineering, Hanyang University, Seoul 04763, Republic of Korea
[2]GRIT Custom-IC Inc., Seoul 01886, Republic of Korea
[3]School of Computer Engineering, Korea National University of Transportation, Chungju-si, Chungcheongbuk-do 27469, Republic of Korea

Corresponding author: Moon-Kyu Cho (moonkyu.cho@ut.ac.kr)

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ABSTRACT A wideband single-ended-to-differential (S-to-D) low-noise amplifier (LNA) for ultra-wideband (UWB) wireless sensors and internet-of-things applications is presented. In order to simultaneously provide wideband input matching characteristics, low-noise performance, and flat in-band gain response, a common-source input stage with on-chip transformer-based reactive feedback network is proposed. With the use of an on-chip transformer that serves as a shunt peaking inductor in differential mode, the LNA achieves improved voltage gain at high frequencies. At the input port, a cross-coupled common-gate stage balances the currents in differential operation, minimizing the gain and the phase mismatches at the differential output node. The proposed S-to-D LNA fabricated in a commercial 180 nm bulk CMOS technology exhibits a peak gain of 10.5 dB, an in-band minimum noise figure of 3.6 dB, and an input return loss of better than 8.8 dB from 3.0 GHz to 5.0 GHz, and a power consumption of 5.5 mA from a 1.8 V dc supply. The measured amplitude and phase mismatches are within 0.2 dB and 2.3 degrees, respectively. In comparison with other state-of-the-art designs, the proposed S-to-D LNA achieves low amplitude and phase mismatches, demonstrating well-balanced performance for 3-5 GHz UWB applications.

INDEX TERMS Balun, CMOS, cross-coupled common-source, low-noise amplifier (LNA), radio-frequency circuit, single-to-differential, transformer-based feedback network, ultrawideband (UWB).

I. INTRODUCTION

Ultrawideband (UWB) technology has gained much attention due to its low power, wide operating bandwidth, and high resolution [1], [2]. From an application perspective, UWB systems provide viable solutions to meet ever-increasing challenging demands for multiband and high-data-rate communications, indoor localization, and edge sensor nodes, biomedical devices in a variety of wireless applications [3], [4], [5]. When it comes to the implementations of UWB-based systems, the design of a low-noise amplifier (LNA) in a receiver requires immediate attention due to the limitations of transmission signal power in UWB applications with a power spectral density as low as -41.3 dBm/MHz. As the first gain stage in the receive chain, an LNA is a critical component since it affects the overall performance

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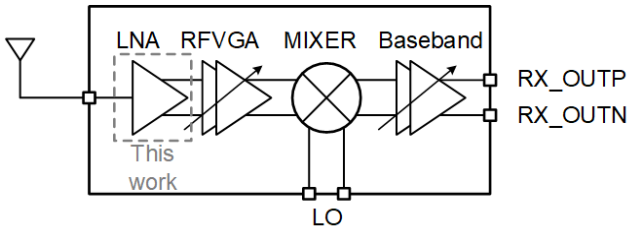


FIGURE 1. Simplified system-level block diagram of a UWB system with the proposed single-to-differential (S-to-D) LNA.

of the signal processing chain in radio-frequency (RF) front-ends [6]. To optimize the performance of UWB systems, an LNA should be able to simultaneously achieve large signal gain, low noise figure, wideband impedance matching, and linearity over spectra of several GHz of bandwidth.

Considering the impact of substrate noise, common-mode rejection, and power-supply rejection in terms of the signal-to-noise ratio, the use of symmetrical and balanced signaling is necessary for robust reliable internal system operation. In contrast, to match interfaces between receivers and other external components such as antennas, dividers, or filters on boards, single-ended signaling is preferred to reduce system complexity and physical form factor. As shown in Fig. 1, single-ended-to-differential (S-to-D) or balun configurations are preferred candidates for satisfying various system requirements. When an antenna senses an incoming signal, the LNA converts the single-ended input signal into differential outputs for subsequent stages including an RF variable-gain amplifier (VGA), a down-conversion mixer, and baseband circuits, providing sufficient gain with minimal noise contribution.

In recent years, the design of wideband S-to-D LNA has been studied to meet system requirements such as noise performance, bandwidth, amplitude/phase mismatches, input-matching characteristics, and flat in-band response [7], [8], [9]. Conventionally, there have been two main approaches for S-to-D LNA design: 1) S-to-D LNAs with an input passive balun and 2) active-based S-to-D LNAs. For the former, S-to-D LNAs employ a passive balun element at the input to generate differential signals [7]. In terms of bandwidth and noise, however, it exhibits narrow operating bandwidth and a large chip area due to the lumped or transmission-line components of a balun. In addition, their noise performance may suffer from inevitable insertion loss which is directly added to the noise figure (NF). To overcome these drawbacks, the latter, an active-based S-to-D LNA, has been suggested, utilizing negative feedback networks [8] or multi-path signal/noise optimization [9]. Despite the improvements in some performance parameters, they still have limitations of generating differential signals with low imbalances at the output due to their circuit structures or asymmetric output load configurations. Since the quality of a demodulation process is sensitive to the mismatches of differential signals or common-mode variations in most advanced transceivers, it is imperative to minimize amplitude/phase errors at the output

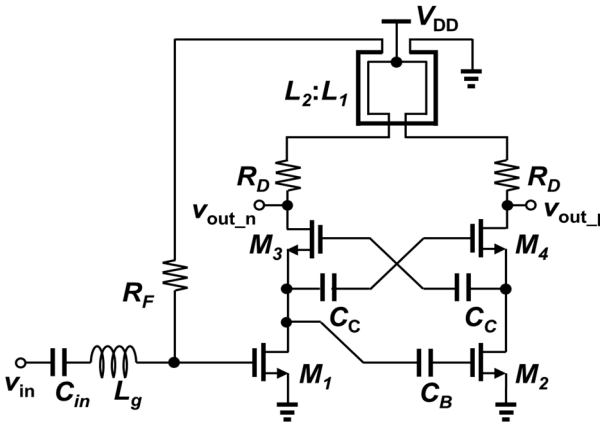


FIGURE 2. Schematic of the proposed S-to-D LNA with the transformer-based reactive negative feedback network. Bias circuitry is not shown.

of S-to-D LNAs for obtaining better signal constellation or lower error vector magnitude.

The present work demonstrates the S-to-D LNA with a transformer-based feedback network to achieve moderate small-signal gain and low NF, wide input matching characteristics, and compact chip size for low-band UWB (3-5 GHz) wireless applications. In addition, the proposed design can minimize phase and amplitude mismatches at the differential output terminals by employing a current balancing technique and a symmetric output load configuration.

II. TRANSFORMER-BASED S-TO-D LNA

A. UWB LNA SCHEMATIC

In Fig. 2, the core schematic of the proposed S-to-D LNA with the transformer-based reactive feedback network is shown without biasing circuitry for simplicity. Unlike the conventional approach that combines a common-gate (CG) and a common-source (CS) stages, the proposed circuit employs two CS stages to generate differential signals. The topology differs from similar S-to-D LNAs in that it utilizes a symmetric load and a current balancer to minimize amplitude and phase mismatches in a simple circuit configuration. Moreover, the use of a transformer supports high-frequency operation and the global resistive feedback reduces loading effects on each branch.

At the input terminal, a capacitor (C_{in}) and an inductor (L_g) are placed in series mainly for dc-blocking and input-matching purposes, respectively. The forward signal path consists of two single-stage CS amplifiers, a cross-coupled CG stage, and an on-chip transformer. In order to implement the S-to-D functionality with a large voltage gain, the output signal of the first CS amplifier (M_1) is connected to the gate terminal of the second CS amplifier (M_2). The series capacitor (C_B) between two CS stages was used at the interstage of the S-to-D LNA for isolating DC bias between the first and the second CS amplifiers. Since two output signals of CS amplifiers may present amplitude and phase differences, the CG stage (M_3 and M_4) with cross-coupled capacitors (C_C) was inserted to minimize them between differential signals.

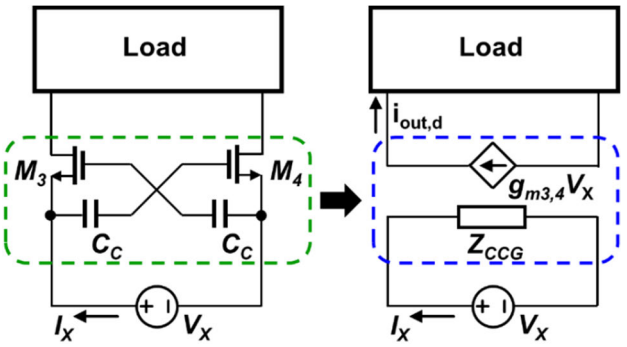


FIGURE 3. Simplified equivalent model of the cross-coupled common-gate (CCG) stages.

As a current balancer, the cross-coupled common-gate stage (CCG) maintains moderate voltage swing at the output terminals of the two CS amplifiers (drain of M_3 and M_4). In addition, it helps improve reverse isolation and overall linearity [10]. If we assume symmetry between both branches, no channel-length modulation, and the condition of $C_C \gg c_{gs3,4}$, the equivalent input impedance of the cross-coupled common-gate stages (CCG) looking from the test voltage source (V_X) and the output differential current ($i_{out,d}$) are derived as follows (see Fig. 3),

$$z_{CCG} = \frac{1}{g_{m3,4} + 2sC_{gs3,4}} \tag{1}$$

$$i_{out,d} = g_{m3,4}V_X \tag{2}$$

As inferred from (1), CCG presents a low equivalent impedance (approximately $1/g_{m3,4}$), leading to small voltage swing at the drain of M_1 and M_2. Considering the potential stability issue associated with C_C in the feedback loop (C_B–M_2–C_C–M_3), the required capacitance should be carefully selected to minimize the instability. Thus, even with unequal voltage swings at each source terminal of M_3 and M_4, CCG is capable of delivering balanced currents (and voltages) to the load, generating differential signals for the next stages, as shown in (2).

Conventional S-to-D LNA examples with the feedback networks present an issue with asymmetric output load due to their circuit topologies, imposing potential imbalances on the differential outputs. To reduce amplitude and phase mismatches, CG-CS LNAs with a symmetrical load and active feedback networks have been proposed [10], [11]. By including additional transistors in the feedback loop, however, they consume more DC power and can support a limited frequency range only. To overcome these drawbacks, the transformer-based feedback network consisting of primary and secondary inductors (L_1 and L_2) and a feedback resistor (R_F) is proposed in this work (Fig. 2). The secondary inductor of the transformer senses the differential output current, and the coupled current from the output is combined with the single-ended input signal at the gate of the first CS stage (M_1).

The amount of feedback current is determined by the voltage across the secondary inductor and the feedback resistance. The loop broadens the input and the output matching characteristics by optimizing feedback impedance and shunt peaking, respectively. For input matching, the combination of the feedforward and the feedback impedance should be set to have an input pole located at higher frequency than the output pole for wideband operation. At the output node, the primary coil acts as a shunt peaking inductor with the series resistors (R_D) to extend the output bandwidth. Therefore, the proposed S-to-D LNA with the transformer-based reactive feedback network can achieve wideband input/output matching characteristics. Due to the use of a symmetrically shaped transformer structure, it presents the well-defined balanced load over the low-band UWB frequency range for differential operation without consuming additional DC power in the feedback network.

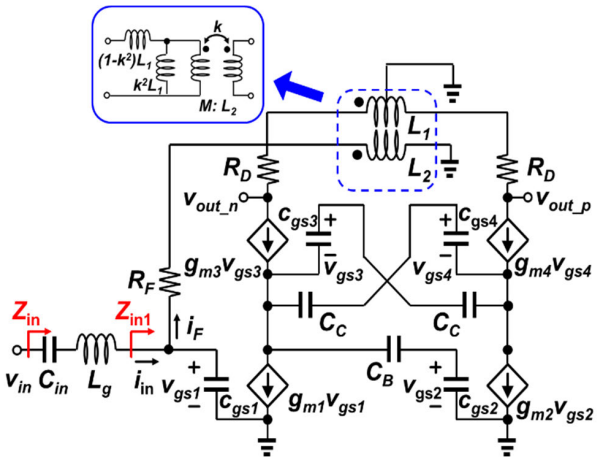


FIGURE 4. Small-signal equivalent circuit of the proposed S-to-D LNA. (Biasing circuity not shown). The simplified equivalent model of the transformer is given in the blue box.

B. INPUT IMPEDANCE MATCHING

The core schematic of the proposed S-to-D LNA with the transformer-based reactive feedback network is in Fig. 4. (Biasing is not shown). All transistors (M_1–M_4) are in saturation region and they are modeled as gate-to-source capacitances (c_{gs1}–c_{gs4}) and transconductance (g_{m1}–g_{m4}). Other parasitic capacitances of MOSFETs and all secondary effects such as channel-length modulation are neglected for simplicity ($r_o = \infty$). In the schematic, CS, CCG, and the load (R_D and the transformer) are assumed to be symmetric. Furthermore, because by-pass or DC-block capacitors are much greater than device capacitances, they are absorbed into the transistor capacitance in the analysis.

$$c_{gs1,2} \cong C_C \parallel c_{gs1,2} \tag{3}$$

$$c_{gs3,4} \cong C_C \parallel c_{gs3,4} \tag{4}$$

Regarding the transformer, the equivalent model is shown in the inset (blue box) of Fig. 4. Its turns ratio (n) and mutual inductance (M) are given below.

$$n = \sqrt{\frac{L_1}{L_2}} \tag{5}$$

$$M = k\sqrt{L_1 L_2}, \tag{6}$$

where k is the coupling factor and $L_{1,2}$ is the self-inductance of the transformer. Since the loop generates a voltage output and returns a current to the input, the configuration is the shunt-shunt negative feedback. To derive the input impedance, we need to know the open-loop impedance by breaking the feedback path. The open-loop impedance ($Z_{in1,OL}$) is obtained as,

$$Z_{in1,OL} = \frac{1}{R_F} \parallel \frac{1}{sc_{gs1}} \times \parallel \left[\frac{2k^2 R_D}{n^2} \parallel sk^2 L_2 + s\left(1-k^2\right) L_2 + R_F \right] \tag{7}$$

In order to derive the closed-loop impedance ($Z_{in1,CL}$), the open-loop transconductance gain ($A_{RO,OL}$) and the feedback factor (k_f), which is the gain from the output voltage to the returned current, are expressed as below.

$$A_{R0,OL} = \frac{sc_{gs1,2}R_F}{1+sc_{gs1,2}R_F} \cdot \frac{g_{m1}^2}{sc_{gs1}\left(g_{m1}+sc_{gs1}\right)} \times \left[2R_D + s\left(1-k^2\right)L_1 + sk^2 L_1 \parallel k^2 n^2 R_F \right] \tag{8}$$

$$k_f = \frac{1}{R_F} \cdot \frac{1}{kn} \times \frac{sk^2 L_1 \parallel k^2 n^2 R_F}{2R_D + s\left(1-k^2\right)L_1 + sk^2 L_1 \parallel k^2 n^2 R_F} \tag{9}$$

Now, the closed-loop impedance ($Z_{in1,CL}$) is divided by the factor of ($1 + A_{RO,OL}$ x k_f [loop gain]). Then, the final input impedance (Z_{in}) of the entire proposed S-to-D LNA is obtained by summing the three series impedance components of C_{in}, L_g, and $Z_{in1,CL}$ as follows.

$$Z_{in1,CL} = \frac{Z_{in1,OL}}{1+k_f A_{R0,OL}} \tag{10}$$

$$Z_{in} = \frac{1}{sC_{in}} + sL_g + Z_{in1,CL} \tag{11}$$

As $Z_{in1,CL}$ is reduced by the feedback loop, the real part of the total input impedance can be adjusted close to 50 Ω and the remaining imaginary is set to zero by the proper selection of C_{in} and L_g. Once the transistor ratio (W/L) is chosen, the device transconductance is fixed under a given bias condition, and then the remaining variables such as transformer parameters (k, n and M) should be optimized for wideband matching.

C. VOLTAGE GAIN AND NOISE FIGURE

The open-loop gain is primarily determined by $g_{m1,2}$ and load impedance with shunt peaking. Since the negative feedback loop is formed, the open-loop gain should be maximized for utilizing feedback properties such as the bandwidth extension of the circuit. As the expressions of the open-loop transconductance gain [$A_{RO,OL}$ in (8)] and the feedback factor [k_f in (9)] have been derived in the previous section, the calculation of the transfer function of the S-to-D LNA is now straightforward. First, the closed-loop gain ($A_{R0,CL}$) is derived using a feedback equation as follows.

$$A_{R0,CL} = \frac{A_{R0,OL}}{1+k_f A_{R0,OL}} \tag{12}$$

Therefore, the overall single-to-differential voltage gain (A_V) based on (12) is shown below.

$$\begin{aligned} A_V &= \frac{v_{out\_p} - v_{out\_n}}{v_{in}} = \frac{i_{in}}{v_{in}} \cdot \frac{v_{out\_p} - v_{out\_n}}{i_{in}} \\ &= \frac{1}{\frac{1}{sC_{in}} + sL_g + Z_{in1,CL}} \cdot A_{R0,CL} \\ &= \frac{1}{\frac{1}{sC_{in}} + sL_g + \frac{Z_{in1,OL}}{1+k_f A_{R0,OL}}} \cdot \frac{A_{R0,OL}}{1+k_f A_{R0,OL}} \end{aligned} \tag{13}$$

Noise figure (NF) of the proposed S-to-D LNA is dependent on the noise sources in the circuit and the voltage gain under the closed-loop configuration. Since the LNA operates in a radio-frequency range, the flicker noise can be neglected in the noise analysis and the white noise of resistors and MOSFETs affects overall noise performance. Among many noise sources, the dominant contributions are from the thermal noise (R_{Lg}) of the on-chip gate inductor, the feedback resistor noise (R_F), and the channel thermal noise ($4kT\gamma g_{m1,2}$) of CS transistors (M_1 and M_2), whereas other noise sources such the parasitics of the transformer, R_D, and channel noise of $M_{3,4}$ were neglected for simplicity. The NF of an LNA can be obtained using the following general equation.

$$NF = 1 + \frac{\overline{V_{n,LNA}^2}}{4kTR_S\,|\alpha|^2 A_v^2}, \tag{14}$$

where k, T, R_S, and α are the Boltzmann constant, absolute temperature, the source impedance, and impedance division factor between the source and the circuit, which will be unity under a perfect input-matching condition, respectively. $\overline{V_{n,LNA}^2}$ in (14) is the power spectrum density of the output noise voltage and its expression is derived as below.

$$\overline{V_{n,LNA}^2} = 4kT\,|\alpha|^2 A_v^2 \left(R_{Lg}+R_F\right) + 4kT\gamma \cdot \left(\frac{1}{g_{m1}} + \frac{\omega^2 c_{gs1,2}^2}{g_{m2}}\right) \cdot Z_{in1,CL}^2 \cdot A_{R0,CL}^2 \tag{15}$$

Whereas the above equations have some limitations due to the simplified parasitics associated with the circuit components and the layout, they could be used for setting initial parameter values and optimizing performance numbers.

D. PERFORMANCE OPTIMIZATION

By using the design equations (7)-(15), the LNA performance parameters such as matching, gain, noise figure can be optimized, while minimizing DC power consumption. Regarding transistor sizing, the length of all core transistors (M_{1-4}) was set to the minimum value available in the design kit for better

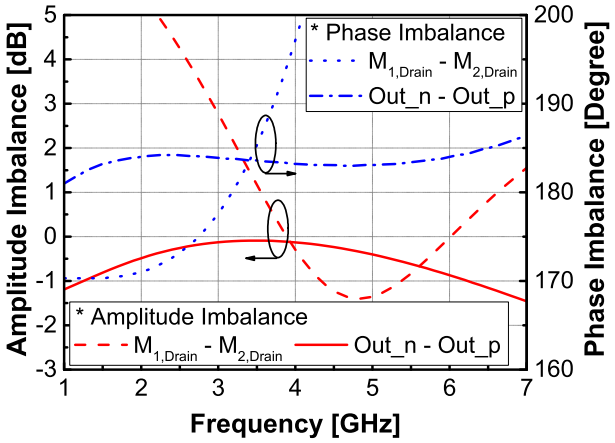


FIGURE 5. Simulation results of (a) amplitude mismatches and (b) phase mismatches.

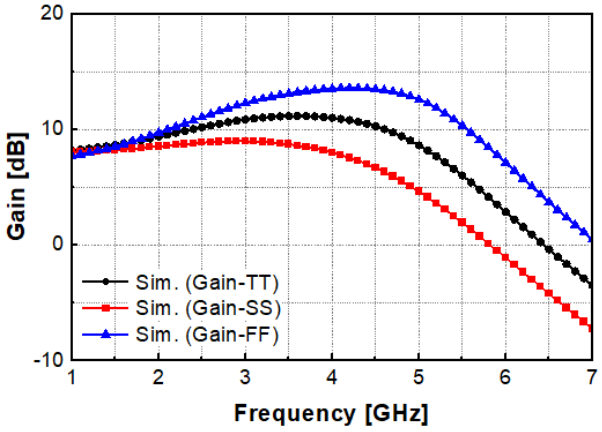


FIGURE 6. Simulation results of the gain of the proposed S-to-D LNA with different process corners.

dc and ac characteristics. The width of the common-source transistors (M_1 and M_2) was determined, considering multiple performance metrics. Under the given power budget of the circuit, the transconductance (g_m) was maximized for better open-loop gain, whereas the parasitic capacitances were optimized to obtain wider operational bandwidth and lower noise figure. For the transistors in the current balancer (M_3 and M_4), since they provided a current gain about unity, their width was set to be wide enough to conduct biasing currents and deal with large signals with minimal addition of parasitic capacitances.

One of the important aspects of the optimization was to minimize mismatches in the output signals. In Fig. 5, simulated amplitude and phase imbalances of differential nodes of the circuit are presented. With the help of the current balancer, overall imbalances were significantly minimized at the differential outputs in comparison with the drain nodes of M_1 and M_2. After passing the current balancer, the amplitude and the phase differences were reduced from 2.6 to 0.5 dB and about 8 to 1.7 degrees, respectively. In addition, the global feedback broadens frequency characteristics of the circuit at the output nodes. It should be noted that the results in Fig. 5 were obtained, using ac simulations, which were in general different from scattering-parameter (S-parameter) simulations.

In terms of process variations, the performance of the proposed S-to-D LNA was affected by transistor corners, as shown in Fig. 6. For example, faster transistors led to an increase in gain and a decrease in NF. Between the fast and the slow corners, the gain and NF variations at the center frequency (4 GHz) were about $+/-$ 3.5 dB and $+/-$ 0.5 dB, respectively. In order to provide tuning knobs after chip fabrication, adjustable bias currents and voltages were implemented.

The layout of a transformer and inductors plays an important role in circuit design to achieve the overall performance. As the key component of the proposed S-to-D LNA design, the transformer feedback network should be carefully drawn to reduce loss associated with its shape and interconnection structures, lowering parasitics and simplifying device the geometry. In Fig. 7, the physical structure of the transformer is shown. The width of the spiral was 4 μm and the spacing was 8 μm. The inner radius was 62 μm and the distance between the outmost spiral and the guard ring was 25 μm. To design the inductor and the transformer with a high quality (Q) factor, the top metal layer (metal 6) was used, which has the maximum thickness with the lowest conductor loss. At the same time, however, the feedback resistor (R_F) was needed to broaden the circuit response with an acceptable noise degradation. All inductors, interconnection lines, and RF pads were simulated with an electromagnetic (EM) solver for accurate performance prediction.

Table 1 summarizes the final values of parameters used in the design of the proposed S-to-D LNA with transformer-based feedback. For MOSFETs, the minimum length was selected for best gain and noise performance and other parameters required iterations for fine optimization. The C's and L's listed refers to values at the center frequency. The full-circuit simulation results will be compared with the measurement in the next section. The experimental results show that the proposed wideband S-to-D LNA with a symmetric output load is a suitable topology for low imbalances in differential signals at the output nodes and wideband matching characteristics for a variety of UWB applications.

III. EXPERIMENTAL RESULTS

The proposed transformer-based S-to-D LNA with negative feedback network was fabricated using a commercial 0.18 μm CMOS process. In order to facilitate the measurement of the large- and small- signal performance under a standard 50 Ω condition, source-follower buffer stages, where MOSFETs with a width of 200 μm were employed, were integrated at the output ports of the S-to-D LNA. The total chip area including the pads was 0.5×0.8 mm^2 ($= 0.4$ mm^2) and its micrograph is shown in Fig. 8. Except the single-ended input and the differential output lines of each side, the core layout of the S-to-D LNA was kept symmetric as much as possible to suppress even order harmonics.

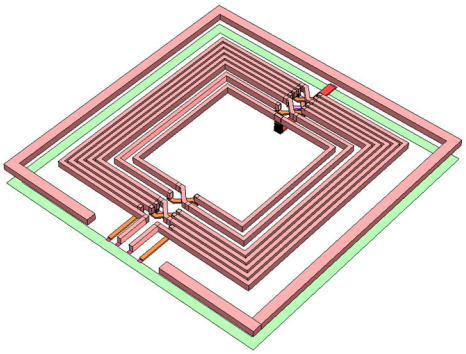


FIGURE 7. A 3D view of transformer layout.

TABLE 1. Summary of design parameters.

Parameter	Value	Unit
W/L (M_1, M_2)	300/0.18	μm
W/L (M_3, M_4)	150/0.18	μm
C_{in}	1.8	pF
C_B	803	fF
C_C	608	fF
L_g	4.31	nH
L_1	6.98	nH
L_2	1.91	nH
k	0.72	-
R_D	81	Ω
R_F	876	Ω

During measurement, the S-to-D LNA chip was connected to a 1.8 V DC voltage supply for biasing and it pulled a quiescent current of 5.5 mA, which corresponded to 9.9 mW, excluding the power consumption of the source-follower output stages. The small-signal performance metrics were characterized by on-wafer probing with a GSG and a GSGSG probes. S-parameters were measured with a 4-port vector network analyzer (Agilent PNA-X N5247A) and for calibration a short-open-load-through (SOLT) substrate kit was utilized.

The measured and the simulated S-parameters are shown in Fig. 9. In general, the simulation results were matched to the measurement response in terms of overall shape and resonant frequencies. The measured (differential) gain was slightly larger than the simulation primarily due to slight under-estimation of the transformer parameters. Within the UWB range (from 3.0 to 5.0 GHz), the measured peak power gain was 12.6 dB. Considering the conventional definition of 3-dB bandwidth, the operation frequency included a range of 1.8-5.8 GHz. In addition to differential gain, the single-ended gain (S_{21} and S_{31}) response was plotted in Fig. 8. Both power gain curves to each output have similar values across the operation bandwidth. Regarding input matching, the return loss was better than 9 dB in the 3-dB bandwidth range. Hence, based on the measured small-signal performance, it is verified that the proposed LNA design approach could be a strong viable solution for the S-to-D conversion with moderate gain and matching characteristics. The output matching response was below 10 dB within the operation frequencies.

In Fig. 10(a), the measured and the simulated noise figure (NF) are presented. The simulated NF was very close until about 3.5 GHz, but at higher frequencies, it showed some deviations against the simulation, which are associated with model accuracies and parasitic extraction. From the measurement, the overall NF was between 3.3 and 5.8 dB across the lower UWB band. The measured large-signal performance is shown in Fig. 10(b). For power measurement, an off-chip balun was connected to the differential outputs of the circuit, and then, a power meter monitored the single-ended signal. The parasitics and the loss of cables and the balun were de-embedded. The input 1-dB compression point (IP1dB) and the input third-order intercept point (IIP3) were approximately about -15 dBm and -5 dBm at 4 GHz, respectively.

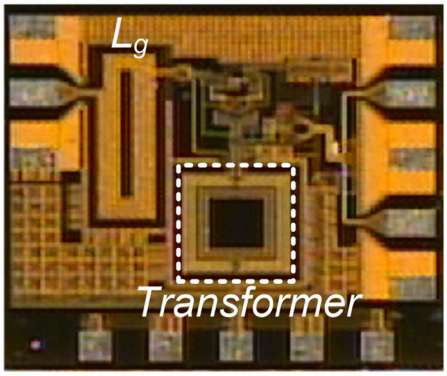


FIGURE 8. Chip micrograph of the proposed S-to-D LNA with the transformer-based negative-feedback network.

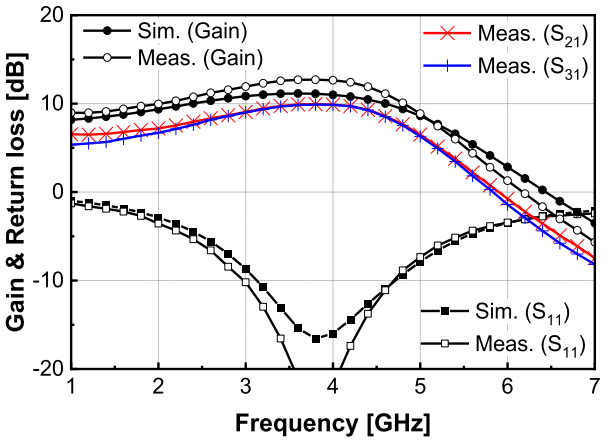


FIGURE 9. Simulated and measured single-to-differential power gain, single-ended-output power gain (S_{21} and S_{31}), and input impedance matching (S_{11}) versus frequency.

IV. DISCUSSION

Table 2 summarizes the key features of recently published wideband S-to-D LNAs and compares the performance of the proposed S-to-D LNA with other designs. The proposed LNA support full-chip integration for simple system configuration and exhibits balanced performance, demonstrating wide operation bandwidth and a symmetric load structure for low mismatches at the output by using the transformer-based negative feedback network and the CCG differential current balancer. The performance parameters such as gain, NF,

TABLE 2. Comparison with recently published wideband CMOS S-to-D LNAs.

Ref.	JSSC 2008 [9]	TCAS I 2020 [12]	TCAS II 2022 [13]	MWCL 2021 [14]	TCAS II 2021 [15]	TCAS I 2022 [16]+	**This work**
Technology [nm]	CMOS 65	CMOS 65	CMOS 65	CMOS 130	CMOS 180	CMOS 130	**CMOS 180**
Architecture	CG-CS w. active feedfoward	CG-CS w. active negative feedback	CG-CS w. positive feedback	CG-CS w. cascaded CS stages	Double CG-CS w. active negative feedback	CS-CS w. active negative feedback	**CS-CS w. transformer negative feedback**
Symmetric Load	No	Yes	Yes	No	No	No	**Yes**
Balun Function	Yes	Yes	Yes	Yes	Yes	Yes	**Yes**
Frequency [GHz]	0.2 - 5.2	0.05 - 1.3	0.47 - 3.3	0.1 - 1.0	0.13 - 0.93	0.05 - 0.7	**3.0 - 5.0**
Power Gain [dB]	7.0 - 9.6	24 - 27.5	19.5 - 22.0	9.0 - 15.0	16.6 - 19.6	23.5 - 26.5	**8.8 - 12.6**
NF [dB]	2.9 - 3.5	2.3 - 3.0	2.6 - 3.5	4.0	3.6 - 5.0	<4.25	**3.3 - 5.8**
IIP3 [dBm]	0.0	-2.2	2.8	2.0	-8.5	-11.5	**-5.0**
P_{DC} [mW]	14.0	5.7	12.5	2.7	3.0	33.6	**9.9**
Size (core) [mm^2]	0.01	0.05	0.06	0.01	0.18	2.0	**0.25 (0.4)***
Full integration (on-chip)	No	No	No	No	Yes	Yes	**Yes**

* Full chip area including measurement pads and output buffer stages
\+ Wideband operation mode

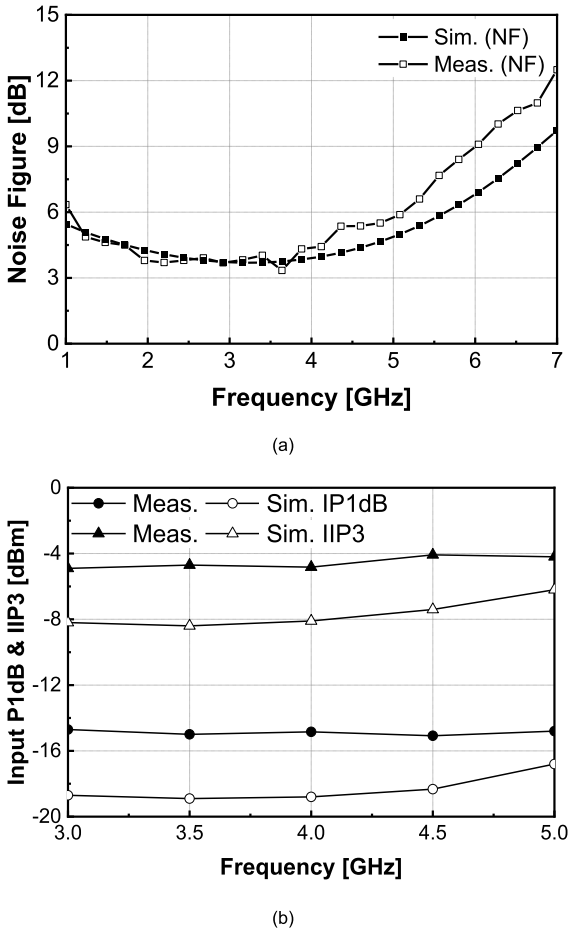


FIGURE 10. Simulated and measured (a) noise figure (NF) of the proposed wideband S-to-D LNA and (b) input 1-dB compression point (IP1dB) and input third-order intercept point (IIP3) versus frequency.

chip size, and power consumption are competitive with the other designs, depending on various system requirements. Regarding the chip size, it is worth noting that the level of integration is different for each design. Some references utilized off-chip inductors, capacitors, or bias tees for injecting RF signals or biasing the circuit [9], [12], [13], [14]. These components, however, are difficult to be integrated on-chip in general due to large areas or poor performance, so they are often placed on circuit boards. In addition, the use of on-chip inductors, as in this work, increases the overall chip area, but it is almost indispensable for supporting high-frequency operation.

Among many parameters of S-to-D LNAs, the imbalance performance deserves special attention since receivers with modern complex modulation/demodulation scheme are sensitive to mismatches in signal amplitude and phase [17]. In Fig. 11, the amplitude and the phase imbalances are shown versus frequency. At low frequencies, the simulation results reasonably match to the measurement response, but the deviations become larger as frequency increases due to physical asymmetries of components and their interconnection parasitics. The proposed S-to-D LNA exhibits the maximum gain and the phase imbalances of 0.2 dB and 2.3° within the target UWB frequency range (3.0 - 5.0 GHz), respectively. This is the benefit of employing the CCG current-balance structure and a symmetric transformer at the output of the LNA.

In order to evaluate the overall performance of the proposed S-to-D LNA in comparison with the state-of-the-art designs, the figure-of-merit (FoM) equation is used for comparison [18].

$$FoM = \frac{1000 \times Gain \times f_{center} \times BW}{(NF - 1) \times P_{DC} \times (A.E. - 1) \times (P.I/360°) \times (f_T)^3}, \quad (16)$$

where a center frequency (f_{center}), a bandwidth (BW), and a unity-gain frequency (f_T) are in GHz unit and noise figure

TABLE 3. Figure-of-merit (FoM) comparison including amplitude and phase imbalance.

Ref.	JSSC 2008 [9]	TCAS I 2020 [12]	TCAS II 2021 [15]	TMTT 2017 [19]	TCAS I 2019 [20]	TMTT 2012 [21]	This work
Technology [nm]	CMOS 65	CMOS 65	CMOS 65	SiGe 180	CMOS 65	CMOS 130	**CMOS 180**
Unity-gain frequency (f_T) [GHz]*	160	160	60	200	160	100	**50**
Frequency [GHz]	0.2 - 5.2	0.05 - 1.3	0.1 - 1	22 – 32.5	0.05 - 1	0.1 – 2.0	**3.0 - 5.0**
Power Gain [dB] (min.)	7.0	24	16.6	15.6	24	13.6	**8.8**
Noise Figure [dB] (max.)	3.5	3.0	5	6	3.3	3.8	**5.8**
Amplitude error [dB] (max.)	0.7	0.25	0.75	1.8	0.4	0.5	**0.2**
Phase imbalance [°] (max.)	2	0.5	7.5	12	5	5	**2.3**
P_{DC} [mW]	14.0	5.7	12.5	2.7	3.0	33.6	**9.9**
FoM [(mW·GHz)$^{-1}$]	0.91	23.3	1.13	1.88	0.13	2.76	**42.7**

* Approximate numbers of the technology used in the implementation of S-to-D LNAs

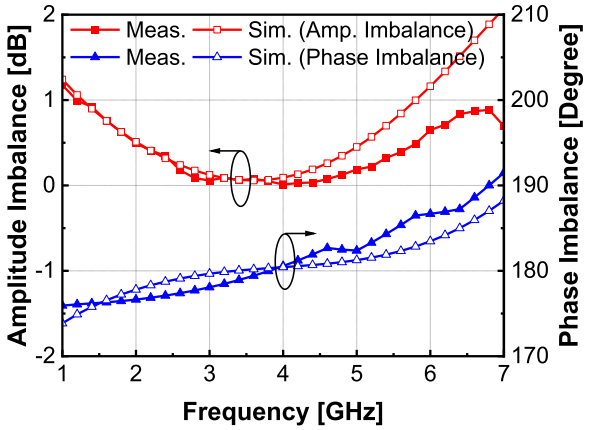


FIGURE 11. Simulated and measured amplitude/phase imbalances at the output nodes.

(NF) and (differential) amplitude error (A.E.) are in absolute scale. In addition, a phase imbalance (P.I.) and power consumption (P_{DC}) are in degree and mW, respectively. In order to remove (or decouple at least) technology-dependency of performance parameters, the term f_T^3 was included in the denominator of the FoM equation.

The performance of relevant S-to-D LNAs are summarized in Table 3. Metrics including amplitude/phase imbalance represent the worst-case number within the operation frequency of the circuits. To calculate FoM of each design, an approximate f_T number of a process technology was used, which may not be accurate in some cases. With the help of the minimized amplitude/phase imbalances, however, the proposed circuit achieved the highest FoM among various high-performance S-to-D LNAs.

V. CONCLUSION

In this work, the wideband single-ended-to-differential (S-to-D) LNA with the transformer-based negative feedback network is introduced. The proposed on-chip transformer feedback not only provides the differential-to-single-ended feedback network with a symmetric output load, but also acts as a shunt-peaking inductor to widen the operation frequency range. The proposed S-to-D wideband LNA achieves a maximum power gain of 12.6 dB, minimum NF of 3.3 dB, while maintaining wide input impedance matching from 3.0 to 5.0 GHz for the low-band UWB applications. Therefore, the proposed S-to-D LNA topology is expected to be applicable to various wideband systems and applications.

REFERENCES

[1] T. Otim, A. Bahillo, L. E. Díez, P. Lopez-Iturri, and F. Falcone, "Towards sub-meter level UWB indoor localization using body wearable sensors," *IEEE Access*, vol. 8, pp. 178886–178899, 2020, doi: 10.1109/ACCESS.2020.3027669.

[2] S. G. Kim, I. C. Ko, and S. H. Jung, "High resolution CMOS IR-UWB radar for non-contact human vital signs detection," in *Proc. IEEE Radio Freq. Integr. Circuits Symp. (RFIC)*, Aug. 2020, pp. 27–30, doi: 10.1109/RFIC49505.2020.9218284.

[3] D.-H. Kim, A. Farhad, and J.-Y. Pyun, "UWB positioning system based on LSTM classification with mitigated NLOS effects," *IEEE Internet Things J.*, vol. 10, no. 2, pp. 1822–1835, Jan. 2023, doi: 10.1109/JIOT.2022.3209735.

[4] T. Liu, B. Li, and L. Yang, "Phase center offset calibration and multipoint time latency determination for UWB location," *IEEE Internet Things J.*, vol. 9, no. 18, pp. 17536–17550, Sep. 2022, doi: 10.1109/JIOT.2022.3155736.

[5] S. K. Gupta, S. Kumar, and A. Sharma, "A miniaturized dual-resonator-based high-capacity chipless radio frequency identification tag sensor," *IEEE Sensors Lett.*, vol. 6, no. 11, pp. 1–4, Nov. 2022, doi: 10.1109/LSENS.2022.3218503.

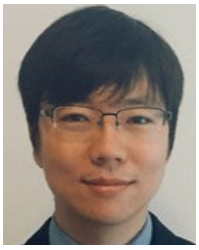
[6] B. Razavi, *RF Microelectronics*, 2nd ed. Upper Saddle River, NJ, USA: Prentice-Hall, 2011.

[7] N. Vitee, H. Ramiah, P.-I. Mak, J. Yin, and R. P. Martins, "A 3.15-mW +16.0-dBm IIP3 22-dB CG inductively source degenerated balun-LNA mixer with integrated transformer-based gate inductor and IM2 injection technique," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 28, no. 3, pp. 700–713, Mar. 2020, doi: 10.1109/TVLSI.2019.2950961.

[8] H. Wang, L. Zhang, and Z. Yu, "A wideband inductorless LNA with local feedback and noise cancelling for low-power low-voltage applications," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 57, no. 8, pp. 1993–2005, Aug. 2010, doi: 10.1109/TCSI.2010.2042997.

[9] S. C. Blaakmeer, E. A. M. Klumperink, D. M. W. Leenaerts, and B. Nauta, "Wideband balun-LNA with simultaneous output balancing, noise-canceling and distortion-canceling," *IEEE J. Solid-State Circuits*, vol. 43, no. 6, pp. 1341–1350, Jun. 2008, doi: 10.1109/JSSC.2008.922736.

[10] P.-I. Mak and R. P. Martins, "A 0.46-mm^2 4-dB NF unified receiver front-end for full-band mobile TV in 65-nm CMOS," *IEEE J. Solid-State Circuits*, vol. 46, no. 9, pp. 1970–1984, Sep. 2011, doi: 10.1109/JSSC.2011.2157264.
[11] D. Im, I. Nam, and K. Lee, "A CMOS active feedback balun-LNA with high IIP2 for wideband digital TV receivers," *IEEE Trans. Microw. Theory Techn.*, vol. 58, no. 12, pp. 3566–3579, Dec. 2010, doi: 10.1109/TMTT.2010.2086375.
[12] S. Kim and K. Kwon, "Broadband balun-LNA employing local feedback gm-boosting technique and balanced loads for low-power low-voltage applications," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 67, no. 12, pp. 4631–4640, Dec. 2020, doi: 10.1109/TCSI.2020.3014194.
[13] B. Shirmohammadi and M. Yavari, "A linear wideband CMOS balun-LNA with balanced loads," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 69, no. 3, pp. 754–758, Mar. 2022, doi: 10.1109/TCSII.2021.3105895.
[14] D. Kim, S. Jang, J. Lee, and D. Im, "A broadband PVT-insensitive all-nMOS noise-canceling balun-LNA for subgigahertz wireless communication applications," *IEEE Microw. Wireless Compon. Lett.*, vol. 31, no. 2, pp. 165–168, Feb. 2021, doi: 10.1109/LMWC.2020.3042233.
[15] S. Tiwari and J. Mukherjee, "An inductorless wideband gm-boosted balun LNA with nMOS-pMOS configuration and capacitively coupled loads for sub-GHz IoT applications," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 68, no. 10, pp. 3204–3208, Oct. 2021, doi: 10.1109/TCSII.2021.3074462.
[16] D. Kim and D. Im, "A reconfigurable balun-LNA and tunable filter with frequency-optimized harmonic rejection for sub-GHz and 2.4 GHz IoT receivers," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 69, no. 8, pp. 3164–3176, Aug. 2022, doi: 10.1109/TCSI.2022.3169364.
[17] M. Mokhtar, A. Gomaa, and N. Al-Dhahir, "OFDM AF relaying under I/Q imbalance: Performance analysis and baseband compensation," *IEEE Trans. Commun.*, vol. 61, no. 4, pp. 1304–1313, Apr. 2013, doi: 10.1109/TCOMM.2013.020813.120576.
[18] M. El-Nozahi, E. Sánchez-Sinencio, and K. Enesari, "A millimeter-wave (23–32 GHz) wideband BiCMOS low-noise amplifier," *IEEE J. Solid-State Circuits*, vol. 45, no. 2, pp. 289–299, Feb. 2010, doi: 10.1109/JSSC.2009.2038126.
[19] C. Geha, C. Nguyen, and J. Silva-Martinez, "A wideband low-power-consumption 22–32.5-GHz 0.18-μm BiCMOS active balun-LNA with IM2 cancellation using a transformer-coupled cascode-cascade topology," *IEEE Trans. Microw. Theory Techn.*, vol. 65, no. 2, pp. 536–547, Feb. 2017, doi: 10.1109/TMTT.2016.2623778.
[20] S. Kim and K. Kwon, "A 50-MHz–1-GHz 2.3-dB NF noise-cancelling balun-LNA employing a modified current-bleeding technique and balanced loads," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 66, no. 2, pp. 546–554, Feb. 2019, doi: 10.1109/TCSI.2018.2866184.
[21] J. Kim and J. Silva-Martinez, "Wideband inductorless balun-LNA employing feedback for low-power low-voltage applications," *IEEE Trans. Microw. Theory Techn.*, vol. 60, no. 9, pp. 2833–2842, Sep. 2012, doi: 10.1109/TMTT.2012.2206825.



ICKHYUN SONG (Member, IEEE) received the B.S. and M.S. degrees in electrical engineering from Seoul National University, Seoul, Republic of Korea, in 2006 and 2008, respectively, and the Ph.D. degree in electrical and computer engineering from Georgia Institute of Technology, Atlanta, GA, USA, in 2016.

From 2008 to 2012, he was a Design Engineer with Samsung Electronics, Hwasung, Republic of Korea, where he contributed to the development of next-generation memory products. From 2017 to 2018, he was a Research Engineer with Georgia Institute of Technology. In 2018, he joined as an Assistant Professor with the School of Electrical and Computer Engineering, Oklahoma State University. Since 2021, he has been with the Department of Electronic Engineering, Hanyang University, Seoul. His research interests include extreme-environment electronics, RF/microwave circuits and systems, memory technologies, and device physics and modeling.

Dr. Song was a recipient of the 2007–2008 Samsung Semiconductor Scholarship, the Silver Paper Award at the 2007 IEEE Seoul Section Student Paper Contest, the Gold Prize at the 2008 Samsung HumanTech Paper Award, the 2012–2013 Fulbright Graduate Study Award, the 2016 Georgia Electronic Design Center (GEDC) Best Poster Award, and the 2022 IEIE Semiconductor Society Excellence Paper Award.

SANG GYUN KIM (Member, IEEE) received the B.S., M.S., and Ph.D. degrees in electronics engineering from Kwangwoon University, Seoul, South Korea, in 2012, 2014, and 2017, respectively.

In 2017, he joined GRIT CIC Inc., Seoul, to develop CMOS RF/analog integrated circuits. His research interests include CMOS RF/analog IC design for satellite communications and UWB/FMCW radar transceivers.

SEUNG HWAN JUNG (Member, IEEE) received the B.S., M.S., and Ph.D. degrees in electronics engineering from Kwangwoon University, Seoul, South Korea, in 2005, 2007, and 2011, respectively.

Since 2009, he has been with Silicon Research and Development, Seoul, where he has been involved in the development of mobile TV RF front-end, GPS, and UWB/FMCW radar. In 2017, he founded GRIT Custom-IC Inc., where he is currently the CEO and develops UWB/FMCW radar ICs and CMOS-based RF/analog RFICs. His research interests include CMOS RF/analog IC design for wired/wireless communication and radar transceivers.

MOON-KYU CHO (Member, IEEE) received the B.S., M.S., and Ph.D. degrees in electronic engineering from Kwangwoon University, Seoul, South Korea, in 2009, 2011, and 2014, respectively.

In October 2014, he joined Georgia Electronic Design Center (GEDC), Institute for Electronics and Nanotechnology (IEN), Georgia Institute of Technology, Atlanta, GA, USA, as a Research Engineer. Since 2021, he has been with the Department of Computer Engineering, Korea National University of Transportation, Chungju-si, Chungcheongbuk-do, Republic of Korea. His current research interests include wide-/narrow-band phased-array antenna systems, integrated radio and radar systems in silicon and III-V technologies for wireless communications, wireless sensing and detection, and imaging applications at RF, microwave, millimeter-wave, and sub-millimeter-wave regimes.

Dr. Cho was a recipient of the 2011 and 2012 Best Paper Award of the IEEE Electron Device Society, Seoul Chapter, and the 2013 Best Paper Award of the IEEE Solid-State Circuits Society, Seoul Chapter. He was also a recipient of the 2012 and 2013 Best Poster Award and the Best Demo Award of the International SoC Design Conference. He was a co-recipient of the 2016 Georgia Electronic Design Center (GEDC) Best Poster Award.