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RESEARCH ARTICLE

A New Calibration Technique of Electromagnetic Simulators for Accurate Analyses of Microwave Components on Epitaxial Wafers

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ABSTRACT This article describes an innovative methodology to calibrate EM simulators, oriented to monolithic microwave integrated circuit design, in order to achieve the highest level of accuracy achievable in electromagnetic simulation. In particular, a two-stage measurement technique based on two types of network analyzer calibrations is adopted as a practical and accurate process for on-wafer S-parameter measurements of suitable test structures on semiconductor epitaxial wafers. Thus, a substrate parameter set for the electromagnetic simulator is appropriately identified by an optimization process that combines measurements of dedicated simple test structures and the corresponding models in the circuit simulator. The proposed approach allows one to accurately estimate the substrate characteristics without realizing expensive on-wafer structures that require a large substrate area. We will demonstrate, through several comparisons between measurements and electromagnetic simulations of different passive structures, how higher accuracy can be achieved, describing and quantifying the limitations that arise from commonly adopted calibration procedures for electromagnetic simulators.

INDEX TERMS Electromagnetic simulations, GaN HEMTs, microwave semiconductor devices, microwave measurements, on-wafer measurements.

I. INTRODUCTION

Nowadays, the use of electromagnetic (EM) simulations permeates the different fields of the microwave electronics, from modeling [1], [2], [3], [4], [5], [6], [7], [8], [9], [10], [11] to circuit design [12], [13], [14], [15], [16], [17], [18], [19], [20], [21], [22], [23], which has made EM simulators a common tool for microwave engineers. It is worth noticing that the new frontiers of the information and communications technology are increasing over and over the device operating frequencies [24], [25], making EM simulators one of the most essential instruments for the design of future state-of-the-art electronic systems.

The word ''instrument'' is intentionally used in this paper as a keyword for EM simulations. In fact, as well as for any other instrument, EM simulators require dedicated calibration procedures. As a matter of fact, the calibration procedure determines the grade of accuracy achievable by EM simulations.

This paper discusses a new calibration procedure that ensures higher accuracy levels with respect to commonly adopted techniques, without requiring to realize large, expensive calibration structures.

In particular, the substrate parameters required in EM simulations include values related to material properties, such as

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relative permittivity and dielectric loss tangent, as well as the ones related to the geometrical structure, such as substrate thickness and electrode width. In our experience, the most critical parameter is represented by the substrate thickness. This is due to both the uncertainty related to its nominal value (typically around ±10%) and its strong impact on other critical parameters, e.g., the source inductance value in transistor modeling. This, for instance, is of paramount importance in the design of low-noise amplifiers [1].

Conventionally, EM simulators are calibrated using only microstrip line (MSL) test structures. However, we will demonstrate that this method may lead to inaccurate estimations of substrate thickness, strongly affecting simulation accuracy. In our proposed technique, substrate parameters are extracted using both MSLs and a test structure containing one via hole. It is quite intuitive that the via hole represents a very effective structure for correctly estimating substrate thickness. Indeed, the proposed procedure can also be considered as an indirect method to correctly estimate the substrate thickness without using invasive procedures based on electron microscopy.

This article is organized as follows. Section II presents the proposed EM simulator calibration technique. Section III focuses on the design and measurement of test structures, describing the S-parameter characterization steps required to optimize the substrate parameters. Section IV presents the procedure to extract the substrate parameters used in EM simulations by means of schematic-level simulations. In Section V, the extracted substrate parameters are applied to EM simulations of several passive elements to assess the effectiveness of the proposed approach. Finally, Section VI concludes this article.

II. CALIBRATION TECHNIQUE FOR EM SIMULATORS

The proposed calibration technique is based on the characterization of dedicated test structures fabricated on wafers, and on the optimization, in a computer-aided-design (CAD) environment, of the geometrical and physical properties of the adopted materials. In particular, we will show the accuracy improvement achievable with respect to conventional techniques when the exact value of the substrate thickness is unknown, and how the discussed approach represents a practical and inexpensive method for microwave designers to perform accurate EM simulations.

Fig. 1 shows the flowchart describing the proposed EM simulator calibration procedure. It should be emphasized why the flow of the EM simulator calibration should start with the Short-Open-Load-Thru (SOLT) vector network analyzer (VNA) calibration. In principle, the accuracy of SOLT calibration is known to be worse than that of Thru-Reflection-Line (TRL) calibration, especially in the high frequency range, due to the broadband stability of the required characteristics of the calibration kit and the algorithm used to calculate the error terms. However, in the proposed EM simulator calibration approach, the SOLT technique is used, as discussed in detail in the following, only for the estimation of the TRL line characteristic impedance.

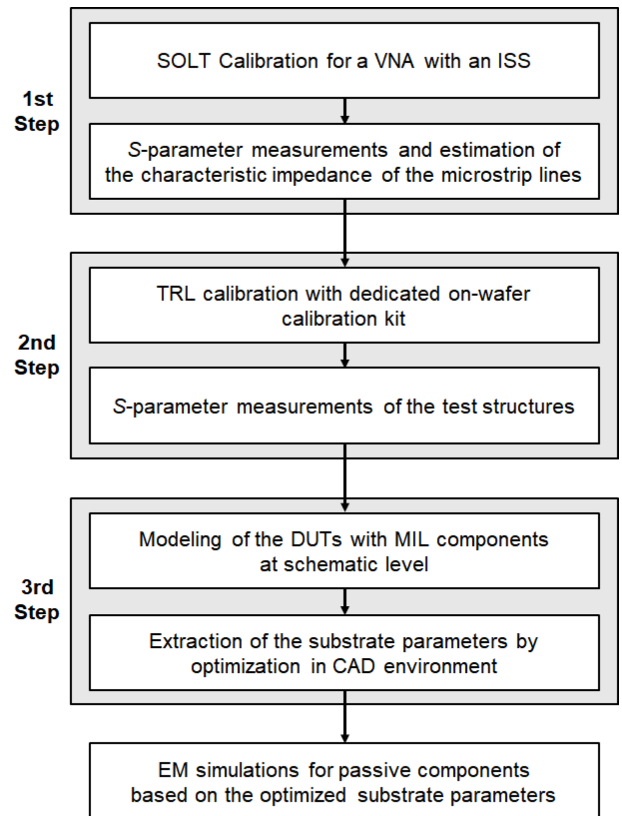

FIGURE 1. Flowchart describing the proposed calibration procedure of the EM simulators.

Usually, the measurement of S-parameters under TRL calibration conditions by a VNA is performed with a reference system impedance of 50 Ω. If the characteristic impedance of the prepared test fixture (pads and feedlines in the case of on-wafer measurement) can be considered sufficiently close to 50 Ω, the accuracy of the measurement is maintained even if the actual characteristic impedance of the calibration standard is unknown. In contrast, if the characteristic impedance of the calibration standard is not so close to 50 Ω, the mismatch with the reference impedance will lead to unacceptable uncertainty in the measurement results, unless its value is estimated in advance by another method [26].

For estimating the characteristic impedance of a feed line for RF probes formed on a semiconductor substrate, an analytical method could be adopted to determine it based on information such as the relative permittivity and thickness of the substrate, and the geometry of the electrodes that configure the feed line [27]. However, it is generally difficult for circuit designers to accurately obtain this information since it requires destructive inspection, such as a detailed observation of the cross-sectional structure, and samples dedicated for analysis. Moreover, there are experimental methods for determining the characteristic impedance of a transmission line based on the propagation constants obtained from

measurement data and on the capacitance in low-frequency measurements [28], [29].

Considering the SOLT-calibrated measurement, at least within the range where an impedance standard substrate (ISS) is valid (up to 15 – 20 GHz), an accurate measurement can be made using 50 Ω as the reference impedance [30]. By using the characteristic impedance obtained from this measurement as the defined value of the characteristic impedance in the subsequent TRL calibration, it is possible to avoid uncertainty regarding the definition of the characteristic impedance in the TRL calibration. Hence, the two-stage calibration of SOLT and TRL provides a practical and sufficiently accurate process for on-wafer measurements for test structures on semiconductor substrates.

In the first step of the proposed procedure in Fig. 1, the VNA is calibrated (SOLT) using the ISS dedicated for RF probes on an alumina substrate. After that, the S-parameters of one on-wafer MSL, shown in Figs. 2(a), 2(c), and 3(c), realized on the investigated substrate, are measured to estimate its characteristic impedance.

The test structures adopted in this work for calibrating the EM simulator, which will be deeply described in the next section, are shown in Fig. 2 and consist of one MSL, having the same characteristic impedance of the lines used in the TRL calibration, not necessarily 50 Ω, and a single via-hole structure. The second step of the EM simulator calibration procedure consists in the S-parameter measurements of both the test structures in Fig. 2. In this phase, we adopt a TRL calibration [31], [32], [33] for which the dedicated on-wafer calibration kit shown in Fig. 3 was preliminary designed and fabricated, and we exploit, in this calibration, the knowledge of the characteristic impedance from step 1.

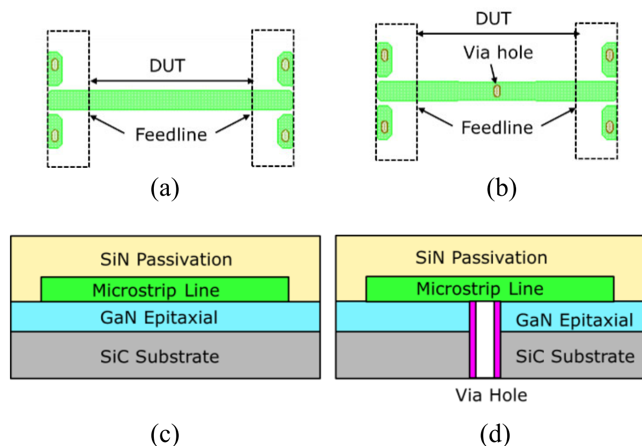

FIGURE 2. Test structures. (a) Top view of the MSL. (b) Top view of the via hole. (c) Cross-sectional view of the MSL. (d) Cross-sectional view of the via hole.

In the third step, the substrate parameters to be used in the EM simulations are optimized by minimizing the discrepancies between the test structure measurements (i.e., MSL and via hole in Fig. 2) and the simulations based on a multilayer interconnect library (MIL) component model provided in the CAD environment [34]. In particular, the models of the test structures, i.e., MSLs and via-hole, are based on the aforementioned MIL component and share the same substrate parameters.

Finally, EM simulations of the passive components are performed using the extracted substrate parameters. The small-signal characteristics are also simulated for DUTs different from those used in the optimization phase, i.e., MSLs with different lengths and via-hole arrays. By comparing these simulations with the measurements, the effectiveness of the extracted substrate parameters for performing accurate EM simulations is definitely assessed.

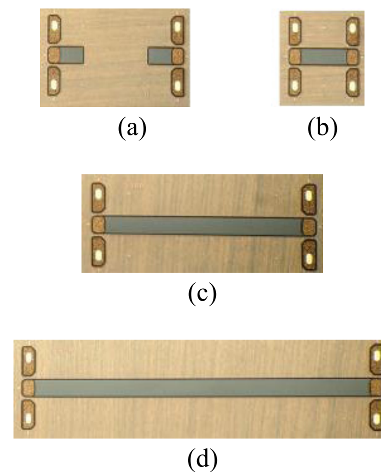

FIGURE 3. On-wafer TRL calibration standards. (a) OPEN. (b) THRU. (c) LINE: 900 μm. (d) LINE: 1800 μm.

III. TEST STRUCTURES AND MEASUREMENTS

This section describes the test structures used to calibrate the EM simulator and reports the required measurements.

Fig. 2 shows the top and cross-sectional views of the MSL and via-hole test structures that were adopted. The test structures consist of the DUT and a feedline, with ground-signal-ground access, for connecting the RF probe to the DUT. This feedline having a length equal to half-thru is directly de-embedded by the TRL calibration, whose standards are reported in Fig. 3. The test structures and calibration kit are both fabricated on top of a GaN epitaxial layer on a SiC substrate with a SiN passivation layer, as shown in the layer structure in Fig. 4, where the nominal thicknesses are also reported. The width and length of the feedline are 110 μm and 200 μm, respectively.

Small-signal characterization was performed using a Keysight Technologies PNA (N5224A) in the frequency range from 1 GHz to 25 GHz.

Initially, the SOLT calibration for the VNA was carried out using an alumina ISS to measure the S-parameters of the microstrip line in Fig. 3(c). These measurements allow one to obtain the characteristic impedance Z_C of the MSLs. In particular, starting from the measured S-parameters and adopting

an ABCD description, Z_C can be obtained as follows:

$$\begin{pmatrix} A & B \\ C & D \end{pmatrix} = \begin{pmatrix} \cosh(\gamma l) & Z_C \sinh(\gamma l) \\ \frac{\sinh(\gamma l)}{Z_C} & \cosh(\gamma l) \end{pmatrix} \quad (1)$$

$$Z_C = \sqrt{\frac{B}{C}} \quad (2)$$

where γ is the propagation constant and l is the line length. Based on the measured S-parameters of the MSL reported in Fig. 2(a), the reference impedance in the TRL calibration was defined as 44 Ω.

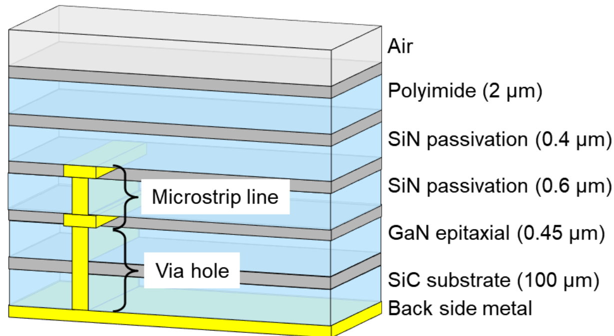

FIGURE 4. Layer structure of the test structures.

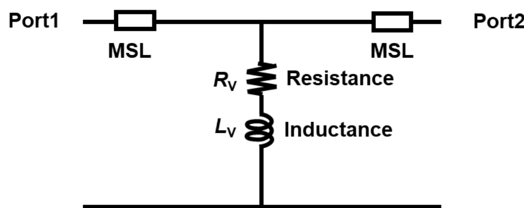

FIGURE 5. Equivalent circuit model of DUT in via-hole test structure.

Then a TRL calibration, fixing the refence plane at the center of the thru, was performed in the frequency range from 1 GHz to 25 GHz. Error boxes were calculated by S-parameter measurements of the standards shown in Fig. 3, adopting the aforementioned SOLT calibration. In particular, we used the StatistiCAL™ VNA Calibration Software Package available from National Institute of Standards and Technology (NIST) [35]. This process completely removes the effects of pads and feedlines in the test structures from the measurement results. To optimize the values of thickness, relative permittivity, and loss tangent of the SiC substrate, GaN epitaxial layer, and SiN passivation layer, the S-parameters of the test structures for both the line and via hole shown in Fig. 2 were measured.

The via-hole test structure consists of a via hole connecting the MSL to the backside metal layer, and is described by a T-shaped equivalent circuit as shown in Fig. 5, where the shunt L corresponds to the inductance of the via hole L_V. This value can be obtained from the imaginary part of Z_{21} by converting the measured S-parameters into Z-parameters, as follows:

$$L_V = Im\left(\frac{Z_{21}}{\omega}\right) \quad (3)$$

where ω is the angular frequency. The inductance of the via hole is inherently related to the geometrical (i.e., thickness) and physical properties of the SiC substrate, GaN epitaxial layer, and SiN passivation layer.

IV. OPTIMIZATION OF SUBSTRATE PARAMETERS

Substrate parameters were extracted based on the S-parameter measurements obtained in Section III. To this end, the MIL components and optimization tools, provided in the CAD environment [34], were used.

TABLE 1. List of nominal values of substrate parameters.

Layer	Thickness (μm)	Relative Permittivity	Loss Tangent
SiN passivation	1	8.6	0.0036
GaN epitaxial	0.45	9.4	0
SiC substrate	100	9.6	0

The MIL is based on the method of moments and can handle arbitrary dielectric layers and arbitrary metal thicknesses, while the skin effect resistance matrix is calculated numerically. Concerning the substrate shown in Fig. 4, the eight parameters to be extracted are the thickness, relative permittivity, and dielectric loss tangent in the SiC substrate and GaN epitaxial layer, and the relative permittivity and dielectric loss tangent in the SiN passivation layer. The thickness of the SiN passivation layer is based on the value monitored during the wafer process. The nominal values of each parameter, which are used as initial values in the optimization, are listed in Table 1. It should be noticed that in the GaN HEMT fabrication process used in this article, the actual SiC substrate thickness of the device may vary from the nominal value within a range of ±10%.

Fig. 6 shows the models that describes the DUTs, i.e., the MSL and via-hole test structures, along with MIL components. The MSL and via hole are described using the *ML1CTL* and *MLVIAHOLE* components of the MIL, respectively. The multilayer structure of the model is described using the *MLSUBSTRATE[N]* component, which corresponds to the layer structure definition in the EM simulator. The thickness of each layer, the relative permittivity, and the width of the MSLs correspond to the values of the respective test structures. The via hole geometry in the model is described as a perfect circle, whereas the actual geometry is a rounded rectangle. However, the diameter values in the model were defined to provide the same inductance value of the rounded rectangle shape when considering the same substrate thickness.

The extraction of the substrate parameters was implemented by minimizing the error between the measurement results obtained in Section II and the simulation results from

TABLE 2. Conditions and results of the substrate optimization.

Condition	Optimized Parameters	Test Structures	Optimized Results		
			Thickness	Permittivity	Loss Tangent
1	Permittivity Loss Tangent	Microstrip Line	T_SiC = 92.0 μm (Fixed) T_GaN = 0.45 μm (Fixed) T_SiN = 1 μm (Fixed)	Er_SiC = 10.0 Er_GaN = 10.1 Er_SiN = 7.7	TanD_SiC = 0.0133 TanD_GaN = 0.0025 TanD_SiN = 0.0045
2	Permittivity Loss Tangent	Microstrip Line	T_SiC = 100.0 μm (Fixed) T_GaN = 0.45 μm (Fixed) T_SiN = 1 μm (Fixed)	Er_SiC = 10.1 Er_GaN = 10.7 Er_SiN = 9.8	TanD_SiC = 0.0053 TanD_GaN = 0.0113 TanD_SiN = 0.0839
3	Thickness Permittivity Loss Tangent	Microstrip Line	T_SiC = 97.3 μm T_GaN = 0.34 μm T_SiN = 1 μm (Fixed)	Er_SiC = 10.1 Er_GaN = 9.7 Er_SiN = 9.1	TanD_SiC = 0.0060 TanD_GaN = 0.0880 TanD_SiN = 0.0616
4	Thickness Permittivity Loss Tangent	Microstrip Line Via Hole	T_SiC = 91.0 μm T_GaN = 0.19 μm T_SiN = 1 μm (Fixed)	Er_SiC = 10.1 Er_GaN = 9.5 Er_SiN = 8.2	TanD_SiC = 0.0115 TanD_GaN = 0.0772 TanD_SiN = 0.0154

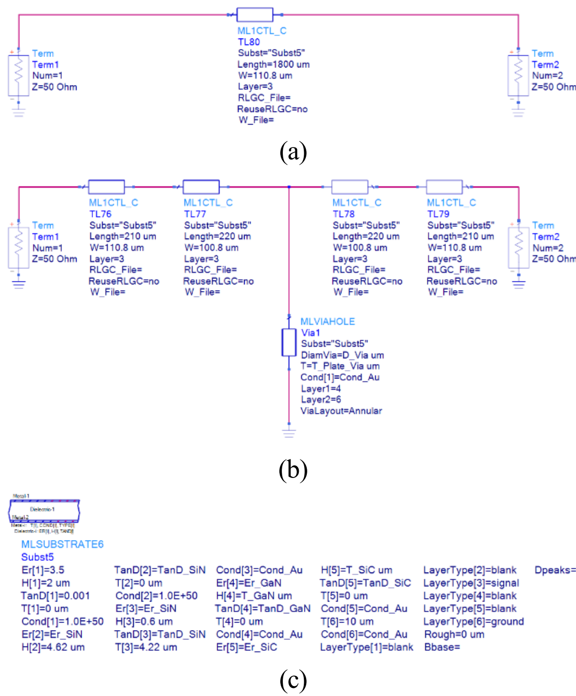

FIGURE 6. MIL component models for the DUTs: (a) MSL and (b) via hole. (c) Multilayer structure.

their MIL models. In addition to the S-parameters, we also considered the characteristic impedance of the MSLs and the via-hole inductance value. The error functions are described by the following equations, where i and j are the port numbers, $freq$ is the frequency index, and the subscripts sim and $meas$ stand for "simulation" and "measurement", respectively:

$$\mathrm{Err1} = \sum_{i,j,freq} \left| Re\left(\frac{S_{ij}^{\mathrm{sim}} - S_{ij}^{\mathrm{meas}}}{S_{ij}^{\mathrm{meas}}} \right) \right| \quad (4)$$

$$\mathrm{Err2} = \sum_{i,j,freq} \left| Im\left(\frac{S_{ij}^{\mathrm{sim}} - S_{ij}^{\mathrm{meas}}}{S_{ij}^{\mathrm{meas}}} \right) \right| \quad (5)$$

$$\mathrm{Err3} = \sum_{freq} \left| Re\left(\frac{Z_{\mathrm{C}}^{\mathrm{sim}} - Z_{\mathrm{C}}^{\mathrm{meas}}}{Z_{\mathrm{C}}^{\mathrm{meas}}} \right) \right| \quad (6)$$

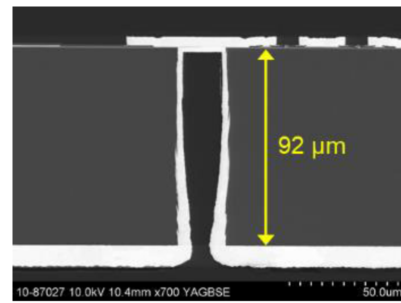

FIGURE 7. Cross-sectional structure of the wafer observed by electron microscopy.

$$\mathrm{Err4} = \sum_{freq} \left| Im\left(\frac{Z_{\mathrm{C}}^{\mathrm{sim}} - Z_{\mathrm{C}}^{\mathrm{meas}}}{Z_{\mathrm{C}}^{\mathrm{meas}}} \right) \right| \quad (7)$$

$$\mathrm{Err5} = \sum_{freq} \left| \frac{L_{\mathrm{V}}^{\mathrm{sim}} - L_{\mathrm{V}}^{\mathrm{meas}}}{L_{\mathrm{V}}^{\mathrm{meas}}} \right| \quad (8)$$

Different experiments were initially considered to extract the substrate parameters. They are reported in Table 2 jointly with the parameter values resulting from the optimization. In conditions 1 and 2, the optimizations were performed using the S-parameters of only one MSL, with the SiC substrate thickness fixed at the value measured by electron microscopy of the cross-section structure shown in Fig. 7, and at the nominal value, respectively. In condition 3, the extraction of all parameters, including substrate thickness, was performed using optimization on only the MSL. Finally, as requested by the new calibration technique we are proposing, condition 4 considers the optimization of all parameters, including substrate thickness, using one MSL and the additional via-hole structure in Fig. 2(b). In Fig. 8, the frequency dependence of the real and imaginary parts of the characteristic impedance of the MSL and the inductance of the via hole calculated with the models shown in Fig. 6 based on the optimized parameters are compared with the measurements. As expected, for the characteristic impedance, condition 3 in Table 2, in which all parameters were optimized using one MSL, showed the best agreement with the measurements, whereas for the via-hole

inductance, condition 1 in Table 2, in which the actual thickness was used, or condition 4 in Table 2, in which MSL and via hole were used together, showed the closest agreement with the measurement. Looking at the error magnitude, it is within ±3 % for all conditions for characteristic impedance, whereas the error in inductance at 10 GHz is as high as 40 % in Condition 2, which shows the main deviation from the measurements. This result suggests that the inductance of the via hole is significantly affected by the optimization results, especially by the substrate thickness.

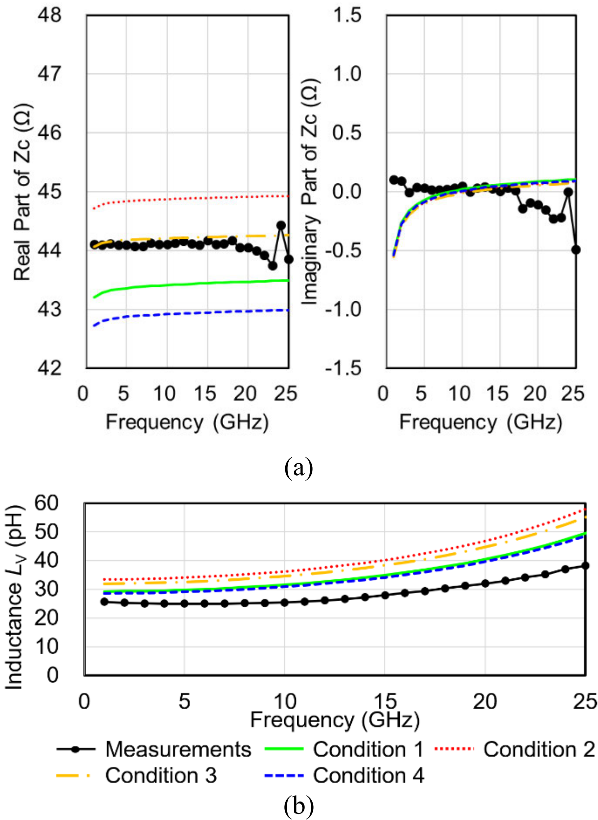

FIGURE 8. Measurements (black circled line) and simulations with the MIL component model based on substrate parameters for condition 1 (green continuous line), condition 2 (red dotted line), condition 3 (yellow dash-dotted line), and condition 4 (blue dashed line) in Table 2 for a MSL of 1800 μm length. (a) Characteristic impedance. (b) Inductance.

It is worth noticing that the actual value of the substrate thickness is generally difficult to determine, as it requires destructive inspection of the device, for example, by observing the cross-sectional structure by means of an electron microscope. If the actual value of the substrate thickness is unknown, this also needs to be optimized together with the relative permittivity. However, as demonstrated by the optimization results of condition 3, the substrate thickness value estimated using only MSLs can be quite different from the actual one. Conversely, it is a first notable advantage of the proposed method that when MSL and via-hole test structures are used together (condition 4), the thickness can be correctly optimized without falling into a local optimum solution.

V. EM SIMULATIONS

To further test and validate the proposed calibration technique, the substrate parameters extracted in Section IV were applied in the EM simulations of several test structures consisting of passive elements. For the EM simulations, Keysight Technologies ADS Momentum was used as a 3D planar EM simulator. This simulator is based on the frequency-domain method of moments and is capable of accurately simulating the layer structure. Throughout the simulations, the boundary conditions were set to open, which means that the layered substrate extends horizontally all the way to infinity. A sheet model was used to define the conductors and a 3D distributed model was used to define the vias. For the mesh density, the number of cells per wavelength was set to 50 for the maximum frequency. The transmission line (TML) feeding method is applied for the port feeding type. The TML calibration technique removes self-inductance, capacitance-to-ground and mutual inductance, as well as capacitance between adjacent structures.

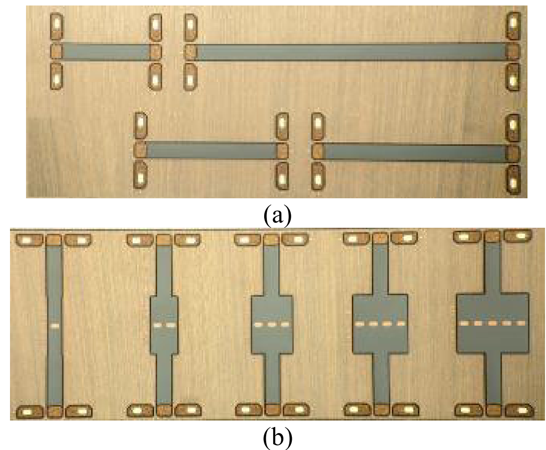

FIGURE 9. Dedicated test structures consisting of passive elements. (a) MSLs. (b) Via holes.

To assess the accuracy of EM simulations, several dedicated test structures consisting of passive elements were designed and fabricated, as shown in Fig. 9. Fig. 9(a) shows four MSLs having different lengths ranging from 300 μm to 1800 μm, while Fig. 9(b) shows test structures containing a different number of via holes in parallel (one to five). All these test structures embed the same access of the feedlines to correctly set the measurement reference planes.

Fig. 10 and Fig. 11 show the comparisons between measurements and EM simulations which are carried out exploiting the four different sets of substrate parameters extracted in Section IV and reported in Table 2. Fig. 10(a) shows the real and imaginary parts of the reflection and transmission characteristics in the S-parameters of a 900-μm MSL. Fig. 10(b) reports the real and imaginary parts of the characteristic impedance of the MSL retrieved by the measured and simulated S-parameters. In these results, the EM simulation based on the substrate parameters obtained with the proposed method (condition 4 in Table 2) exhibits

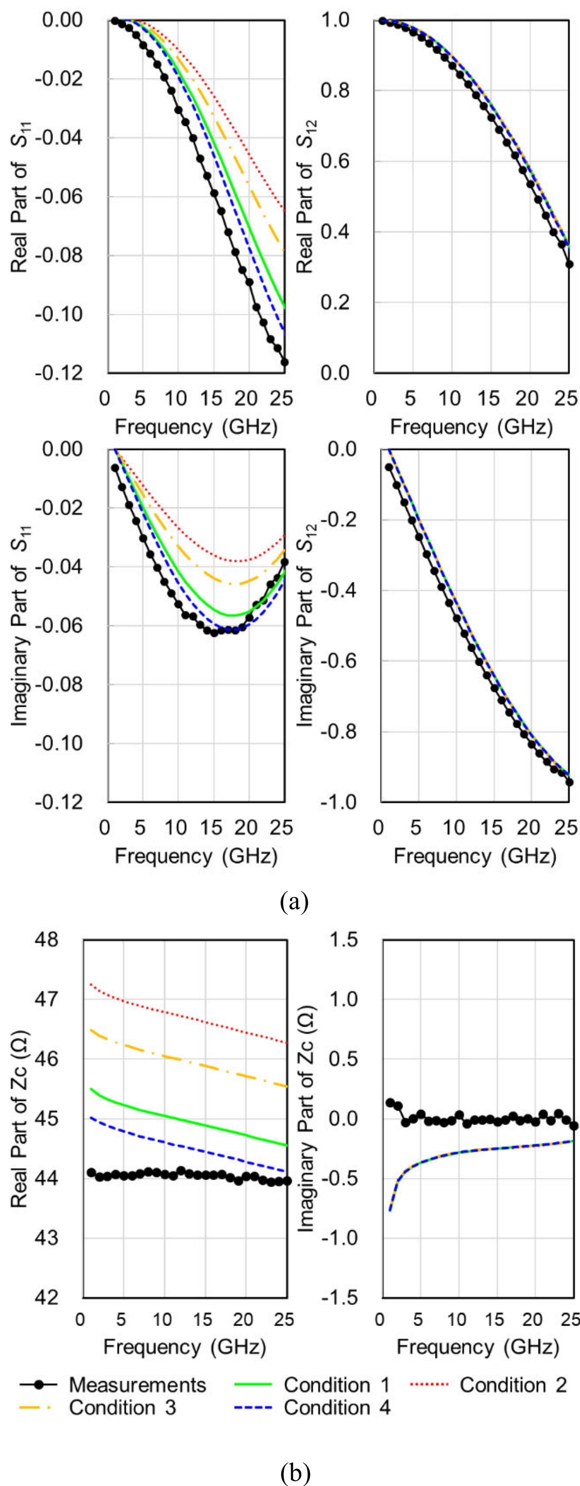

FIGURE 10. Measurements (black circled line) and EM simulations based on substrate parameters for condition 1 (green continuous line), condition 2 (red dotted line), condition 3 (yellow dash-dotted line), and condition 4 (blue dashed line) in Table 2 for a MSL of 900 μm length. (a) Small-signal characteristics. (b) Characteristic impedance.

the best agreement with the measurements, and similar results were obtained for the other lengths of the MSL test structures.

It is worth noticing that, differently from what happened at the schematic level, the proposed method (condition 4) provides better results than condition 1, where the actual values of substrate thickness were used. Different considerations apply to other methods where the accuracy is strongly reduced. In terms of substrate thickness, difference between the values obtained under condition 1 and condition 4 is small, and in fact, it is difficult to accurately detect this difference even if destructive inspection is performed. The fact that condition 4 provides more accurate results in the EM simulations clearly demonstrates the usefulness of the optimization process based on the proposed method.

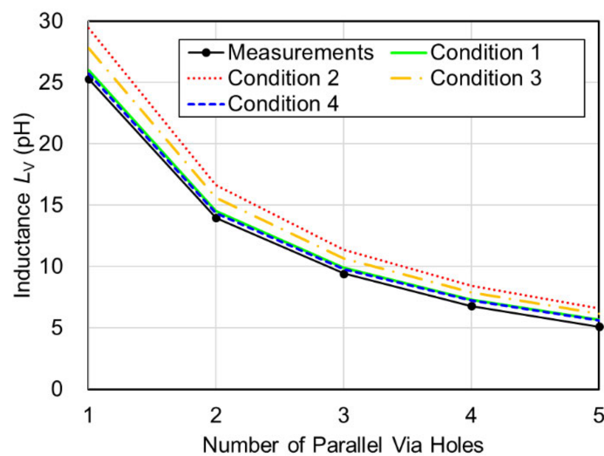

FIGURE 11. Measurements (black circled line) and EM simulations based on substrate parameters for condition 1 (green continuous line), condition 2 (red dotted line), condition 3 (yellow dash-dotted line), and condition 4 (blue dashed line) in Table 2 for the dependence on the number of parallel via holes of the inductance.

Similar considerations can be drawn for the results in Fig. 11, where the inductance values for the via hole structures in Fig. 9(b) are reported. The inductance values were obtained by (3) considering a frequency of 10 GHz. Also in this case, the EM simulations based on the substrate parameters extracted using the nominal values of the substrate thickness (condition 2 in Table 2) and only MSL (condition 3 in Table 2) show important deviations with respect to the measurements. In contrast, EM simulations based on substrate parameters extracted using the measured substrate thickness (condition 1 in Table 2) and the proposed method, i.e., using MSL and via hole as test structures, clearly show a very high level of accuracy.

VI. CONCLUSION

In this article, we have proposed a practical calibration technique for EM simulators based on the experimental characterization of few test structures and the optimization of material properties and dimensions at schematic level. Comparisons between measurements and simulations of different passive structures clearly assess the accuracy of our approach. In particular, we demonstrated that considering one MSL and one via hole test structure allows a correct optimization not only of the material properties but also of their geometrical dimensions.

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