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METHODS

Accelerated Lifetime Model-Based Design Optimization Strategy With Efficiency, Reliability, and Cost Trade-Off for High-Power Modular AFE Rectifiers

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ABSTRACT This paper presents a design optimization for grid-connected modular Active Front-End (AFE) rectifiers with an evaluation of efficiency, lifetime, cost, volume, and weight. This tool optimizes the rectifier switching frequency, component sizing and selection, and the number of parallel converters by designing and evaluating every possible configuration of the AFE rectifier system defined by the end user. The design of the LCL filter, magnetic design of inductors, selection of the inductor core and winding, and selection of SiC switches and MLC capacitors are discussed. Rapid Low-Fidelity (Lo-Fi) electro-thermal and lifetime models that are fast enough to be used in an optimization process have been developed. The rapid Lo-Fi models estimate component losses, temperatures, and lifetime for given load profiles and converter configurations. This Lo-Fi approach accelerates the processing time to generate the thermal data for the converter mission profile and allows us to skip rainflow-counting algorithm to assess the accumulated thermal damage to the SiC switches at the design and development stage. This in turn allows engineers to design converters with a longer predicted lifetime. Moreover, optimization of the grid-side three-phase LCL filter is performed considering efficiency, cost, and volume trade-off between the grid-side and converter-side inductors to achieve up to 50% decrease in losses, and 23% decrease in cost. Moreover, a 21-22% decrease in the system losses, 23-27% decrease in system cost, and tenfold improvement of the system lifetime can be achieved by optimizing the converter switching frequency and number of parallel modules. A 15 kW hardware prototype consisting of three 5 kW AFE rectifier modules is built and used to validate the efficiency from the fast Lo-Fi models. The validation of the detailed loss model and junction temperature swing is performed against a High-Fidelity (Hi-Fi) simulation in MATLAB Simulink environment.

INDEX TERMS Active front-end rectifier, modular, optimization, parallel converters, rapid electro-thermal model, lifetime model, LCL design.

I. INTRODUCTION

The transport sector is one of the leading contributors to global CO2 emissions along with power, industry, and buildings sectors [1]. Increasing the use of Electric Vehicles

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(EVs) instead of Internal Combustion Engine (ICE) vehicles can help reduce CO2 emissions. Some of the barriers to EV adoption in developing countries are performance, range, cost, and poor infrastructure [2]. Even in countries with a higher market penetration of Electric Vehicle (EV)s like the UK, there is a risk that the development of the necessary infrastructure might not keep up with the EV growth [3]. Therefore, the presence of high-power fast charging infrastructure is equally important to popularize EVs in emerging markets and to maintain their growth in established markets.

Fast charging, although advantageous in many aspects, demands high power levels and poses several challenges. First, advanced cooling systems are necessary to manage the dissipated heat. Maintaining the temperature of components within their designed values is essential for their lifetime. Even temperature fluctuations within the operating range can cause damage to the components due to mechanical stress [4]. With the increase in power level, the junction temperature swings of semiconductor switches may increase even further, causing the component to age at a rapid pace [5]. Moreover, fast chargers strain the local power networks [6]. With the 55-60% increase in the number of fast chargers (22kW-350kW) that occurred globally in 2022 [7], new fast-charging systems should be designed to reduce the stress on the grid. Another challenge that high-power chargers can face is the availability of the components suitable for that power level.

To mitigate these issues, a modular approach to the converter design is explored as shown in Figure 1. Prominent examples of modular approach in the industry are ABB Terra HP modular charger (175 kW modules, up to 350 kW system), EVBox Troniq (30 kW modules in 150 kW, 210 kW, 240 kW configurations). These Input-Parallel Output-Parallel (IPOP) modular systems give users the advantages of being flexible, versatile, and scalable. They can be used to charge one vehicle at full capacity or to charge several in parallel with reduced capacity.

Some of the important metrics to evaluate an AFE system are cost, current Total Harmonic Distortion (THD), efficiency, thermal behavior, reliability, and size [8]. Earlier studies demonstrated that splitting the power of the AFE system among several parallel modules can increase the system efficiency and expected lifetime [5], while also decreasing its grid impact [9]. However, increasing the number of modules can increase the system's cost and complexity. Therefore, it is important to select the optimal number of parallel modules in a modular AFE system based on the use case priorities.

Design optimization of AFE design in high-power chargers has been presented in [10] and [11]. This optimization is based on rapid "Fast Lo-Fi" electro-thermal models and optimizes a single converter for higher efficiency by changing the switching frequency. However, this optimization does not consider component lifetime, system modularity or LCL filter optimization. Fast Lo-Fi models in [10] and [11] use average

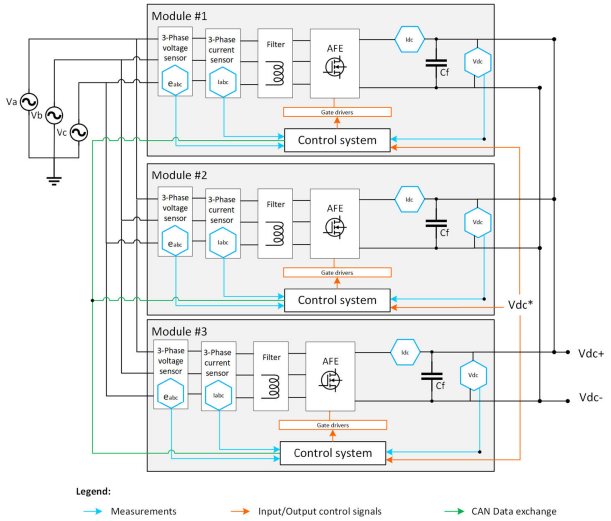

FIGURE 1. An example of the Modular AFE rectifier system architecture in EV charging applications.

values of voltage and currents. This is the fastest and the least detailed of the four modeling fidelity levels defined in [12]: Fast Lo-Fi, Lo-Fi, M-Fi, Hi-Fi. Fast Lo-Fi models can be used to estimate average losses and average temperatures. However, this level of fidelity is not enough to estimate junction temperature swings, as they would depend on the grid-frequency changes in current. Therefore, Fast Lo-Fi models cannot be used to estimate the switching component's lifetime. The next higher level of fidelity is "Lo-Fi", where actual grid-frequency waveforms are used. While this fidelity level allows the estimation of junction temperature swings, it is substantially slower, and is not suitable for the optimization process where many different options have to be evaluated. Therefore, in this paper, a combination of "Fast Lo-Fi" and "Lo-Fi" electro-thermal and lifetime models is used to optimize the design of a grid-connected modular AFE rectifier system containing several parallel modules. Additionally, models for cost, mass, and volume are created.

Section II outlines an overview of the optimization process. Section III covers the design of AFE rectifier, namely filter sizing. Section IV presents a fast analytical model of the AFE system, highlighting the assumptions, including the control and modulation approach. Calculations for the RMS and averaged currents, voltages, and duty cycle are presented. Section V detail the design and selection of key AFE components like capacitors, inductors, and SiC MOSFET switches, as well as evaluation of their thermal behavior, estimation of lifetime, cost, and size. The section is concluded by combining the efficiency, cost, size, and reliability metrics of different AFE components into one system-level evaluation. The validation of the Lo-Fi models is presented in Section VI. Section VII presents the optimization results for LCL filter design, different numbers of parallel modules, and switching frequencies. Section VIII presents the conclusions of this paper.

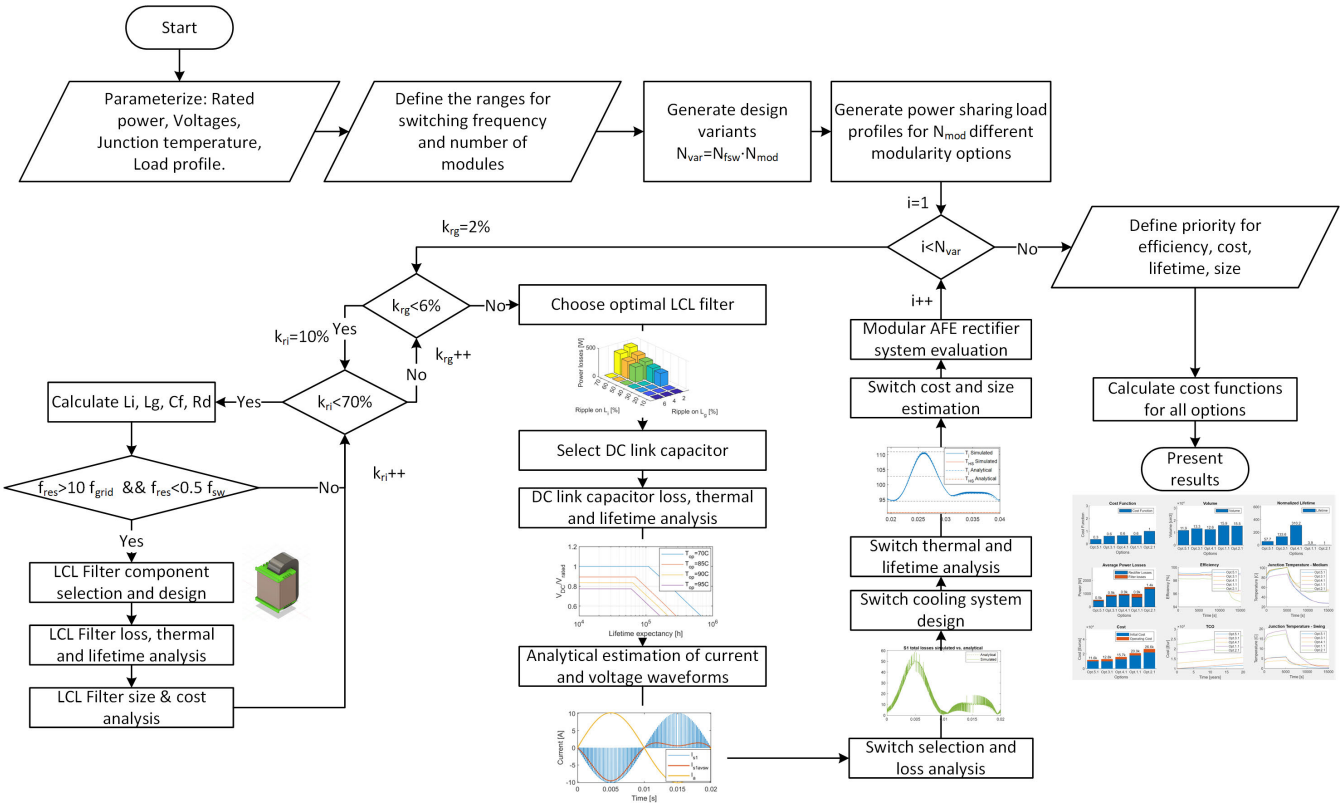

FIGURE 2. Block diagram of the iterative optimization workflow of the modular AFE rectifier system.

II. OPTIMIZATION WORKFLOW

The optimization process consists of several steps as shown in Figure 2. First, the design and evaluation parameters are defined, the pool of design variants and load profiles is created, and then each variant is designed and evaluated. The results are presented based on the user-defined cost function.

In the first step, AFE rectifier parameters such as rated power, grid frequency, grid voltage, DC link voltage, and the nominal value of MOSFET junction are defined. These values are used as base parameters when designing the converter. They do not change and apply to all design configurations of the converter. Then, the load profile and current sharing strategy to evaluate the performance of the designed AFE are selected. There are two main current sharing strategies under consideration. The first uses the minimum number of modules necessary for the given load. Depending on the load profile and efficiency map of the converter, that may result in increased system efficiency. The second strategy is to share the current between the modules equally. This option may be beneficial in applications where turning modules on and off during operation is undesirable, and it may also improve the lifetime of the AFE system.

The last step of parameterization is to define the pool of variants to be evaluated. The main variants are the switching frequency and the number of parallel modules. The switching frequency can be defined as a range of frequencies with the lower and upper limits and the step. The number of parallel modules can be defined as a range between the minimum and maximum number of modules.

In the next step, all the design variants are created based on the specified parameters. For example, if there are $N_{fsw} = 4$ options for the switching frequency and $N_{mod} = 5$ options for the number of modules, $N_{var} = 20$ variants will be generated. Then new load profiles based on the number of parallel modules, and the preferred current sharing method will be generated for N_{mod} different modularity options.

Then each one of the N_{var} AFE rectifier system design variants is designed and evaluated in an iterative process as shown in Figure 2. First, the grid-side LCL filter is optimized as a trade-off between the allowed ripple on the grid side and the converter side currents, as well as the resonant frequency. In this step magnetic components are designed for the selected power rating and power-sharing strategy, and losses and temperature are estimated for the load profile. The size and cost of the inductors are estimated. Then DC link capacitor is selected, its losses are evaluated, and thermal and lifetime analysis is performed. After this step, the analytical fast model of the system with current and voltage waveforms can be derived. Then SiC MOSFET switches are selected, and the estimation of MOSFET power losses is performed for the mission profile. The heatsink is sized according to the power losses and the desired MOSFET junction temperature. With this information, thermal and lifetime analyses are performed for the switch. The cost and size of the switch and its cooling system are estimated.

When the individual components of AFE rectifier are designed, selected, and evaluated, all those metrics are joined in a system-level evaluation for the single AFE rectifier module, then parallel AFE rectifier system. Then, when the design and evaluation process is completed for all the variants, the user defines the cost function weight of the power losses α_p, cost α_c, lifetime α_l, volume α_v and mass α_m of the AFE rectifier system to be used as α_Θ in (1). The final cost of the AFE rectifier system design is calculated as in

$$J_i = \sum \frac{\Theta_i}{\Theta_{max}} \alpha_\Theta, \tag{1}$$

where Θ_i represents one of the main optimization parameters: power losses, cost, lifetime, volume, or mass of the design option i. The maximum value of the given parameter Θ_{max} is extracted from the list of final design options. With that, the final optimization results are presented as shown in Section VII.

III. DESIGN OF AFE

A three-phase two-level boost type AFE rectifier with an LCL-filter is considered in this study as shown in Figure 3. This section will discuss the filter sizing for the AFE. The detailed design and component selection of each part of the AFE rectifier will be discussed in the corresponding subsections of Section V.

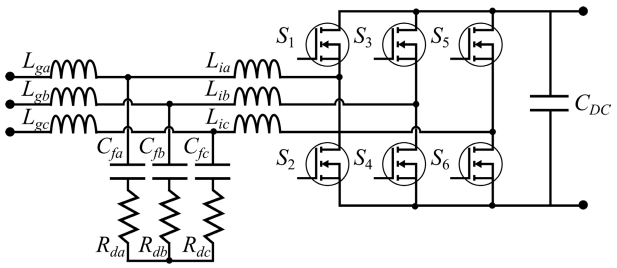

FIGURE 3. Schematic of a 2-level 3-phase boost-type AFE rectifier with LCL filter.

A. DC-LINK CAPACITOR SIZING

The DC link capacitor can be sized for the voltage ripple of 1% to 10% depending on the application. If the AFE rectifier is part of a two-stage AC/DC+DC/DC converter system, then the ripple requirements can be more relaxed, as the DC/DC converter can further reduce the voltage ripple. If the AFE rectifier is connected to the battery directly without a DC/DC, then the ripple requirements should be more stringent to avoid aging the battery. Moreover, the excessive voltage ripple would affect the capacitor's lifetime as well. In this case, the DC side capacitor is designed for a maximum of 1% peak-to-peak ripple on the DC link voltage [11]. Therefore, for a 700 V DC link, the voltage would be within the 696.5 V to 703.5 V range. The DC link capacitance C_{DC} for the three-phase active rectifier switching at f_{sw} can be calculated as

$$C_{DC} = \frac{I_{pk}}{2 f_{sw} \Delta V_{DC}}, \tag{2}$$

where I_{pk} is the amplitude of the phase current, and ΔV_{DC} is the peak-to-peak voltage ripple. The 1% peak-to-peak voltage ripple is calculated from the nominal DC link voltage V_{DC} as in

$$\Delta V_{DC} = 0.01\ V_{DC}. \tag{3}$$

The peak current is calculated as

$$I_{pk} = \sqrt{2} \frac{P_{mod}}{\sqrt{3} V_{AC}}, \tag{4}$$

where P_{mod} is the rated power of the AFE rectifier module, V_{AC} is the RMS line-to-line voltage of the three-phase grid.

B. AC-SIDE LCL-FILTER DESIGN

The AC side LCL-filters are sized to keep the Total Demand Distortion (TDD) of grid-side currents under 5% as defined in IEEE519 [13]. While the simple L-filter has to be designed to ensure a specified TDD on the grid-side currents, in the case of the LCL-filter different combinations of the grid-side and converter-side inductors, and the capacitor can result in the same TDD. The LCL filter is designed using the procedure presented in [14]. The converter side inductor L_i is designed for a selected peak-to-peak switching frequency ripple k_{ri} at the converter side currents, as in

$$L_i = \frac{V_{DC}}{4\sqrt{3} f_{sw} \Delta I_{pp}}, \tag{5}$$

where V_{DC} is the DC link nominal voltage, and ΔI_{pp} is the maximum peak-to-peak current ripple in Amperes [15]. This value is calculated as

$$\Delta I_{pp} = I_{pk} k_{ri}. \tag{6}$$

The capacitor of the LCL filter is designed for the percentage of reactive power x and the base capacitance C_b

$$C_f = x C_b. \tag{7}$$

The base capacitance is calculated using the AFE module power P_{mod}, grid frequency f_g and the line-to-line RMS voltage V_{AC}

$$C_b = \frac{P_{mod}}{2\pi f_g V_{AC}^2}. \tag{8}$$

The grid-side inductor is calculated as

$$L_g = r L_i, \tag{9}$$

where the index r is calculated as a function of the desired ripple attenuation from the inverter-side k_{ri} to grid-side k_{rg} [14] as in

$$r = \frac{\frac{k_{ri}}{k_{rg}} - 1}{|1 - x L_i C_b (2\pi f_{sw})^2|}. \tag{10}$$

While a value of $k_{rg} = 6\%$ is enough to keep the TDD under 5% as specified in IEEE519, it may not be possible due to resonance frequency constraints as will be shown in

the optimization results section. The resonant frequency ω_{res} calculated as

$$\omega_{res} = \sqrt{\frac{L_i + L_g}{L_i L_g C_f}}, \tag{11}$$

should satisfy the following requirements:

$$10\omega_g < \omega_{res} < 0.5\omega_{sw}. \tag{12}$$

Then the damping resistor value is selected as a function of the resonance frequency

$$R_d = \frac{1}{3\omega_{res} C_f}. \tag{13}$$

The coefficient for reactive power is selected for 1% reactive power $x = 0.01$. The ripple coefficient of the converter-side inductor k_{ri}, and the ripple coefficient of the grid-side inductor k_{rg} are selected as a trade-off between efficiency, weight, and cost of the LCL filter while maintaining the condition for the resonant frequency during the optimization process. The results of this optimization are presented in Section VII-A.

IV. SYSTEM MODEL AND ASSUMPTIONS

To obtain the highest accuracy data on the performance of the AFE system, Hi-Fi modeling is used [12]. With the Hi-Fi model, it can sometimes take up to a week to simulate a 30-minute load profile. Therefore, it is not suitable for optimization, as we would have to analyze system performance for various designs in a short amount of time. So, we have created an analytical model of the AFE that can evaluate its performance for a given load profile in a short time which corresponds to a combination of Lo-Fi and Fast Lo-Fi models described in [12]. The Fast Lo-Fi model uses averaged sinusoidal voltages and currents and is used at the design stage to calculate average losses and to design the cooling system. The Lo-Fi model with the actual sinusoidal waveforms is used to obtain the waveform of power losses during the 0.02 s (50 Hz) period, and the junction temperature swing in the same timeframe. Moreover, the actual FFT of the waveform with the switching frequency ripple is important for the evaluation of inductor losses. The evaluation is performed for a charging load profile, which can range from minutes to several hours depending on the charger power levels. For example, the load profile uploaded by the user in this optimization process is a CC-CV load profile that lasts 1 h and is defined via a 22-point power and time dataset. Lo-Fi models of 0.02 s are created for each of the 22 points in the load profile for further electro-thermal evaluation.

To create a fast model several assumptions and simplifications have to be made in regards to the control system. First, a Voltage-oriented control (VOC) with an outer DC link voltage control loop and inner dq-axis current control loops with simple PI controllers is used as shown in Figure 4 and described in [8].

Also, a carrier-based PWM with a symmetrical triangle waveform is used, where the carrier is a triangular wave at

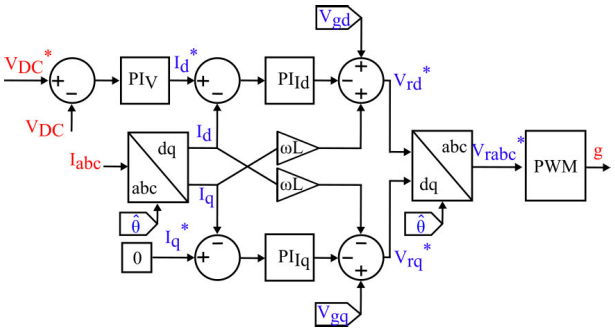

FIGURE 4. Schematic of Voltage-oriented Control.

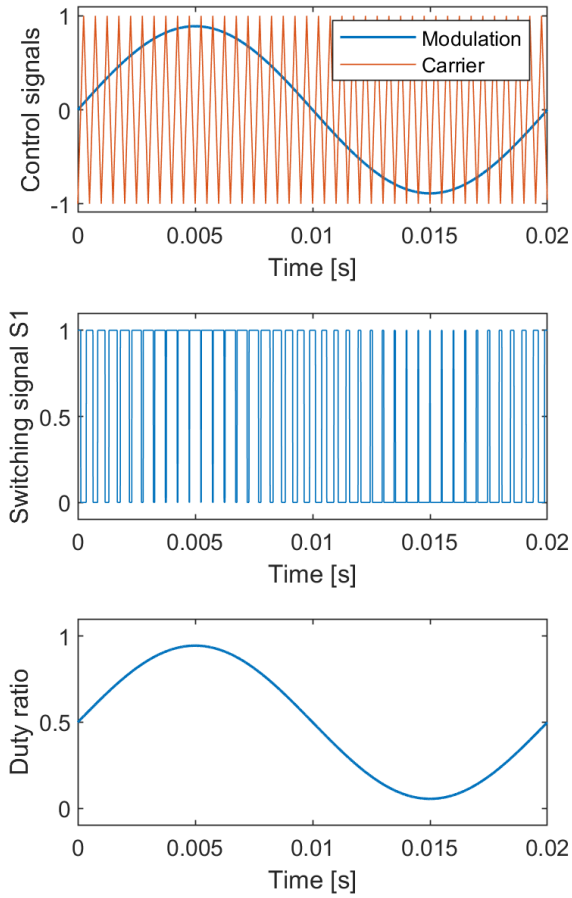

FIGURE 5. Carrier-based PWM with $m_f = 40$: switching signal vs. Duty ratio.

f_{sw} (orange), and the modulation waves are three sinusoidal waveforms at f_g received from the control system (blue), as shown in Figure 5. When the modulation signal is above the carrier signal, the gate signal is 1 (turn on), and 0 (turn off) otherwise.

The ratio between the amplitude of the sinusoidal modulation wave and the triangular carrier wave is called amplitude modulation index m_a. The modulation factor for this specific control and modulation strategy is calculated from the reference voltages created by the PI controllers of the corresponding dq-axis currents V_{rd}^* and V_{rq}^*, and the DC

link voltage V_{DC} as

$$m_a = \frac{\sqrt{V_{rd}^{*\,2} + V_{rq}^{*\,2}}}{0.5\ V_{DC}}. \tag{14}$$

In Voltage Oriented Control (VOC) the V_{rd}^* is defined from d-axis grid voltage V_{gd}, PI's output V_{dPI} and a feedforward compensation component:

$$V_{rd}^* = V_{gd} - V_{dPI} + \omega L i_q. \tag{15}$$

The d-axis grid voltage V_{gd} is obtained from the PLL. However, for the sake of this optimization problem, in steady-state under a balanced grid, the d-axis grid voltage V_{gd} can be equated to the peak line-to-neutral voltage, which can be calculated from the RMS line-to-line voltage V_{AC}. If a perfect power factor of 1 is achieved, then i_q will be zero. In steady-state the output of the PI controller only needs to create enough voltage difference between the grid and converter (over the filter) to create a current flow of I_p.

$$V_{rd}^* = V_{AC}\sqrt{\frac{2}{3}} - V_f. \tag{16}$$

This peak current I_p is calculated from the load profile using (4). The average voltage drop over the filter V_f is estimated as

$$V_f = (2\pi f_g(Li + Lg) + R_{Li} + R_{Lg})I_p. \tag{17}$$

The q-axis voltage reference in VOC is comprised of q-axis grid voltage V_{gq}, q-axis PI output V_{qPI}, and the feed-forward compensation component

$$V_{rq}^* = V_{gq} - V_{qPI} - \omega L i_d. \tag{18}$$

In steady-state, in a balanced grid with unity power factor, $V_{gq} = 0$ can be assumed zero, and so is the q-axis PI controller's output $V_{qPI} = 0$, such that only the feed-forward compensation is present with $i_d = I_p$

$$V_{rq}^* = -2\pi f_g L_i I_p. \tag{19}$$

To calculate the losses and temperatures over switches, the current during one grid cycle can be described as a sinusoidal with an amplitude of I_p at the grid frequency f_g

$$I_{ph} = I_p \sin(2\pi f_g t), \tag{20}$$

where t is an array of time from zero to 0.02 s at sampling intervals $T_s = 1\ \mu$s.

The duty cycle is calculated as

$$d = 0.5\ ma \sin(2\pi f_g t) + 0.5. \tag{21}$$

It is adjusted for the dead time T_{dt} by subtracting $T_{dt}f_{sw}$ from the duty cycle, keeping in mind that the duty cycle should be a number between zero and one as shown in Figure 5.

The RMS of the grid side currents of a three-phase AFE is calculated as

$$I_{rms} = \frac{I_p}{\sqrt{2}}, \tag{22}$$

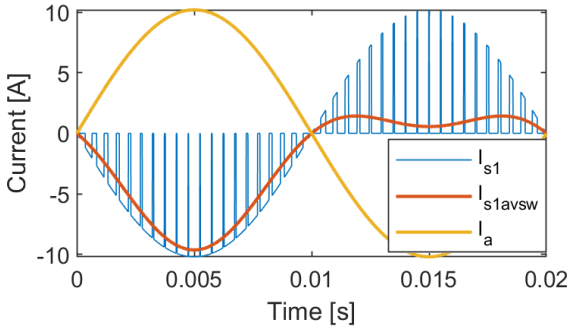

FIGURE 6. AFE MOSFET S1 drain current vs. phase current.

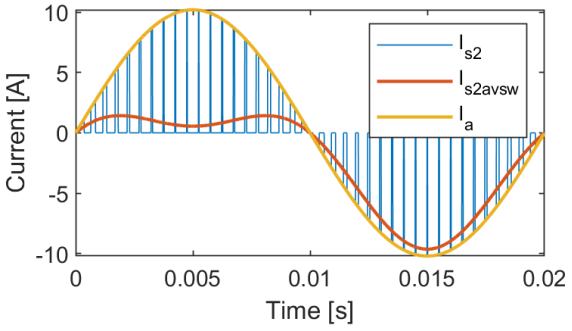

FIGURE 7. AFE MOSFET S2 drain current vs. phase current.

where the amplitude of the sinusoidal phase current I_p is calculated for the specific load point within the profile using (4).

Assuming that phase-A current I_a is positive as shown in Figure 3 when it passes through S1, it goes from source to drain, which is considered the "opposite" direction of the current for the MOSFET, therefore the negative sign in (23). The average of MOSFET S1 drain current over a switching period is calculated as

$$I_{s1avsw} = -I_a d. \tag{23}$$

Figure 6 demonstrates how the phase-A current I_a compares to the S1 MOSFET drain current I_{s1} and its average over a switching frequency I_{s1avsw}.

Figure 7 shows the comparison of the phase current I_a, S2 MOSFET drain-to-source actual current I_{s2}, and the MOSFET current averaged over the switching frequency I_{s2avsw}, calculated as

$$I_{s2avsw} = I_a\,(1 - d)\,. \tag{24}$$

MOSFET's body diode will only conduct when there is a "negative" drain current ($I_{ph} > 0$) and the MOSFET is receiving a zero gate signal. So, in normal AFE operation that happens during the dead time in the negative half-cycle of the current. So the average current through the body diode of S1 can be calculated as

$$I_{d1avsw} = I_{ph}(I_{ph} > 0) T_{dt} f_{sw}, \tag{25}$$

where $(I_{ph} > 0)$ is an array of logical values. Similarly for the lower MOSFET's body diode

$$I_{d2avsw} = I_{ph}(I_{ph} < 0) T_{dt} f_{sw}. \tag{26}$$

When considering the current flow over the inductors, a simplified model as follows is used:

$$I_L = I_p \sin(2\pi f_g t) + I_p k_{rL} f_{\triangle}(2\pi f_{sw} t), \tag{27}$$

where $f_{\triangle}$ is a periodic triangle waveform function at the switching frequency f_{sw}. The ripple coefficient k_{rL} is equal to either k_{ri} or k_{rg} depending on which inductor's power losses are being calculated. Then the FFT of this waveform is used for the calculation of inductor losses.

V. COMPONENT SELECTION, DESIGN AND EVALUATION

A. CAPACITORS SELECTION AND EVALUATION

1) CAPACITOR SELECTION

In this study, Multilayer Ceramic (MLC) capacitors are selected due to their reliability in high-frequencies and high-temperature applications [8], [16]. The voltage rating of the capacitor is selected to be at least 20% higher than the DC link nominal voltage, and the RMS value of the ripple current filtered by the capacitor should not exceed the rated value to prevent overheating and failure. For the given modulation strategy, assuming the ideal power factor, the RMS current I_{CRMS} over the DC link capacitor of the three-phase AFE can be estimated according to [17] as

$$I_{CRMS} = I_p \sqrt{\frac{3m_a}{4\pi}}. \tag{28}$$

The DC link capacitor database used in this study contains capacitors rated for RMS current range 5 A-35 A, voltage range 450 V-1600 V, and capacitance values 5 µF-110 µF. The capacitor is selected from the database as shown in Figure 8. If a single capacitor for the desired RMS current I_{CRMS}, DC voltage V_{DC} and capacitance C_{DC} is not found, then options paralleling several capacitors are considered until a solution is found.

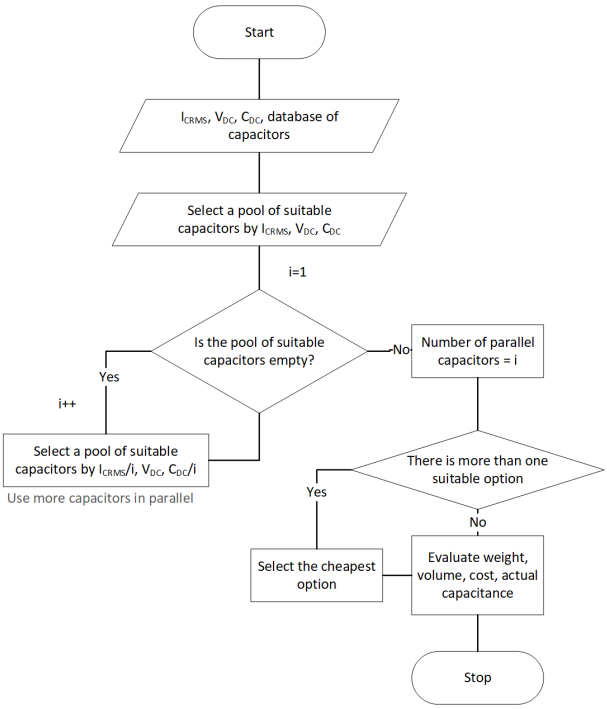

FIGURE 8. Flowchart for optimal capacitor selection.

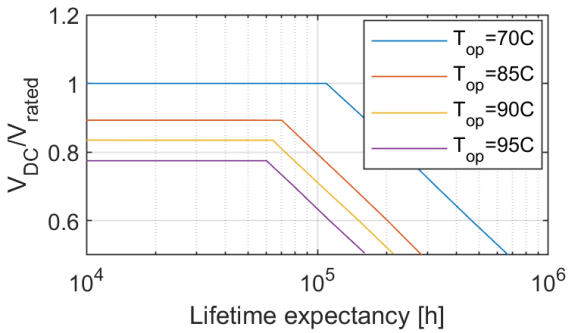

FIGURE 9. Lifetime of film capacitors as given by the manufacturer (TDK).

2) CAPACITOR LOSSES

The capacitor losses can be calculated from the capacitor's RMS current I_{CRMS} and its equivalent series resistance (ESR) R_{ESR} [18]

$$P_{cap} = I_{CRMS}^2 R_{ESR}. \tag{29}$$

3) CAPACITOR THERMAL MODEL

The capacitor equivalent heat coefficient G_{cap} measured in [mW/°C] is dependent on the capacitor packaging, and is provided in the datasheet. This coefficient is used to estimate the temperature T_{op} on the lateral surface of the capacitor's outer plastic box as

$$T_{op} = T_{amb} + \frac{P_{cap}}{G_{cap}}. \tag{30}$$

4) CAPACITOR LIFETIME

Two main factors affecting the capacitor lifetime are the operating voltage V_{DC}, and the temperature of the outer packaging T_{op} as shown in the example from the manufacturer's datasheet in Figure 9. During the evaluation process, the appropriate lookup table from the manufacturer is used to obtain the expected lifetime of the capacitor based on the DC link voltage and the operating temperature.

5) CAPACITOR SIZE AND COST

The size and cost of the capacitor are taken directly from the database, and calculated for the corresponding number of parallel capacitors, and number of parallel AFE modules as shown in Figure 10.

B. INDUCTOR DESIGN, SELECTION AND EVALUATION

1) INDUCTOR COMPONENT SELECTION

As shown in Figure 11 the magnetic design of inductors entails selecting the appropriate core (highlighted in green) and wire (highlighted in blue), and determining the number of turns, and the air gap (highlighted in orange). The input parameters for inductor design are the desired inductance, switching frequency, cooling system, and peak and RMS current values.

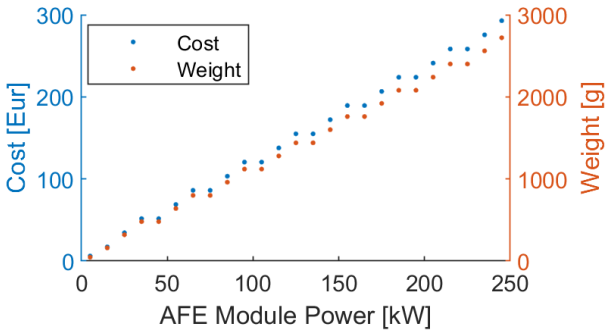

FIGURE 10. Cost and weight of DC link capacitor bank vs. AFE module power at 700VDC, 20kHz.

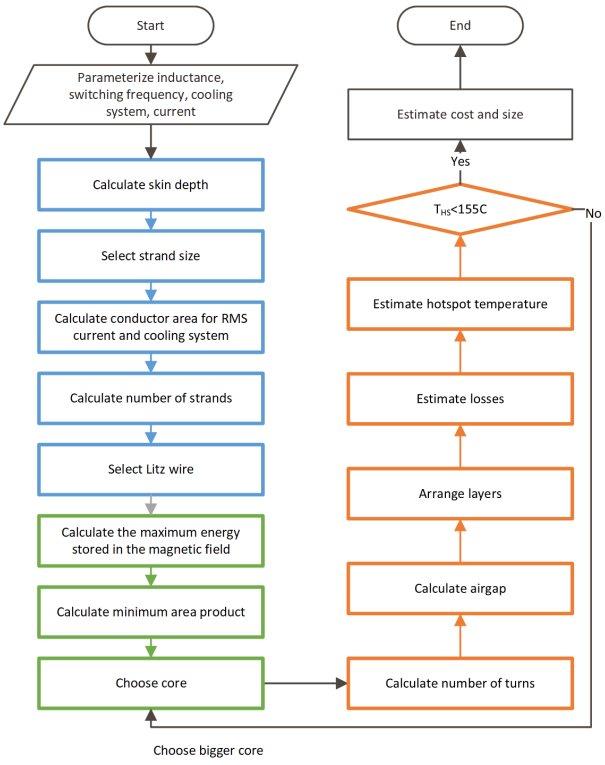

FIGURE 11. Flowchart of the inductor design and component selection process.

The first step is to select the wire for inductor windings. In this study, Litz wires are considered [8]. The strand width of the wire is selected to be less than the skin depth δ at the switching frequency f_{sw}.

$$\delta = \sqrt{\frac{\rho_{cu}}{\pi f_{sw} \mu_0}}, \tag{31}$$

where $\rho_{cu} = 1.72 \times 10^{-8}\,\Omega\,\text{m}$ is the resistivity of copper, and $\mu_0 = 1.256\,637\,06 \times 10^{-6}\,\text{NA}^{-2}$ is the permeability of free space.

The total conductor area A_c is calculated from the RMS current that passes through the inductor I_{RMS} and the maximum current density J_{max} allowed by the cooling system, as in

$$A_c > \frac{I_{RMS}}{J_{max}}. \tag{32}$$

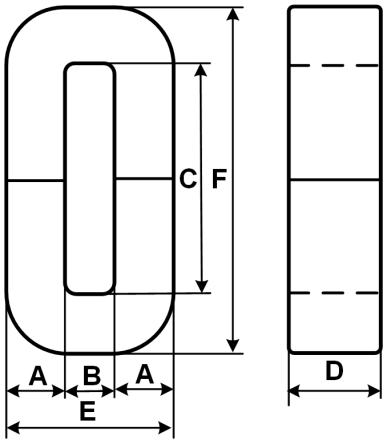

FIGURE 12. Shape of the inductor's cut core (C-core).

The maximum current density J_{max} for natural cooling is selected to be $4\,\text{A/mm}^2$, for forced air cooling $5\,\text{A/mm}^2$, and for liquid cooling $9\,\text{A/mm}^2$ as an average from the literature [19], [20], [21].

The number of strands is calculated as a ratio of conductor and strand areas. Litz wire with a conductor size higher than A_c with strand diameter less than the skin depth δ is selected.

Next, the core needs to be selected. In this study, amorphous cut cores have been considered as shown in Figure 12.

To choose the core size the magnetic energy method is used, where the maximum energy stored in the magnetic field of the inductor W_L is calculated as

$$W_L = \frac{1}{2} L I_{pk}^2. \tag{33}$$

Then the peak flux density is defined. For the cut cores made of 2605-SA1, the amorphous foil saturation flux density is 1.56 T [22], so a peak flux density of $B_{pk} = 1.25\,\text{T}$ is selected with a safety margin. The minimum inductor core size for a given energy W_L, flux density B_{pk}, and current density J_{max} is determined as in

$$A_p > \frac{2W_L}{B_{pk} * J_{max} * K_u}, \tag{34}$$

where the area product A_p is equal to the product of the core cross-section area $A_c = A * D$ and core window area $A_w = C * B$ as shown in Figure 12, and $K_u = 0.4$ is the window utilization factor [23]. An amorphous cut core with an area product larger than A_p is selected. If in the following stages, it is identified that this core size causes the inductor to overheat, then the next larger core size is selected.

In the next step, the number of turns N_t is calculated as

$$N_t = \frac{L I_{pk}}{A_c B_{pk}}, \tag{35}$$

where A_c is the cross-section of the selected inductor core [23].

The air gap length l_{ag} is calculated as

$$l_{ag} = \frac{N_t^2 \mu_0 A_c}{2L} - \frac{l_c}{2\mu_r}, \tag{36}$$

where l_c is the core mean magnetic path length and $\mu_r = 5000$ is the relative permeability of the amorphous core material. The mean magnetic path length can be estimated using the dimension from Figure 12 as

$$l_c = 2 * (A + B) + (C + F). \tag{37}$$

The length of the Litz wire used to obtain the necessary number of turns is essential to estimate the cost, volume, weight, and losses of the inductor windings in the evaluation step. To find this length, the winding turns need to be arranged in layers on the core. The turns will be arranged on the portion of the core annotated "C" in Figure 12. The thickness of the coil former l_b will be subtracted from the length available for winding. The number of turns on a single layer is calculated as

$$N_{tl} = \lfloor 0.8 \frac{C - 2l_b}{d_w} \rfloor, \tag{38}$$

where d_w is the outer diameter of the wire, and 0.8 is a margin of error. The number of layers necessary to accommodate all of the turns is

$$N_l = \lceil \frac{N_t}{N_{tl}} \rceil. \tag{39}$$

All the layers of the inductor windings except for the last one will contain N_{tl} turns, while the last one will have N_{last} turns

$$N_{last} = N_t - (N_l - 1)N_{tl} \tag{40}$$

The Mean Length per Turn (MLT) for the first layer l_{mlt1} compensated for the thickness of the coil former l_b is

$$l_{mlt1} = 2A + 2D + 8l_b. \tag{41}$$

Every layer the MLT will keep increasing by a factor of $8d_w$ to account for the existing layers of winding on top of the coil former. So, the total used Litz wire length can be calculated in two parts: the first part is for the length of wire if all turns were located in the first layer, and the second part is the compensation of the increasing MLT diameter.

$$l_{lw} = N_t l_{mlt} + 8\, d_w \left(N_{tl} \frac{(N_l - 1)(N_l - 2)}{2} + N_{last}(N_l - 1) \right). \tag{42}$$

This concludes the design stage of the inductor. The evaluation of this inductor design will be given in the appropriate sections for the loss, cost, and size models.

2) INDUCTOR LOSSES

From the wire length l_{lw}, the DC resistance R_{LDC} of the wire can be calculated as

$$R_{LDC} = \frac{\rho_{cu} l_{lw}}{A_s n_s}, \tag{43}$$

where ρ_{cu} is the resistivity of copper as given in (31), A_s is the cross-sectional area of a single strand, and n_s is number of strands within the Litz wire.

To estimate how the skin effect and proximity effect will change the resistance, Dowell's equations are used [24] as in

$$R_{LAC} = R_{LDC} A_o \left[\frac{e^{2A_o} - e^{-2A_o} + 2\sin 2A_o}{e^{2A_o} + e^{-2A_o} - 2\cos 2A_o} + \frac{2\left(N_{la}^2 - 1\right)}{3} \frac{e^{A_o} - e^{-A_o} - 2\sin A_o}{e^{A_o} + e^{-A_o} + 2\cos A_o} \right], \tag{44}$$

where the constant A_o is calculated as

$$Ao = \left(\frac{\pi}{4}\right)^{\frac{3}{4}} \frac{d_s}{\delta} \sqrt{\frac{d}{p}}, \tag{45}$$

where d is the wire diameter and p is the distance between the centers of the adjacent wires. Ideally, this ratio would be 1 if the wires are in full contact, however, a value of 0.7 is more realistic. And the N_{la} is the adjusted number of layers calculated as

$$N_{la} = N_l \sqrt{n_s}. \tag{46}$$

Finally, the winding power losses can be calculated as

$$P_{Lw} = I_{RMS}^2 R_{LAC}. \tag{47}$$

To estimate the core losses, first, the FFT of the current passing through the inductor is performed. The 20 highest harmonics are saved in an array. Once the current components at different frequencies I_f are obtained, the peak flux density for each frequency component B_{pkf} should be calculated as

$$B_{pkf} = \frac{LI_f}{A_c N_t}. \tag{48}$$

With that, the core power losses can be calculated as a product of the core mass m_c and the sum of core power losses per kilogram at different frequencies as in

$$P_{Lc} = m_c \sum kf^{\alpha} B_{pkf}^{\beta} \tag{49}$$

where $k = 6.5$, $\alpha = 1.51$, and $\beta = 1.74$ are the parameters provided by the manufacturer for C-Cores made of 2605SA1 amorphous alloy. Total inductor losses P_L are found as a sum of winding losses P_{Lw} and core losses P_{Lc}

$$P_L = P_{Lc} + P_{Lw}. \tag{50}$$

3) INDUCTOR THERMAL MODEL

The temperature of the inductor hotspot is calculated using the process given in [23] as in

$$T_{hs} = T_{amb} + \frac{P_{Lw} R_{wc} + P_{Lw} R_{ca} + P_{Lc} R_{ca}}{R_{wc} + R_{wa} + R_{ca}} R_{wa}, \tag{51}$$

where R_{wc} is the winding-to-core thermal resistance, R_{ca} is the core-to-ambient thermal resistance, and R_{wa} is the winding to ambient thermal resistance. For the selected core, the maximum operating temperature is 155 °C. Therefore, if the estimated hotspot temperature is above this value, the selected core size is increased by one step until the desired temperature is reached as shown in Figure 11.

4) INDUCTOR SIZE AND COST

The weight of the inductor is calculated from its parts. The core weight and volume are extracted from the datasheet, while the wire volume and weight are calculated from the length of the wire calculated previously and the conductor cross-section A_c. The copper density of 8.96 g/cm^3 is used to calculate the winding mass. The cost of the winding is calculated using an estimated average price of 63 euros per kg. The resulting cost is shown in Figure 13. This is purely a component cost, not taking into account the cost of manufacturing, design, etc.

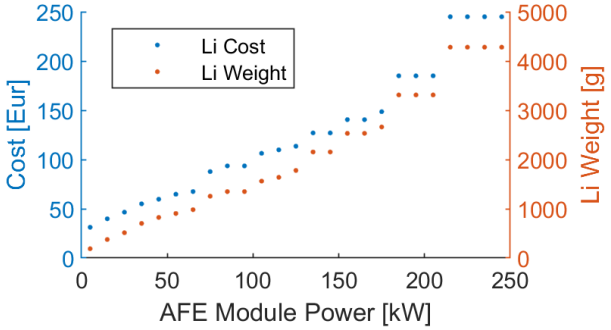

FIGURE 13. Converter-side inductor cost vs. AFE module power.

C. SWITCH SELECTION AND EVALUATION

1) SIC MOSFET SELECTION

A database of 62 discrete SiC MOSFETs and 26 SiC MOSFET-based half-bridge power modules is considered as a set of options. The discrete MOSFETs are rated for currents from 5 A to 120 A, while the power modules are rated for 84 A to 760 A. The current given in the database corresponds to the continuous drain current at room temperature. The current for higher temperature operation is normally 30-40% lower. Assuming a 400 V RMS three-phase grid, and a 700 V DC link, and accounting for lower current ratings at higher junction temperatures, this pool of MOSFETs covers the power range of a single AFE rectifier module up to 250 kW.

To select a suitable MOSFET from this database, first, the peak current for the converter's operating conditions is calculated according to (4). Then the pool of MOSFETs is narrowed down to the options that have current ratings of more than 1.35 I_p, and voltage rating of 1.3 V_{DC}. From this pool of options, the MOSFET is selected iteratively based on a cost function as a trade-off between the cost and drain-to-source on-state resistance. The iterations are limited to a maximum of five options with a lower current rating to avoid long computational time.

2) SIC MOSFET LOSSES

MOSFET conduction losses are calculated using the MOSFET drain current's RMS value and the on-state resistance R_{DSon} extracted from the datasheet-based lookup tables based on the peak drain current and MOSFET junction temperature. The peak drain current is equal to the reverse of the phase current. In the following formulas, all values are given for S1. The RMS current through the MOSFET S1 can be calculated from the phase current I_{ph}, and the corresponding duty cycle d_{s1} [25].

$$P_{CM1} = R_{DSon}\left(T_j, -I_{ph}\right)(-I_{ph})^2 d_{s1} \tag{52}$$

MOSFET body diode conduction losses are calculated based on the diode forward voltage and the average forward current [25]:

$$P_{CD1} = V_{DS}\left(T_j, I_{ph}\right) I_{d1avsw} \tag{53}$$

MOSFET Switching on/off losses are calculated based on the switching on/off energy extracted from the datasheet-based lookup tables and the switching frequency:

$$P_{on1} = E_{on}\left(T_j, I_{ph}, V_{DC}\right) f_{sw} \tag{54}$$

$$P_{off1} = E_{off}\left(T_j, I_{ph}, V_{DC}\right) f_{sw} \tag{55}$$

MOSFET body diode reverse recovery losses are calculated from the reverse recovery charge and DC link voltage:

$$P_{rr1} = E_{rr} f_{sw} = \frac{Q_{rr} V_{DC}}{4} f_{sw} \tag{56}$$

The total losses over one MOSFET are given by [25]:

$$P_{s1} = P_{CM1} + P_{CD1} + P_{rr1} + P_{on1} + P_{off1} \tag{57}$$

3) SWITCH HEATSINK SELECTION

The input to the cooling system design is the power loss of the rectifier at the rated power. The goal of this design is to select the heatsink with appropriate thermal resistance to keep the junction temperature at the requested level. In this study, one heatsink per half-bridge is considered to make it suitable for both discrete and power module options. To estimate the junction temperature of the SiC MOSFETs a Foster thermal network model is used as shown in Figure 14.

The model consists of three parts: the junction-to-case model from the SiC MOSFET datasheets, Thermal Interface Material (TIM) model, and the heatsink model. To calculate the required thermal resistance of the heatsink for a given junction temperature, the junction-to-case and case-to-heatsink thermal resistances need to be obtained first.

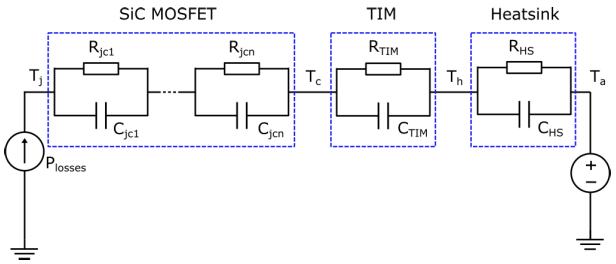

FIGURE 14. Foster thermal network model.

The junction-to-case thermal equivalent models of discrete SiC MOSFETs and SiC MOSFET half-bridge modules were obtained from PLECS models provided by the manufacturers.

TABLE 1. Estimation of thermal resistance of TIM for different SiC MOSFET packages from CREE and Infineon at t=150 µm, λ=2 W/mK.

Package	Type	Contact area, mm^2	Thermal resistance, K/W	Rated current, A
TOLL	Discrete	56	1.33	39-49
TO-263-7	Discrete	70	1.07	5-80
TO-247-3	Discrete	140	0.53	5-120
TO-247-4	Discrete	140	0.53	22-120
Easy 1B	Module	1034	0.1451	15-150
FM3	Module	1140	0.1316	84-117
GM3	Module	2295	0.0654	141-200
XM3	Module	4240	0.0354	320-450
62mm	Module	6255	0.024	120-530
HM	Module	7150	0.021	380-760

The total junction-to-case thermal resistances of the SiC MOSFETs considered in this study range from 0.0538 K/W for 650 A power module SiC MOSFET to 2.88 K/W for a 7 A discrete SiC MOSFET. The thermal resistance of TIM is calculated using the following equation:

$$R_{TIM} = \frac{t}{A\lambda}. \tag{58}$$

Here t is the thickness of the material, it is normally between 100 µm and 500 µm for the given application. The thermal conductivity λ can range from 0.02 W/mK for air and up to 8 W/mK or higher for some commercial TIMs [26]. The area of thermal contact A depends on the package of the specific MOSFET. In this study, the TIM thickness of 150 µm and thermal conductivity of 2 W/mK is used to calculate the thermal resistance of TIM for different SiC MOSFET packages using (58). The results are shown in Table 1. In the case of half-bridge modules, to calculate the case to heatsink thermal resistance per MOSFET, the thermal pad area of the module is divided by two.

After obtaining junction-to-case thermal resistance R_{jc} and the thermal resistance of the thermal interface material R_{TIM} for the selected MOSFET, the nominal heatsink temperature T_{hs} to obtain an average junction temperature of T_{jn} at rated conditions is calculated as

$$T_{hs} = T_{jn} - P_{MOSFET} * (R_{jc} + R_{TIM}), \tag{59}$$

where P_{MOSFET} are the power losses of one MOSFET switch (and its body diode).

Then the thermal resistance R_{hs} of the heatsink for a half-bridge can be calculated as a function of the desired heatsink temperature at nominal conditions T_{hs}, the ambient temperature T_{amb}, and losses of the two MOSFETs that are part of a half-bridge, as in

$$R_{hs} = \frac{T_{hs} - T_{amb}}{2 * P_{MOSFET}}. \tag{60}$$

With this value, the appropriate heatsink and speed of airflow, or liquid flow rate can be selected.

4) SWITCH THERMAL MODEL

State-space model of the thermal network given in (14) is considered from the junction to the heatsink as in

$$\begin{cases} \dot{x} = Ax + Bu \\ y = Cx + Du. \end{cases} \tag{61}$$

The matrix of states x of the model are the temperature increments that correspond to each of the parallel RC branches of the Foster model.

$$x = \begin{bmatrix} \Delta T_{jc1} \\ \Delta T_{jc2} \\ \Delta T_{jc3} \\ \Delta T_{jc4} \\ \Delta T_{TIM} \end{bmatrix} \tag{62}$$

The inputs to the system are the power losses of the switch and the heatsink temperature as shown in (63). The power losses of the SiC MOSFET calculated for one 20 ms (50 Hz) grid cycle of the given operating point within the load profile. The heatsink temperature is calculated for each operating point based on the average losses since the time constant of the heatsink is in the 10 s-100 s range, and therefore can be considered constant for the 20 ms interval that is modeled using this state-space model.

$$u = \begin{bmatrix} P_{loss} \\ T_h \end{bmatrix} \tag{63}$$

The outputs are the junction temperature and the case temperature as shown in (64).

$$y = \begin{bmatrix} T_j \\ T_c \end{bmatrix} \tag{64}$$

Equations (65)-(68) give the A, B, C, D matrices of the state-space model.

$$A = \begin{bmatrix} \frac{-1}{\tau_{jc1}} & 0 & 0 & 0 & 0 \\ 0 & \frac{-1}{\tau_{jc2}} & 0 & 0 & 0 \\ 0 & 0 & \frac{-1}{\tau_{jc3}} & 0 & 0 \\ 0 & 0 & 0 & \frac{-1}{\tau_{jc4}} & 0 \\ 0 & 0 & 0 & 0 & \frac{-1}{\tau_{TIM}} \end{bmatrix} \tag{65}$$

$$B = \begin{bmatrix} \frac{1}{C_{jc1}} & 0 \\ \frac{1}{C_{jc2}} & 0 \\ \frac{1}{C_{jc3}} & 0 \\ \frac{1}{C_{jc4}} & 0 \\ \frac{1}{C_{TIM}} & 0 \end{bmatrix} \tag{66}$$

$$C = \begin{bmatrix} 1 & 1 & 1 & 1 & 1 \\ 0 & 0 & 0 & 0 & 1 \end{bmatrix} \tag{67}$$

$$D = \begin{bmatrix} 0 & 1 \\ 0 & 1 \end{bmatrix} \tag{68}$$

5) SWITCH LIFETIME ANALYSIS

Normally, the first step of evaluating the lifetime of a switch based on the junction temperature profile is to run Rainflow cycle counting (RCC) [5]. RCC analyses the temperature profile and provides an array of median temperatures, temperature swing, pulse duration, and number of repetitions of that cycle. For the typical grid-connected AFE this array consists of the main cycle that covers the major temperature changes within the load profile, and several grid-frequency cycles at different operation points. In this study, the SiC MOSFET junction temperature profile is available as an array of medium junction temperatures and swings for each 0.02 s interval within the load profile. Therefore there is no need to run the RCC algorithm for the whole junction temperature profile. Instead, RCC is run for the profile of median temperatures to get the major cycles, which accelerates the process of lifetime estimation.

In the next step, the number of cycles to failure is estimated using Scheuermann's model [27] as in

$$N_f = A\Delta T_j^{\alpha} a_r^{\beta_1 \Delta T_j + \beta_0} \left[\frac{C + t_{on}{}^{\gamma}}{C+1} \right] e^{\frac{E_a}{k_b T_{jm}}}. \tag{69}$$

Then life consumption of a single SiC MOSFET in the given mission profile is calculated as

$$LC_{sw} = \sum_{i=1}^{k} \frac{n_i}{N_{fi}}. \tag{70}$$

6) SWITCH SIZE AND COST

The main factor deciding the SiC MOSFETs cost is its current rating as shown in Figure 15. Other factors are voltage, package, and on-state resistance. The cost model utilizes the actual costs of purchase for a single MOSFET or power module from distributors.

D. AFE DESIGN SYSTEM LEVEL EVALUATION

At this stage, the cost, volume, weight, and power losses of the AFE components are consolidated. Additional cost and weight are added for sensors and control systems. Moreover, the reliability of the whole system is calculated using

$$R_{sys} = \left(R_{sw}^6 R_{CDC} R_{CLCL} \right)^n, \tag{71}$$

where n is the number of parallel modules, R_{sw} is the reliability of a single MOSFET, R_{CDC} is the reliability of the DC link capacitor, and R_{CLCL} is the reliability of the LCL filter capacitor. In the final stage, to compare the different design variants with each other, this system-level reliability is normalized and used as a comparative reliability metric.

VI. VALIDATION

Due to the difficulty of measuring MOSFET junction temperature experimentally, in this paper only the efficiency and THD are validated using hardware measurements for different load levels. The detailed MOSFET loss profile and junction temperature are validated against the Hi-Fi Simulation in MATLAB Simulink.

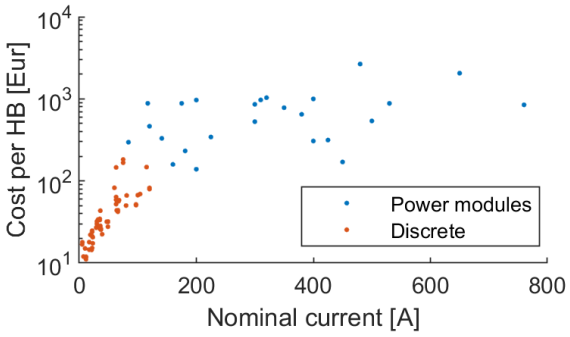

FIGURE 15. Cost of commercially available SiC MOSFETs.

A. VALIDATION AGAINST HI-FI SIMULATION

Figure 16 demonstrates the comparison between MOSFET power losses calculated using Fast Lo-Fi model described in Section V and the losses obtained from the 100 ns step-time Hi-Fi simulation in MATLAB Simulink for one 0.02 s cycle. The losses from the Hi-Fi are averaged over the switching period to compare to the Lo-Fi data.

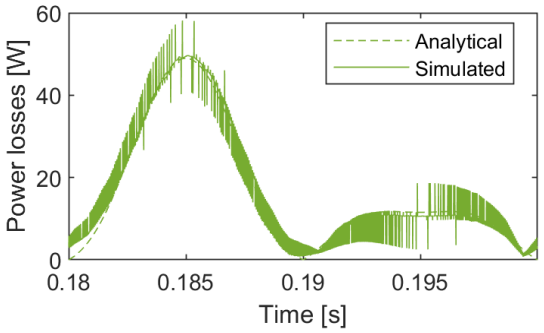

FIGURE 16. MOSFET losses: analytical calculation vs. Hi-Fi simulation.

The profile of power losses shown in Figure 16 is then given as an input to the thermal model described in Section V. MOSFET junction temperature profile within one 0.02 s cycle obtained from the Lo-Fi and Hi-Fi models compared as shown in Figure 17.

B. VALIDATION AGAINST HARDWARE MEASUREMENTS

To validate the Lo-Fi model, a scaled-down 15 kW AFE rectifier system prototype consisting of three 5 kW modules was built as shown in Figure 18.

For the inductors, AMCC0025 cores were selected for both grid-side and converter-side inductors for ease of purchasing. A 300-strand Litz wire with a 0.1 mm strand diameter was selected. The overall wire diameter is 2.38 mm, and the conducting area is 2.3568 mm^2. For 10.2 A peak, 7.2 A RMS current, it results in a current density of 3.06 A/mm^2, which is suitable for natural cooling. Following the procedure outlined in Section V, both grid-side and converter-side inductors were

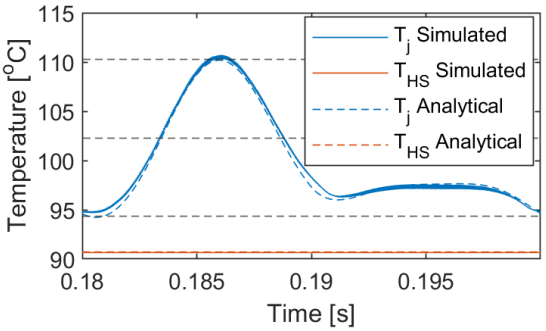

FIGURE 17. MOSFET Junction temperature: analytical calculation vs. Hi-Fi simulation.

TABLE 2. Details of the hardware prototype used to validate the model.

Parameter	Value	Unit
Module power rating	5	kW
DC Link voltage	700	V
Peak phase current per module	10.2	A
Grid line-to-line voltage	400	V
Switching frequency	20	kHz
LCL Grid side inductor	500	µH
LCL Converter side inductor	2.65	mH
LCL capacitance	0.82	µF
LCL damping resistor	10	Ω
DC link capacitance	100	µF

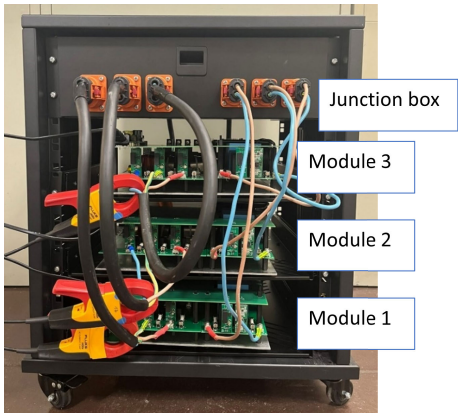

FIGURE 18. 15kW AFE Rectifier system prototype with 3 modules.

designed and manufactured. The converter side inductor has 81 turns, arranged in 4 layers. The resulting inductances were in the range 2.62 mH to 2.67 mH, which is within the acceptable range for the design value of 2.65 mH. The estimated DC resistance from the model is 57.4 mΩ. The actual resistance of nine inverter-side inductors ranges from 60 mΩ to 65 mΩ due to manual manufacturing and the excess wire necessary for mounting.

Figure 19 shows the close match between the efficiency maps obtained from the hardware test measurements and the Lo-Fi model.

During this test, the THD of grid side currents stayed under 3%, and the currents were balanced and sinusoidal as shown in Figure 20.

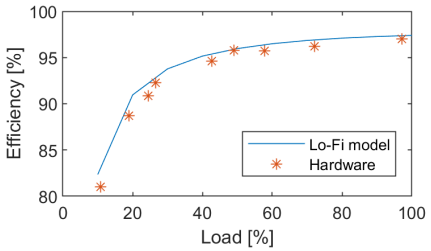

FIGURE 19. Comparison of the efficiency maps from Lo-Fi model and hardware.

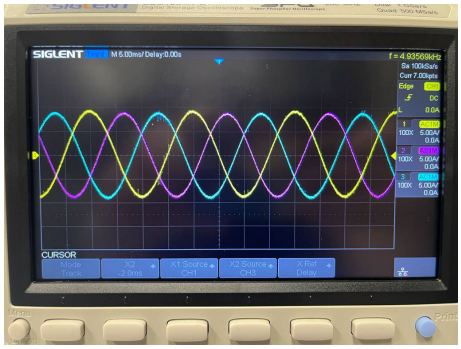

FIGURE 20. Three-phase grid-side currents of an AFE rectifier module.

VII. OPTIMIZATION RESULTS AND DISCUSSION

The optimization tool can select the optimal LCL-filter design, switching frequency, and number of parallel converter modules as part of the same optimization process. However, in this section, we present each of them separately to highlight the main trends. First is the detailed view of the optimization of an LCL filter for a 150 kW AFE rectifier module switching at 20 kHz. Trade-offs between the efficiency, cost, and volume of the grid-side and converter-side inductors are addressed, taking into consideration the LCL resonant frequency stability requirements. Then, a 150 kW AFE rectifier module is optimized in terms of switching frequency. The dependency of cost, efficiency, and junction temperature on the switching frequency is seen. Third, number of parallel converter modules in a 150 kW AFE rectifier system is optimized. In all cases, a 3960 s long CC-CV charging load profile consisting of 23 points is selected. Using the Fast Lo-Fi approach, 23 individual 20 ms long intervals are evaluated, totalling a 460 ms of modelling, instead of the entire 3960 s. Resulting in roughly 8600 times fewer data points compared to the Hi-Fi model. The runtime of the Lo-Fi electro-thermal and lifetime model for one 20 ms period was 0.18 s. The entire 23-point load profile was evaluated in 4.14 s.

A. LCL OPTIMIZATION

To design the LCL filter for a 150 kW AFE rectifier module switching at 20 kHz, the peak-to-peak ripple coefficients of the converter-side inductor k_{ri} and grid-side inductor k_{rg} are selected as a trade-off between several design criteria: the resonant frequency requirement shown in (12), desired attenuation, the expected filter losses, and expected filter cost.

The peak-to-peak ripple coefficients of the grid-side inductor $k_{rg} = 6\%$ is enough to maintain the TDD level under 5% as specified in IEEE519 for this voltage range. However, as shown in Figure 21, it is not always possible due to the resonant frequency requirement specified in (12). Therefore, $k_{rg} = 4\%$ and $k_{rg} = 2\%$ are also considered. These lower k_{rg} options would result in larger inductors and lower TDD than necessary. Figure 21 shows how the losses of the LCL filter change with the k_{rg} and k_{ri}. In this case, options with $k_{rg} = 6\%$ for all values of k_{ri} are not possible due to resonance frequency requirements. Moreover, some of the options where $k_{rg} = 4\%$ and $k_{rg} = 2\%$ are not possible too, and are portrayed as ''empty''.

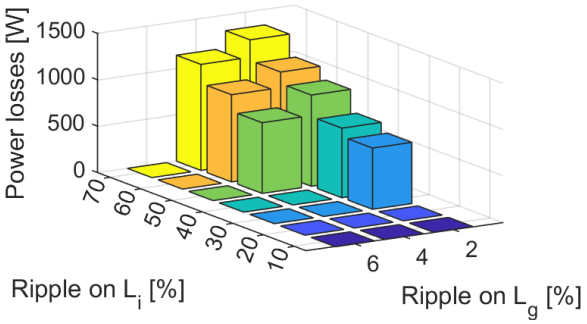

FIGURE 21. Power losses of an LCL filter as a function of the ripple on the converter-side and grid-side inductors. Options not satisfying the resonance frequency condition are portrayed as "empty."

The breakdown of losses occurring on different components, and their types for the case when $k_{rg} = 2\%$ is shown in Figure 22. The inductance of the converter-side inductor needs to be higher for current ripple $k_{ri} = 30\%$, resulting in a larger inductor, with a higher number of turns. While the core losses will be minimal because the high-frequency ripple causing the core losses is only 30%. As seen in Figure 22, this option has the highest winding losses of L_i. In contrast, when an exaggerated ripple of 70% is allowed, it results in a smaller inductance on the converter side and a larger one on the grid side. A lot of the filtering and attenuation happens on the grid-side converter and the capacitor, increasing the losses on the windings of the grid-side inductor and damping resistor of the LCL. This option shows the highest core losses of L_i, the highest losses on the damping resistor R_d, and the highest winding losses on L_g. Core losses on L_g are always low, since $k_{rg} = 2\%$.

The cost of LCL filter will be better for higher k_{rg} as shown in Figure 23.

As shown in Figure 24, with the increase of k_{ri} the cost of the converter-side inductor decreases, while the cost of the grid-side inductor increases. The minimum cost for this case is at $k_{ri} = 40\%$. It will be different for each case.

B. OPTIMIZATION OF SWITCHING FREQUENCY

In this subsection, optimization of the switching frequency of 150 kW AFE rectifier module is presented for frequency range of 10 kHz to 30 kHz.

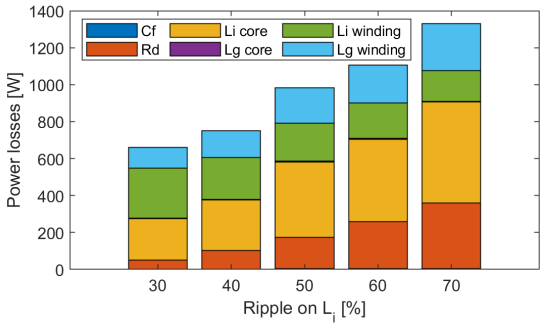

FIGURE 22. Breakdown of power losses of an LCL filter as a function of the ripple on the converter-side inductor, for $k_{rg} = 2\%$.

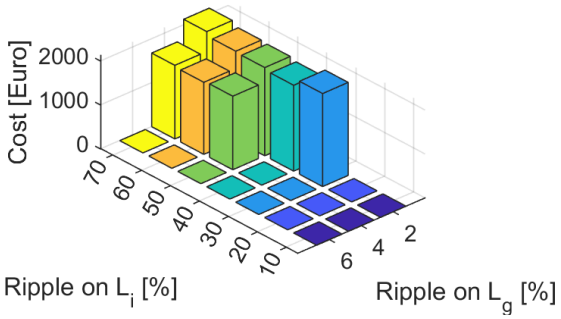

FIGURE 23. Cost of an LCL filter as a function of the ripple on the converter-side and grid-side inductors. Options not satisfying the resonance frequency condition are portrayed as "empty."

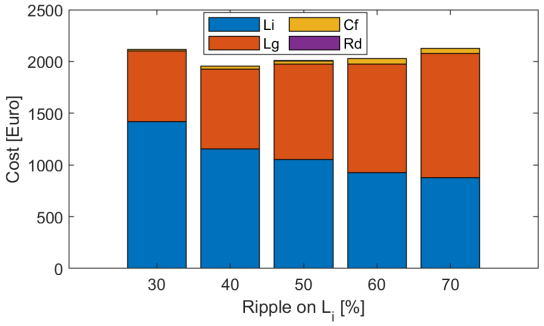

FIGURE 24. Breakdown of power losses of an LCL filter as a function of the ripple on the converter-side inductor, for $k_{rg} = 2\%$.

The general trend in Figure 25 is that the power losses on switches increase with the increasing switching frequency, while the filter losses mostly decrease. In this case, 10 kHz case has the highest average efficiency of 98.5%. The average, maximum, and minimum efficiencies during the mission profile are given in Figure 25.

Since losses at the switch increase with the switching frequency, the junction temperature swings also increase as shown in Figure 26. Since all converters are designed for the median junction temperature of 100 °C, the temperature swings given in Figure 26 mean that with 10 kHz switching frequency the MOSFET junction temperatures change from 88.9 °C to 111.1 °C, while for 30 kHz case the junction temperature varies from 84.9 °C to 115.1 °C.

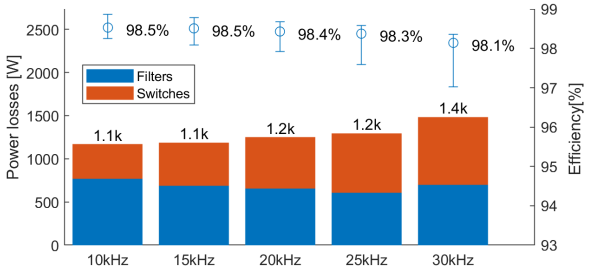

FIGURE 25. Power losses of a 150kW AFE rectifier module. The error bar signifies the upper and lower efficiency ranges during a CC-CV charging profile.

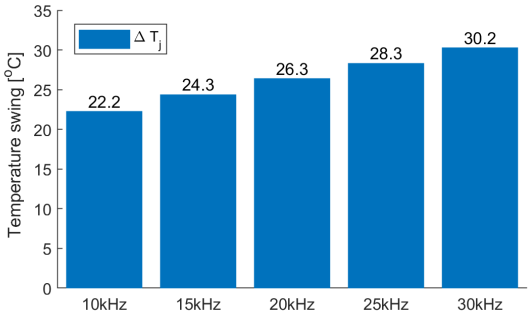

FIGURE 26. Maximum junction temperature swing of a SiC MOSFET used in a 150kW AFE rectifier module.

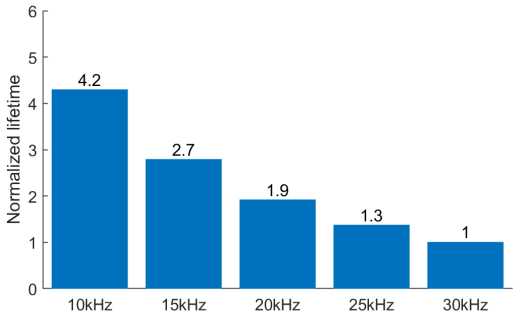

FIGURE 27. Normalized lifetime of a SiC MOSFET used in a 150kW AFE rectifier module.

The higher junction temperature swings are associated with faster aging of the component, it also negatively affects the lifetime of the switch as shown in Figure 27.

Figure 28 shows that with the increase of switching frequency, the cost of the filters decreases. While the cost of the switches doesn't change much, since generally the same switch can be used for a range of frequencies.

C. OPTIMIZATION OF MODULARITY

In this subsection, optimization of the number of parallel converter modules for a 250 kW AFE rectifier system is presented. The tendencies here are not as straightforward as with the switching frequency due to the availability of components at different power levels.

Figure 29 shows comparison of 250 kW AFE rectifier systems with 1 to 9 modules. Having 6 modules of 41.7 kW each would result in the highest average efficiency of 98.5%, which ranges from 96.74% to 98.73% during the mission

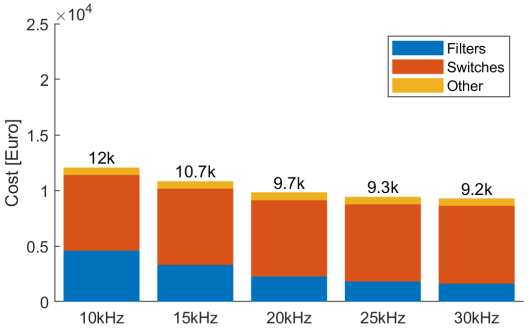

FIGURE 28. Cost of a 150kW AFE rectifier module.

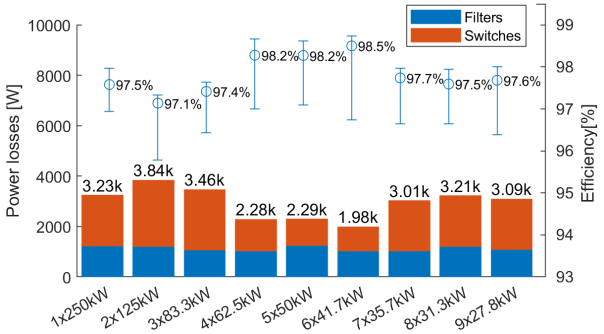

FIGURE 29. Power losses of a 250kW AFE rectifier system with varying number of parallel modules. The error bar signifies the upper and lower efficiency ranges during a CC-CV charging profile.

profile. The losses in this case are around 1.98 kW. This is 48% less than the option with the largest average losses: 2×125 kW with 3.84 kW power losses. So, if efficiency was the main priority, the user could decrease the losses by 48% by choosing 6 modules instead of 2.

Figure 30 demonstrates how the junction temperature swing of a SiC MOSFET changes depending on the number of parallel AFE rectifier modules in a 250 kW system. Increasing the number of parallel modules within the same MOSFET footprint can reduce the junction temperature swings as shown in Figure 30. The 62 mm power modules have the biggest area to dissipate the heat. "Easy 1B" modules are slightly smaller than the 62 mm modules, and the discrete modules are the smallest. The option with 3 modules of 83.3 kW has the lowest temperature swings (13.9 °C). Compared to the worst case at 7 modules of 35.7 kW with 127 °C, this is an 89% decrease. All options are designed for a 100 °C median junction temperature at maximum rated load.

Figures 31 and 32 show how the SiC MOSFET junction temperature changes during the mission profile. The main line is the median temperature, while the error bars show the maximum and minimum junction temperatures. The difference between the maximum and the minimum value is the temperature swing. While median temperatures stay similar in both cases, in the case of 3 modules of 83.3 kW the temperature swings are much lower.

Lower junction temperature swing for the higher number of modules can be explained with Figures 33. Within the same package, lower power results in lower temperature swings,

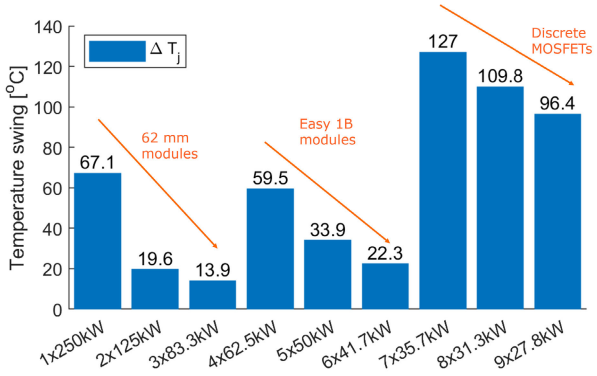

FIGURE 30. Junction temperature swings of a SiC MOSFET in a 250kW AFE rectifier system with varying number of parallel modules.

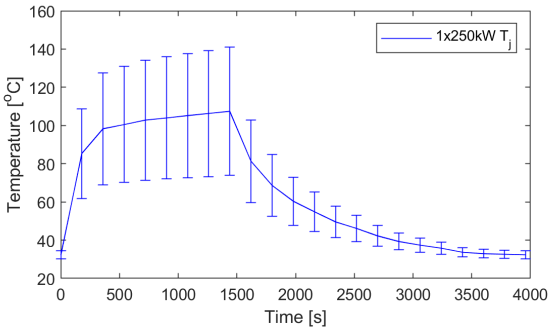

FIGURE 31. Junction temperature of a SiC MOSFET in a 250kW AFE rectifier system with 1 × 250kW module.

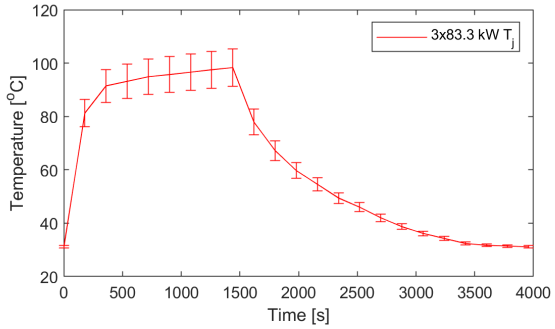

FIGURE 32. Junction temperature of a SiC MOSFET in a 250kW AFE rectifier system with 3 × 83.3kW modules.

and can improve component lifetime, which aligns with the findings in [5].

The individual switch's lifetime will be exponentially correlated to the junction temperature swings that occur during the mission profile according to (69). However, when applied to the whole system with different numbers of parallel modules as shown in (71), it results in normalized lifetimes as shown in Figure 34. The seven-module option will result in the shortest lifetime due to high junction temperature swings. The three-module option will have the longest predicted lifetime due to a good combination of an individual component lifetime and a total number of components.

The cost of individual filters used in the 250 kW AFE rectifier system will decrease due to lower power levels

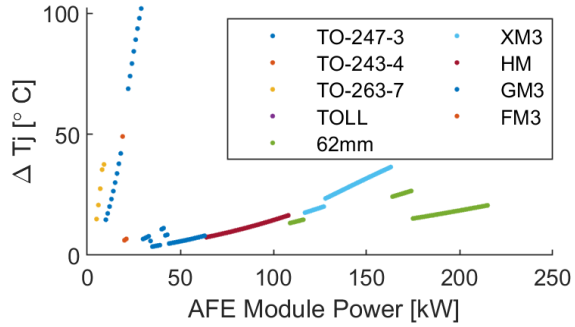

FIGURE 33. Maximum junction temperature swing vs. AFE module power.

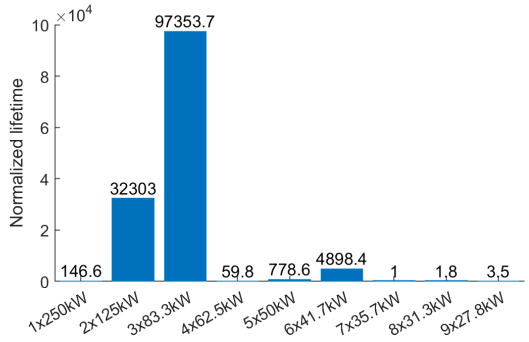

FIGURE 34. System lifetime of a 250kW AFE rectifier system with varying number of parallel modules.

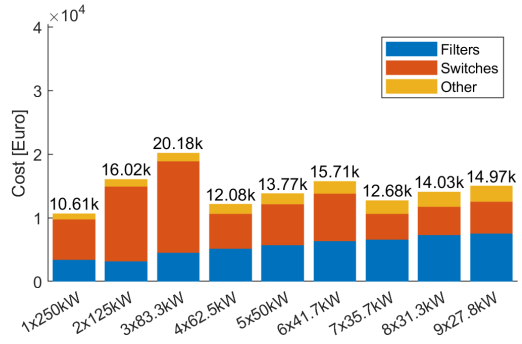

FIGURE 35. Component cost of a 250kW AFE rectifier system with varying number of parallel modules.

with the increasing number of modules. However, since the total number of filters increases, the total filter cost will also increase as shown in Figure 35. The cost of individual switches will decrease due to the decreasing power levels, while the total number of used switches will increase. Due to this, there is no clear trend, the total cost of switches will be different in each case as shown in Figure 35. In this optimization example, the cheapest option is a single module, and it is 47% cheaper than the most expensive three-module option.

VIII. CONCLUSION

A design optimization for grid-connected modular AFE rectifiers with an evaluation of efficiency, lifetime, cost, volume, and weight has been presented. Fast Lo-Fi electro-thermal and lifetime models have been developed and validated against Hi-Fi models and hardware prototype

measurements. This novel hybrid modeling approach has a speed advantage of ''Fast Lo-Fi'' models with the added benefit of lifetime estimation.

Detailed design and selection procedure for the inductors, capacitors, and switches used in the AFE rectifier is presented. A hardware prototype is designed following this design process and used to validate the Lo-Fi models.

Designing an LCL filter with the approach described in this paper, its losses can be decreased by 50%, while the cost can be decreased by 23%. Optimizing the AFE rectifier module by a switching frequency can lead to 22% lower power losses, 23% decrease in cost, and 4.2 times increase in predicted lifetime for the case of 150 kW AFE switching between 10 kHz and 30 kHz. However, the lowest cost option has the lowest efficiency and lifetime. Therefore it is up to the user to use the analysis provided by the tool and make their own decisions. Optimizing the number of parallel converter modules in the AFE rectifier system can lead to 48% lower power losses, 47% decrease in cost, and an exponential increase in predicted lifetime for the analyzed case of 250 kW AFE of one to nine IPOP modules. Here the single-module option has the lowest cost, while the 3-module option has the best thermal characteristics and lifetime, and the 6-module version has the highest efficiency. Once again, it is up to the user to make the final decision considering all aspects of different design options provided by the design tool.

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