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RESEARCH ARTICLE

# Design and Investigation of InGaAs/InP/InAlAs MOSFET With Optimized Switching Efficiency

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**ABSTRACT** In this research, the DC performance of four InGaAs MOSFETs having different technology of 22nm, 14nm, 10nm, and 7nm with highly doped source and drain region is successfully examined. A high-performance MOSFET is designed as a large current of 12mA/$\mu$m for a low $V_{gs}$ of 0.25V is observed for InGaAs MOSFET with 7nm technology. Two multiple-layer caps are designed in both the source and drain region to reduce the parasitic capacitance. A high transconductance gain of 1.96mA/V for 7nm technology and subthreshold slope of 76.69mV/dec are achieved for InGaAs MOSFET with 14nm technology, which shows that high-performance InGaAs were created. An excellent off-state current of $2.5 \times 10^{-10}$ A/$\mu$m is achieved for 22nm technology. The designed InGaAs MOSFETs are also capable to operate successfully in low voltage ranges, as a high amount of output current can be achieved under such conditions, which is a very demanding aspect in the present scenario.

**INDEX TERMS** InGaAs, InAlAs, InAs, MOSFETs, nano-meter technology, DC characteristics.

## I. INTRODUCTION

InGaAs and InAs are promising channel materials because of their excellent electron transport properties for future CMOS applications [1]. Over the last few decades, enormous efforts have been made to produce high-performance InGaAs MOSFETs. The switching performance has been optimized by using heterojunction diode with split-gate SIC trench MOSFET [2] which offers advantages by reducing the surface area of the depletion layer in JFET and also by increasing the breakdown voltage of the device. According to the analysis, the structure provides high speed and high power devices with effective drain voltages [3]. The integration of the heterojunction diode with the split-gate SiC trench MOSFET also contributes to an increase in the breakdown voltage of the device [4]. The technology has transformed the world rapidly over the past few decades. Though the first transistor was invented in 1947 [5], now-a-days transistors are part of every human's life. The first transistor was a point-contact diode that was embedded in Ge semiconductor at Bell Laboratory. The first integrated circuit was invented by Jack Kilby in the year 1958 at Texas Instruments [6]. From the year 1960, remarkable improvements are seen in transistor performance and the number of devices on a chip doubling in every eighteen months stated by Moore's Law has been achieved by geometrical scaling of MOSFETs [7]. Silicon technology has dominated the semiconductor industry for more than five decades and the scaling of devices has been the major factor contributing to the growth of the industry. Currently, in the industry, 7nm technology is used and work is going for 5nm technology. Moreover, the abundant nature of Si is another reason to get enormous achievements in the semiconductor industry. Silicon technology has many advantages but it has low carrier mobility and low saturation velocity which diminishes its suitability in modern electronic applications like mobile, satellite, and radar. Hence, research on new materials has started to gain momentum, with the aim of substituting the existing silicon technology. New channel materials with high electron/hole mobility can then be needed to get higher injection velocities and during this manner continue the

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historical trend of scaling and also the expectations of Moore's law. It is found that materials such as SiC, SiGe, and group III-V semiconductors can replace Si successfully and among them, III-V compounds have shown to have an outstanding electron mobility, making them promising candidates for the post-Si era. III-V electronic products have constituted a multi-billion-dollar industry with a large number of applications such as lasers, LEDs, wireless networks, radar, and smartphones. To design high-performance MOSFET we can replace substrate with Indium Phosphide (InP) compound because of its favorable properties. The study gives evidence of massive efforts in this field [8], [9], [10], [11], [12], [13], [14], [15]. Again, in the last two decades, an explosion of interest has been witnessed in high-speed semiconductor devices and integrated circuits suitable for ultra-high speed applications, low power applications, and low-noise applications [1]. Indium gallium arsenide (InGaAs) and indium aluminum arsenide (InAlAs) are ternary alloys. Both these alloys have very high electron mobility which helps to get high-speed devices in electronics, photonics, and modern IC in VLSI circuits [16]. To summarize, this study addresses the challenge of optimizing InGaAs and InAs as channel materials for high-performance MOSFETs in future CMOS applications. It investigates the limitations of silicon technology, exploring alternative materials like InP and III-V semiconductors. The study also highlights a surge in interest in high-speed semiconductor devices and ternary alloys like InGaAs and InAlAs for potential applications.

Gallium and Indium compound semiconductor with direct bandgap materials have better electron mobility than Silicon. But, the energy bandgaps of GaAs, GaN, and InP are all greater than those of Silicon. However, no comparable tendency has been found for hole mobility. When comparing Aluminium compound semiconductor materials, all Aluminium compound semiconductor materials have higher bandgap energy than Silicon. So it's now intriguing to observe which Gallium, Aluminum, and Indium compound semiconductor material(s) outperform Silicon [17]. Comparison of various MOSFETs with similar structure to that of the proposed structure has been given in Table 1 for a brief overview [18].

**TABLE 1. Comparision of various mosfets with different dielectric oxide.**

| Dielectric Oxide | $L_g$ (nm) | $I_{D\,max}$ (mA /μm) |
|---|---|---|
| GaN | 22 | 0.950 |
| HfSiON | 15 | 2.57 |
| $SiO_2$ | 10 | 1.4 |
| $Al_2O_3$, $HfO_2$ and HfAlO | 60 | 1.8 |

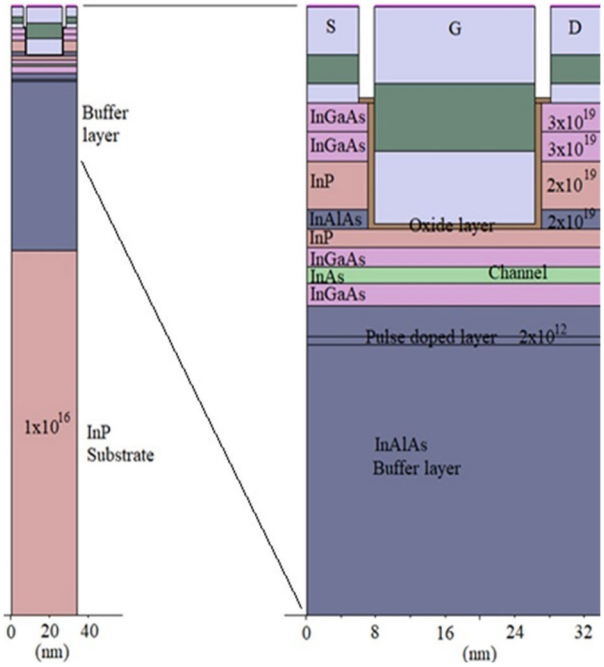


**FIGURE 1. Structure of InGaAs MOSFET using 14nm technology.**

## II. PROPOSED STRUCTURE

The cross-sectional view of the InGaAs MOSFET is shown in Figure.1. The proposed MOSFET has an InP substrate over which a 200nm $In_{0.52}Al_{0.48}As$ buffer layer is placed. This buffer layer is used to reduce defects that are present in the substrate. A delta-doped layer or pulse doped layer with a doping density of $2 \times 10^{12}$ per $cm^3$ is employed above the buffer layer. This delta-doped layer supplies carriers to the intrinsic channel of the MOSFET. On the top of this pulse doped layer, a spacer layer of 5nm $In_{0.52}Al_{0.48}As$ is placed. A composite channel is used which consists of a 3nm thick $In_{0.7}Ga_{0.3}As$ upper sub-channel, 2nm InAs intrinsic channel, and 5nm thick $In_{0.7}Ga_{0.3}As$ lower sub-channel. A 2nm thick InP layer is employed just above the composite channel as an upper spacer layer.

The source and the drain cap layer are designed just above the spacer layer. To reduce access resistance in the source and drain region a heavily doped n-type multilayer cap layer is employed. The multilayer cap layer consists of a 2nm $In_{0.52}Al_{0.48}As$ layer, 10nm thick InP layer, 6nm thick $In_{0.53}Ga_{0.47}As$ layer, and 6nm thick $In_{0.7}Ga_{0.3}As$ layer. In the upper two layers, high n+ Si doping of $3 \times 10^{19}$ is used and for the lower two layers, slightly less doping of $2 \times 10^{19}$ is taken. This multiple-layer cap is used to enhance various performances of the MOSFET, like mobility, transconductance, and saturation current. An oxide layer of 1nm thickness is placed as displayed in Figure.1. Here two alloys $In_{0.52}Ga_{0.48}As$ and $In_{0.53}Ga_{0.47}As$ have the same lattice constant as InP with a direct band gap and trap carriers more effectively. But the alloy $In_{0.7}Ga_{0.3}As$ and InAs do not have the same lattice constant of InP. As the thickness of the layers is less, atoms are strained and lattices are

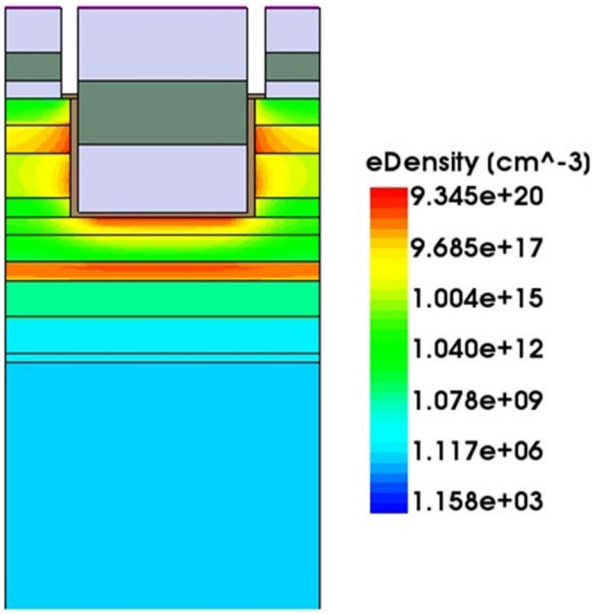


**FIGURE 2.** Electron density profile of MOSFET for 14nm technology.

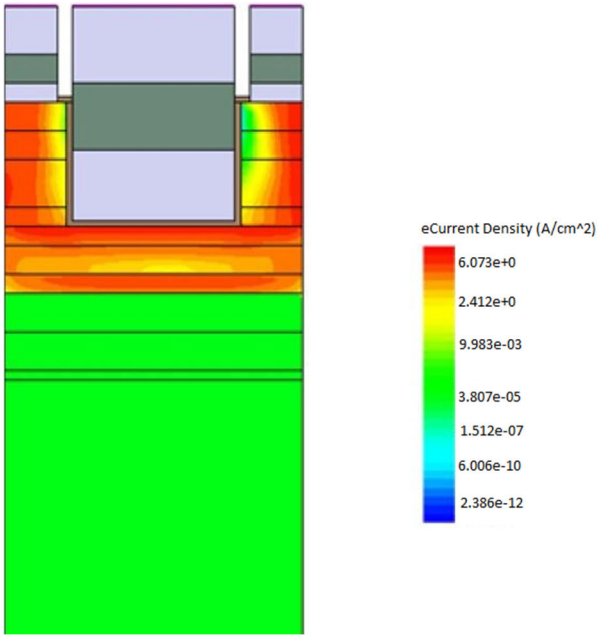


**FIGURE 3.** Electron current density profile of MOSFET for 14nm technology.

matched properly, otherwise, lattice match is not possible for the structure. Therefore, these materials are used for the design of high-speed electronic devices. Here 4 MOSFETs are designed with 4 different technologies (22nm, 14nm, 10nm, and 7nm). The high 70% In fraction layer offers enhanced transport properties and the 53% In layers mitigate impact ionization effects. In this research work, in the channel region, $In_{0.7}Ga_{0.3}As$ and InAs are used and those are having high electron mobility, therefore high-performance InGaAs MOSFET is designed successfully.

**TABLE 2.** Calibration of model and device parameters.

| SL No. | Parameter | Specification |
|---|---|---|
| 1 | Technology | 22nm, 14nm, 10nm, and 7nm |
| 2 | Doping Conc. | $10^{19}$ |
| 3 | Doping type | N-type |
| 4 | Temperature | 300K |
| 5 | Leakage current | $2.5\times10^{-10}$ A/μm |
| 6 | Electron Density at Intrinsic Channel | $5\times10^{18}$ per $cm^3$ |
| 7 | Meshing | Adaptive Meshing |
| 8 | Recombination Model | Shockley-Read-Hall (SRH) |

**TABLE 3.** Device layers, materials and dimensions.

| SL No. | Region | Material | Dimension (in nm) |
|---|---|---|---|
| 2 | Buffer Layer | $In_{0.52}Al_{0.48}As$ | 200 |
| 3 | Spacer layer | $In_{0.52}Al_{0.48}As$ | 5 |
| 4 | Composite Channel | $In_{0.7}Ga_{0.3}As$ | 3 |
| | | InAs | 2 |
| | | $In_{0.7}Ga_{0.3}As$ | 5 |
| 5 | Cap Layer | $In_{0.52}Al_{0.48}As$ | 2 |
| | | InP | 10 |
| | | $In_{0.53}Ga_{0.47}As$ | 6 |
| | | $In_{0.7}Ga_{0.3}As$ | 6 |

The calibration model, device parameters, and other simulation details are presented in Table 2. And details of layers, materials and their dimension are presented in Table 3. Standard material parameters are used in the TCAD simulation which are briefly represented in Table 4.

For the simulation a mesh grid was created that discretizes the device structure. The doping profiles were incorporated

**TABLE 4. Material parameters used for the TCAD simulation.**

| Parameters | InGaAs | InAlAs | InP |
|---|---|---|---|
| Band Gap (eV) | 0.798 | 1.56 | 1.35 |
| Electron Affinity | 4.67 | 4.17 | 4.34 |
| Static Dielectric Constant | 13.8 | 12.5 | 12.5 |
| Electron Effective Mass | $0.041m_0$ | $0.352m_0$ | $0.077m_0$ |
| Density of States (Conduction Band) | $1.7x10^{17}$ $cm^{-3}$ | $6.83x10^{17}$ $cm^{-3}$ | $5.68x10^{17}$ $cm^{-3}$ |
| Density of States (Valence Band) | $8.12x10^{18}$ $cm^{-3}$ | $1.44x10^{19}$ $cm^{-3}$ | $8.87x10^{18}$ $cm^{-3}$ |

into the simulation, including the delta-doped layer and the multilayer cap layer. After that simulations were started to predict key MOSFET characteristics such as current-voltage (I-V) characteristics, transconductance etc. The performance of the MOSFET at different technology nodes (22nm, 14nm, 10nm, and 7nm) was analyzed. The proposed MOSFET has an InP substrate over which a 200nm $In_{0.52}Al_{0.48}As$ buffer layer is placed. This buffer layer is used to reduce defects that are present in the substrate. It is critical to treat interface defects in order to optimize MOSFET performance. In the context of InGaAs MOSFETs, the inclusion of a buffer layer, delta-doped layers, and careful material and doping profile selection can all help to reduce interface defects and optimize the subthreshold slope. In MOSFETs, a low subthreshold slope is critical for achieving high switching efficiency.

## III. RESULTS AND DISCUSSION

Based on the designed structure, different characteristics of high-performance InGaAs MOSFET are obtained during their operation. Those characteristics are electron density profile, electron current density profile, transfer characteristics, static characteristics, and off-state current respectively. Let us assume the width of all MOSFETs is 1 $\mu$m.

The electron density profile and electron current density profile of the designed MOSFET using 14nm technology are presented in Figure.2 and Figure.3 respectively. Those two Figures show that the channel is perfectly created as the channel region is designed in the structure. The electron density at the intrinsic channel is approximately $5 \times 10^{18}$ per $cm^3$ and

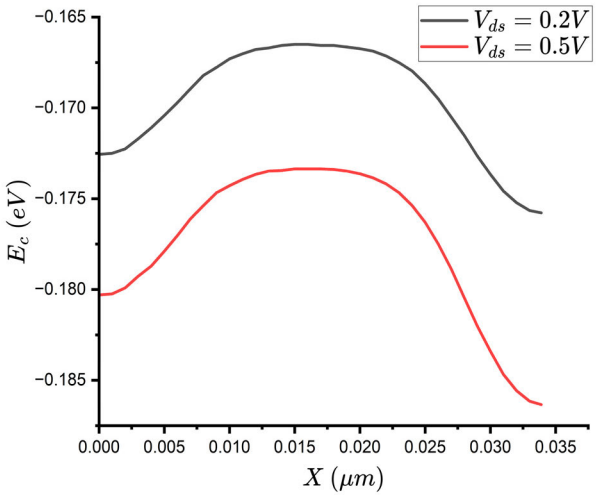


**FIGURE 4. Conduction band energy of MOSFET with 14nm technology with $V_{ds}$ 0.2 volt and 0.5 volt.**

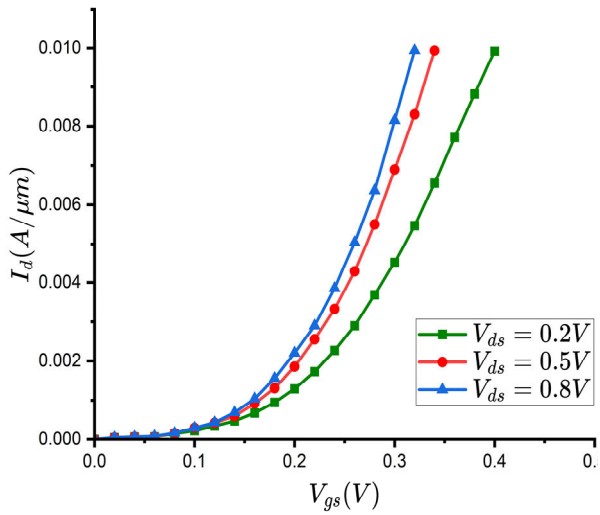


**FIGURE 5. $I_d$ vs $V_{gs}$ curves for 22nm technology with different Vds.**

the electron current density is approximately 4 A/$cm^2$. Those two profiles help to flow current through the MOSFET.

A cutline is taken across the channel and the conduction energy band diagram is shown in Figure.4. It shows as $V_{ds}$is applied positive voltage, conduction band moves downward in drain side and a negative voltage is applied to $V_{gs}$, therefore conduction band energy below the gate region increases. For more $V_{ds}$, conduction band energy is lesser as noticed in Figure.4. It is also confirmed that the short channel effect cannot affect more for the designed MOSFET. The $I_d$ Vs $V_{gs}$ transfer characteristics on a linear scale for the InGaAs MOSFETs with 22nm technology is shown in Figure.5. The figure shows the ideal MOSFET characteristics. High current flows through the MOSFET as the drain to source voltage ($V_{ds}$) of the MOSFET is increased for lower $V_{gs}$. The threshold voltage of the MOSFET also decreases for high $V_{ds}$.

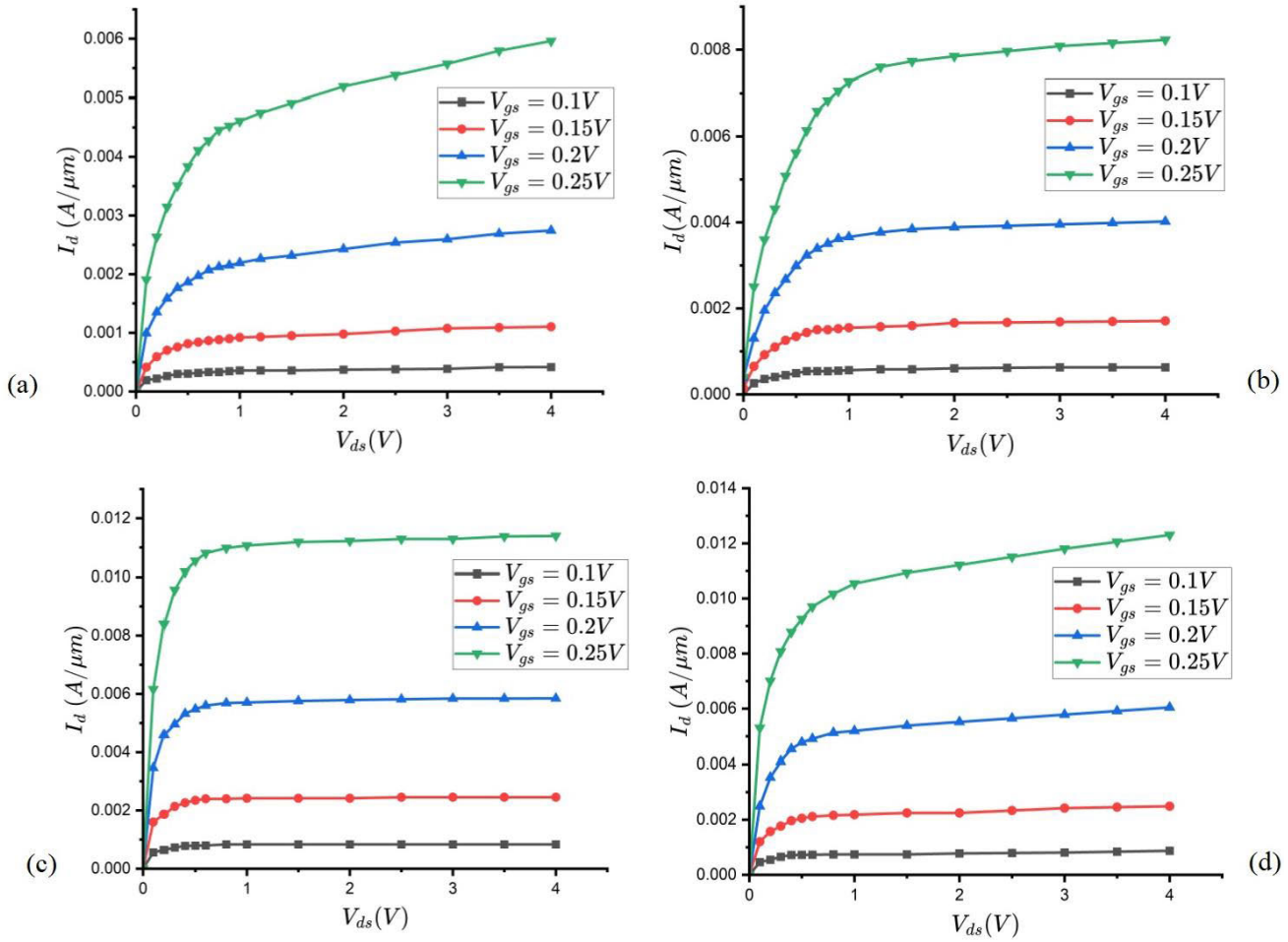


**FIGURE 6.** (a) $I_d$ vs $V_{ds}$ Characteristics For 22nm Technology (b) $I_d$ vs $V_{ds}$ characteristics for 14nm technology (c) $I_d$ vs $V_{ds}$ characteristics for 10nm technology (d) $I_d$ Vs $V_{ds}$ characteristics for 7nm technology.

The current that passes through a transistor when it is off is known as the off-state current. The inherent imperfections in the design of the transistor are what cause this current. Off-state current can waste power even when a circuit is not in use, which can have a major impact on a circuit's switching efficiency. The term ''switching efficiency'' generally relates to how well a switch or transistor can be turned on and off. So, a smaller off-state current may cause better switching efficiency. The threshold voltage of this MOSFET is -0.18V and the off-state current is approximately 0.25 nA/$\mu$m for $V_{gs}$ = -0.5V. So, a negligible current is flown in the off-state which confirms better switching efficiency. $I_d$ Vs $V_{ds}$ output characteristics of MOSFETs with 4 different technologies (22nm, 14nm, 10nm, and 7nm) is shown in Figure.6(a), Figure.6(b), Figure.6(c), and Figure.6(d) respectively. In Figure.6 output characteristics of the MOSFET having 22nm technology are shown having a different gate to source voltages with 0.05V step from 0.1V to 0.25V. The characteristic obeys the ideal characteristics of the MOSFET. For low voltages, it operates in a linear region and afterward for saturation region on the application of high $V_{ds}$. For a constant voltage $V_{gs}$ = 0.25 V, a current of 5.5 mA/$\mu$m flows through the MOSFET in a saturation region.

The output characteristic of InGaAs MOSFET with 14nm technology is pictured in Figure.6(b). The figure shows $I_d$ Vs $V_{ds}$ characteristics with different $V_{gs}$ from 0.1V to 0.25V with a step voltage of 0.05V. It shows better performance as compared to 22nm technology. For $V_{gs}$ = 0.25V a high current of approximately 8mA/$\mu$m is passed through the MOSFET. The $I_d$ Vs $V_{ds}$ output characteristic of InGaAs MOSFET with 10nm and 7nm technology is pictured in Figure.6(c) and Figure.6(d) respectively with a step voltage of 0.05V for $V_{gs}$ from 0 to 0.25V. Figure.6(c) shows better performance as compared to 22nm and 14nm technology and Figure.6(d) shows the best among all technology. A high amount of current of 11mA/$\mu$m and 12mA/$\mu$m are noticed for a fixed $V_{gs}$ of 0.25V for 10nm and 7nm technology respectively.

The transconductance gain and subthreshold slope of the designed MOSFETs are shown in Table 5 (transconductance gain and subthreshold slope for different technology with a fixed $V_{ds}$ of 0.5V) and Table 6 (transconductance gain and

subthreshold slope for 7nm technology with different $V_{ds}$). Table 5 is resulting from a fixed drain to source voltage of 0.5V with $V_{gs}$ varied from -0.4V to 0V. From technology to new technology transconductance gain is achieved more and an excellent subthreshold slope of 76.69mV/dec for 14nm technology is also noticed. For a high value of $V_{ds}$ high transconductance gain is also observed. The current through MOSFET in saturation region for various technology nodes for a constant $V_{gs} = 0.25V$ has been represented in Table 7.

Several factors contribute to the modulation of output resistance as technology nodes reduce from 22nm to 7nm, and the relationship between them is not necessarily monotonic. The transistor's dimensions are larger at the 22nm node than at smaller nodes. The channel length and width, as well as other process factors, all have an effect on the output resistance. Because of the bigger transistor size, the output resistance is typically higher. With the transition to the 14nm node, transistor dimensions shrink, resulting in reduced channel lengths and widths.

The lower dimensions could end up in improved control of the channel by the gate, resulting in a reduction in output resistance. Further size reduction happens in the 10nm node, and the output resistance may continue to reduce. With a much lower transistor size, the 7nm node represents an even more advanced technology. As dimensions decrease, quantum mechanical phenomena become more evident, and transistor behaviour can become more complex. This may result in non-monotonic output resistance behaviors.

The influence of channel length on on-state current, subthreshold slope, and transconductance controls the output resistance in MOSFETs. A shorter channel length produces a larger on-state current, a smaller sub-threshold slope, and a higher transconductance. Furthermore, modulation effects on channel length contribute to changes in the effective channel length, which affects output resistance, particularly at higher drain-source voltages. The complex interaction between these parameters is critical in maximizing MOSFET performance in a wide range of applications.

The comparison of our proposed models with previously published results [19], [20] serves as a critical validation of the superior device performance of the proposed models. To ensure a fair assessment, our 14nm and 7nm devices were compared against the highly performing devices documented in the literature [19], [20]. This comparison involved maintaining a consistent $V_{gs}$ of 0.2V across all devices, while $V_{ds}$ was systematically varied from 0 to 1V. The distinct advantage of our proposed models over the published ones is clearly evident, showcasing a substantial performance margin. Figure 7 graphically illustrates this comparison, providing a visual representation of the superior performance exhibited by our models. Through meticulous analysis and rigorous testing, our models have demonstrated their efficacy and reliability in enhancing device performance, thereby contributing significantly to the advancement of the semiconductor technology.

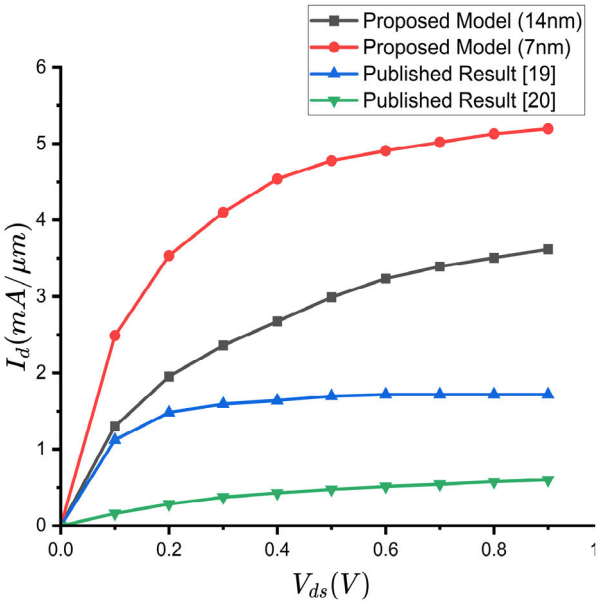


**FIGURE 7.** Performance comparison of the proposed model with the published results.

**TABLE 5.** Transconductance gain and subthreshold slope for different technology with a fixed $V_{DS}$ OF 0.5V.

| Technology Node | Transconductance Gain | Subthreshold Slope |
|---|---|---|
| 22nm | 0.71mV/A | 81.46mV/dec |
| 14nm | 1.39mV/A | 76.69mV/dec |
| 10nm | 1.65mV/A | 79.16mV/dec |
| 7nm | 1.75mV/A | 78.98mV/dec |

**TABLE 6.** Transconductance gain and subthreshold slope for 7nm technology with different $V_{DS}$.

| Drain Voltage | Transconductance Gain | Subthreshold Slope |
|---|---|---|
| 0.2V | 1.53mV/A | 79.32mV/dec |
| 0.5V | 1.75mV/A | 78.98mV/dec |
| 0.8V | 1.96mV/A | 77.48mV/dec |

The MOSFET should have faster switching time to minimize the time duration of operation. Faster switching time reduces the switching losses. Whereas, transconductance gain

**TABLE 7. Current through mosfet in saturation region for various technology nodes for a constant $V_{GS} = 0.25V$.**

| Technology node | $V_{gs}$ (in Volt) | Current |
|---|---|---|
| 22nm | 0.25 | 5.5mA/μm |
| 14nm | 0.25 | 8mA/μm |
| 10nm | 0.25 | 11mA/μm |
| 7nm | 0.25 | 12mA/μm |

is a measure for an electronic component's capacity for amplification. By enabling faster switching speeds, lowering power dissipation and requiring fewer control signals, a larger transconductance gain can cause improved switching efficiency.

- Faster Switching Speed: The device can switch between the on and off states more quickly if the transconductance gain is higher. The device works in the intermediate states for a shorter period of time because of the quicker switching speed, which decreases power losses and increases efficiency.
- Lower Power Dissipation: The device can function with lower voltage drop across its internal components due to a larger transconductance gain. As a result of the smaller voltage drop, efficiency is increased and less power is wasted.
- Reduced Control Signal Requirements: As transconductance gain increases, the voltage or current of the control signal required to operate the device is reduced. This can make control circuit design simpler, use less energy, and enhance the overall efficiency.

## IV. CONCLUSION

Four high-performance InGaAs MOSFETs with different technology nodes have been successfully modeled with verification of their better static and transfer characteristics in comparison to the conventionally available previous contenders. The output characteristics have improved more and more from old technology to new technology. The obtained output characteristics validate that for short channel length MOSFET, the resultant terminal current is considerably high. A high electron density profile and high electron current density profile are noticed for 14nm technology, an excellent off-state current of $2.5 \times 10^{-10}$ A/$\mu$m is achieved for 22nm technology. With 7nm technology, InGaAs MOSFET designed in this research, concludes a remarkable amount of large current production in the order of 12mA/$\mu$m, a high transconductance of 1.96mV/A, and an excellent subthreshold slope of 77.48mV/dec, which confirms the formation of high-performance InGaAs MOSFET.

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